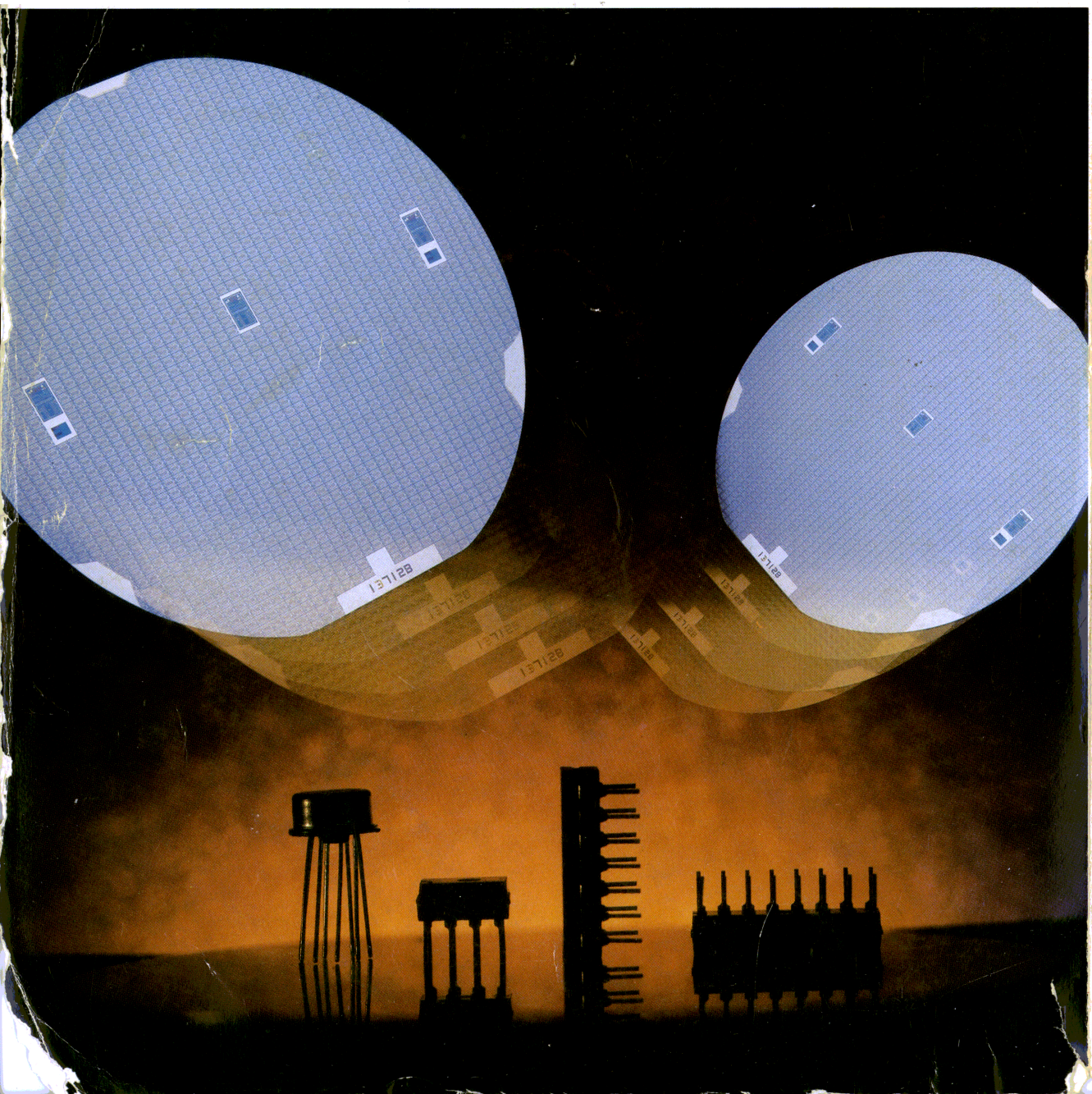
RCA Solid State

DATABOOK



RCA Integrated Circuits for Linear Applications

RCA offers an extensive line of integrated circuits for a wide range of diverse functions that historically have been classified as linear applications. This classification, however, has become somewhat outmoded in that, frequently, such circuit functions are accomplished best by either digital techniques or a combination of digital and analog techniques. For example, many telecommunications functions that, in the past, were considered strictly in the linear domain are now implemented more effectively by digital circuitry; moreover, digital electronics have made possible substantial expansions in the functional capabilities and sophistication of telecommunications systems. Similarly, data-conversion and interface circuits, which have interconnected linear and digital sections, must be considered as a special category. This DATABOOK provides detailed technical information of such types and on a broad spectrum of other types that exhibit predominantly analog characteristics and for which the term "linear" is a more precise classification.

The first section contains a general over-all guide to available products, package options, and recommended operating and handling procedures. This general section is followed by technical data on individual types grouped into fourteen categories. A "Supplementary Information" section lists RCA high-reliability types, shows dimensional outlines for all package types, and lists current RCA application notes on linear integrated circuits.

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The device data shown for some types are indicated as product preview or advance information/preliminary data. **Product preview** data are intended for engineering evaluation of product under development. The type designations and data are subject to change or withdrawal, unless otherwise arranged. **Advance information/preliminary** data are intended for guidance purposes in evaluating new product for equipment design. Such data are shown for types currently being designed for inclusion in our standard line of commercially available products. No obligations are assumed for notice of change of these devices. For current information on the status of product preview or advance information/preliminary data programs, please contact your local RCA sales office.

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Guide to Linear Integrated Circuits

General Guide to Linear Integrated Circuits — Technical Data

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CD40107B	E	F	H	—	—	—	1015	—
CD40109B	E	D	F	K	H	—	1018	—
CD40110B	E	D	F	H	—	—	1125	—
CD40116	E	D	H	—	—	—	1234	—
CDP65C51	E	D	—	—	—	—	1470	—
CDP —								
68HC04P2	M	—	—	—	—	—	1554	—
68HC04P3	M	—	—	—	—	—	1554	—
68HC05C4	—	—	—	—	—	—	TSM-203	—
68HC05D2	E	D	—	—	—	—	1557	—
68HC68A1	E	—	—	—	—	—	1556	—
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68HC68T1	E	D	—	—	—	—	1547	—
CDP1802A	E	D	H	—	—	—	1305	—
CDP1804A	E	D	—	—	—	—	1371	—
CDP1805A	E	D	—	—	—	—	1370	—
CDP6402	E	D	—	—	—	—	1328	—
CDP6805E2	E	D	H	—	—	—	1363	—
CDP6805E3	E	D	—	—	—	—	1503	—
CDP6805F2	E	D	—	—	—	—	1369	—
CDP6805G2	E	D	H	—	—	—	1364	—
CDP6823	E	D	—	—	—	—	1377	—
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LM311N	E	—	—	—	—	—	797	442
LM324N	E	—	—	—	—	—	796	204
LM339AN	E	—	—	—	—	—	795	437
LM339N	E	—	—	—	—	—	795	437
LM358N	E	—	—	—	—	—	1019	210
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LM741CH	T	—	—	—	—	—	531	225
LM741CN	E	—	—	—	—	—	531	225
LM741H	T	—	—	—	—	—	531	225
LM741N	E	—	—	—	—	—	531	225
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LM748CN	E	—	—	—	—	—	531	225
LM748H	T	—	—	—	—	—	531	225
LM748N	E	—	—	—	—	—	531	225
LM1458H	T	—	—	—	—	—	531	225
LM1458N	E	—	—	—	—	—	531	225
LM1558H	T	—	—	—	—	—	531	225
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■ No designated suffix letter for this type in TO-5 style package.

• No designated suffix letter for this type in dual-in-line plastic package.

† No designated suffix letter for this type in dual-in-line ceramic package.

†† Product preview data only.

No designated suffix letter for this type in quad-in-line plastic package.

* In 8-lead dual-in-line Mini-DIP package

‡ In 14-lead dual-in-line plastic package.

★ No designated suffix letter for this type in TO-220-style package with vertical-mount lead form.

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For data on CDPXXXX types, refer to *DATABOOK SSD-260*, CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices*.

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Telecommunications Circuits (Cont'd)

Type No.	Description	Page No.
Codecs/Filters		
CD22352	Codec with A/B Signaling (μLaw)	115
CD22354	Single Chip, Full Feature PCM Codec (μLaw)	116
CD22357	Single Chip, Full Feature PCM Codec (ALaw)	116
CD22302	Single Chip PCM Codec with Filters	106
CD22303	Single Chip PCM Codec with Filters	106
Microcomputers		
CDP68HC05C4	8-Bit with RAM, ROM, I/O, Counter/Timer	—
CDP68HC05D2	8-Bit with RAM, ROM, I/O, Counter/Timer	—
Decoder/Drivers		
CD7211, CD7211A	Four-Digit LCD Decoder/Drivers	174
CD7211M, CD7211AM	Four-Digit LCD Decoder/Drivers	179
DTMF Receivers		
CD22202	Low Power Receiver/Decoder	89
CD22204	Low Power, Low Cost Receiver/Decoder	94
CD22203	5-V Low Power Receiver	93
Generator		
CD22859	DTMF Generator	125
Modems		
CD22223	1200 — Baud FSK	98
Crosspoint Switches		
CD22100	4x4x1 Crosspoint	64
CD22101	4x4x2 Crosspoint	72
CD22102	4x4x2 Crosspoint Set/Reset Input	72
CD54/74HC22106	8x8x1 Crosspoint	130
CD54/74HCT22106	8x8x1 Crosspoint	130
Transient Suppressor—Surgectors		
SGT03U13	30 Volts Uni-Directional	—
SGT06U13	60 Volts Uni-Directional	—
SGT23U13	230 Volts Uni-Directional	—
SGT10S10	100 Volts, 3 Terminal Crowbars—SCR	—
Interface (UARTS)		
CDP1854A	Programmable UART	—
CDP6402	CMOS Universal Asynchronous Receiver/Transmitter (UART)	—
CDP65C61	CMOS Asynchronous Communications Interface Adapter (ACIA)	—
CDP6853	CMOS Asynchronous Communications Interface Adapter (ACIA), Motel Bus	—
Data Transmission and Interface		
CD54/74HC/HCT240	Octal Buffer/Line Drivers, 3-State, Inverting	—
CD54/74HC/HCT241	Octal Buffer/Line Drivers, 3-State, Non-Inverting	—
CD54/74HC/HCT244	Octal Buffer/Line Drivers, 3-State, Non-Inverting	—
CD54/74HC/HCT245	Octal-Bus Transceivers, 3-State, Non-Inverting	—
CD54/74HC/HCT373	Octal Transparent Latches, 3-State Output	—
CD54/74HC/HCT533	Octal Inverting Transparent Latches, 3-State Output	—
CD54/74HC/HCT540	Octal Buffer and Line Drivers, 3-State, Inverting	—
CD54/74HC/HCT541	Octal Buffer & Line Drivers, 3-State, Non-Inverting	—
CD54/74HC/HCT563	Octal Inverting Transparent Latches, 3-State Output	—
CD54/74HC/HCT573	Octal Transparent Latches, 3-State Output	—
CD54/74HC/HCT640	Octal 3-State Bus Transceivers, Inverting	—
CD54/74HC/HCT643	Octal 3-State Bus Transceivers, True/Inverting	—
CD54/74HC/HCT646	Octal Bus Transceivers/Registers,3-State, Non-Inverting	—
CD54/74HC/HCT648	Octal-Bus Transceiver/Registers, 3-State, Inverting	—
CD54/74HC/HCT40105	4-Bits x 16 Words FIFO Registers	—
CD22103	CMOS/SOS 2.048/8.448 Mb/S Transcoder	82
CD22301	PCM Line Repeater	101
CD40116	High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290,* QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CDPXXXX types, refer to *DATABOOK SSD-260,* CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on SGT types, refer to the specific data bulletin for that type shown in the *Index to Devices.*

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Type No.	Description	Page No.
	Telecommunications Circuits (Cont'd)	
Switching Systems		
CD54/74HC/HCT4016	Quad Bilateral Switches	—
CD54/74HC/HCT4051	Single 8-Channel Analog MUX/DEMUX	—
CD54/74HC/HCT4052	Differential 4-Channel Analog MUX/DEMUX	—
CD54/74HC/HCT4053	Triple 2-Channel Analog MUX/DEMUX	—
CD54/74HC/HCT4316	Quad Analog Switches with Latches	—
CD54/74HC/HCT4351	Single 8-Channel Analog MUX/DEMUX with Latches	—
CD54/74HC/HCT4352	Differential 4-Channel Analog MUX/DEMUX with Control Latches	—
CD54/74HC/HCT4353	Triple 2-Channel Analog MUX/DEMUX with Control Latches	—
CD4016	Quad Bilateral Switch	—
CD4051	Single 8-Channel Analog Multiplexer/Demultiplexer	—
CD4052	Differential 4-Channel Analog MUX/DEMUX	—
CD4053	Triple 2-Channel Analog MUX/DEMUX	—
CD4066	Quad Bilateral Switch	—
	Interface Circuits	
Display Drivers, LED		
CA3161	BCD-to-7 Segment Decoder/Driver, Current Output Drive, Common Anode	154
CA3168	Dual BCD-to-7 Segment Decoder/Driver, Common Anode	158
CD4511B	BCD-to-7 Segment Decoder/Driver, Input Latch, Lamp Test and Blanking Controls, Common Cathode	—
CD74HC/HCT4511	High Speed Version of CD4511	—
Display Drivers, LCD		
CD4054	4-Segment Driver, Level Shifters, Input Latch	—
CD4055	BCD-to-7 Segment Decoder/Driver, Level Shifters, Backplane Drive Output	—
CD4056	BCD-to-7 Segment Decoder/Driver, Level Shifters, Input Latch	—
CD4543	BCD-to-7 Segment Decoder/Driver, Input Latch, Blanking Input	—
CD54/74HC/HCT4543	High Speed Version of CD4543B	—
CD7211	4-Digit Decoder/Driver, Input Latches & 4 Independent Strobe Lines	174
CD7211A	Decimal Decoded Version of CD7211	174
CD7211M	4-Digit Decoder/Driver, Input Latches with Microprocessor Interface	179
CD7211AM	Decimal Decoded Version of CD7211M	179
Counter/Decoder/Drivers		
CD4026	BCD Counter/Decoder, CMOS Output	—
CD4033	BCD Counter/Decoder, CMOS Output	—
CD40110	BCD Up/Down Counter/Decoder/Driver	—
Vacuum Fluorescent Drivers		
CA3207	Divide-by-14 Counter, 1 of 14 Decoder/Driver for Vacuum Fluorescent Anode Drive	162
CA3208	14-Bit Shift Register with Output Latch/Driver for Vacuum Fluorescent Grid Drive	162
Arrays for 7 or 8 Segment Interface		
CA3081	7 Transistor Common Emitter Array	151
CA3082	7 Transistor Common Collector Array	151
CA3250	8 Transistor Common Collector Array	171
CA3250	8 Transistor Common Emitter Array	171
Relay or Motor Drivers		
CA3169	Solenoid and Motor Driver (½ H Driver)	595
CA3219A	Quad-Power NAND Driver	603
CA3242	Quad-Gated Inverting Power Driver	606
CA3252	Quad-Gated Non-Inverting Power Driver	610
CD40107B	Dual 2-Input NAND Buffer/Driver	—
Floppy Disk (Read/Write)		
CA570	2-Channel Floppy Disk Read/Write Circuit	142
CA575	4-Channel Floppy Disk Read/Write Amplifier	147

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

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Type No.	Description	Page No.
	Interface Circuits (Cont'd)	
Logic Level Converters		
CD4049UB	Hex Inverting High-to-Low Voltage Interface	—
CD54/74HC/HCT4049	High Speed Version of CD4049UB	—
CD4050B	Hex Non-Inverting High-to-Low Voltage Interface	—
CD54/74HC/HCT4050	High-Speed Version of CD4050B	—
CD40109B	Quad Low-to-High Voltage Interface	—
CD40116	Octal Bi-Directional Inverting High/Low Interface	—
Schmitt Triggers		
CA3098	Programmable Schmitt Trigger with Memory	450
CA3099	Similar to the CA3098 with Voltage Regulator	457
CD4093B	Quad 2 Input NAND Schmitt Triggers	—
CD40106B	Hex Inverter Schmitt Trigger	—
CD54/74HC/HCT14	High Speed Quad 2-Input NAND Schmitt Trigger	—
CD54/74HC/HCT132	High Speed Hex Inverter Schmitt Trigger	—
Quad Analog Switches		
CD4016	Quad Bilateral Switch	—
CD54/74HC/HCT4016	High Speed, Low R_{ON} Version of the CD4016B	—
CD4066B	Improved Linearity Version of CD4016B	—
CD54/74HC/HCT4066	High Speed, Low R_{ON} Version of CD4066B	—
CD54/74HC/HCT4316	Quad Bilateral Switch	—
Analog Multiplexers/Demultiplexers		
CD4051B	Single 8 Channel	—
CD54/74HC/HCT4051	High Speed, Low R_{ON} Version of CD4051B	—
CD54/74HC/HCT4351	Similar to HC/HCT4051 with Latch	—
CD4052B	Differential 4 Channel	—
CD54/74HC/HCT4052	High Speed, Low R_{ON} Version of CD4052B	—
CD54/74HC/HCT4352	Similar to HC/HCT4051 with Latch	—
CD4053B	Triple 2 Channel	—
CD54/74HC/HCT4053	High Speed, Low R_{ON} Version of CD4053B	—
CD54/74HC/HCT4353	Similar to HC/HCT4053 with Latch	—
CD4067B	Single 16 Channel	—
CD4097B	Differential 8 Channel	—
	Operational Amplifiers	
General Purpose — Single Amplifier		
CA081	BiMOS MOS Input Internally Compensated	191
CA101	Externally Compensated	198
CA201	Externally Compensated	198
CA301A	Externally Compensated	198
CA307	Internally Compensated	221
CA741	Internally Compensated	225
CA748	Externally Compensated	225
CA3193	BiMOS Precision OP Amp	344
CA3420	Low Voltage BiMOS Op Amp	398
CA3440	Nanopower BiMOS Op Amp	403
CA3450	Video Line Driver, High Speed	409
CA3493	Precision BiMOS Op Amp	414
CA6741	Low Noise Version of CA741	430
General Purpose — Dual Amplifiers		
CA082	BiMOS MOS Input, Internally Compensated	191
CA158	Internally Compensated, PNP Input	210
CA258	Internally Compensated, PNP Input	210
CA358	Internally Compensated, PNP Input	210
CA747	Dual 741 with offset Null	225
CA1458	Dual 741 without OFF-Null	225
CA1558	Dual 741 without OFF-Null	225
CA2904	Internally Compensated, PNP Input	210
CA5422	Low Voltage BiMOS Op Amps/Comparators	425

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

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Type No.	Description	Page No.
	Differential Amplifier Circuits	
CA3000	DC Amplifier	475
CA3001	Video and Wideband Amplifier	482
CA3002	IF Amplifier	488
CA3005	RF Amplifier	494
CA3006	RF Amplifier	494
CA3026	Dual Independent	501
CA3028	Differential/Cascade Amplifier	509
CA3040	Video and Wideband Amplifier	520
CA3049	Dual High-Frequency	526
CA3050	Dual Differential Amplifier	531
CA3051	Dual Differential Amplifier	531
CA3053	Differential/Cascade Amplifier	509
CA3054	Dual Differential Amplifier	501
CA3102	Dual High-Frequency	526
	Power Control Circuits	
Voltage Regulators		
CA723	Adjustable Regulator	541
CA1523	Variable Interval Pulse Regulator	549
CA1524	Pulse Width Modulator	554
CA2524	Pulse Width Modulator	554
CA3085	Adjustable Regulator	588
CA3177	Operational Amplifier/Comparator	601
CA3524	Pulse Width Modulator	554
Schmitt Triggers		
CA3098	Programmable with Memory	450
CA3099	Similar to CA3098 with Voltage Regulator	457
Power Amplifiers		
CA3020	Multi-Purpose Wideband Power Amplifier	569
CA3094	Single Transconductance Amplifier	275
AC Power Control		
CA3059	Zero-Voltage Crossing Switch System	577
CA3079	Same as CA3059 Without Protection and Inhibit Functions	577
Solenoid & Motor Drivers		
CA3169	½ H Driver	595
CA3219A	Quad-Gated Inverting Power Driver	603
CA3242	Similar to CA3219A, but with Output Overcurrent Protection	606
CA3252	Similar to CA3219A, Non-Inverting	610
CD40107B	Dual 2-Input NAND Buffer/Driver	—
Automotive		
CA3165	Ignition Switch Driver	727
CA3169	Solenoid & Motor Driver	595
CA3228	Speed Control System	733
	Special Function Circuits	
CA555	Analog Timer	836
CA3020	Multi-Purpose Wideband Diff. Input & Output Power Amplifier	569
CA3048	Four Independent AC Amplifiers	763
CA3052	Same as CA3048 except RIAA Noise Tests	770
CA3059	Zero-Voltage Crossing Switch System	577
CA3079	Same as CA3059 without Protection and Inhibit Functions	577
CA3091	Analog Multiplier	615
CA3094	Single Transconductance Amplifier	275
CA3164A	Single Chip Alarm System	627
CA3177	Operational Amplifier/Comparator	601
CA3215	FM-IF Amplifier/Sector Limiter	825

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

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Type No.	Description	Page No.
	Special Function Circuits (Cont'd)	
CD4046B	CMOS Micropower Phase-Locked Loop	—
CD4045B	21-Stage Oscillator/21-Stage Counter	—
CD4536B	Oscillator/Programmable 24-Stage Counter	—
CD4541B	Oscillator/Programmable 24-Stage Counter, Only 4 Stage Available	—
	Arrays	
Amplifier		
CA3026	Dual Differential Amplifier	501
CA3048	Four Independent AC Amplifiers	763
CA3049	Dual High Freq. Differential	526
CA3050	Dual Differential Amplifier with emitter follower inputs	531
CA3051	Same as CA3050, except in a plastic pkg.	531
CA3052	Same as CA3048, except RIAA noise Tests	770
CA3054	Same as CA3026, except in a plastic pkg.	501
CA3060	Triple Transconductance Amplifier	247
CA3102	Similar to CA3049 except in a plastic pkg.	526
Diode		
CA3019	One full wave bridge & two independent diodes	646
CA3039	Five independent diodes with cathode connected to substrate	648
CA3141	10 High Voltage Diodes, 3 pairs common cathode, 2 pairs common anode	703
Transistor		
CA1724	Four individual 80V, 1A transistor	637
CA1725	Four individual 70V, 1A transistor	637
CA3018	Four Monolithic transistors, 2 independent, emitter follower	640
CA3045	Five Monolithic transistors, 3 independent, 2 diff. connected	652
CA3046	Same as CA3045 except in a plastic pkg.	652
CA3050	Dual differential amp. with emitter follower	531
CA3051	Same as CA3050 except in a plastic pkg.	531
CA3081	Seven transistor common emitter array	151
CA3082	Seven transistor common collector array	151
CA3083	Five monolithic, independent, gen. purpose trans.	658
CA3086	Five mnolithic transistors, 3 independent, 2 diff. connected	662
CA3096	2 PNP, 3 NPN Monolithic transistors	667
CA3097	Thyristor - PUT, SCR, Zener PNP/NPN, and independent NPN transistor	677
CA3118	High voltage version of CA3018	688
CA3127	Five independent transistors	695
CA3138	Four individual high current transistors	700
CA3146	High voltage version of CA3046	688
CA3183	High voltage version of CA3083	688
CA3227	High freq. version of CA3127	706
CA3246	High freq. version of CA3146	706
CA3250	Common-emitter array	171
CA3251	Common-collector array	171
CA3600	CMOS array, 3 PMOS, 3NMOS Device	709
CD74HCU04	Hex Inverter (Unbuffered)	—
	Automotive Circuits	
Engine and Drive Train Controls		
CA324	Quad operational amplifier	204
CA339	Quad voltage comparator	437
CA358	Dual operational amplifier	210
CA3165	Electronic switching circuit	727
CA3169	Solenoid and Motor Driver	595
CA3219A	Quad-Power NAND Driver	603
CA3242	Quad-Gated Inverting Power Driver	606
CA3252	Quad-Gated Non-Inverting Power Driver	610
CD4538B	CMOS Dual Precision Monostable Multivibrator	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

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Type No.	Description	Page No.
	Automotive Circuits (Cont'd)	
Engine and Drive Train Controls (Cont'd)		
CDP1802A	8-Bit Microprocessor	—
CDP1804A	8-Bit Microcomputer	—
CDP1805A	8-Bit Microprocessor	—
CDP6805E2	8-Bit Microprocessor	—
CDP6805E3	8-Bit Microprocessor	—
CDP6805F2	8-Bit Microcomputer	—
CDP6805G2	8-Bit Microcomputer	—
CDP6823	Parallel Interface	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05C4	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68A1	SPI A/D Converter	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—
Features (Optional Equipment)		
CA3169	Solenoid and Motor Driver	595
CA3219A	Quad-Power NAND Driver	603
CA3228	Speed Control System	733
CA3232	÷20 Prescaler	828
CA3242	Quad-Gated Inverting Power Driver	606
CA3252	Quad-Gated Non-Inverting Power Driver	610
CA3259	Stereo Sound Volume/Tone Control	832
CD4517B	CMOS Dual 64-Stage Static Shift Register	—
CD40106B	CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC05F2	8-Bit Microcomputer	—
Multiplex Communications		
CD4016B	CMOS Quad Bilateral Switch	—
CD4006B	CMOS 18-stage Static Shift Register	—
CD4512B	CMOS 8-Channel Data Selector	—
CD54/74HC/HCT157	Quad 2-Input Multiplexer	—
CD54/74HC/HCT257	Quad 2-Input Multiplexer, 3-State	—
CDP1802A	8-Bit Microprocessor	—
CDP1804A	8-Bit Microcomputer	—
CDP1805A	8-Bit Microprocessor	—
CDP1863	8-Bit Programmable Counter	—
CDP6402	Programmable UART	—
CDP6823	Parallel Interface	—
CDP6853	Asynchronous Communications Interface Adapter	—
CDP6805E2	8-Bit Microprocessor	—
CDP6805E3	8-Bit Microprocessor	—
CDP6805F2	8-Bit Microcomputer	—
CDP6805G2	8-Bit Microcomputer	—
CDP65C51E1	Asynchronous Communications Interface Adapter	—
CDP65C51E2	Asynchronous Communications Interface Adapter	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC68A1	SPI A/D Converter	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290,* QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CDPXXXX types, refer to *DATABOOK SSD-260,* CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices.*

Product Selection Guide

Automotive Circuits (Cont'd)

Type No.	Description	Page No.
Body Computer		
CD54/74HC/HCT00	Quad 2-Input NAND Gate	—
CD54/74HC/HCT244	Octal Buffer/Line Driver; 3-State	—
CD54/74HC/HCT245	Octal Bus Transceiver; 3-State	—
CD54/74HC/HCT373	Octal Transparent Latch; 3-State	—
CD54/74HC/HCT374	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State	—
CDM5364	8K x 8 ROM	—
CDM5365	8K x 8 ROM	—
CDM6116	2K x 8 RAM	—
CDM6264	8K x 8 RAM	—
CDM53128	16K x 8 ROM	—
CDM53256	32K x 8 ROM	—
CDP1851	Programmable I/O Interface	—
CDP1852	Byte-Wide I/O Port	—
CDP1855	8-Bit Programmable Multiply/Divide Unit	—
CDP1863	8-Bit Programmable Counter	—
CDP6818	Real Time Clock, MOTEL Bus	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05C4	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—
CDP68HC68T1	SPI Real-Time Clock	—
Entertainment		
CA3088	AM Receiver Subsystem and general purpose amplifier array	781
CA3089	FM IF System	785
CA3130	BiMOS OpAmp	292
CA3189	FM IF System	804
CA3195	RC Phase-Lock-Loop Stereo Decoder	810
CA3202	TV Horiz./Vert. Countdown Digital Sync System	1020
CA3209	FM IF System	820
CD4052	CMOS Analog Multiplexer/Demultiplexer	—
CDP6818	Real Time Clock, MOTEL Bus	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68R2	SPI RAM 256 Bytes	—
CDP68HC68T1	SPI Real Time Clock	—
Driver Information/Display		
LCD		
CD4054B	4-Segment Display Driver	—
CD4055B	BCD-to-7 Segment Decoder/Driver with Display freq. output	—
CD4056B	BCD-to-7 Segment Decoder/Driver with Strobed-latch function	—
CD4543B	BCD-to-7 Segment Decoder/Driver with Strobed-latch function	—
CD7211	Four-Digit LCD Decoder/Driver	174
CD7211A	Four-Digit LCD Decoder/Driver	174
CD7211M	Four-Digit LCD Decoder/Driver	179
CD7211AM	Four-Digit LCD Decoder/Driver	179
CD54/74HC/HC74543	BCD-to-7 Segment Latch/Decoder/Driver	—
LED		
CA3081	Common-emitter transistor array	151
CA3082	Common-collector transistor array	151
CA3083	High-Current NPN Transistor Array	658
CA3161	BCD-to-7-Segment Decoder/Driver, Current Output Driver, common anode	154

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CDPXXXX types, refer to *DATABOOK SSD-260*, CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices*.

Product Selection Guide

Type No.	Description	Page No.
	Automotive Circuits (Cont'd)	
Led (Cont'd)		
CA3168	Dual BCD-to-7-Segment Decoder/Driver, common anode	158
CA3250	Common-emitter array	171
CA3251	Common-collector array	171
CD4026B	Decade counter/divider with 7-segment display outputs and display enable	—
CD4033B	Decade counter/divider with 7-segment display outputs and ripple blanking	—
CD4511B	BCD-to-7-Segment Latch Decoder Driver	—
CD54/74HC/HCT4511	High-Speed version of the CD4511B	—
CD40110B	Decade Up-Down Counter/Latch/Display Driver	—
Incandescent		
CA3081	Common-emitter transistor array	151
CA3082	Common-collector transistor array	151
CD4026B	Decade Counter/Divider with 7-segment display outputs and display enable	—
CD4033B	Decade counter/divider with 7-segment display outputs and ripple blanking	—
CD4511B	BCD-to-7 Segment Latch Decoder Driver	—
CD54/74HC/HCT4511	High-Speed Version of the CD4511B	—
CD4041UB	Quad true/complement buffer	—
CD4049UB	Hex buffer/converter (inverting)	—
CD54/74HC/HCT4049	High Speed Version of the CD4049UB	—
CD4050B	Hex buffer/converter (non-inverting)	—
CD54/74HC/HCT4050	High Speed Version of the CD4050B	—
CD40107B	Dual 2-Input NAND buffer/driver	—
Vacuum Fluorescent		
CA3207	Divide-by-14 counter, 1 of 14 Decoder/Driver for vacuum fluorescent anode drive	162
CA3208	14-Bit shift register with output latch/driver	162
CD4026B	Decade counter/divider with 7-segment display outputs and display enable	—
CD4033B	Decade counter/divider with 7-segment display outputs and ripple blanking	—
CD4511B	BCD-to-7-Segment latch decoder driver	—
CD54/74HC/HCT4511	High speed version of the CD4511B	—
General Purposes		
CD4094B	8-Stage Shift-and-Store Bus Register	—
CDM5364	8K x 8 ROM	—
CDM5365	8K x 8 ROM	—
CDM53128	16K x 8 ROM	—
CDM53256	32K x 8 ROM	—
CDP1863	8-Bit Programmable Counter	—
CDP6818	Real Time Clock, MOTEL Bus	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—
	Radio/Communication Circuits	
AM/FM Radio		
CA2111A	FM IF Amplifier-Limiter and Quadrature Detector	743
CA2136A	FM IF Amplifier-Limiter and Quadrature Detector	748
CA3011	Wideband amplifier	750
CA3012	Wideband amplifier	750

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CDPXXXX types, refer to *DATABOOK SSD-260*, CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices.*

Product Selection Guide

Product Selection Guide

Type No.	Description	Page No.
	Video Monitor Circuits (Cont'd)	
525/625 Line Horizontal/Vertical Systems		
CA555	Timer	836
CA1391	TV Horiz. Processor, Positive Sawtooth Input	842
CA1394	TV Horiz. Processor, Negative Sawtooth Input	842
CA3154	TV Sync/AGC/Horiz. Signal Processor	868
CA3210	Horiz./Vert. Countdown digital sync system for 525-line operation	882
CA3218	TV Horiz./Vert. Countdown digital sync. system	901
CA3223	Horiz./Vert. Countdown digital sync. system for 625-line operation	882
Sync AGC		
CA3142	TV Sync Processor	995
Auto CRT Bias		
CA3224	Automatic picture tube bias circuit	906
Modulators		
CA1890	TV Video/Audio RF Modulator	847
CA3026	Dual Independent Diff. Amplifier Array	501
CA3049	Dual High-Freq. Differential Amplifier	526
CA3054	Dual Independent Diff. Amplifier Array	501
CA3102	Similar to the CA3049 Except Separate Substrate Connection	526
Video Switch/Multiplexers		
CA3256	CMOS/BiMOS Analog Video Switch and Amplifier	925
CD4097B	Differential 8-Channel Multiplexer/Demultiplexer	—
CD54/74HC/HCT4016	Quad Bilateral Switch	—
CD54/74HC/HCT4051	8-Channel Analog Multiplexer/Demultiplexer	—
CD54/74HC/HCT4052	Dual 4-Channel Analog Multiplexer/Demultiplexer	—
CD54/74HC/HCT4053	Triple 2-Channel Analog Multiplexer/Demultiplexer	—
CD54/74HC/HCT4066	Quad Bilateral Switch	—
CD54/74HC/HCT4067	16-Channel Analog Multiplexer/Demultiplexer	—
Regulators		
CA723	Voltage Regulator	541
CA1523	Voltage Regulator Control Circuit For Variable Switching Regulator	549
CA3085	Positive Voltage Regulator	588
CA3177	Operational Amplifier/Comparator	601
CA3524	Regulating Pulse Width Modulator	554
Broadland Video Amplifiers		
CA081	BiMOS Op Amp — Single Amplifier	191
CA082	BiMOS Op Amp — Dual Amplifier	191
CA3001	Video & Wideband Amplifier	482
CA3002	IF Amplifier	488
CA3020	Multi-Purpose Wideband Power Amplifier	569
CA3040	Video and Wideband Amplifier	520
CA3054	Dual Differential Amplifier	501
CA3071	Chroma Signal Processor	966
CA3080	Programmable Op Amp	266
CA3094	Programmable Power Switch/Amplifier	275
CA3100	Wideband Single Amplifier	286
CA3130	BiMOS Operational Amplifier	292
CA3183	High Voltage Transistor Arrays	688
CA3227	High Voltage Transistor Array	706
CA3246	High Voltage Transistor Array	706
CA3250	Common-Emitter Array	171
CA3256	Analog Video Switch and Amplifier	925
CA3280	Dual Variable Op Amp	375
CA3410	Quad Operational Amplifier	388
CA3450	Video Line Driver, High Speed	409
CD74HCU04	Hex Inverter (Unbuffered)	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

Product Selection Guide

TV/CATV Circuits

Type No.	Description	Page No.
AFT		
CA7607	Video IF Amplifier System	1030
CA7611	Video IF Amplifier System	1030
LM1822N	Video IF Amplifier/PLL Detector System	1034
Chroma/Luma Systems		
CA1398	TV Chroma Processor	948
CA3070	TV Chroma System	966
CA3071	TV Chroma System	966
CA3072	TV Chroma System	966
CA3121	TV Chroma Amplifier/Demodulator	981
CA3125	TV Chroma Demodulator	987
CA3126	TV Chroma Processor	854
CA3135	TV Luminance Processor	861
CA3151	Single Chip TV Chroma Processor/Demodulator	1002
CA3170	TV Chroma System	1011
CA3172	TV Chroma Demodulator	1017
CA3194	Single-Chip PAL Luminance/Chroma Processor	874
CA3217	Single Chip TV Chroma/Luma Processor	892
Tuning Control		
CA3140	BiMOS Op Amp	307
CA3163	VHF/UHF Prescaler	791
CA3199	VHF/UHF ÷4 Prescaler	815
Regulators		
CA1523	Variable Interval Pulse Regulator	549
CA1524	Pulse Width Modulator	554
CA2524	Pulse Width Modulator	554
CA3085	Adjustable Regulator	588
CA3524	Pulse Width Modulator	554
CA3177	Operational Amplifier/Comparator	601
IR Remote Control		
CA3237	IR Remote-Control Amplifier	1027
525-Line/625-Line Horizontal/Vertical Systems		
CA1391	TV Horiz. Processor, Positive Sawtooth Input	842
CA1394	TV Horiz. Processor, Negative Sawtooth Input	842
CA3154	TV Sync/AGC/Horiz. Signal Processor	868
CA3177	Operational Amplifier/Comparator	601
CA3202	TV Horiz./Vert. Countdown Digital Sync System	1020
CA3210	Horiz./Vert. Countdown Digital Sync System for 525-line operation	882
CA3218	TV Horiz./Vert. Countdown Digital Sync. System	901
CA3223	Horiz./Vert. Countdown Digital Sync System for 625-line operation	882
Sync/AGC		
CA3142	TV Sync Processor	995
Luminance Processors		
CA3135	TV Luminance Processor	861
CA3156	Video/Chroma Processor	1006
Pix IF		
CA3068	TV Video IF System	959
CA7607	Video IF Amplifier System	1030
CA7611	Video IF Amplifier System	1030
LM1822N	Video IF Amplifier/PLL Detector System	1034
Sync Generators		
CA3254	RS-170 Sync Generator	915
CA3255	RS-170 Sync Generator	915
CD22402	LSI Sync Generator	930

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

Product Selection Guide

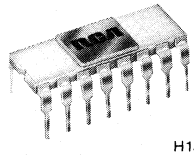
Packages

RCA linear and digital device packages are identified by letters as indicated in the following chart. When ordering a linear or digital device, it is important that the appropriate suffix letter(s) be affixed to the basic type number of the device.

Package	Suffix Letter		
	CA Types	CD Types	LM Types
Dual-In-Line Welded-Seal Ceramic Package	D	D	—
Single-In-Line Plastic Package (SIP)	—	—	—
Dual-In-Line Plastic Package	E	E	N
Dual-In-Line Frit-Seal Ceramic Package	F	F	—
Chip	H	H	—
Modified Dual-In-Line Plastic Package with "Power Slab"	EM	—	—
Modified Quad-In-Line Plastic Package	QM	—	—
Quad-In-Line Plastic Package	Q	—	—
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)	S	—	—
TO-5 Style Package with Straight Leads	T	—	H
TO-220 Style Package with Vertical-Mount Lead Form *	—	—	—
TO-5 Style Package with Radial Formed Leads	V1	—	—
Staggered Quad-In-Line Plastic Package	W	—	—
Ceramic Flat Package	—	K	—
Small Outline Packages (SO)	M	M	—

*TO-220 Style Package is also available with horizontal-mount lead form. Indicate "M" suffix for modified version, i.e., CA3169M.

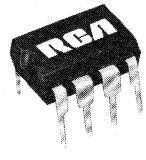
D Suffix
Dual-In-Line Welded-Seal Ceramic Package



H1844

14, 16, and 18-lead versions

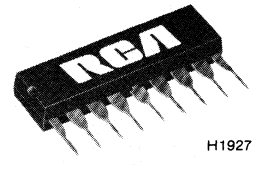
E Suffix
Dual-In-Line Plastic Package



H1934

8, 14, 16, 18, 20, 22, 24, 28, and 40-lead versions

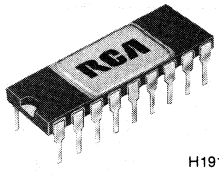
Single-In-Line (SIP) Plastic Package



H1927

9-Lead

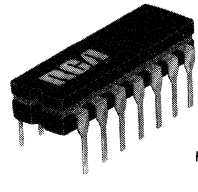
D Suffix
Dual-In-Line
Side-Brazed Ceramic Package



H1910

16 and 18-lead versions

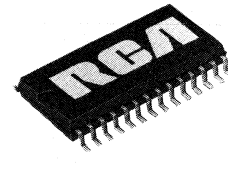
F Suffix
Dual-In-Line Frit-Seal Ceramic Package



H1806

14, 16, and 18-lead versions

M Suffix
Small-outline Package (SO)

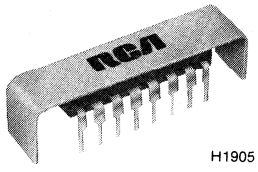


H1943

8, 14, 16, 20, 24, and 28-lead versions

Packages (Cont'd.)

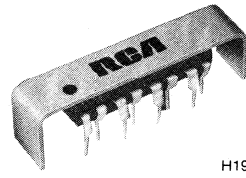
EM Suffix
Modified 16-lead Dual-In-Line Plastic Package with "Power Slab"



H1905

CA3134EM only

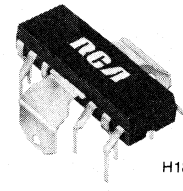
QM Suffix
Quad-In-Line Plastic Package (QUIP) with "Power Slab"



H1906

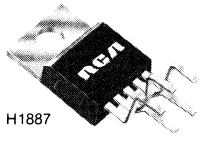
16-lead version

Q Suffix
Modified 16-lead QUIP



H1825

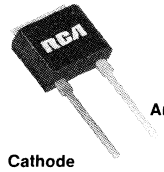
VERSA-V1 TO-220 Style Plastic Package with Vertical-Mount Lead Form



H1887

(Versions with horizontal-mount lead form are also available).

No Designated Suffix For This Package Type Modified TO-202 Vertical-Mount Lead Form



Anode

Cathode

H1940

S Suffix
TO-5 Style Package with Dual-In-Line Formed Leads (DIL-CAN)

H1787

8-lead version

T Suffix
TO-5 Style Package with Straight Leads

H1463

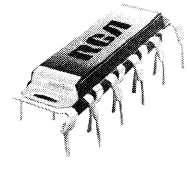
8, 10, and 12-lead versions

V1 Suffix
TO-5 Style Package with Radial Formed Leads

H1561

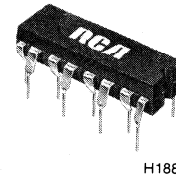
8, 10, and 12-lead versions

No Designated Suffix for this Package Type Shielded 20-lead Quad-In-Line Plastic Package



H1704

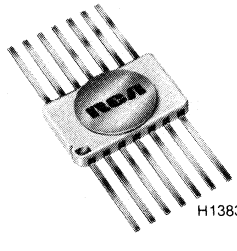
W Suffix
Staggered Quad-In-Line Plastic Package



H1885

14 and 16-lead versions

K Suffix
Ceramic Flat Package



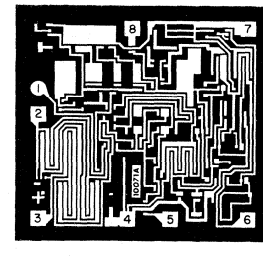
H1383R1

14, 16, and 24-lead version

JEDEC TO-72

H1299

H Suffix Chip



92CM-32235

Operating and Handling Considerations

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of linear integrated circuits and MOS field-effect transistors.

The ratings included in RCA data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by integrated circuits and MOSFET's makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of these devices provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

SMALL-SIGNAL MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOSFETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in a MOSFET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOSFETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOSFETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene insulating "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

INTEGRATED CIRCUITS

Mounting

Integrated circuits are normally supplied with tin-lead dipped leads to facilitate soldering into circuit boards.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat packages, less than the lead thickness. When solder-dipped leads are formed, they must be reflowed or redipped within 40 mils of package body. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

*Mil-M-38510A, paragraph 3.5.6.1(a), lead material

Operating and Handling Considerations

CMOS INTEGRATED CIRCUITS

Handling

All CMOS gate inputs have a diode or resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect CMOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. It is desirable to use ionizers in the handling and assembly areas to minimize damage from electrostatic discharge (ESD). See ICAN-6525, "Handling and Operating Considerations from MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either the low rail (V_{SS}, V_{EE}, or GND) or the high rail (V_{CC} or V_{DD}), whichever is appropriate for the logic circuit involved. A floating input on a high-current type operating at a supply voltage above 5 V such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum rated power dissipation to be exceeded and may result in damage to the device.

Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to the high or low voltage supply rails. A useful range of values for such resistors, is from 10 kilohms to 1 megohm. Pins that are I/O must have a terminating resistor.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value or less than the absolute maximum rating. This value is either 10 mA or 20 mA depending on device family. Input currents of less than the maximum rating prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to the high or low supply rail can damage many of the higher-output-current types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For the QMOS HC/HCT/HCU types, outputs may be shorted to V_{CC} (5 V ± 10%) for 1 second maximum and only one output at a time. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below the device maximum rated output power.

For detailed CMOS IC operating and handling considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated circuits".

POWER SUPPLY DISTRIBUTION AND DECOUPLING

Higher speeds, faster edges and higher output-drive currents cause higher-frequency current transients to be imposed on ground and V_{CC} rails of an IC.

For LSI, HC and HCT families, consideration of power supply distribution and decoupling become important. Before decoupling can be utilized for noise reduction, there must first be a good power supply distribution network. A good ground connection system and capacitive decoupling must be employed. For details refer to Application Note ICAN-7329.

CMOS Power Distribution

Power distribution should be a prime consideration in all CMOS designs. Although dc power dissipation is very low, dynamic power (due to switching transients) can be high. High voltage and/or low temperature operation will increase dynamic current transients.

A low impedance power source and supply to ground capacitance bypassing near each device will significantly reduce noise generation on signal and power lines; system reliability is greatly enhanced.

LINEAR INTEGRATED CIRCUITS
BiMOS, Bipolar, and CMOS

In linear integrated circuits that employ diode isolation techniques, there are numerous parasitic devices associated with the primary circuit components. These devices may be activated or turned on by driving inputs and/or outputs beyond the supply-voltage range of the integrated circuit. For example, externally driving the collector terminal of a transistor array below the isolation potential or substrate will forward bias the parasitic isolation diode shown in Fig. 1. Since the collector region and substrate form a comparatively large-area diode, high currents will be sustained, often at levels sufficiently high to melt the metalization to these devices.

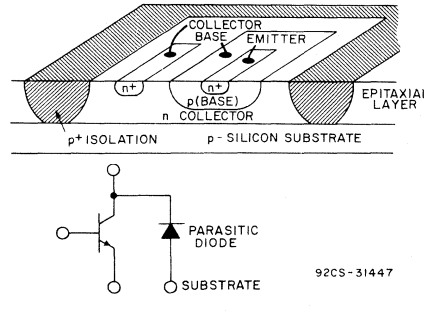


Fig. 1 - Sectional view of conventional "vertical" n-p-n transistor commonly used on IC chip. Also shown is the equivalent circuit and associated parasitic diode.

Operational amplifiers like the 741 and other similar structures can be damaged by driving a positive-going signal into the input device with power off. The signal will forward bias the collector-to-base junction of the input transistor and, if the positive supply impedance is low enough, drive current back into the supply. Current above the maximum rating may result in damage to the amplifier.

Supply transients are another possible source of damage. They can activate or trigger parasitic SCR devices which can cause an integrated circuit to draw extremely high current. If the supply impedance is sufficiently high, the SCR gate drive in the latched condition is removed by the

Operating and Handling Considerations

limiting action of the supply. If the supply impedance is too low, the device will continue to demand high currents until the metalization of either the device or the pc board fuses open.

Although device manufactures take precautions to keep the number of these parasitic devices at a minimum, normal device process variations occasionally make the formation of parasitic devices inevitable. It is essential, therefore, that the user take precautions to insure that an integrated circuit is never operated beyond its maximum ratings, even under momentary transient conditions.

SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40° C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. MOS chips that are ESD sensitive should be handled in an environment where ionizers are employed.
4. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
5. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Interchangeability Directory

Industry Type	RCA Replacement Type
AD301AH	CA301AT,LM301AH
AD301AN	CA301AE,LM301AN
AD741H	CA741T,LM741H
AD741N	CA741E,LM741N
AD741CH	CA741CT,LM741CH
AD741CN	CA741CE,LM741CN
AD2020	CA3162E
AMLM301AH	CA301AT,LM301AH
AMLM301H	CA301T,LM301AH
AMLM307H	CA307T,LM307H
AMLM311H	CA311T,LM311H
AM723HC	CA723CT,LM723CH
AM723HM	CA723T,LM723H
AM741HC	CA741CT,LM741CH
AM741HM	CA741T,LM741H
AM747HC	CA747CT
AM747HM	CA747T
AM748HC	CA748CT,LM748CH
AM1458H	CA1458T,LM1458H
AM1558H	CA1558T,LM1558H
HA1-2630	CA3020
HA1-2650	LM1558A,CA1558E
HA1-2655	LM1458H,CA1458E
HA1-2720	CA6078
HA2-2311-5	CA311T,LM311H
HA2-2520	CA3100T
HA2-2650	CA1558T,LM1558H
HA2-2655	CA1458T,LM1458H
HA2-2720	CA3078E
ITT3065N	CA3065E
LA2113	CA3258
LA3373	CA3259
LF356J	CA081E
LM100	CA3085E
LM124N	CA124E
LM139J	CA139F
LM139AN	CA139AE
LM139AJ	CA139AF
LM139N	CA139E
LM158AH	CA158AT
LM158AN	CA158AE
LM158AT	CA158AT
LM158N	CA158E
LM158P	CA158E
LM158T	CA158T
LM201AN	CA201AE
LM201AP	CA201AE
LM201AV	CA201AE
LM201H	CA201T
LM201N	CA201E
LM201T	CA201T
LM224N	CA224E
LM239AD	CA239AF
LM239AF	CA239AF
LM239AJ	CA239AF
LM239AN	CA239AE
LM239D	CA239F
LM239F	CA239F
LM239J	CA239F
LM239N	CA239E
LM258AH	CA258AT
LM258AN	CA258AE
LM258AT	CA258AT
LM258H	CA258T
LM258L	CA258T
LM258N	CA258E
LM258P	CA258E
LM258T	CA258T
LM301AH	CA301AT,LM301AH
LM301AL	CA301AT,LM301AH
LM301AN	CA301AE,LM301AN
LM301AP	CA301AE,LM301AN
LM301AT	CA301AT,LM301AH
LM301AV	CA301AE,LM301AN
LM307H	CA307T,LM307H
LM307N	CA307E,LM307N
LM307T	CA307T,LM307H
LM311H	CA311T,LM311H
LM311L	CA311T,LM311H
LM311N	CA311E,LM311N
LM311P	CA311E,LM311N
LM311T	CA311T,LM311H
LM324N	CA324E,LM324N
LM339AJ	CA339AF
LM339AN	CA339AE,LM339AN
LM339D	CA339F
LM339F	CA339F
LM339J	CA339F
LM339N	CA339E,LM339N
LM358AH	CA358AT
LM358AN	CA358AE
LM358AT	CA358AT
LM358H	CA358T
LM358L	CA358T
LM358N	CA358E
LM358P	CA358E
LM358T	CA358T
LM393N	CA3290E
LM555CH	CA555CT,LM555CH
LM555CN	CA555CE,LM555CN
LM555H	CA555T
LM555N	CA555E,LM555N
LM723CH	CA723CT,LM723CH
LM723CN	CA723CE,LM723CN
LM723H	CA723T,LM723H
LM723N	CA723E,LM723N
LM741CH	CA741CT,LM741CH
LM741CN	CA741CE,LM741CN
LM741H	CA741T,LM741H
LM741N	CA741E,LM741N
LM746N	CA3072
LM747CH	CA747CT
LM747CN	CA747CE
LM747H	CA747T
LM748CH	CA748CT,LM748CH
LM748CN	CA748CE,LM748CN
LM748H	CA748T,LM748H
LM1391N	CA1391E
LM1394N	CA1394E
LM1458H	CA1458T,LM1458H
LM1458N	CA1458E,LM1458N
LM1558H	CA1558T,LM1558H
LM1558N	CA1558E
LM2111N	CA2111AE
LM2901J	CA2901F
LM2901N	LM2901N
LM2902N	LM2902N
LM2904N	CA2904N,LM2904N
LM2904P	CA2904E,LM2904N
LM3011H	CA3011
LM3018H	CA3018
LM3018AH	CA3018A
LM3019H	CA3019
LM3026H	CA3026
LM3028AH	CA3028A
LM3028B	CA3028B
LM3039H	CA3039
LM3045D	CA3045,CA3045F
LM3046N	CA3046
LM3053H	CA3053
LM3054N	CA3054
LM3065N	CA3065
LM3070N	CA3070
LM3071N	CA3071
LM3075N	CA3075
LM3086N	CA3086
LM3089N	CA3089E, CA3189E
LM3126N	CA3126E
LM3146AN	CA3146AE
LM3401N	CA3401E
M5141T	CA741CT,LM741CH
MC1357P	CA2111AE
MC1357PQ	CA2111AQ
MC1358P	CA3065
MC1370P	CA3070
MC1371P	CA3071
MC1375P	CA3075
MC1389P	CA3089E, CA3189E
MC1391P	CA1391E
MC1394P	CA1394E
MC1398P	CA1398E
MC1455G	CA555CT,LM555CH
MC1455P1	CA555CE,LM555CN
MC1458G	CA1458T,LM1458H
MC1458P1	CA1458E,LM1458N
MC1458T	CA1458T,LM1458H
MC1555G	CA555T
MC1555P1	CA555CE,LM555CN
MC1558G	CA1558T,LM1558H
MC1558P1	CA1558E
MC1558T	CA1558T,LM1558H
MC1723CG	CA723CT,LM723CH
MC1723CP	CA723CE,LM723CN
MC1723G	CA723T,LM723H
MC1741CG	CA741CT,LM741CH
MC1741CP1	CA741CE,LM741CN
MC1741G	CA741T,LM741H
MC1747CG	CA747CT
MC1747G	CA747T
MC1748CG	CA748CT,LM748CH
MC1748CP1	CA748CE,LM748CN
MC1748G	CA748T,LM748H
MC3346P	CA3046
MC3386P	CA3086
MC34001BP	CA081AE
MC34001P	CA081E
MC34002BP	CA082AE
MC34002P	CA082E
MC3401P	CA3401E
MPS7682	CA3306CE
NE555P	CA555CE,LM555CN
NE555L	CA555CT,LM555CH
NE555T	CA555CT,LM555CH
NE555V	CA555CE,LM555CN
PM741J	CA741T,LM741H
PM741CJ	CA741CT,LM741CH
PM747K	CA747T
PM747CK	CA747CT
RC555NB	CA555CE,LM555CN
RC555T	CA555CT,LM555CH
RC723CN	LM723CN
RC723DB	CA723CE,LM723CN
RC723T	CA723CT,LM723CH
RC1458NB	CA1458E,LM1458N

Interchangeability Directory

Industry Type	RCA Replacement Type
RC1458T	CA1458T,LM1458T
RC3401DB	CA3401E
RC741DB	CA741CE,LM741CN
RC741NB	CA741CE,LM741CN
RC741T	CA741T,LM741H
RC747DB	CA747CE
RC747T	CA747T
RM555T	CA555T,LM555H
RM723T	CA723T,LM723H
RM741T	CA741T,LM741H
RM747T	CA747T
RM1558T	CA1558T,LM1558H
SE555L	CA555T
SE555N	CA555E
SE555P	CA555E
SE555T	CA555T
SFC2301A	CA301AT,LM301AH
SFC2301ADC	CA301AE,LM301AN
SFC2307	CA307T,LM307H
SFC2311	CA311T,LM311H
SFC2741C	CA741CT,LM741CH
SFC2741M	CA741T,LM741H
SFC2748DC	CA748CE,LM748CN
SFC2748C	CA748CT,LM748CH
SG301AN	CA301AE,LM301AN
SG301AT	CA301AT,LM301AH
SG307N	CA307E,LM307N
SG307T	CA307T,LM307H
SG311M	CA311E,LM311N
SG311T	CA311T,LM311H
SG723CN	CA723CE,LM723CN
SG723CT	CA723CT,LM723CH
SG723T	CA723T,LM723H
SG741CN	CA741CE,LM741CN
SG741CT	CA741CT,LM741CH
SG741T	CA741T,LM741H
SG747CN	CA747CE
SG747CT	CA747CT
SG747T	CA747T
SG748CN	CA748CE,LM748CN
SG748CT	CA748CT,LM748CH
SG748T	CA748T,LM748H
SG1458M	CA1458E,LM1458N
SG1458T	CA1458T,LM1458H
SG1558T	CA1558T
SG2524N	CA2524E
SG3018T	CA3018
SG3018AT	CA3018A
SG3059J	CA3059
SG3079J	CA3079
SG3081N	CA3081
SG3081J	CA3081F
SG3082N	CA3082
SG3082J	CA3082F
SG3083J	CA3083F
SG3401N	CA3401E
SG3524N	CA3524E
SN76242N	CA3070
SN76243AN	CA3071
SN76264N	CA3072
SN76298N	CA1398E
SN76666N	CA3065
SN76675N	CA3075
SN76689N	CA3089E, CA3189E
SSI570	CA575E
SSI575	CA575E
SSS301AJ	CA301AT,LM301AH
SSS301AP	CA301AE,LM301AN
SSS741CJ	CA741CT,LM741CH
SSS1458J	CA1458T,LM1458H
SSS1558J	CA1558T,LM1558H
TBB0747	CA747CT
TBB0748	CA748CT,LM748CH
TBB0748B	CA748CE,LM748CN
TBB1458B	CA1458E,LM1458N
TBC0747	CA747T
TDA3081N	CA3081
TDA3082N	CA3082
TDA5550	CA3259
TDA7607	CA7607E
TDA7611	CA7611E
TDB0723	CA723CT,LM723CH
TDB0723A	CA723CE,LM723CN
TDC0723	CA723T,LM723H
TL081CP	CA081E
TL081ACP	CA081AE
TL082CP	CA082E
TL082ACP	CA082AE
TL084ACN	CA084AE
TL084CN	CA084E
U5B7741312	CA741T,LM741H
U5B7741393	CA741CT,LM741CH
U5B7748312	CA748T,LM748H
U5B7748393	CA748CT,LM748CH
U5R7723312	CA723T,LM723H
U5R7723393	CA723CT
U6A7723393	CA723CE,LM723CN
U9T7741393	CA741CE,LM741CN
ULN2111A	CA2111AE
ULN2111N	CA2111AQ
ULN2114A	CA3072
ULN2124A	CA3070
ULN2127A	CA3071
ULN2129A	CA3075
ULN2165A	CA3065
ULN2212B	CA3012
ULN2262A	CA3126E
ULN2269A	CA3121E
ULN2289A	CA3089E,CA3189E
ULN2298A	CA1398E
μA301AH	CA301AT,LM301AH
μA301AT	CA301AE,LM301AN
μA307H	CA307T,LM307H
μA307T	CA307E,LM307N
μA311H	CA311T,LM311H
μA311T	CA311E,LM311N
μA555HC	CA555CT,LM555CH
μA555HM	CA555T
μA555TC	CA555CE,LM555CN
μA723CA	CA723CE,LM723CN
μA723CL	CA723CT,LM723CH
μA723CN	CA723CE,LM723CN
μA723HC	CA723CT,LM723CH
μA723HM	CA723T,LM723H
μA723MN	CA723E,LM723N
μA723ML	CA723T,LM723H
μA723PC	CA723CE,LM723CN
μA741CN	CA741CE,LM741CN
μA741CL	CA741CT,LM741CH
μA741CP	CA741CE,LM741CN
μA741CT	CA741CE,LM741CN
μA741HC	CA741CT,LM741CH
μA741HM	CA741T,LM741H
μA741ML	CA741T,LM741H
μA741MN	CA741E,LM741N
μA741MP	CA741E,LM741N
μA741PC	CA741CE,LM741CN
μA746PC	CA3072
μA747CA	CA747CE
μA747CL	CA747CT
μA747CN	CA747CE
μA747HC	CA747CT
μA747HM	CA747T
μA747ML	CA747T
μA747MN	CA747E
μA747PC	CA747CE
μA747A	CA747E
μA748CL	CA748CT,LM748CH
μA748CN	CA748CE,LM748CN
μA748CP	CA748CE,LM748CN
μA748CT	CA748CT,LM748CH
μA748HC	CA748CT,LM748CH
μA748HM	CA748T,LM748H
μA748ML	CA748T,LM748H
μA748MN	CA748E,LM748N
μA748MP	CA748E,LM748N
μA748T	CA748E,LM748N
μA748TC	CA748CE,LM748CN
μA780PC	CA3070
μA781PC	CA3071
μA787PC	CA3126E
μA1391T	CA1391E
μA1394T	CA1394E
μA1458HC	CA1458T,LM1458H
μA1458TC	CA1458E,LM1458N
μA1558HM	CA1558T
μA3018HM	CA3018
μA3018AHM	CA3018A
μA3019HM	CA3019
μA3026HM	CA3026
μA3039HM	CA3039
μA3045DM	CA3045,CA3045F
μA3046DC	CA3046
μA3054PC	CA3054
μA3065PC	CA3065
μA3075PC	CA3075
μA3086DC	CA3086F
μA3089E	CA3089E, CA3189E
μA3401P	CA3401E
μPC151A	CA741CT,LM741CH
μPC151C	CA741CE,LM741CN
μPC157A	CA301AT,LM301AH
μPC157C	CA301AE,LM301AN
μPC251A	CA747CT
μPC251C	CA747CE
μPC301AC	CA301AE,LM301AN
μPC311C	CA311E,LM311N
μPC324C	CA324E,LM324N
μPC339C	CA339E,LM339N
μPC741C	CA741CE,LM741CN
μPC1458C	CA1458E,LM1458N

The RCA types listed as replacements are electrically and mechanically equivalent to the corresponding industry types and can be used as direct replacements in most applications. The recommendations are based on the electrical and mechanical data published by various solid-state device manufacturers. Before substituting any replacement type in a particular application, the user should review the operating conditions of the particular application with respect to the specifications of the planned substitute type.

Data Conversion Circuits

Data Conversion Circuits — Technical Data

For data on CDPXXXX types, refer to *DATABOOK SSD-260,* CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices.*

Data-Conversion Circuits

Type	Technology	Resolution (Bits)	Resolution (Digits)	Clock Rate (MHz)	Conversion Time (μs)	Conversion Time (ms)	At Supply Voltage (V)	Typ. Power Dissip. (mW)	Integral Linearity (LSB)	Integral Linearity (Count)	Diff. Linearity (LSB)	At Full-Scale Input (V)	Package Size (Pins)	Comments
A/D Converters Parallel (Flash) Types														
CA3304A•	CMOS/SOS	4	—	25	—	—	5	35	¼	—	¼	1	16	Has data change output
CA3300C	CMOS/SOS	6	—	9	—	—	8	100	0.8	—	0.8	7.68	18	Has internal zener
CA3300	CMOS/SOS	6	—	15	—	—	8	175	0.8	—	0.8	7.68	18	Faster version of CA3300C
CA3306C	CMOS/SOS	6	—	10	—	—	5	55	½	—	½	4.8	18	CA3300 with improved linearity. Has lower supply and reference voltages.
CA3306	CMOS/SOS	6	—	15	—	—	5	70	½	—	½	4.8	18	Higher-speed version of CA3306C
CA3306A	CMOS/SOS	6	—	15	—	—	5	70	¼	—	¼	4.8	18	CA3306 with improved linearity
CA3307•	CMOS/SOS	7	—	20	—	—	5	100	TBE	—	TBE	4.8	18	Dither input allows 8-bit resolution
41051	CMOS/SOS	8	—	15	—	—	5	125	1.5	—	+1/ -0.8	6.4	24	Has errors at higher clock speeds and input bandwidths. For new designs, use CA3318 family
CA3318C	CMOS/SOS	8	—	15	—	—	5	150	1.5	—	+1/ -0.8	6.4	24	41051 without clock induced errors. Has extra ½ cycle output delay. Has input bandwidth restriction.
CA3318•	CMOS/SOS	8	—	20	—	—	5	200	1.5	—	±0.8	6.4	24	Higher-speed version of CA3318C. No input bandwidth restriction.
Subranging Types														
CA3388•	CMOS/SOS	8	—	5	—	—	5	TBE	TBE	—	TBE	TBE	22	Very-low-power 8-bit type. "Almost Flash"
Successive Approximation Types														
CA3310•	CMOS	10	—	—	13	—	5	15	1	—	1	4.608	24	Integral track and hold, rail-to-rail input range
CA3310A•	CMOS	10	—	—	13	—	5	15	½	—	½	4.608	24	CA3310 with improved linearity
CDP68HC68•	CMOS	10	—	—	100	—	5	TBE	TBE	—	TBE	TBE	16	Serial microprocessor interface, 8-input multiplexer, and reference in space-saving package
Integrating Types														
CA3162	I^2L	—	3	—	—	10	5	60	—	1	NMC	+1/ -0.1	16	Part of 2-chip set. To make complete DPM, add CA3161 and 3 PNP transistors.
CA3162A	I^2L	—	3	—	—	10	5	60	—	1	NMC	+1/ -0.1	16	-40° C to +85° C specified version of CA3162
CA3999•	CMOS	—	3¾	—	—	300	5	TBE	—	TBE	TBE	±2	40	Complete DPM with auto-zeroed reference, LED drive and BCD outputs. Full ±2-volt (±3999 count) inputs.
D/A Converters High-Speed R-2R Types														
CA3338•	CMOS/SOS	8	—	50	—	—	5	TBE	½	—	½	5	16	Data complement control and input latch

NOTES: •Product preview data only. TBE=To be established NMC=No missing codes

Power dissipation is at given sampling rate, at given supply voltage, and does not include reference current.
All converters operate from single supply. Specifications are limit values unless noted as typical.
All flash and subranging A/D converters have three-state CMOS bus driver bit and overflow outputs.
Unless noted, all flash and subranging A/D converters will accept Nyquist rate input bandwidths.

CA3162, CA3162A

A/D Converter for 3-Digit Display

Features:

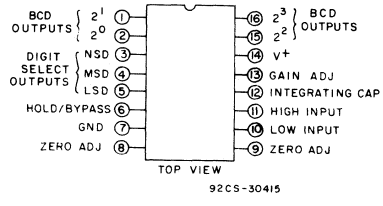
- *Dual-slope A/D conversion*
- *Multiplexed BCD display*
- *Ultra-stable internal band-gap voltage reference*
- *Capable of reading 99 mV below ground with single supply*
- *Differential input*
- *Internal timing - no external clock required*
- *Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate*
- *"Hold" inhibits conversion but maintains delay*
- *Overrange indication - "EEE" for reading greater than +999 mV, "-" for reading more negative than -99 mV when used with CA3161E BCD-to-Seven Segment Decoder/Driver*
- *Extended temperature range version available*

The CA3162E and CA3162AE are I^2L monolithic A/D converters that provide a 3-digit multiplexed BCD output. They are used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete 3-digit display. The CA3162AE is identical to the CA3162E except for an extended operating temperature range.

The CA3162 is supplied in a 16-lead dual-in-line plastic package (E suffix). The CA3162 is also available in chip form (H suffix).

* The CA3161E is described in RCA data bulletin File No. 1079.

TERMINAL ASSIGNMENT
CA3162E



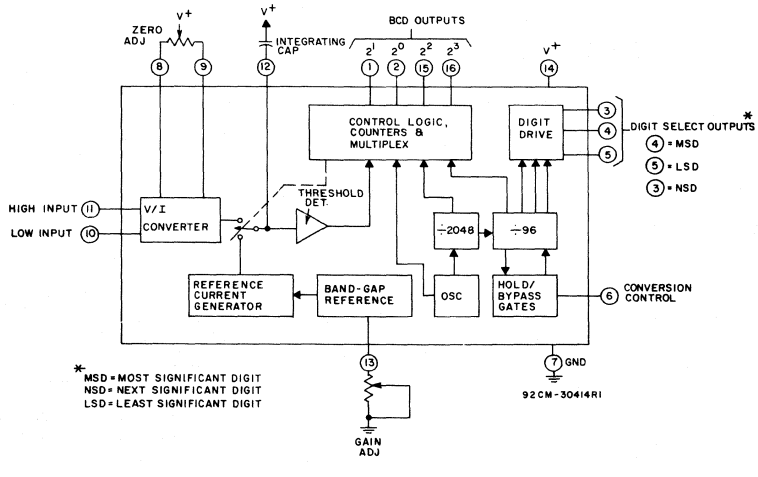


Fig. 1 - Functional block diagram of the CA3162E.

File Number **1080**

CA3162, CA3162A

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14) ..... +7 V
INPUT VOLTAGE (terminal 10 or 11 to ground) ..... ±15 V
DEVICE DISSIPATION:
Up to T_A = +55°C ..... 750 mW
Above T_A = +55°C ..... Derate Linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating, CA3162E ..... 0 to +75°C
Operating, CA3162AE ..... -40 to +85°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V + = 5 V, Zero pot centered, gain pot = 2.4 kΩ unless otherwise stated

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Supply Voltage Range V +	—	4.5	5	5.5	V
Supply Current, I+	100 kΩ to V+ on terms. 3, 4, 5	—	—	17	mA
Input Impedance, Z_I	—	—	100	—	MΩ
Input Bias Current, I_{IB}	Terms. 10 and 11	—	-80	—	nA
Unadjusted Zero Offset	V_{11} -V_{10} = 0 V, read decoded output	-12	—	+12	mV
Unadjusted Gain	V_{11} -V_{10} = 900 mV, read decoded output	846	—	954	mV
Linearity	See Notes 1 and 2	-1	—	+1	Count
Conversion Rate:					
Slow Mode	Term. 6 = open or gnd	—	4	—	Hz
Fast Mode	Term. 6 = 5 V	—	96	—	
Conversion Control Voltage (Hold Mode) at Terminal 6	—	0.8	1.2	1.6	V
Common-Mode Input Voltage Range, V_{ICR}	See Note 3, 4	-0.2	—	+0.2	V
BCD Sink Current at terms. 1, 2, 15, 16	$V_{BCD} \geq$ 0.5 V, at logic zero state	0.4	1.6	—	mA
Digit Select Sink Current at terms. 3, 4, 5	$V_{Digit\ Select}$ = 4 V at logic zero state	1.6	2.5	—	mA
Zero Temperature Coefficient	V_I = 0 V, zero pot centered	—	10	—	μV/°V
Gain Temperature Coefficient	V_I = 900 mV, gain pot = 2.4 KΩ	—	0.005	—	%/°C

Notes:

1. Apply zero volts across V_{11} to V_{10}. Adjust zero potentiometer to give 000 mV reading. Apply 900 mV to input and adjust gain potentiometer to give 900 mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ± 0.5 count bit digitizing error.
3. For applications where negative terminal 10 is not operated at terminal 7 potential, a return path of not more than 100 kΩ resistance must be provided for input bias currents.
4. The common-mode input voltage above ground cannot exceed +0.2 V if the full input signal range of 999 mV is required at terminal 11. That is, terminal 11 may not operate higher than 1.2 V positive with respect to ground or 0.2 V negative with respect to ground. If the maximum input signal is less than 999 mV, the common-mode input voltage may be raised accordingly.

CA3162, CA3162A

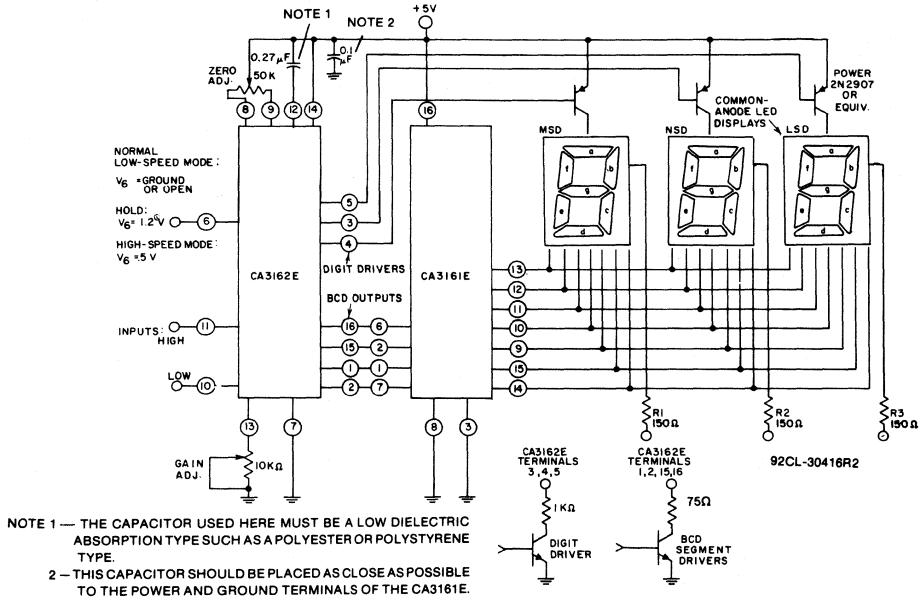
Circuit Description

The functional block diagram of the CA3162E is shown in Fig. 1. The heart of the system is the V/I converter and reference-current generator. The V/I converter converts the input voltage applied between terminals 10 and 11 to a current that charges the integrating capacitor on terminal 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band-gap reference constant-current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786-Hz ring oscillator, and the input at terminal 6 determines the sampling rate. A 5-V input provides a high-speed sampling rate (96 Hz), and grounding or floating terminal 6 provides a low-speed (4 Hz) sampling rate. When terminal 6 is fixed at + 1.2 V (by placing a 12 K resistor between terminal 6 and the + 5-V supply) a "hold" feature is available. While the CA3162E is in the hold mode, sampling continues at 4 Hz but the display data are latched to the last reading prior to the application of the 1.2 V. Removal of the 1.2 V restores continuous display changes. Note, however, that the sampling rate remains at 4 Hz.

Fig. 3 shows the timing of sampling and digit select pulses for the high-speed mode. Note that the basic A/D conversion process requires approximately 5 ms in both modes.

The "EEE" or "---" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to -99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (---) and 1011 for a positive overrange (EEE).



NOTE 1 — THE CAPACITOR USED HERE MUST BE A LOW DIELECTRIC ABSORPTION TYPE SUCH AS A POLYESTER OR POLYSTYRENE TYPE.
2 — THIS CAPACITOR SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE POWER AND GROUND TERMINALS OF THE CA3161E.

Fig. 2 - Basic digital readout system using the CA3162E and the CA3161E.

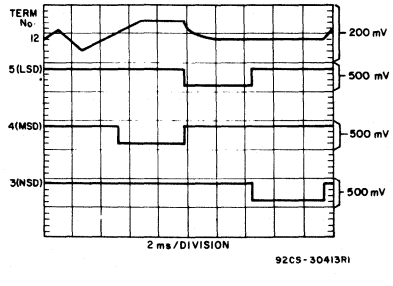


Fig. 3 - High speed mode timing diagram.

CA3162E Liquid Crystal Display (LCD) Application

Fig. 4 shows the CA3162E in a typical LCD application. LCD's may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCD's must be driven by an ac signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder using the inverted digit-select outputs of the CA3162E as strobes.

The capacitors on the outputs of inverters G3 and G4 filter out the decode spikes on the MSD and NSD signals. The capacitors and pull-up resistors connected to the MSD, NSD and LSD outputs are there to shorten the digit drive signal thereby providing proper timing for the CD4056B latches.

Inverters G1 and G2 are used as an astable multivibrator to provide the ac drive to the LCD backplane. Inverters G3, G4, and G5 are the digit-select inverters and require pull-up resistors to interface the open-collector outputs of the CA3162E to CMOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (-) as an "L" and the positive overload indicator (E) as an "H".

The circuit as shown in Fig. 4, using G7, G8 and G9, will decode the negative sign (-) as a negative sign (-), and the positive overload indicator (E) as "H".

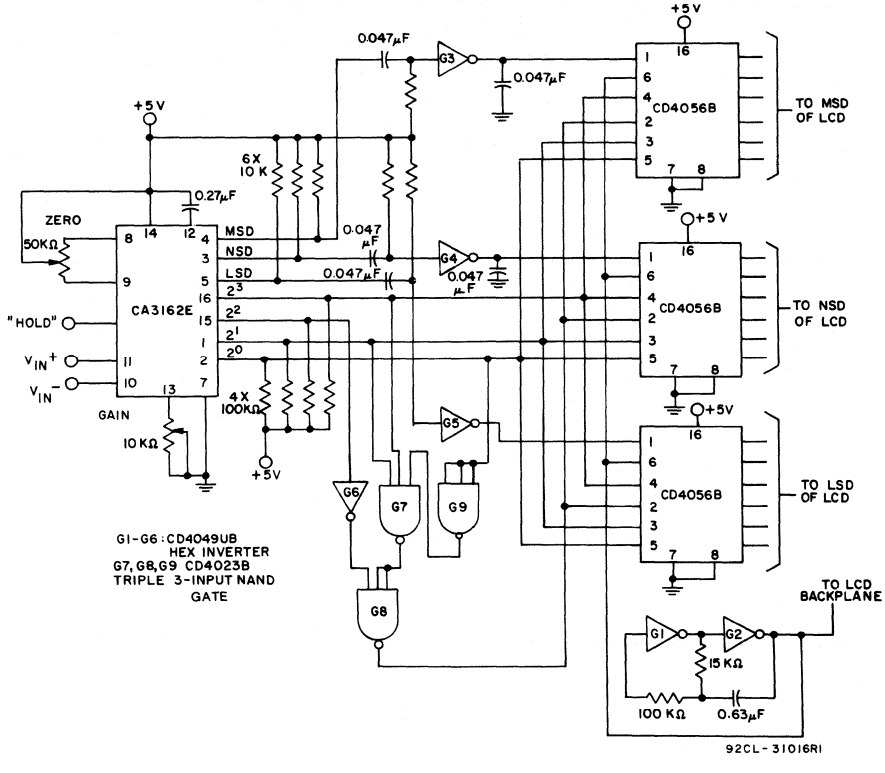


Fig. 4 - Typical LCD application.

CA3162, CA3162A

CA3162E Common-Cathode, LED Display Application

Fig. 5 shows the CA3162E connected to a CD4511B decode/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999 mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank instead of (-), and during a negative or positive overrange the display blanks.

The additional logic shown within the dotted area of Fig. 5 restores the negative sign (-), allowing the display of negative numbers as low as -99 mV. Negative overrange is indicated by a negative sign (-) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed. One inverter from the CD4049B is used to operate the decimal points. By connecting the inverter input to either the MSD or NSD line either DP1 or DP2 will be displayed. Fig. 7 shows the P.C. board and component placement.

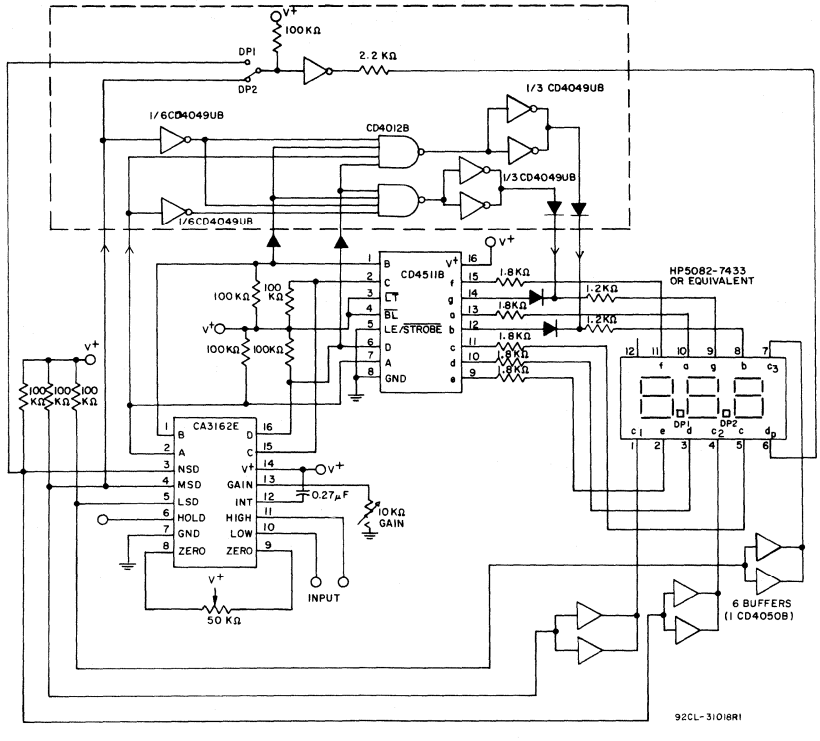
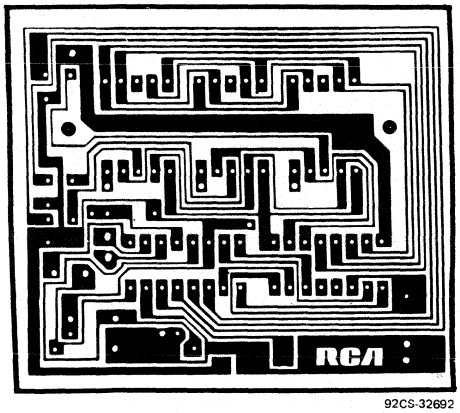


Fig. 5 - Typical common-cathode LED application.



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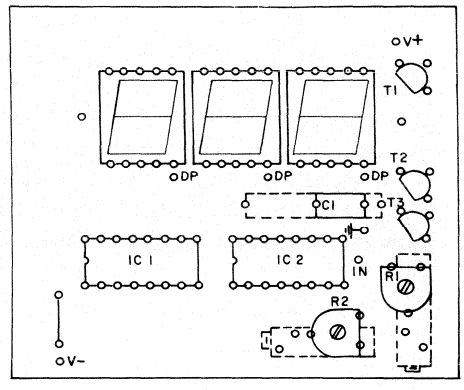
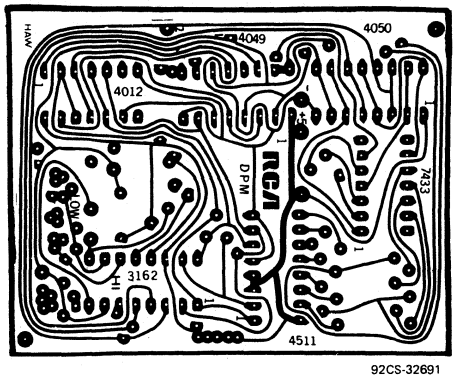


92CS-32693

Fig. 6 - P.C. board template (actual size ± 3%) and component layout guide for circuit shown in Fig. 2.*



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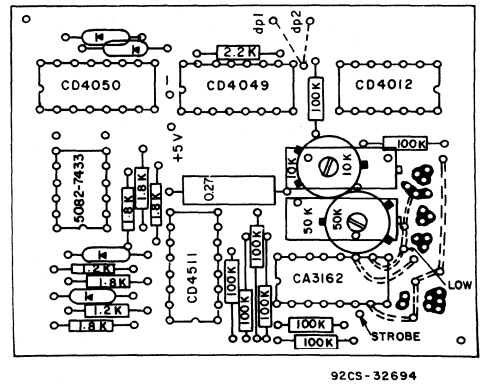
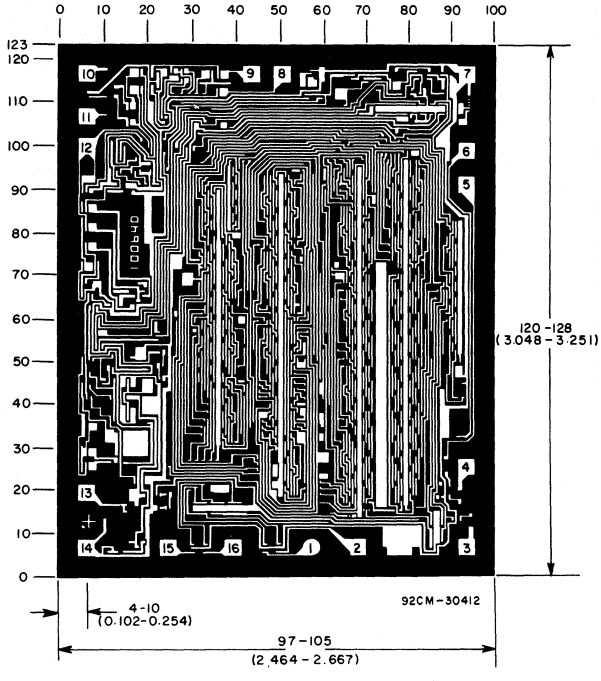


92CS-32694

Fig. 7 - P.C. board template (actual size ± 3%) and component layout guide for circuit shown in Fig. 5.

**P.C. board courtesy ETS. Velleman P.V.B.A., St. Amandsberg, Belgium*

CA3162, CA3162A



Dimensions and pad layout for CA3162H chip.

The photographs and dimensions of each Linear chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3300

CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:

- *CMOS low power with speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *6-bit latched 3-state output with overflow bit*
- *±½ LSB accuracy*
- *Single supply voltage (3 to 10 V)*
- *2 units in series allow 7-bit output*
- *2 units in parallel allow 30-MHz sampling rate*
- *Internal V_{REF} with ext V_{REF} option*
- *Available with EVP processing for improved reliability*

The RCA-CA3300 types are CMOS 50-mW parallel (FLASH) analog-to-digital converters designed for applications demanding both low-power consumption and high-speed digitization.

The CA3300 types operate over a wide full-scale input-voltage range of 2.4 volts up to the dc supply voltage with maximum power consumption as low as 50 to 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 11 MHz, the power consumption of the CA3300 is less than 50 mW. When operated from an 8-volt supply at a frequency of 15 MHz, the power consumption is less than 150 mW.

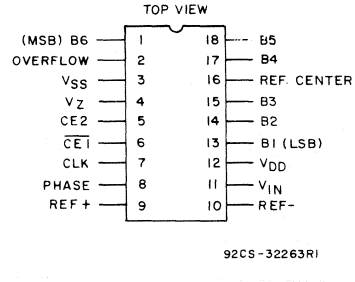
The intrinsic high conversion rate makes the CA3300 types ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3300's in series to increase the resolution of the conversion system. A series connection of two CA3300's may be used to produce a 7-bit high-speed converter. Operation of two CA3300's in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3300's in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very-high-speed A/D converter.

Sixty-four paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3300. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3300 types are available as follows: Types CA3300D and CA3300DX in an 18-lead dual-in-line ceramic package (D suffix), types CA3300E and CA3300CE in an 18-lead dual-in-line plastic package (E suffix), or in chip form (H suffix). The CA3300DX offers the additional advantage of improved reliability as a result of EVP (Extra Value Program) processing. For further information on EVP, see RCA publication EVP-300B or contact your RCA representative.

Applications:

- *The CA3300 types are especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADC's*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*



TERMINAL ASSIGNMENT

File Number **1316**

CA3300

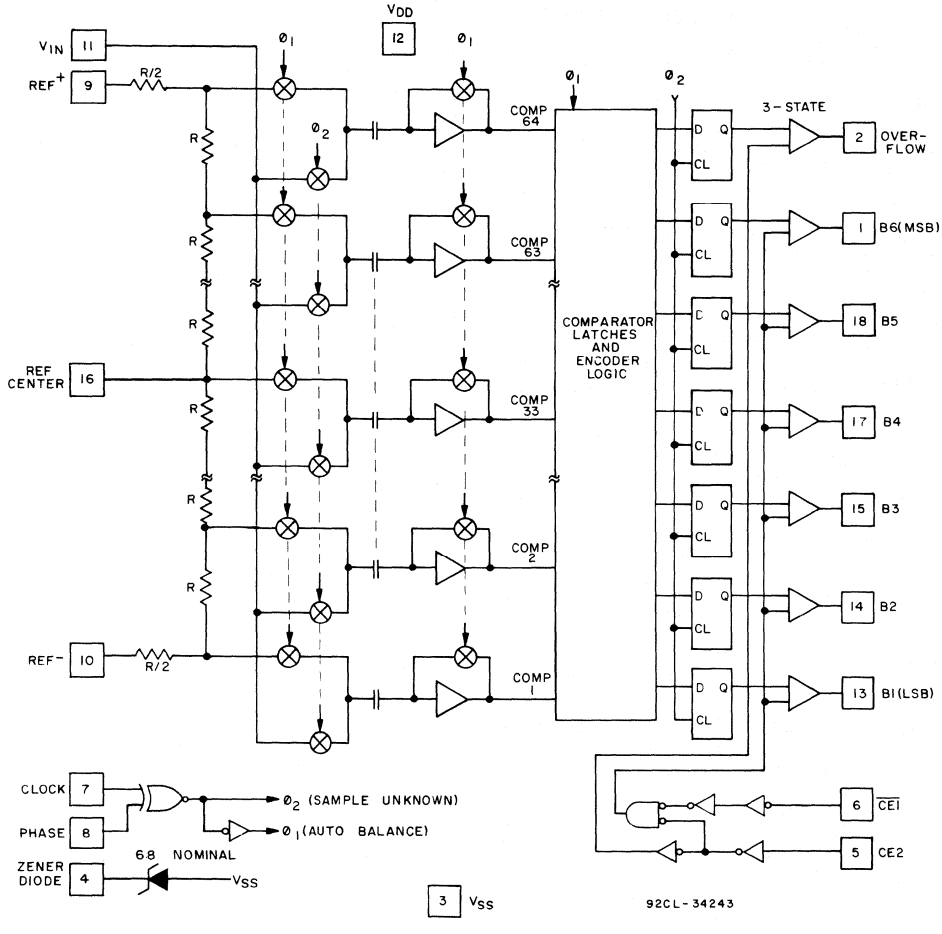


Fig. 1 - Block diagram for the CA3300.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... -0.5 to 10 V
INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -55 to +55°C ..... 315 mW
FOR T_A = +55°C to +125°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE
OPERATING (CA3300DX, Refer to Fig. 3) ..... -55 to +125°C
OPERATING (CA3300D, E, CE) ..... -40 to +85°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS CA3300D, DX, E			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	
Quantizing Error		-½	—	½	
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=15 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	
Device Current	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
(Excludes I_{REF}, I_Z)	V_{DD}=8 V (CLK=15 MHz)	—	22	—	
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	
	V_{DD}=8 V (Auto Balance State)	—	24	40	
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
(Sink) Current	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	
Output High	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	
(Source) Current	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	

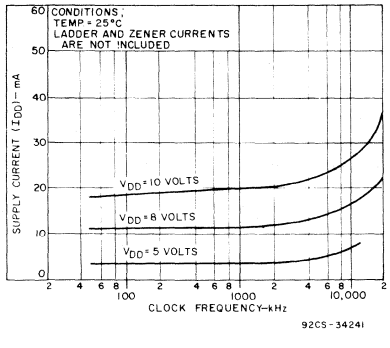


Fig. 2 - Typical current drain versus sampling rate as a function of supply voltage.

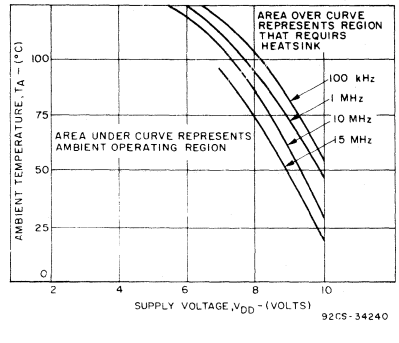


Fig. 3 - Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

CA3300

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS CA3300CE			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=9 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=9 MHz	—	±0.5	±0.8	
Quantizing Error		-½	—	½	
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=9 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	450	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=9 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	6M	—	—	SPS
	V_{DD}=8 V	9M	19M	—	
Device Current	V_{DD}=5 V (CLK=7 MHz)	—	4	—	mA
(Excludes I_{REF}, I_Z)	V_{DD}=8 V (CLK=9 MHz)	—	12	—	
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	
	V_{DD}=8 V (Auto Balance State)	—	24	40	
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
(Sink) Current	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	
Output High	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	
(Source) Current	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	

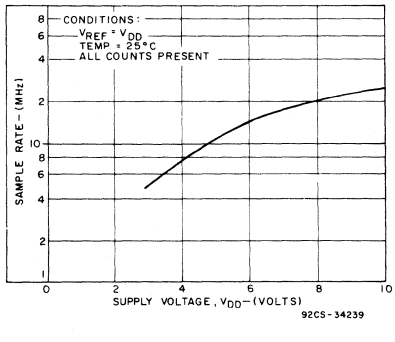


Fig. 4 - Typical maximum sample rate versus supply voltage.

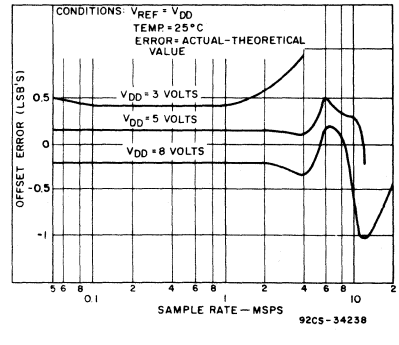


Fig. 5 - Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)

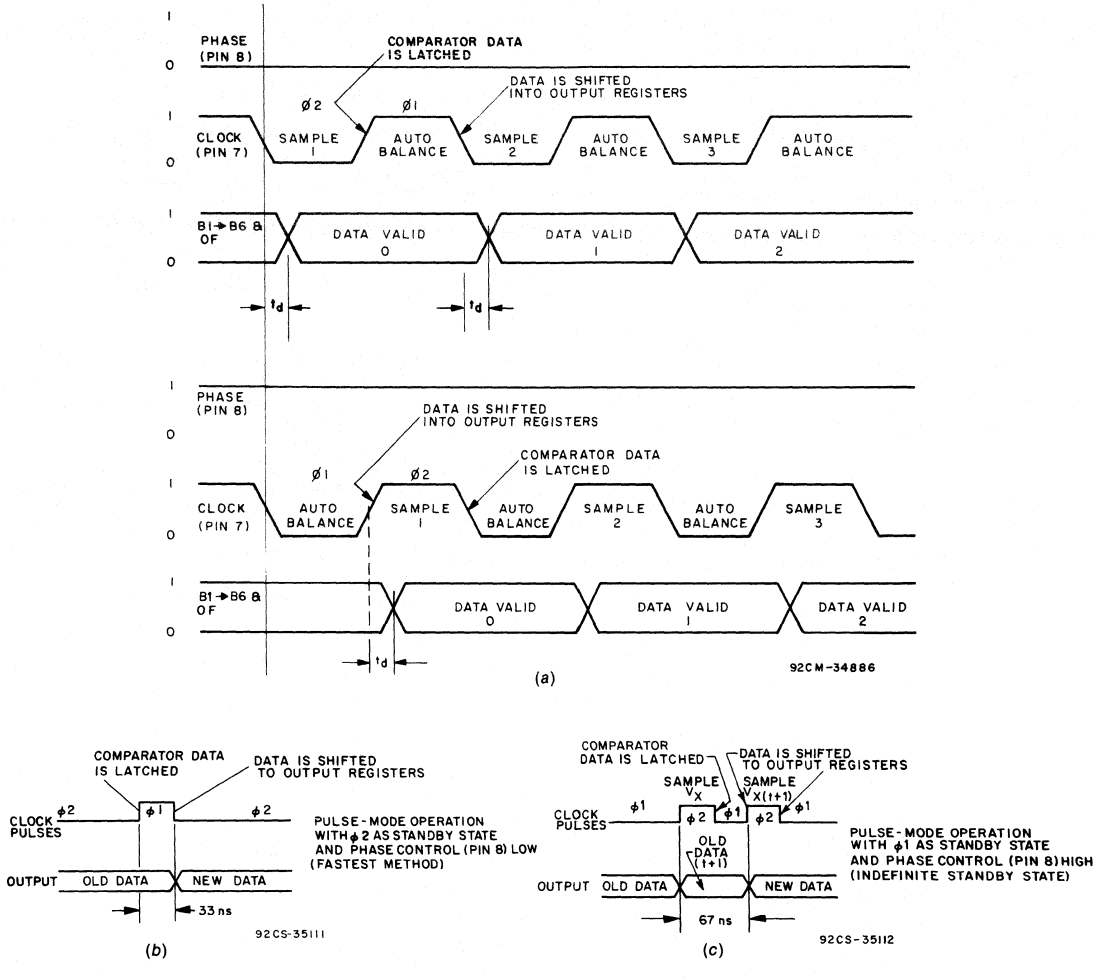


Fig. 6 - Timing diagrams for the CA3300.

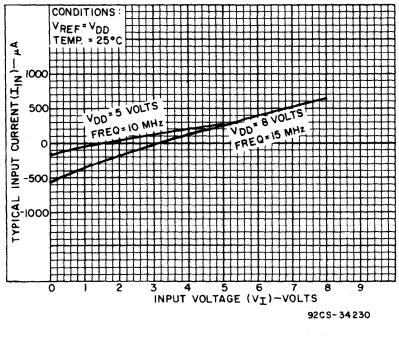


Fig. 7 - Typical input current versus input voltage as a function of supply voltage.

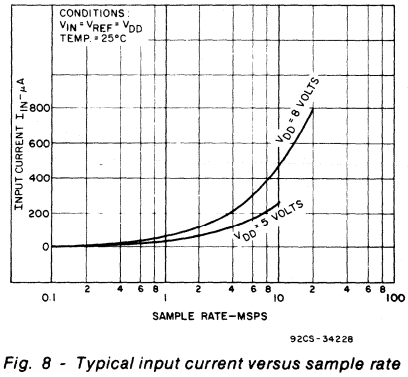


Fig. 8 - Typical input current versus sample rate as a function of supply voltage.

CA3300

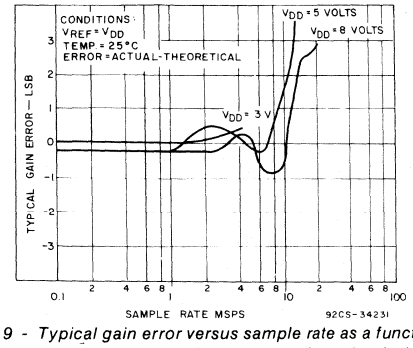


Fig. 9 - Typical gain error versus sample rate as a function of supply voltage. (See literature for gain trim.)

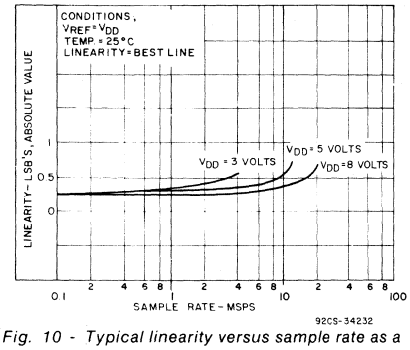


Fig. 10 - Typical linearity versus sample rate as a function of supply voltage.

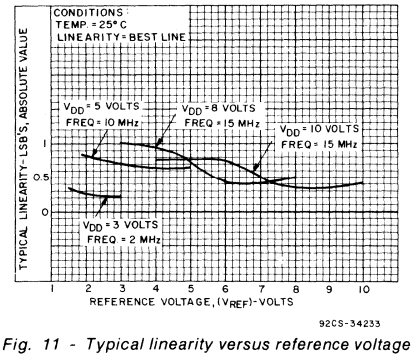


Fig. 11 - Typical linearity versus reference voltage as a function of supply voltage.

Device Operation

A sequential parallel technique is used by the CA3300 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase $\phi 1$ and the "Sample Unknown" phase $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) low, the "Auto Balance" ($\phi 1$) occurs during the High period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/128]$$

Where: $V_{tap}(n)$ = reference ladder tap voltage at point n

V_{REF} = voltage across R^- to R^+

N = tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD}-V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than V_{IN} will drive the comparator outputs to a "low" state, all comparators with tap voltage lower than V_{IN} will drive the comparator outputs to a "high" state.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi 2$), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-to 7-bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi 2$.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3300 via the following steps. (Refer to timing diagram Fig. 6a.) With the phase control in a 'High' state, the rising edge of the clock input will start a "sample" phase. During this entire 'High' state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this 'Low' state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of two ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The

*This device requires only a single phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

device can now be pulsed through the Auto Balance phase with as little as 33 ns. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started within 33 ns, but not later than 5 μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See timing diagram Fig. 6b.)

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 67 ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See timing diagram Fig. 6c.)

Increased Accuracy

In most cases the accuracy of the CA3300 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the R^- (pin 10) input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between R^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between R^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF} and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}\,(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF} until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC), pin 16, is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 32½ LSB's. That voltage is as follows:

$$V_{IN} \text{ (32 to 33 transition)} = 32.5\ (V_{REF}/64)$$

An adjustable voltage follower can be connected to the RC pin or a 2-K pot can be connected between R^+ and R^- with the wiper connected to RC. Set V_{IN} to the 32 to 33 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create some unique transfer functions. For example, if R^- is grounded, RC is connected to 3.25 volts, and R^+ is connected to 4.8 volts then the lower order counts, 1 through 33, will have an LSB value of 100 mV while the upper order counts, 34 through Overflow, will have an LSB value of 50 mV. This effectively provides twice the sensitivity in the upper counts as compared to the lower counts.

7-Bit Resolution

To obtain 7-bit resolution, two CA3300's can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls—all of which are available on the CA3300.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Fig. 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit A/D converter is shown in Fig. 14.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the CA3300 allows 12-bit conversions in the 500 to 900-ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Fig. 15. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

  The first converter can be offset-biased by adding a 20-Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.40-voltage reference is used in the system, for example, then the first CA3300 will require a 6.5-V reference.

CA3300

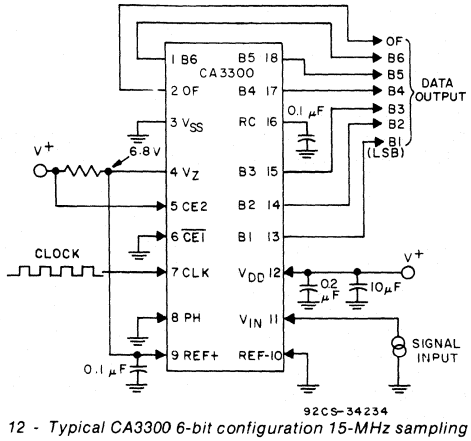


Fig. 12 - Typical CA3300 6-bit configuration 15-MHz sampling rate.

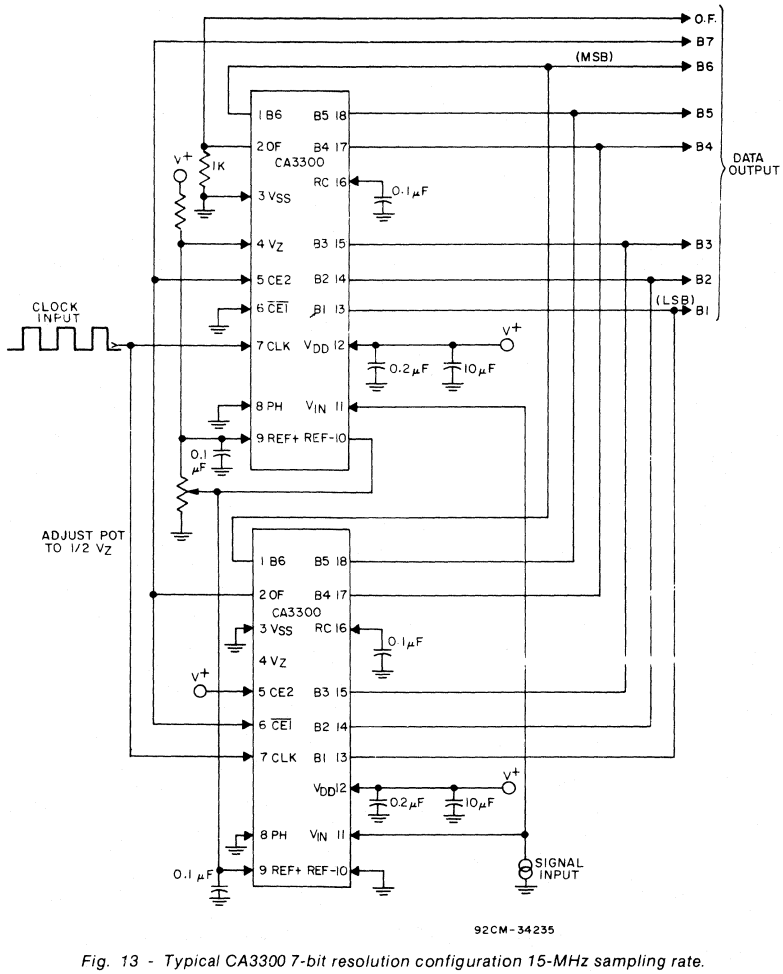


Fig. 13 - Typical CA3300 7-bit resolution configuration 15-MHz sampling rate.

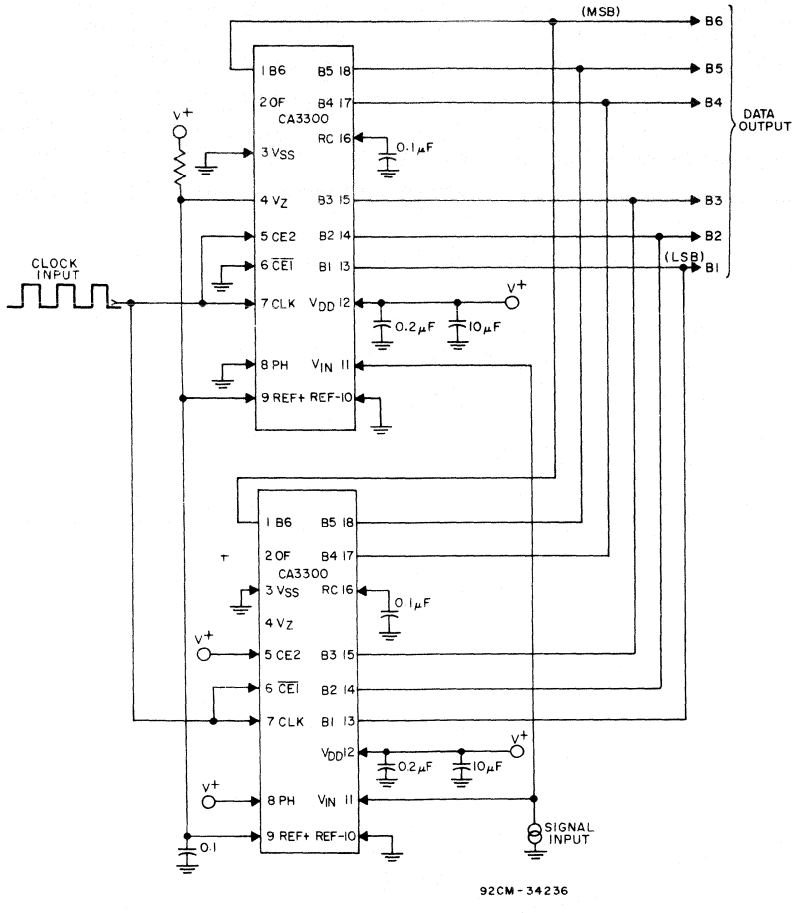


Fig. 14 - Typical CA3300 6-bit resolution configuration 30-MHz sampling rate.

CA3300

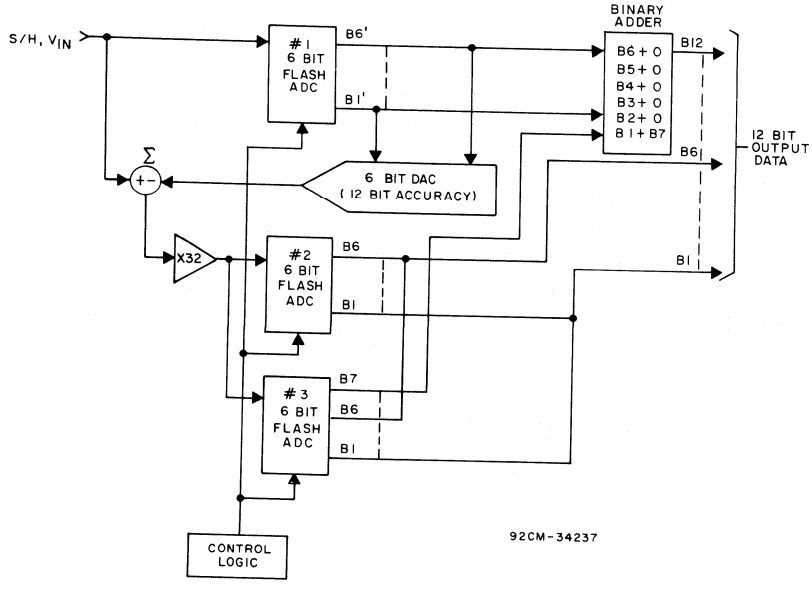


Fig. 15 - Typical CA3300 800-ns 12-bit ADC system.

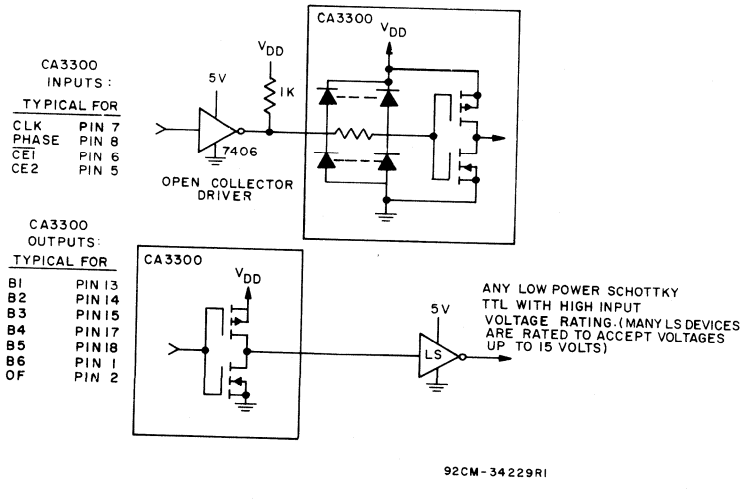
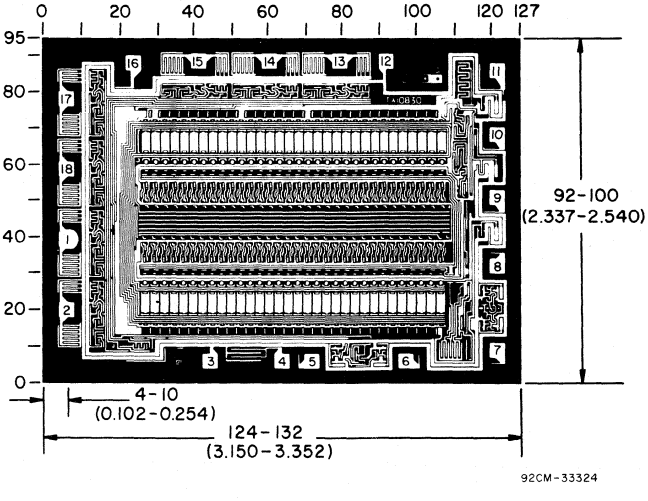


Fig. 16 - TTL interface circuit for $V_{DD} > 5.5$ volts.

OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF} 7.68 (V)	V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 3.20 (V)	BINARY OUTPUT CODE (LSB) 0F	B6	B5	B4	B3	B2	B1	DECIMAL COUNT
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.12	0.10	0.08	0.05	0	0	0	0	0	0	1	1
2 LSB	0.24	0.20	0.16	0.10	0	0	0	0	0	1	0	2
"		"						"				"
"		"						"				"
"		"						"				"
"		"						"				"
½ Full Scale — 1 LSB	3.72	3.10	2.48	1.55	0	0	1	1	1	1	1	31
½ Full Scale	3.84	3.20	2.56	1.60	0	1	0	0	0	0	0	32
½ Full Scale +1 LSB	3.96	3.30	2.64	1.65	0	1	0	0	0	0	1	33
"		"						"				"
"		"						"				"
"		"						"				"
"		"						"				"
Full Scale — 1 LSB	7.44	6.20	4.96	3.10	0	1	1	1	1	1	0	62
Full Scale	7.56	6.30	5.04	3.15	0	1	1	1	1	1	1	63
Overflow	7.68	6.40	5.12	3.20	1	1	1	1	1	1	1	127

*The voltages listed below are the ideal centers of each output code shown as a function of its associated reference voltage.



Dimensions and pad layout for CA3300H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3304

Product Preview

CMOS High-Speed 4-Bit Flash A/D Converter

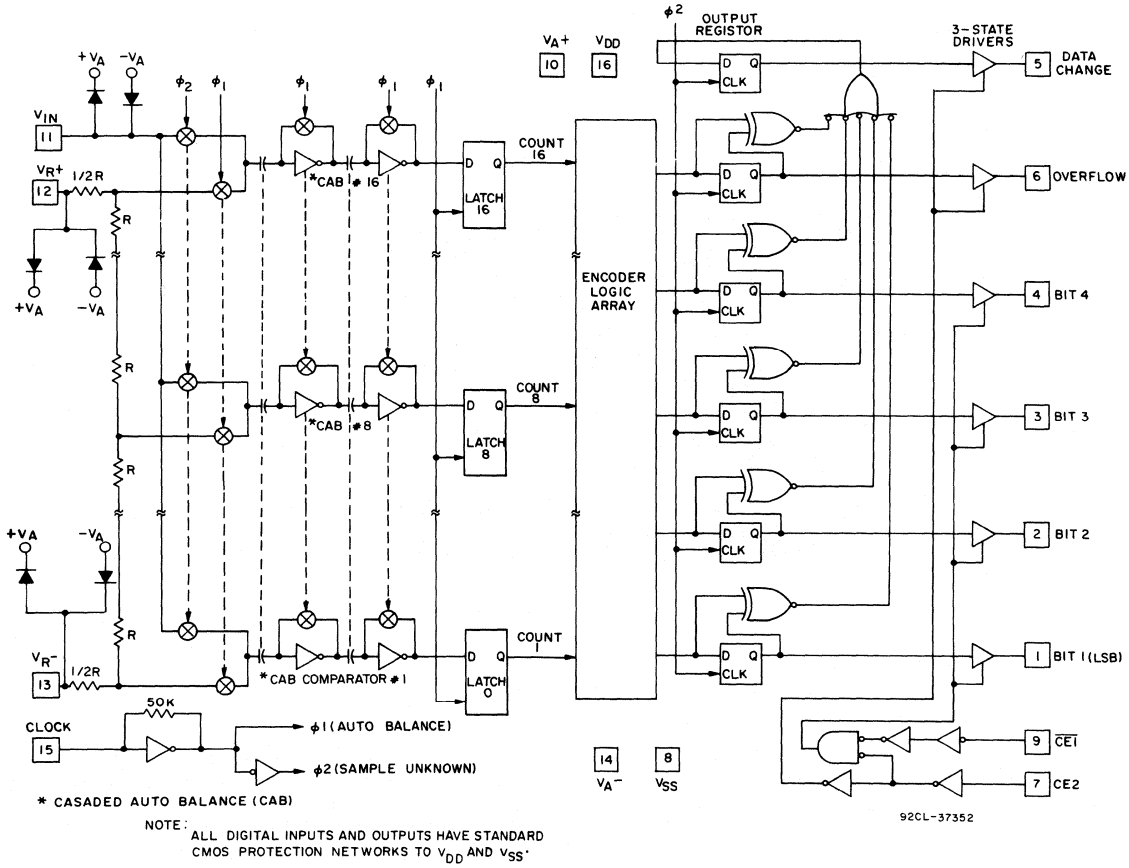
Features:

- *CMOS low power*
- *Flash (Parallel) conversion technique*
- *25 MSPS conversion rate at 5 V*
- *1/4 LSB accuracy*
- *Single 3 to 6 V supply*
- *4-latched bit outputs plus overflow*
- *May be stacked for higher resolution*
- *May be parallel for double speed*

The RCA CA3304 is a CMOS 4-bit Flash analog-to-digital converter featuring video speeds with a single 5-volt supply. The device is similar in operation to the CA3300 6-bit A/D converter (File No. 1316), and may be stacked or paralleled to increase resolution or speed.

The CA3304 has the additional feature of separate analog and digital supply pins, thus allowing analog supply noise isolation or accepting analog inputs outside the digital supply range.

The CA3304 is supplied in a 16-lead dual-in-line plastic package (E suffix) and in a 16-lead dual-in-line ceramic package (D suffix).



Block Diagram of the CA3304

Preview Data only

Product Preview

CA3306, CA3306A, CA3306C

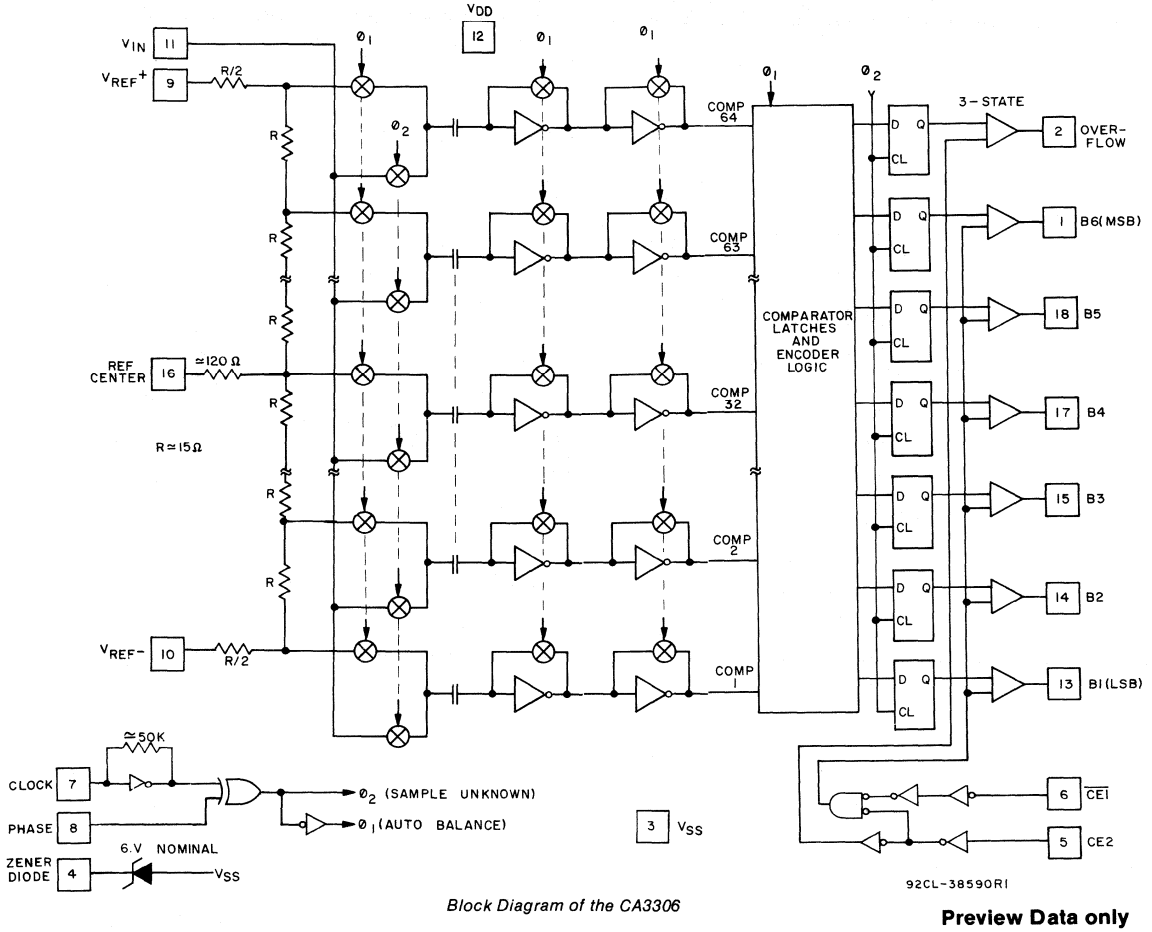
CMOS High-Speed 6-Bit Flash A/D Converter

Features:

- *Improved pin-for-pin retrofits for CA3300*
- *CMOS/SOS low power*
- *Flash (Parallel) conversion technique*
- *15 MSPS conversion rate at 5 V*
- *1/4 LSB accuracy*
- *Single 3 to 6 V supply*
- *6 latched-bit outputs plus overflow*
- *May be stacked for higher resolution*
- *May be parallel for double speed*

The CA3306 family members are pin-for-pin retrofits for the CA3300 (File 1316), but offering improved speed and linearity. All functions of the CA3300 are carried over: the ability to stack devices for higher resolution, parallel devices for doubled speed, and the availability of a built-in zener reference. Accurate digitizing at video speeds is now possible with only a single 5 volt supply (8 volts required for CA3300), and a tighter linearity is guaranteed at a lower reference (full scale) range.

The CA3306-series devices are supplied in 18-lead dual-in-line plastic packages (E suffix) and in 18-lead dual-in-line ceramic packages (D suffix).



Block Diagram of the CA3306

Preview Data only

CA3307

Product Preview

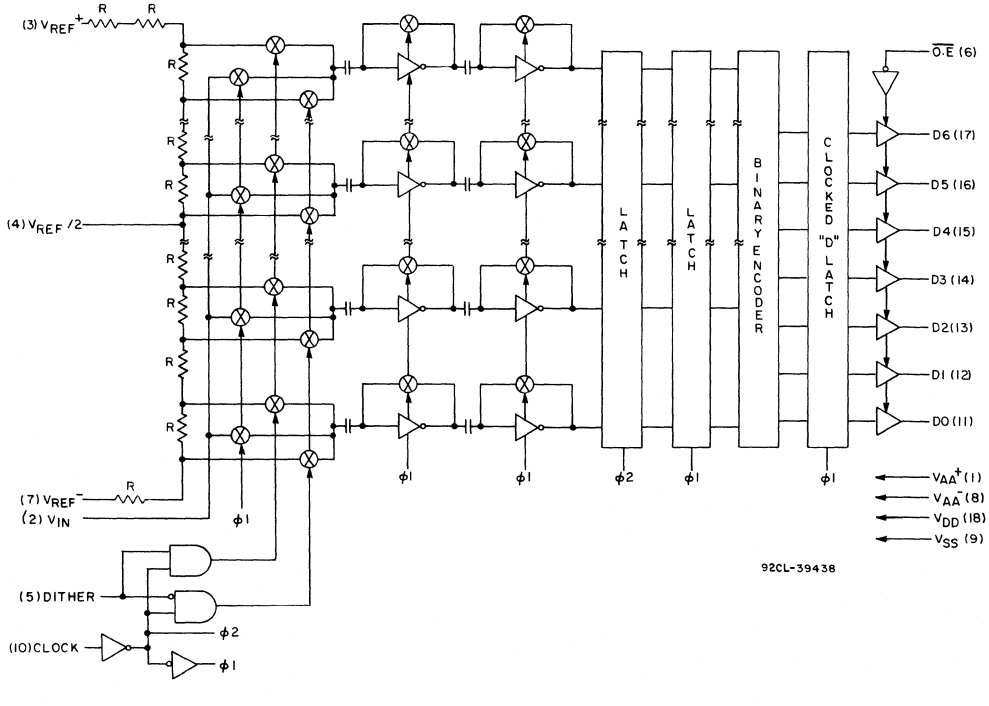
CMOS High-Speed 7-Bit Flash A/D Converter

Features:

- *CMOS/SOS low power*
- *Flash (Parallel) conversion technique*
- *15 MSPS conversion rate at 5 V*
- *3/4 LSB accuracy*
- *Single 3 to 8 V supply*
  "dither" input for increasing resolution
- *Space saving 18 pin package*

The RCA CA3307 is a CMOS 7-bit Flash analog-to-digital converter featuring video speeds with a single 5 volt supply. The device is similar in operation to the CA3300 6-bit A/D converter (File 1316), but with the output delayed by an additional 1/2 clock cycle. The CA3307 features a "dither" input pin which internally offsets the reference by 1/2 LSB. This allows an 8-bit resolution in two conversion cycles: it would be effective, for instance, in reducing contouring on video displays if "dithered" up and down on alternate horizontal sweeps.

The CA3307 is available in an 18-lead dual-in-line plastic package (E suffix), and in an 18-lead dual-in-line ceramic package (D suffix).



Block Diagram of the CA3307

Preview Data only

Product Preview

CA3310, CA3310A

CMOS 10-Bit A/D Converter With Internal Track and Hold

For use in low power, medium speed digitization applications

Features:

- *CMOS low power*
- *Single 3 to 6 volt supply*
- *13 μs conversion time at 5 V*
- *Built-in track and hold*
- *Rail-to-rail input range*
- *Latched 3-state output drivers*
- *Microprocessor compatible control lines*
- *Internal or External clock*

The RCA CA3310 is a fast, low-power, 10-bit successive approximation A/D converter, with microprocessor compatible outputs. It uses only a single 3 to 6 volt supply and typically draws just 2 mA when operating at 5 volts. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100 ns (typ.) input time constant. Conversion time takes as little as 13 μs with a 5 volt supply.

The 10 data outputs feature full QMOS three-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

Applications:

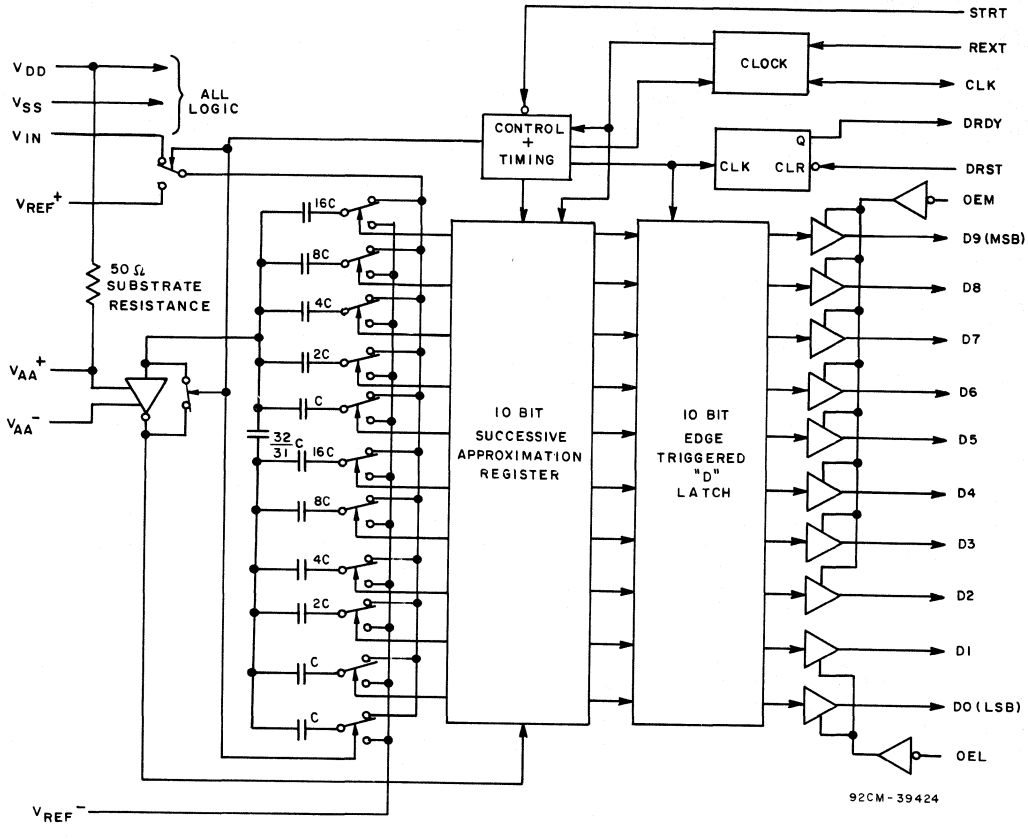
- *Fast, no-droop, sample and hold*
- *Voice grade digital audio*
- *DSP Modems*
- *Remote low power data acquisition systems*
- *Microprocessor controlled systems*

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

The CA3310 is available in two linearity grades, and in 24-lead dual-in-line plastic packages (E suffix) and in 24-lead dual-in-line ceramic packages (D suffix).

Preview Data only

CA3310, CA3310A



Block Diagram of the CA3310

Product Preview

CA3318, CA3318C

CMOS High-Speed 8-Bit Flash A/D Converter

Features:

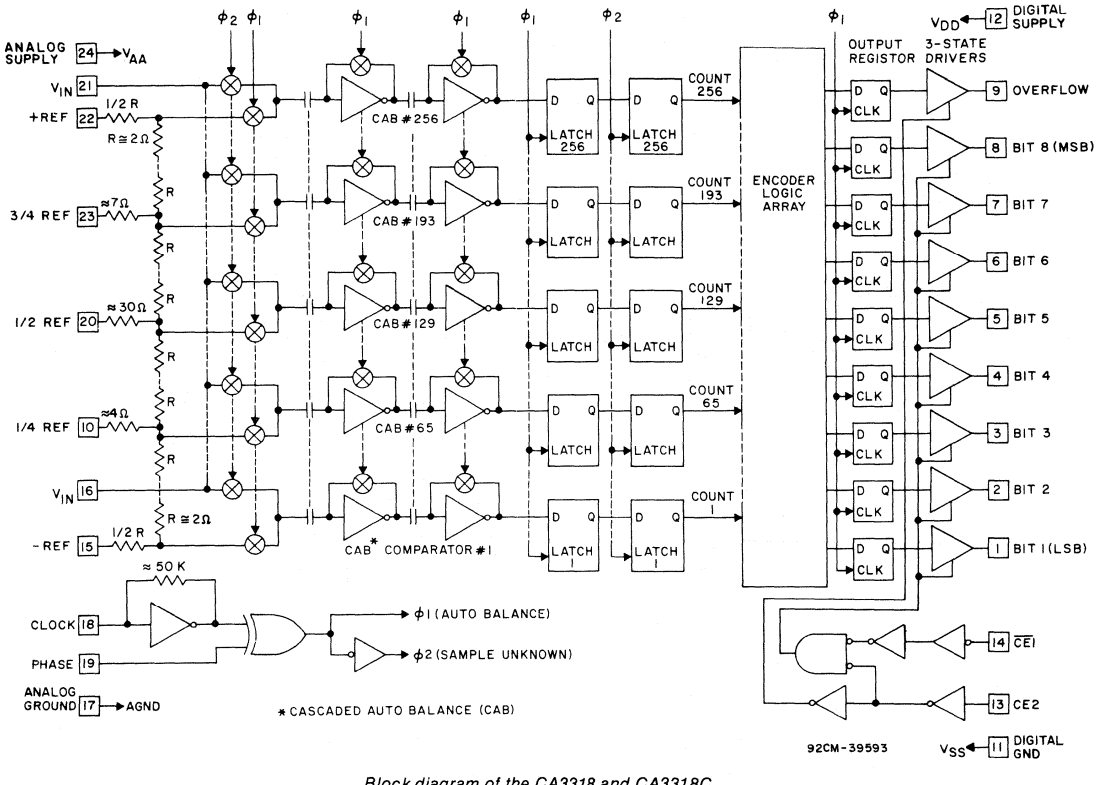
- *Pin compatible with 41051/CA3308*
- *CMOS/SOS low power*
- *Flash (Parallel) conversion technique*
- *15 MSPS conversion rate at 5 V (CA3318C)*
- *20 MSPS conversion rate at 5 V (CA3318)*
- *1 LSB differential linearity*
- *1.5 LSB integral linearity*
- *Single 4 to 6.5 V supply*
- *8 latched bit outputs plus overflow*
- *May be stacked for higher resolution*
- *May be paralleled for double speed*

Applications:

- *Especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *General-purpose hybrid ADC's*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*

The RCA CA3318 and CA3318C are pin compatible retrofits for the 41051/CA3308, but with the output data changing 1/2 clock cycle later. They have features similar to the CA3300 (File No. 1316), such as the control inputs and outputs necessary to allow stacking or paralleling for higher resolution or doubled speed. Separate analog and digital ground pins are available to allow analog to digital isolation. The reference resistor string is available at both + and - ends, and at the 1/4, 1/2, and 3/4 points, thus allowing the tailoring of non-linear transfer functions. In addition, the + reference (positive full scale) may be used above the analog + supply.

The CA3318 and CA3318C are available in a 24-lead dual-in-line plastic package (E suffix) and in a 24-lead dual-in-line ceramic package (D suffix).



Block diagram of the CA3318 and CA3318C.

Preview Data only

CA3338

CMOS High-Speed R-2R D/A Converter

Product Preview

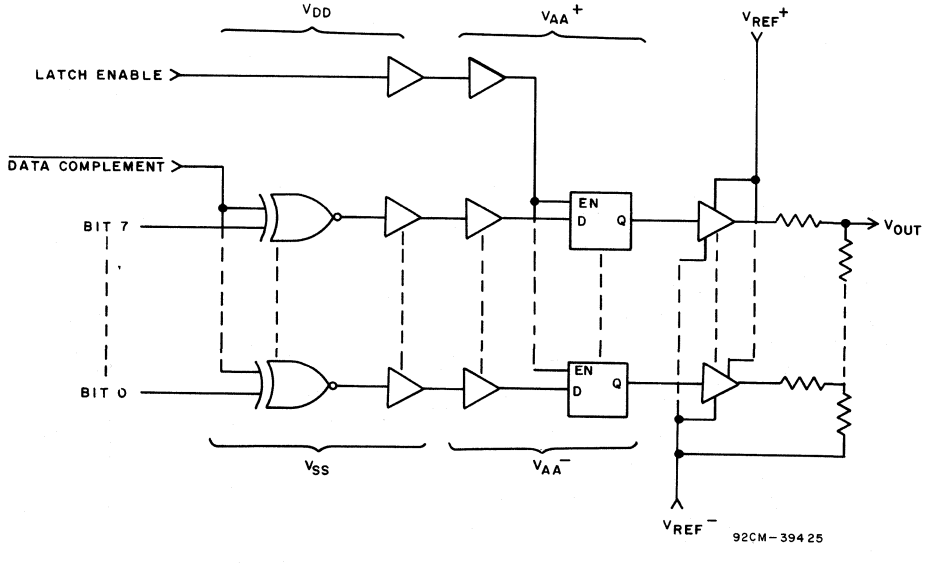
Features:

- *CMOS/SOS low power*
- *300 ohm R-2R ladder output*
- *20 MHz update rate*
- *1/2 LSB accuracy*
- *Single 3 to 8 V supply*
- *Input latch*
- *Data complement input*
- *Low glitch energy*
- *Level shifteres for bipolar output*

The RCA CA3338 is a CMOS 8-bit R-2R output D/A converter. It has separate analog and digital supply pins for isolation, and, due to level shifters on the data input lines, may operate with the output below digital ground. A data complement control inverts the output waveform, and a latch control allows the D/A to follow or hold the input data.

Careful attention has been paid to reducing output "glitch" energy and allowing clean video signals.

The CA3338 is available in a 16-lead dual-in-line plastic package (E suffix) and in a 16-lead dual-in-line ceramic package D suffix).



Block Diagram of the CA3338

Preview Data only

Product Preview

CA3999

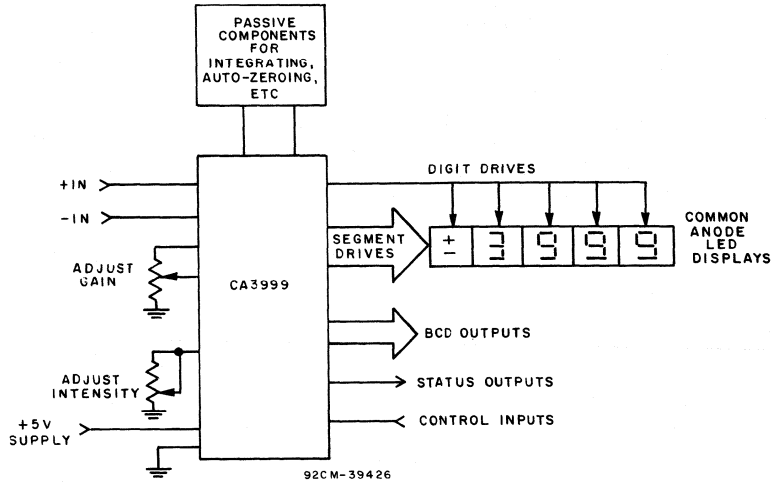
CMOS Complete 3-3/4 Digit DPM

Features:

- *Full ± 3999 count range*
- *True differential inputs*
- *Single +5 V supply*
- *Direct multiplexed LED drive*
- *Accurate on-chip reference*
- *BCD outputs available*
- *Good 50/60 cycle rejection*
- *LED brightness control*
- *Under and over-voltage outputs*

The RCA CA3999 is a true differential input ± 3999 count DPM with direct LED drive capability. It operates from a single + 5 V source and generates a negative supply (needed for negative input signals) on chip. A stable on-chip referenced is auto-zeroed for low-drift, as is the input integrator and comparator. The dual-slope converter integrates for an integral number of 50 or 60 cycles, thus providing good AC rejection. BCD data is output as well as multiplexed 7 segment LED drive. No external components are needed to interface to LEDs; the addition of an external pot will control brightness, however.

The CA3999 is available in a 40-lead dual-in-line plastic package (E suffix).



Block Diagram of the CA3999

Preview Data only

41051

Product Preview

CMOS High-Speed 8-Bit Flash A/D Converter

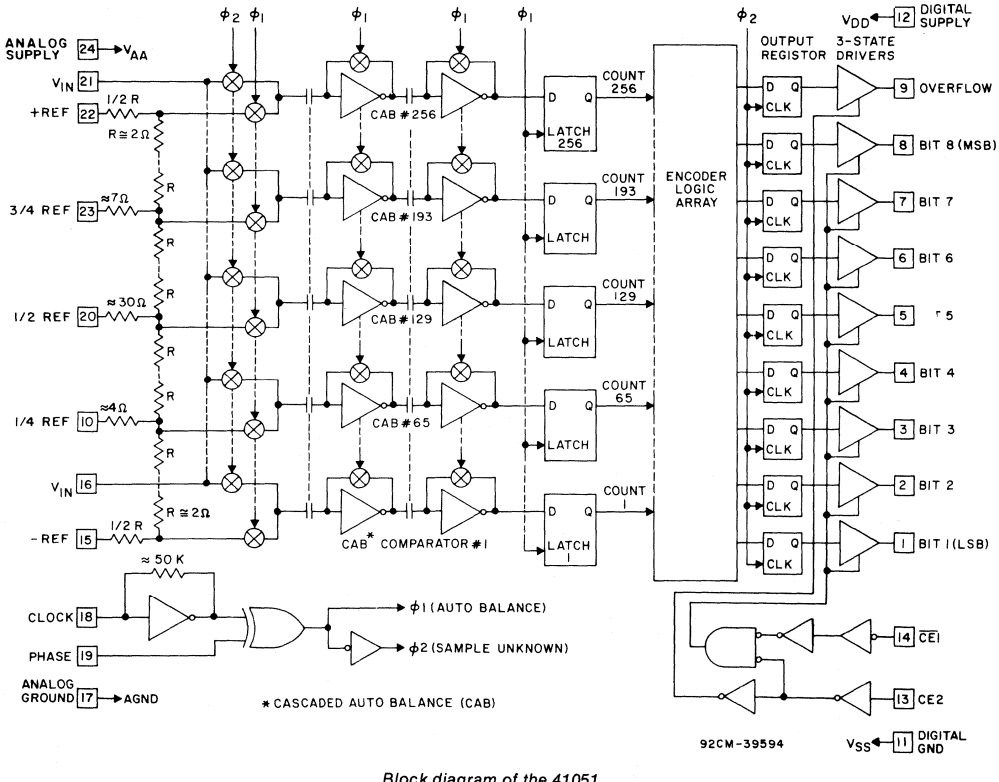
Features:

- *CMOS/SOS low power*
- *Flash (Parallel) conversion technique*
- *15 MSPS conversion rate at 5 V*
- *1 LSB differential linearity*
- *1.5 LSB integral linearity*
- *Single 5 V supply*
- *8 latched bit outputs plus overflow*
- *May be stacked for higher resolution*
- *May be paralleled for double speed*

The RCA 41051 is a low power (150 mW typ) 8-bit video speed analog-to-digital converter. It is similar in operation to the CA3300 (File No. 1316) and has the control inputs and outputs necessary to allow stacking or paralleling for higher resolution or doubled speed. Separate analog and digital ground pins are available to allow analog to digital isolation. The reference resistor string is available at both + and - ends, and at the 1/4, 1/2, and 3/4 points, thus allowing the tailoring of non-linear transfer functions. In addition, the + reference (positive full scale) may be used above the analog + supply.

The 41051 is available in a 24-lead dual-in-line ceramic package (D suffix).

For new equipment designs, the CA3318 or CA3318C is recommended.



Block diagram of the 41051.

Preview Data only

Telecommunication Circuits — Technical Data

Telecommunication Circuits (Cont'd)

Type No.	Description	Page No.
Modems		
CD22223	1200 — Baud FSK	98
Crosspoint Switches		
CD22100	4x4x1 Crosspoint	64
CD22101	4x4x2 Crosspoint	72
CD22102	4x4x2 Crosspoint Set/Reset Input	72
CD54/74HC22106	8x8x1 Crosspoint	130
CD54/74HCT22106	8x8x1 Crosspoint	130
Transient Suppressor—Surgectors		
SGT03U13	30 Volts Uni-Directional	—
SGT06U13	60 Volts Uni-Directional	—
SGT23U13	230 Volts Uni-Directional	—
SGT10S10	100 Volts, 3 Terminal Crowbars—SCR	—
Interface (UARTS)		
CDP1854A	Programmable UART	—
CDP6402	CMOS Universal Asynchronous Receiver/Transmitter (UART)	—
CDP65C61	CMOS Asynchronous Communications Interface Adapter (ACIA)	—
CDP6853	CMOS Asynchronous Communications Interface Adapter (ACIA), Motel Bus	—
Data Transmission and Interface		
CD54/74HC/HCT240	Octal Buffer/Line Drivers, 3-State, Inverting	—
CD54/74HC/HCT241	Octal Buffer/Line Drivers, 3-State, Non-Inverting	—
CD54/74HC/HCT244	Octal Buffer/Line Drivers, 3-State, Non-Inverting	—
CD54/74HC/HCT245	Octal-Bus Transceivers, 3-State, Non-Inverting	—
CD54/74HC/HCT373	Octal Transparent Latches, 3-State Output	—
CD54/74HC/HCT533	Octal Inverting Transparent Latches, 3-State Output	—
CD54/74HC/HCT540	Octal Buffer and Line Drivers, 3-State, Inverting	—
CD54/74HC/HCT541	Octal Buffer & Line Drivers, 3-State, Non-Inverting	—
CD54/74HC/HCT563	Octal Inverting Transparent Latches, 3-State Output	—
CD54/74HC/HCT573	Octal Transparent Latches, 3-State Output	—
CD54/74HC/HCT640	Octal 3-State Bus Transceivers, Inverting	—
CD54/74HC/HCT643	Octal 3-State Bus Transceivers, True/Inverting	—
CD54/74HC/HCT646	Octal Bus Transceivers/Registers,3-State, Non-Inverting	—
CD54/74HC/HCT648	Octal-Bus Transceiver/Registers, 3-State, Inverting	—
CD54/74HC/HCT40105	4-Bits x 16 Words FIFO Registers	—
CD22103	CMOS/SOS 2.048/8.448 Mb/S Transcoder	82
CD22301	PCM Line Repeater	101
CD40116	High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter	—
Switching Systems		
CD54/74HC/HCT4016	Quad Bilateral Switches	—
CD54/74HC/HCT4051	Single 8-Channel Analog MUX/DEMUX	—
CD54/74HC/HCT4052	Differential 4-Channel Analog MUX/DEMUX	—
CD54/74HC/HCT4053	Triple 2-Channel Analog MUX/DEMUX	—
CD54/74HC/HCT4316	Quad Analog Switches with Latches	—
CD54/74HC/HCT4351	Single 8-Channel Analog MUX/DEMUX with Latches	—
CD54/74HC/HCT4352	Differential 4-Channel Analog MUX/DEMUX with Control Latches	—
CD54/74HC/HCT4353	Triple 2-Channel Analog MUX/DEMUX with Control Latches	—
CD4016	Quad Bilateral Switch	—
CD4051	Single 8-Channel Analog Multiplexer/Demultiplexer	—
CD4052	Differential 4-Channel Analog MUX/DEMUX	—
CD4053	Triple 2-Channel Analog MUX/DEMUX	—
CD4066	Quad Bilateral Switch	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290,* QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CDPXXXX types, refer to *DATABOOK SSD-260,* CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on SGT types, refer to the specific data bulletin for that type shown in the *Index to Devices.*

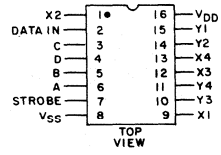
CD22100

COS/MOS 4 x 4 Crosspoint Switch with Control Memory

High-Voltage Types (20-Volt Rating)

Features:

- *Low ON resistance - 75 Ω typ. at V_{DD} = 12 V*
- *"Built-in" control latches*
- *Large analog signal capability - ± $V_{DD}/2$*
- *10-MHz switch bandwidth*
- *Matched switch characteristics*
  ΔR_{ON} = 18 Ω typ. at V_{DD} = 12 V
- *High linearity - 0.5% distortion (typ.) at f = 1 kHz,*
  V_{IN} = 5 Vp-p, V_{DD} = 10 V, and R_L = 1 kΩ
- *Standard COS/MOS noise immunity*
- *100% tested for maximum quiescent current at 20 V*



Terminal Assignment

The RCA-CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data-in low, then addressing all switches in succession.

The CD22100 is supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

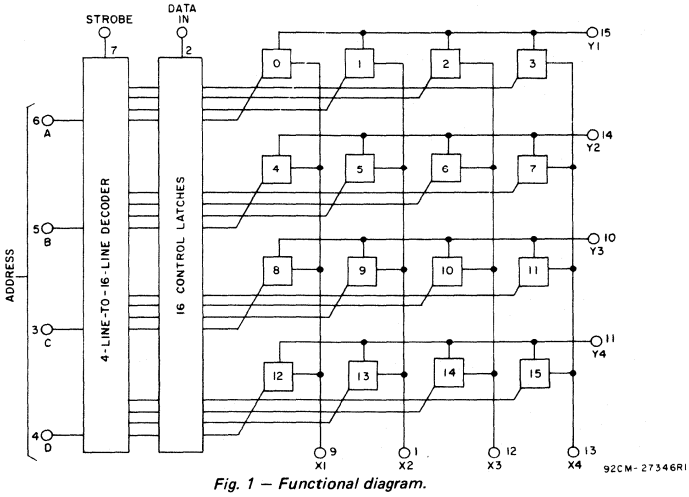


Fig. 1 – Functional diagram.

File Number **1076**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT * ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER TRANSMISSION GATE
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

* Maximum current through transmission gates (switches) = 25 mA.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

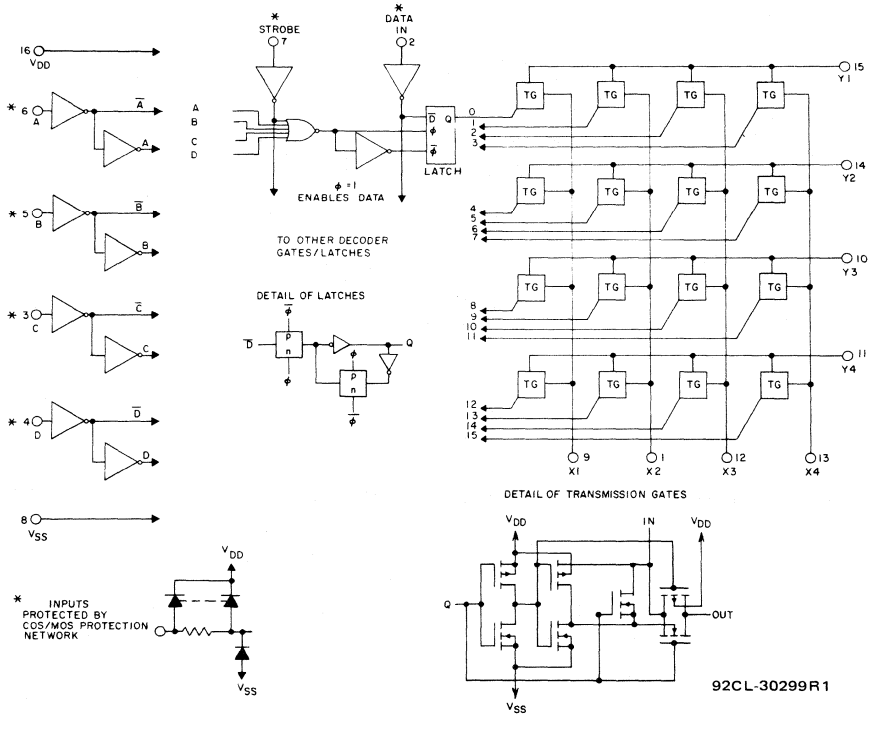


Fig. 2 – Schematic diagram.

CD22100

TRUTH TABLE									
Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg							Units
		V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	μA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	450	1000	1440	1625	–	225	1250	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	35	–	Ω
		–	10	–	–	–	–	–	20	–	
		–	12	–	–	–	–	–	18	–	
		–	15	–	–	–	–	–	15	–	
OFF Switch Leakage Current I_L Max.	All switches OFF	0,18	18	±100		±1000		–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 μA	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

* Determined by minimum feasible leakage measurement for automatic testing.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	$C_L = 50pF$; t_r, $t_f = 20$ ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion)	1	1	5	10	–	0.5	–	%
Feedthrough (All Switches OFF)	1.6	1	5	10	–	–80	–	dB
	Sine wave input							
Frequency for Signal Crosstalk Attenuation of 40 dB	–	1	10	10	–	1.5	–	MHz
Attenuation of 110 dB	Sine wave input					0.1		kHz
Capacitance, X_n to Ground		–	–	5-15	–	18	–	pF
Y_n to Ground		–	–	5-15	–	30	–	
Feedthrough		–	–	–	–	0.4	–	
CONTROLS			See Fig.					
Propagation Delay Time: Strobe to Output, t_{PZH} (Switch Turn-ON to High Level)	R_L=1kΩ, C_L=50pF, t_r,t_f = 20 ns		16	5	–	300	600	ns
				10	–	125	250	
				15	–	80	160	
Data-In to Output, t_{PZH} (Turn-On to High Level)			17	5	–	110	220	
				10	–	40	80	
				15	–	25	50	
Address to Output, t_{PZH} (Turn-ON to High Level)			18	5	–	350	700	
				10	–	135	270	
				15	–	90	180	
Propagation Delay Time: Strobe to Output, t_{PHZ} (Switch Turn-OFF)			16	5	–	165	330	ns
				10	–	85	170	
				15	–	70	140	
Data-In to Output, t_{PZL} (Turn-ON to Low Level)			17	5	–	210	420	
				10	–	110	220	
				15	–	100	200	
Address to Output, t_{PHZ} (Turn-OFF)			18	5	–	435	870	
				10	–	210	420	
				15	–	160	320	
Minimum Setup Time, Data-In to Strobe, Address, t_{SU}				5	–	95	190	ns
				10	–	25	50	
				15	–	15	30	
Minimum Hold Time, Data-In to Strobe, Address, t_H				5	–	180	360	ns
				10	–	110	220	
				15	–	35	70	

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$.

CD22100

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CONTROLS (CONT'D)								
Maximum Switching Frequency, f_ϕ	R_L=1kΩ, C_L=50 pF; t_r, t_f = 20 ns			5	0.6	1.2	–	MHz
				10	1.6	3.2	–	
				15	2.5	5	–	
Minimum Strobe Pulse Width, t_W				5	–	300	600	ns
				10	–	120	240	
				15	–	90	180	
Control Crosstalk, Data-In, Address, or Strobe to Output	–	10	10	10	–	75	–	mV (peak)
	Square wave input t_r, t_f = 20 ns							
Input Capacitance, C_{IN}	Any Control Input			—	–	5	7.5	pF

●Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$

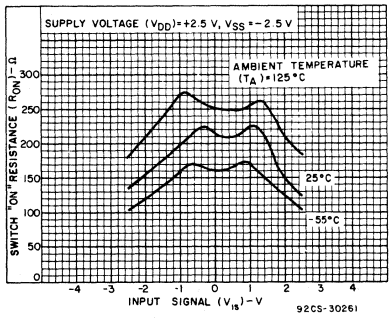


Fig. 3 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} =$ 2.5 V.

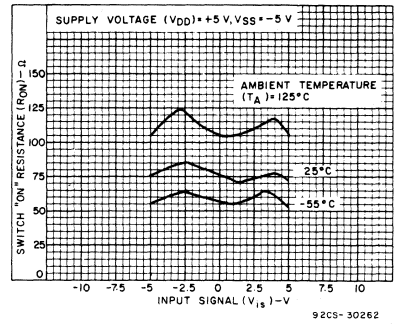


Fig. 4 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} =$ 5 V.

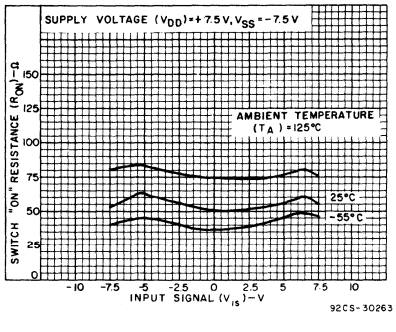


Fig. 5 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} =$ 7.5 V.

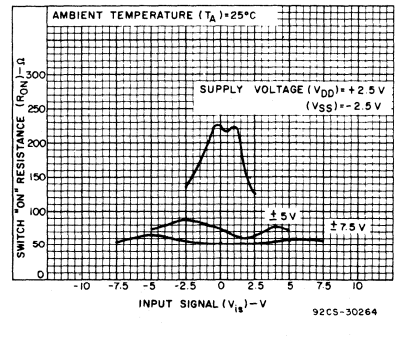


Fig. 6 – Typical ON resistance as a function of input signal voltage at $T_A = 25^\circ C$.

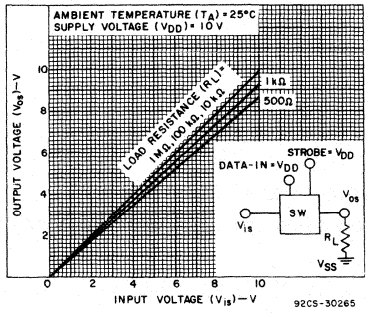


Fig. 7 – Typical switch ON transfer characteristics (1 of 16 switches).

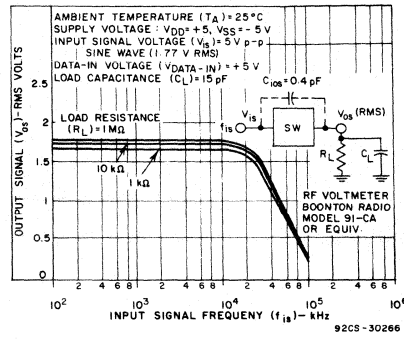


Fig. 8 – Typical switch ON frequency response characteristics.

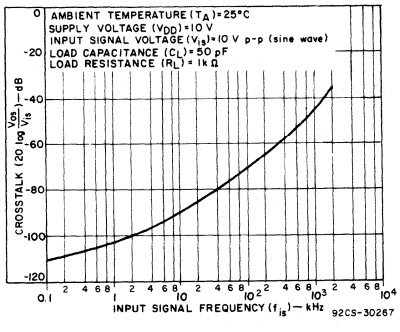


Fig. 9 – Typical crosstalk between switches as a function of signal frequency.

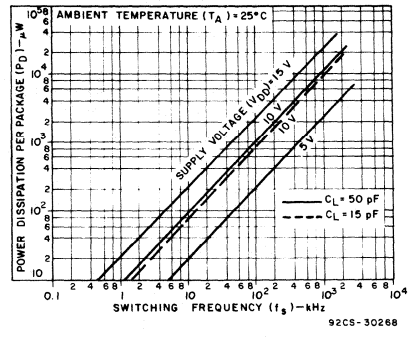


Fig. 10 – Typical dynamic power dissipation as a function of switching frequency.

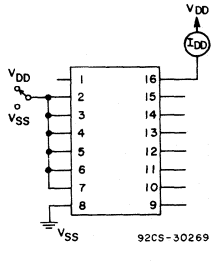


Fig. 11 – Quiescent current test circuit.

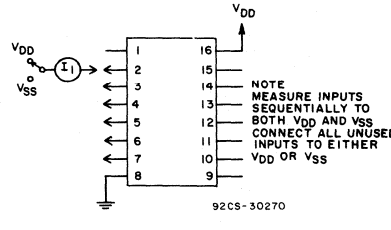


Fig. 12 – Input current test circuit.

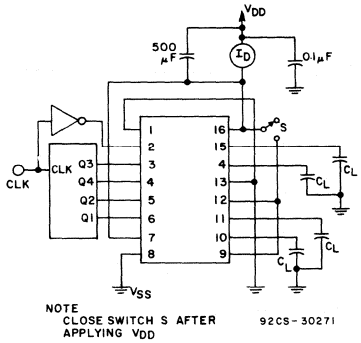


Fig. 13 – Dynamic power dissipation test circuit.

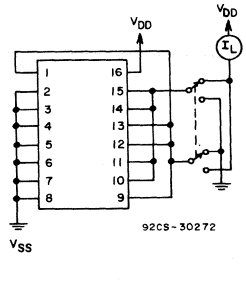


Fig. 14 – OFF switch input or output leakage current test circuit.

CD22100

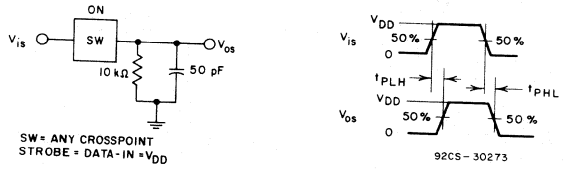


Fig. 15 — Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

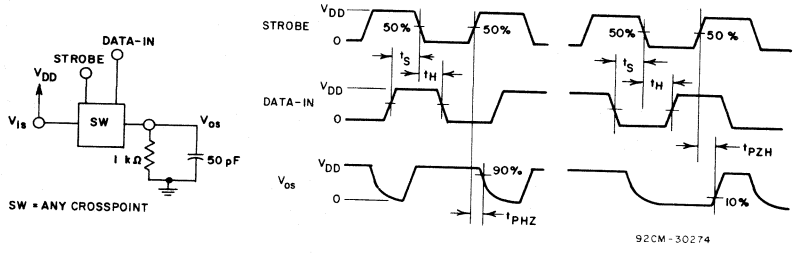


Fig. 16 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

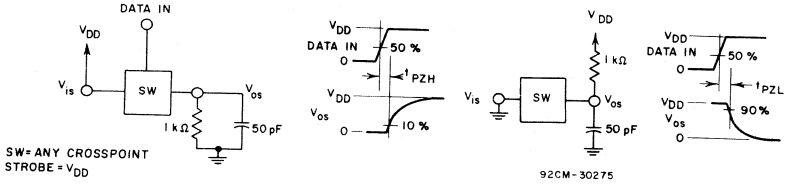


Fig. 17 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

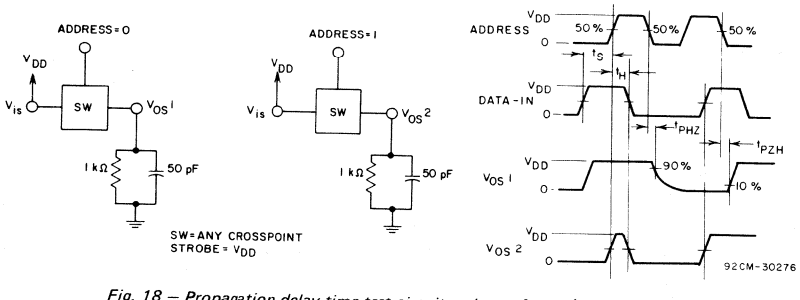


Fig. 18 — Propagation delay time test circuit and waveforms (address to signal output, switch Turn-On or Turn-OFF).

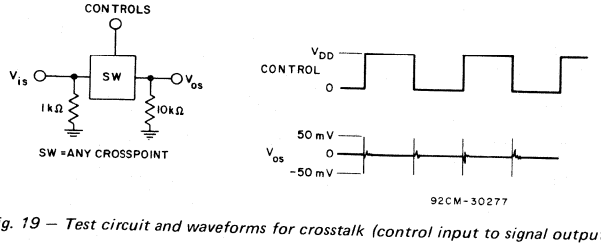


Fig. 19 — Test circuit and waveforms for crosstalk (control input to signal output).

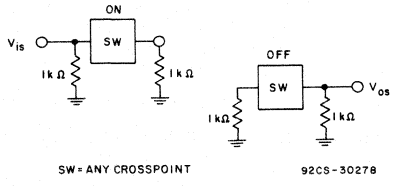
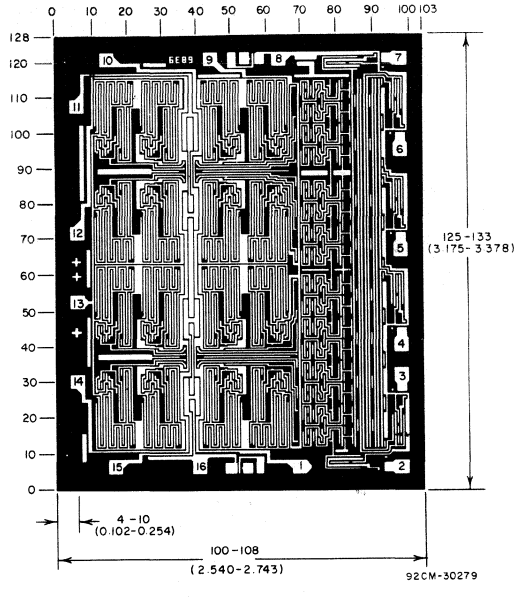


Fig. 20 – Test circuit for crosstalk between switch circuits in the same package.



Dimensions and pad layout for CD22100H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

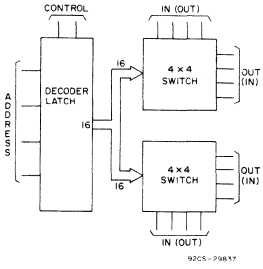
The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CD22101, CD22102

COS/MOS 4 x 4 x 2 Crosspoint Switches With Control Memory

Features:

- *Low ON resistance - 75 Ω typ. at V_{DD} = 12 V*
- *"Built-in" latched inputs*
- *Large analog signal capability - ± V_{DD}/2*
- *10-MHz switch bandwidth*
- *Matched switch characteristics*
  ΔR_{ON} = 8 Ω typ. at V_{DD} = 12 V
- *High linearity - 0.25% distortion (typ.) at f = 1 kHz,*
  V_{IN} = 5 Vp-p, V_{DD} - V_{SS} = 10 V, and R_L = 1 kΩ
- *Standard COS/MOS noise immunity*



CD22101, CD22102
Functional Diagram

The RCA-CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be ON simultaneously. Corresponding crosspoints in each array are turned on and off simultaneously, also.

In the CD22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

Applications:

- *Telephone system*
- *Studio audio switching*
- *Multisystem bus interconnect*
- *PBX*

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT * ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

* Maximum current through transmission gates (switches) = 25 mA.

File Number **1039**

CD22101, CD22102

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

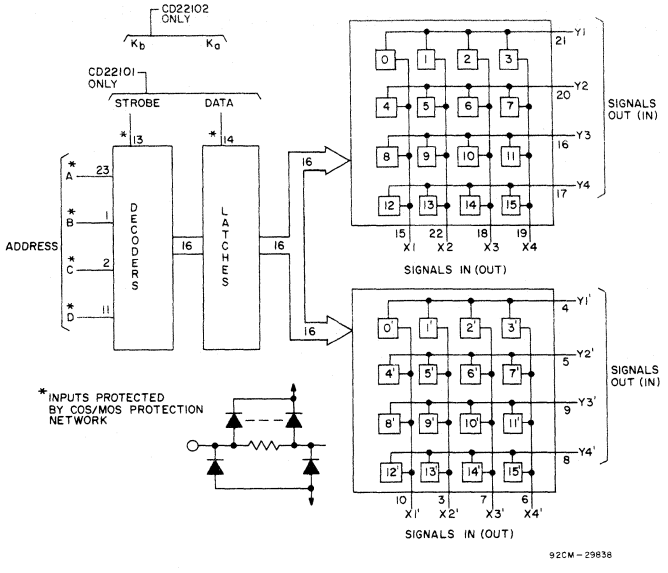


Fig. 1 — Functional block diagram.

DECODER TRUTH TABLE

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1 & X1′Y1′	0	0	0	1	X1Y3 & X1′Y3′
1	0	0	0	X2Y1 & X2′Y1′	1	0	0	1	X2Y3 & X2′Y3′
0	1	0	0	X3Y1 & X3′Y1′	0	1	0	1	X3Y3 & X3′Y3′
1	1	0	0	X4Y1 & X4′Y1′	1	1	0	1	X4Y3 & X4′Y3′
0	0	1	0	X1Y2 & X1′Y2′	0	0	1	1	X1Y4 & X1′Y4′
1	0	1	0	X2Y2 & X2′Y2′	1	0	1	1	X2Y4 & X2′Y4′
0	1	1	0	X3Y2 & X3′Y2′	0	1	1	1	X3Y4 & X3′Y4′
1	1	1	0	X4Y2 & X4′Y2′	1	1	1	1	X4Y4 & X4′Y4′

CONTROL TRUTH TABLE FOR CD22101

Function	Address				Strobe	Data	Select
	A	B	C	D			
Switch On	1	1	1	1	1	1	15 (X4Y4) & 15′ (X4′Y4′)
Switch Off	1	1	1	1	1	0	15 (X4Y4) & 15′ (X4′Y4′)
No Change	X	X	X	X	0	X	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

CD22101, CD22102

CONTROL TRUTH TABLE FOR CD22102

Function	Address				K_a	K_b	Select
	A	B	C	D			
Switch On	1	1	1	1	1	0	15 (X4Y4) & 15′ (X4′Y4′)
Switch Off	1	1	1	1	0	1	15 (X4Y4) & 15′ (X4′Y4′)
All Switches Off#	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

In the event that K_a and K_b are changed from levels 1,1 to 0,0 K_b should not be allowed to go to 0 before K_a, otherwise a switch which was off will inadvertently be turned on.

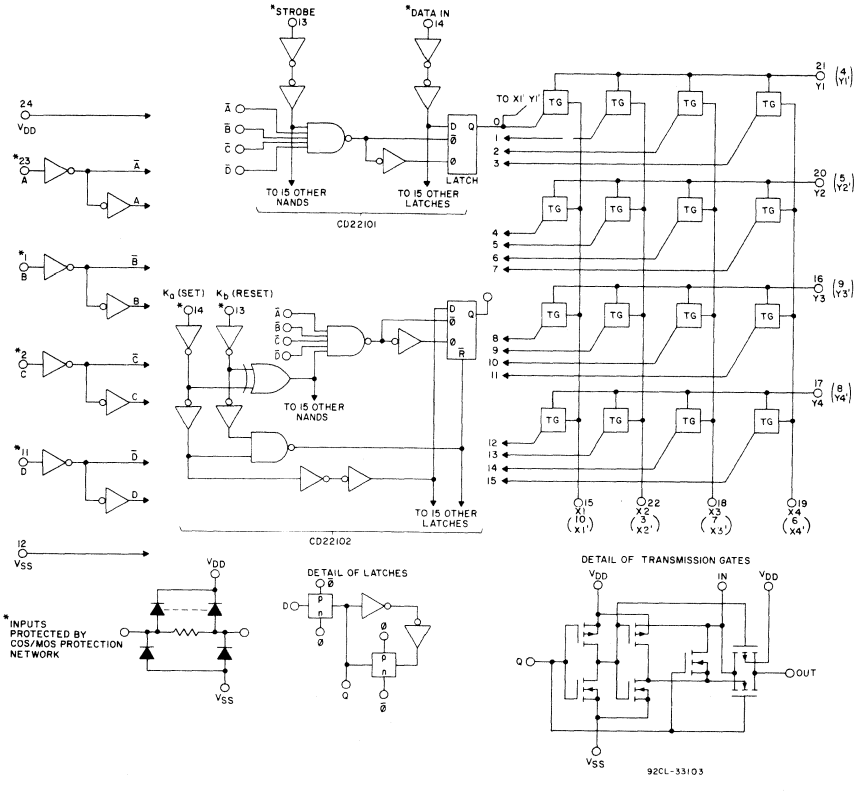


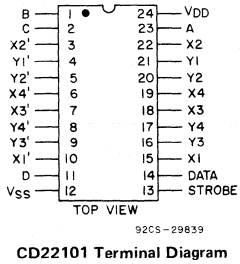
Fig. 2 – Logic diagram.

CD22101, CD22102

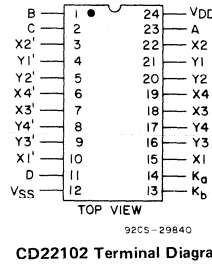
STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg							Units
		V_{IS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	μA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	475	500	725	800	–	225	600	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	25	–	Ω
		–	10	–	–	–	–	–	10	–	
		–	12	–	–	–	–	–	8	–	
		–	15	–	–	–	–	–	5	–	
OFF Leakage Current I_L Max.	All switches OFF	0,18	18	±1000				–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 μA;	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

* Determined by minimum feasible leakage measurement for automatic testing.



CD22101 Terminal Diagram



CD22102 Terminal Diagram

CD22101, CD22102

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion	1	1	2.5	5	–	1	–	%
	1	1	5	10	–	0.25	–	
	1	1	7.5	15	–	0.15	–	
Feedthrough All Switches OFF (See Fig. 24)	1.6	0.6	2■	10	–	–96	–	dB
	Sine wave input							
Frequency for Signal Crosstalk Attenuation of 40 dB	–	0.6	1■	10	–	2.5	–	MHz
Attenuation of 95 dB (See Fig. 23)	Sine wave input					0.1		kHz
Capacitance,								
X_n to Ground		–	–	–	–	25	–	
Y_n to Ground		–	–	–	–	60	–	pF
Feedthrough		–	–	–	–	0.6	–	
CONTROLS			See Fig.					
Propagation Delay Time, High Impedance to High Level or Low Level, t_{PZH}, t_{PZL} Strobe to Output, CD22101	R_L = 1 kΩ, C_L = 50 pF, t_r, t_f = 20 ns		16	5	–	500	1000	ns
				10	–	230	460	
				15	–	170	340	
Data-In to Output, CD22101			17	5	–	515	1000	
				10	–	220	440	
				15	–	170	340	
K_a to Output, CD22102				5	–	500	1000	
				10	–	215	430	
				15	–	160	320	
Address to Output, CD22101, CD22102			18	5	–	480	960	
				10	–	225	450	
				15	–	155	300	
Propagation Delay Time, High Level or Low Level to High Impedance, t_{PHZ}, t_{PLZ} Strobe to Output, CD22101			16	5	–	450	900	
				10	–	200	400	
				15	–	135	270	
K_b to Output, CD22102				5	–	450	900	
				10	–	200	400	
				15	–	130	260	
Data-In to Output, CD22101				5	–	450	900	
				10	–	165	330	
				15	–	110	220	
$K_a \cdot K_b$ to Output, CD22102				5	–	280	560	
				10	–	130	260	
				15	–	90	180	

● Peak-to-peak voltage symmetrical about V_{DD} unless otherwise specified. ■ RMS

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CONTROLS (cont'd)			See Fig.					
Address to Output, CD22101, CD22102	R_L = 1 k, C_L = 50 pF, t_r,t_f = 20 ns		18	5	–	425	850	ns
				10	–	190	380	
				15	–	130	260	
Minimum Strobe Pulse Width t_W CD22101				5	–	260	500	
				10	–	120	240	
				15	–	80	160	
Address to Strobe Setup or Hold Times, t_{SU}, t_h, CD22101			19	5	–	−160	0	
				10	–	−70	0	
				15	–	−50	0	
Strobe to Data-In Hold Time, Time, t_{hHL}; t_{hLH}, CD22101			20	5	–	200	400	
				10	–	80	160	
				15	–	60	120	
Address to K_a and K_b Setup or Hold Times, t_{SU}, t_H, CD22102				5	–	−160	0	
				10	–	−70	0	
				15	–	−50	0	
Minimum K_a·K_b Pulse Width, t_W CD22102				5	–	375	750	
				10	–	160	320	
				15	–	110	220	
Minimum K_a Pulse Width, t_W CD22102				5	–	425	850	
				10	–	175	350	
				15	–	120	240	
Minimum K_b Pulse Width, t_W CD22102				5	–	200	400	
				10	–	90	180	
				15	–	70	140	
Control Crosstalk, Data-In, Address, or Strobe to Output,	100	10	21	5	–	75	–	mv (peak)
	Square wave input = 5 V, t_r,t_f=20 ns, R_s=1kΩ							
Input Capacitance, C_{IN}	Any Control Input			–	–	5	7.5	pF

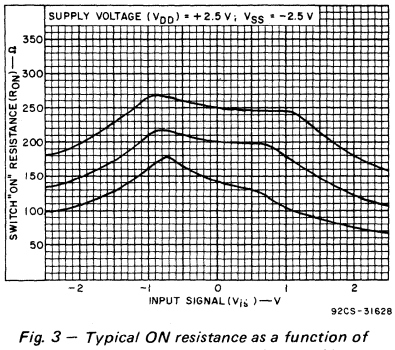


Fig. 3 — Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 2.5$ V.

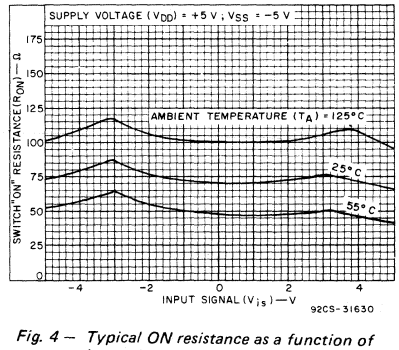


Fig. 4 — Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 5$ V.

CD22101, CD22102

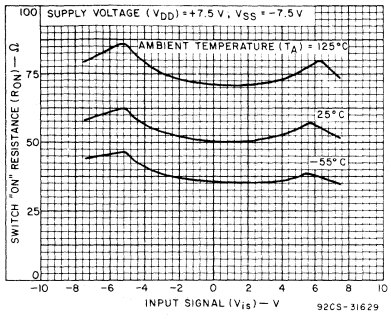


Fig. 5 — Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 7.5$ V.

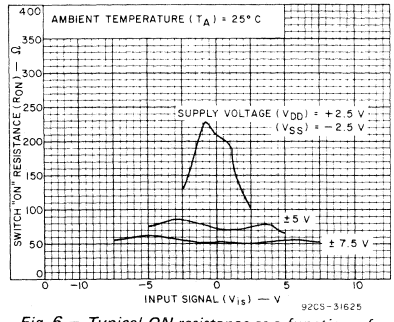


Fig. 6 — Typical ON resistance as a function of input signal voltage at $T_A = 25°C$.

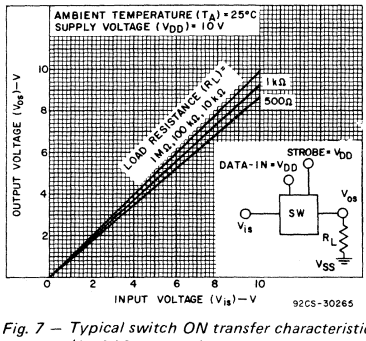


Fig. 7 — Typical switch ON transfer characteristics (1 of 16 switches).

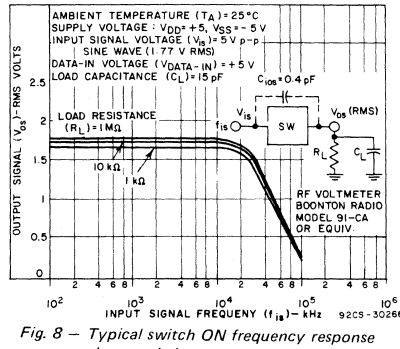


Fig. 8 — Typical switch ON frequency response characteristics.

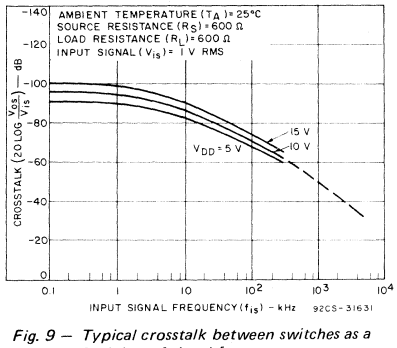


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

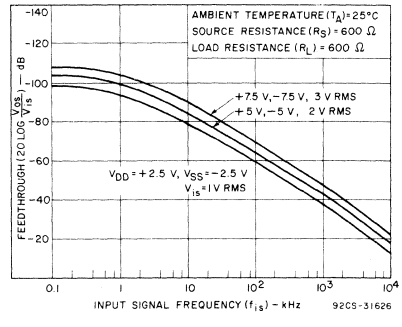


Fig. 10 — Typical feedthrough, any OFF switch as a function of frequency.

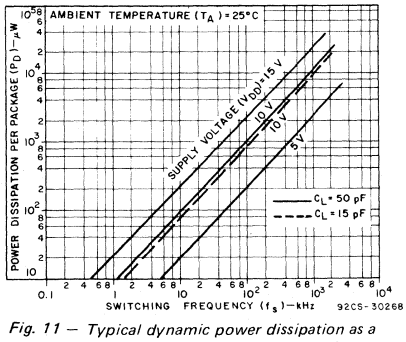


Fig. 11 — Typical dynamic power dissipation as a function of switching frequency for CD22101.

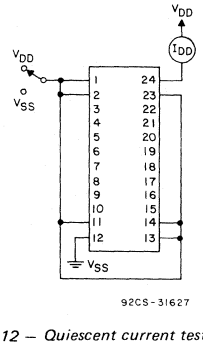


Fig. 12 — Quiescent current test circuit.

CD22101, CD22102

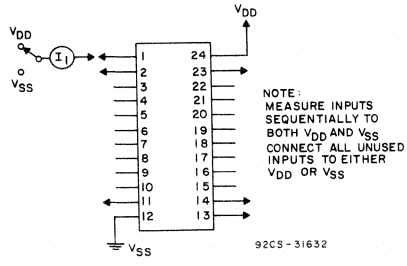


Fig. 13 – Input current test circuit.

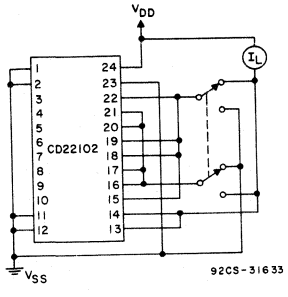


Fig. 15 – OFF switch input or output leakage current test circuit (16 of 32 switches).

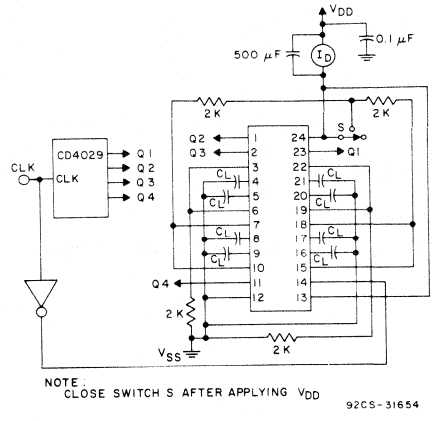


Fig. 14 – Dynamic power dissipation test circuit for CD22101.

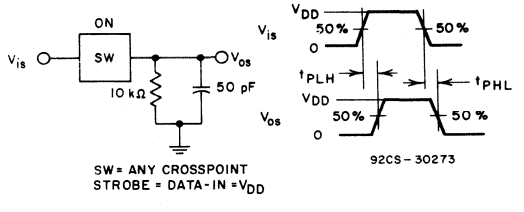


Fig. 16 – Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

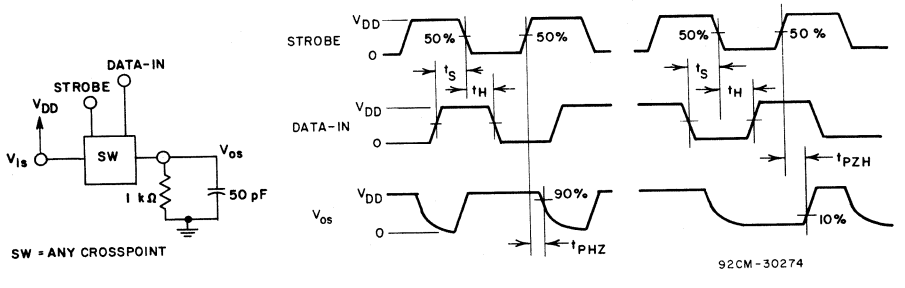


Fig. 17 – Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

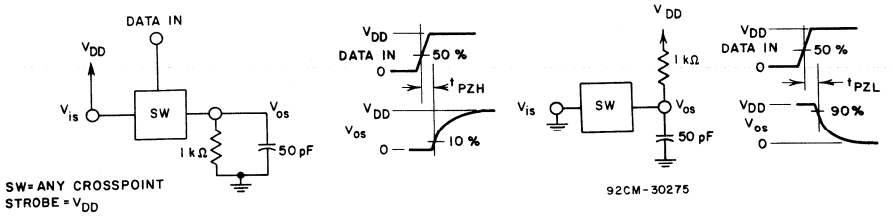


Fig. 18 – Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

CD22101, CD22102

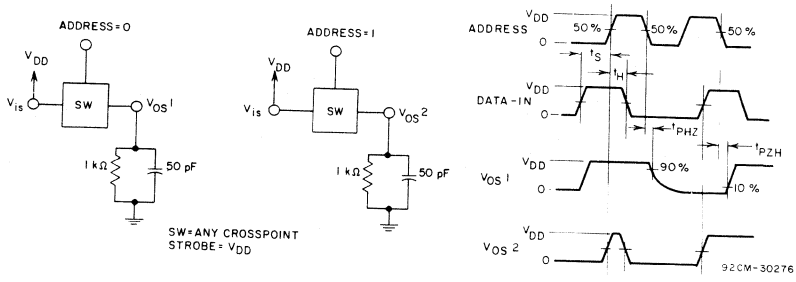


Fig. 19 – Propagation delay time test circuit and waveforms (address to signal output, switch turn-ON or Turn-OFF).

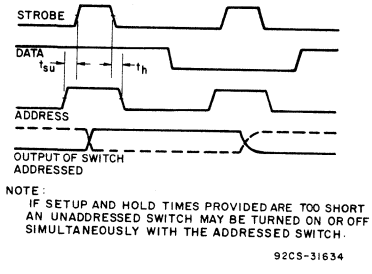


Fig. 20 – Address to strobe setup and hold times.

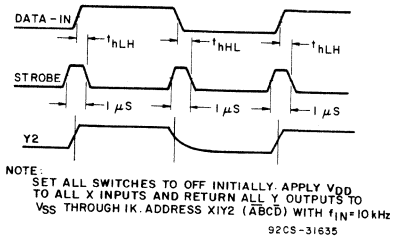


Fig. 21 – Strobe to Data-In hold time t_h, for CD22101.

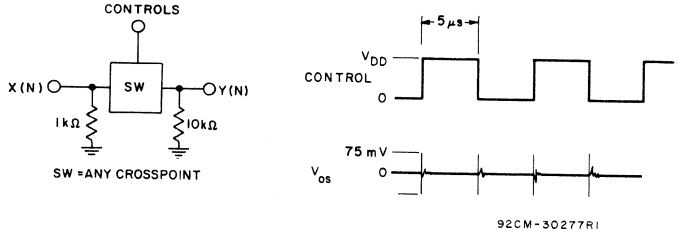


Fig. 22 – Test circuit and waveforms for crosstalk (control input to signal output).

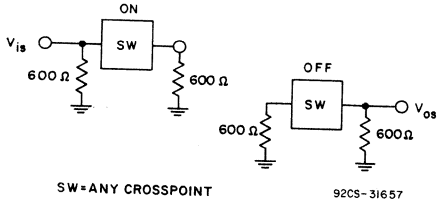


Fig. 23 – Test circuit for crosstalk between switch circuits in the same package.

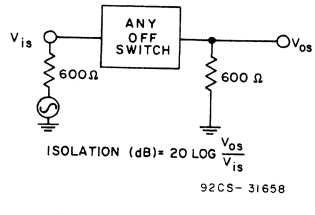


Fig. 24 – Test circuit for feedthrough (any OFF switch).

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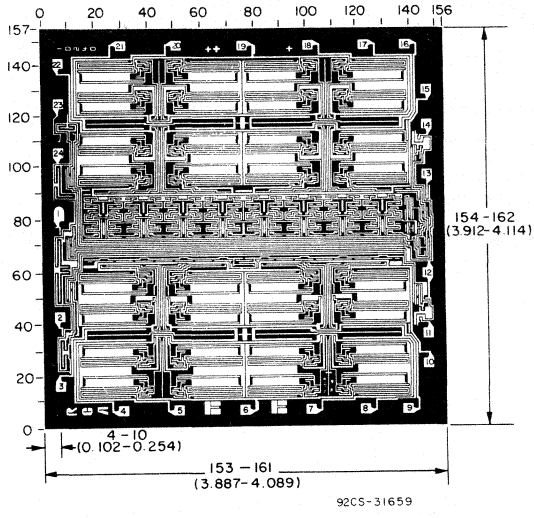
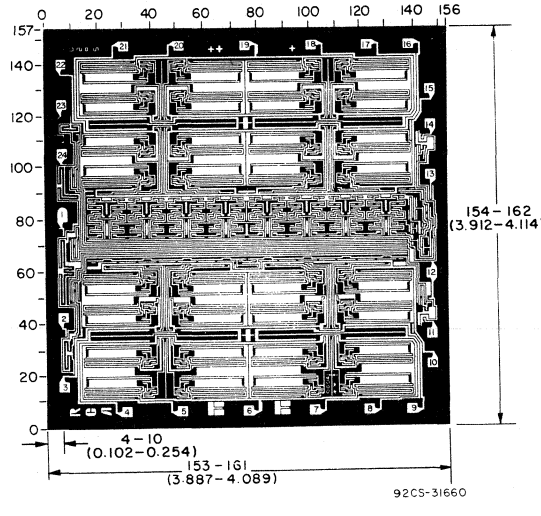


Dimensions and pad layout for CD22101H.



Dimensions and pad layout for CD22102H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

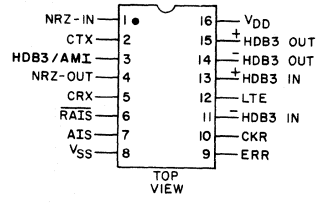
Advance Information/
Preliminary Data

CD22103A

CMOS HDB3 (High-Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications

Features:

- *HDB3 coding and decoding for data rates from 50 Kb/s to 10 Mb/s in a manner consistent with CCITT G703 recommendations*
- *HDB3/AMI transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections*
- *All transmitter and receiver inputs/outputs are TTL compatible*
- *Internal Loop Test capability*



Terminal Assignment

The RCA-CD22103A is an LSI SOS integrated circuit which performs the HDB3 transmission coding and reception decoding functions with error detection. It is used in 2.048 and 8.448 Mb/s transmission applications. The CD22103A performs HDB3 coding and decoding for data rates from 50 Kb/s to 10 Mb/s in a manner consistent with CCITT G703 recommendations.

HDB3 transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections. All transmitter and receiver inputs/outputs are TTL compatible.

The HDB3 transmitter coder codes an NRZ binary unipolar input signal (NRZ-IN) and a synchronous transmission clock (CTX) into two HDB3 binary unipolar RZ output signals (+HDB3 OUT, -HDB3 OUT). The TTL compatible output signals +HDB3 OUT, -HDB3 OUT are externally mixed to generate ternary bipolar HDB3 signals for driving transmission lines.

The receiver decoder converts binary unipolar inputs (+HDB3 IN, -HDB3 IN), which were externally split from ternary bipolar HDB3 signals, and a synchronous clock signal (CRX) into binary unipolar NRZ signals (NRZ-OUT).

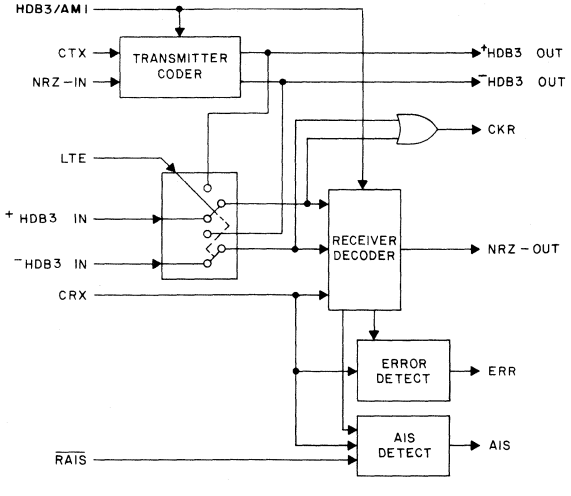


Fig. 1 - Block diagram of the CD22103A.

File Number **1310**

Received signals not consistent with HDB3 coding rules are detected as errors. The receiver error output (ERR) is active high during one CRX period of each bit of received data that is inconsistent with HDB3 coding rules.

An input string consisting of all ones (or marks) is detected and signaled by a high level at the Alarm Signal (AIS) output. The AIS output is set to a high level when less than three zeros are received during two consecutive periods of the Reset Alarm Inhibit Signal (RAIS). The AIS output is subsequently reset to a low level when three or more zeros are received during two periods of the reset signal (RAIS).

A diagnostic Loop-Test Mode may be entered by driving the Loop Test Enable Input (LTE) high. In this mode the HDB3 transmitter outputs (+HDB3 OUT, -HDB3 OUT) are internally connected to the HDB3 receiver inputs, and the external HDB3 receiver inputs (+HDB3 IN, -HDB3 IN) are disabled. The NRZ binary output signal (NRZ - OUT) corresponds to the NRZ binary input signal (NRZ - IN) delayed by approximately 8 clock periods.

The Clock Receiver Output (CKR) is the product of the two HDB3 input signals or-ed together. The CRX clock signal may be derived from the CKR signal with external clock extraction circuitry. In the Loop Test Mode (LTE = 1) CKR is the product of the +HDB3 OUT and -HDB3 OUT signals or-ed together.

The CD22103A may also be used to perform the AMI to NRZ coding/decoding function. To use the CD22103A in this mode, the HDB3/AMI control input is driven low.

The RCA-CD22103A operates with a 5 V ±10% power supply voltage over the full military temperature range at data rates from 50 Kb/s up to 10 Mb/s.

The RCA-CD22103A is similar in function and pin configuration to type MJ1471.

The CD22103A types are supplied in 16-lead hermetic dual-in-line welded-seal ceramic packages (D suffix), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to + 8 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to + 60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, H ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Supply Voltage Range (For T_A=Full Package-Temperature Range)	4.5	5.5	V

CD22103A

STATIC ELECTRICAL CHARACTERISTICS, V_{DD} = 5 V ±10%; T_A = 25° C

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}	—	—	100	μA
Operating Device Current (f_{CL} = 10 MHz)		—	—	8	mA
HDB3 Output Low (Sink) Current (V_{OL} = 0.5 V)	I_{OL1}	1.6	—	—	
HDB3 Output High (Source) Current (V_{OH} = 2.8 V)	I_{OH1}	-10	—	—	
All Other Outputs Low (Sink) Current (V_{OL} = 0.5 V)	I_{OL2}	1.6	—	—	
All Other Outputs High (Source) Current (V_{OL} = 2.8 V)	I_{OH2}	-1.6	—	—	
Input Low Current	I_{IL}	—	—	-1	μA
Input High Current	I_{IH}	—	—	1	
Input Low Voltage (Max.)	V_{IL}	—	—	0.8	V
Input High Voltage (Min.)	V_{IH}	2	—	—	
Input Capacitance	C_{IN}	—	—	5	pF

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A range of -40° C to +85° C for plastic package; -55° C to +125° C for ceramic package; V_{DD} range of 4.5 V to 5.5 V, C_L = 15 pF

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
INPUT					
CTX, CRX Input Frequency	f_{CTX}, f_{CRX}	0.05	—	10	MHz
CTX, CRX Input Rise Time *	t_{rcl}	—	—	1	μs
Fall Time *	t_{fcl}	—	—	1	
NRZ-IN to CTX					
Data Setup Time *	t_s	15	—	—	ns
Data Hold Time *	t_H	15	—	—	
HDB3 IN to CRX					
Data Setup Time §	t_s	55	—	—	ns
Data Hold Time *	t_H	0	—	—	
CRX to CKR					
CRX = 8.448 MHz					
Pretrigger •	t_p	—	—	20	ns
Delay	t_d	—	—	20	

* See Fig. 4 § See Fig. 5 • See Fig. 6

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A range of -40° C to +85° C for plastic package; -55° C to +125° C for ceramic package; V_{DD} range of 4.5 V to 5.5 V, C_L = 15 pF

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
OUTPUT					
Transmitter Coder					
CTX to HDB3 OUT:					
Data Propagation Delay Time *	t_{DD}	—	—	90	ns
Handling Delay Time	t_{HD}	—	4	—	clock period
HDB3 OUT Output Pulse Width *					
(Clock duty cycle = 50%)					
f_{CL} = 2.048 MHz	t_w	238	—	260	ns
f_{CL} = 8.448 MHz	t_w	53	—	65	
Receiver Decoder					
CRX to NRZ OUT:					
Data Propagation Delay Times §	t_{DD}	—	—	90	ns
Handling Delay Time #	t_{HD}	—	4	—	clock period
HDB3 IN to CKR					
HDB3 Propagation Delay Time §					
LTE = 0	$t_{IN\ CKR}$	—	—	65	ns
LTE = 1		—	—	30	

§ See Fig. 5 * See Fig. 4 § See Fig. 2 # See Fig. 3

TRANSCODER OPERATION

Transmitter Coder (See Fig. 2)

The HDB3/AMI transmitter coder operates on 4-bit serial strings of NRZ binary data and a synchronous transmitter clock (CTX). NRZ binary data is serially clocked into the transmitter on the negative transition of the (CTX) clock. HDB3/AMI coding is performed on the 4-bit string, and HDB3/AMI binary output data is clocked out to the (+HDB3 OUT, -HDB3 OUT) outputs on the positive transition of the transmitter clock (CTX) 4 clock pulses after the data appeared at the (NRZ-IN) input.

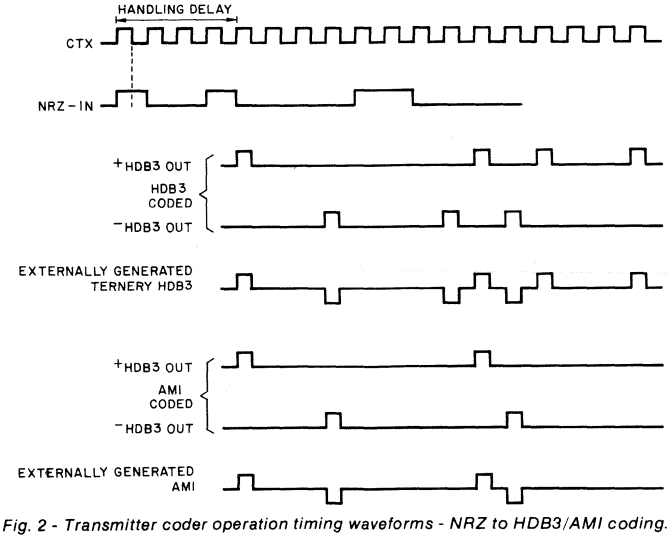


Fig. 2 - Transmitter coder operation timing waveforms - NRZ to HDB3/AMI coding.

CD22103A

Receiver Decoder (See Fig. 3)

The HDB3/AMI receiver decoder operates on 4-bit serial strings of binary coded HDB3/AMI signals, and a synchronous receiver clock (CRX), HDB3/AMI binary data is serially clocked into the receiver on the positive transition of the (CRX) clock. HDB3/AMI decoding is performed on the 4-bit string, and NRZ binary output data is clocked out to the (NRZ-OUT) output on the positive transition of the receiver clock (CRX) 4 clock pulses after the data appeared at the (+ HDB3 IN, -HDB3 IN) inputs.

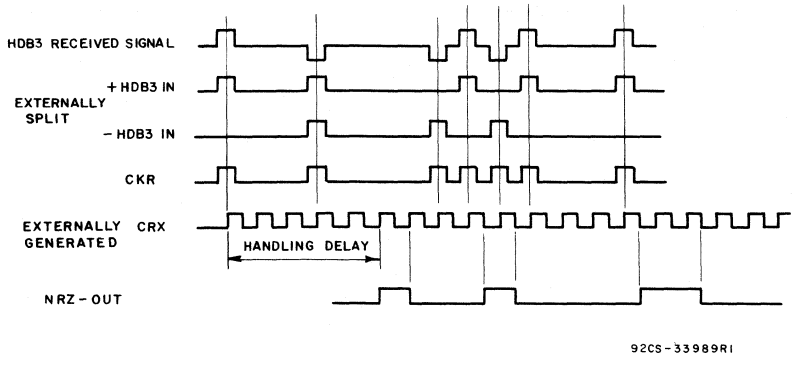


Fig. 3 - Receiver decoder operation timing waveforms - HDB3 to NRZ decoding.

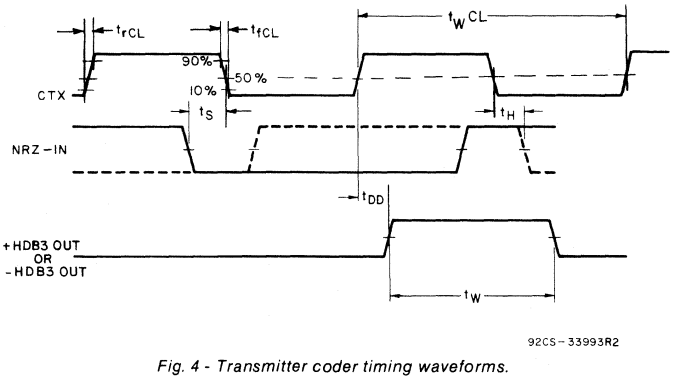


Fig. 4 - Transmitter coder timing waveforms.

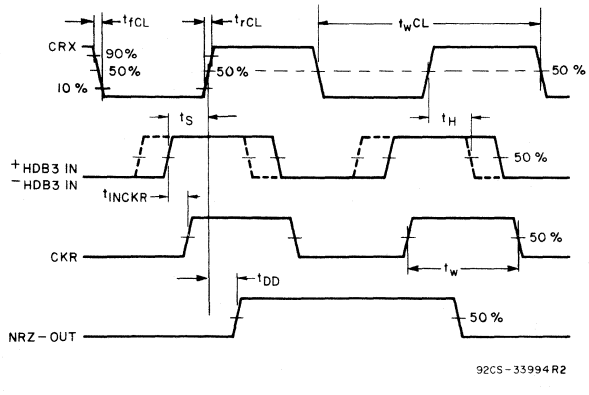


Fig. 5 - Input requirements and output characteristics.

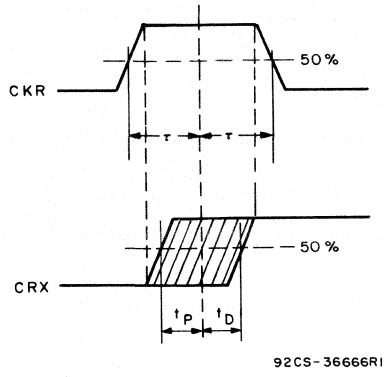


Fig. 6 - CRX reconstruction requirements.

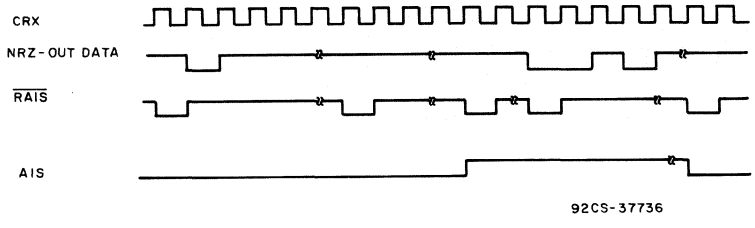


Fig. 7 - Receiver alarm-inhibit-signals timing waveforms.

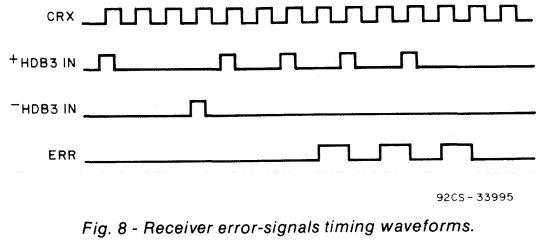


Fig. 8 - Receiver error-signals timing waveforms.

Definition of HDB3 Code Used In CD22103A HDB3 Transcoder (As Per CCITT G703 Annex Recommendations) and Error Detection

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. HDB3 signal is pseudoternary; the three states are denoted B+, B−, and 0.
2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (See Item 4 below).
3. Marks in the binary signal are coded alternately as B+ and B− in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (See Item 4 below).
4. Strings of four spaces in the binary signal are coded according to the following rules:

A) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself; it is coded as a mark, i.e., not a violation (i.e., B+ or B−), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternate polarity so that no dc component is introduced.

B) The second and third spaces of a string are always coded as spaces.

C) The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V− according to their polarity.

CD22103A

The CD22103A is designed to code and decode HDB3 signals which are coded as binary digital signals (NRZ-IN) and (+ HDB3 IN, -HDB3 IN), accompanied by sampling clocks (CTX) and (CRX). The two binary coded HDB3 outputs, (+ HDB3 OUT, -HDB3 OUT) may be externally mixed to create the ternary HDB3 signals (See Fig. 2).

The two binary HDB3 input signals have been split from the input ternary HDB3 in an external line receiver.

Error Detection

Received HDB3/AMI binary input signals are checked for coding violations, and an error signal (ERR) is generated as described below.

HDB3 Signals HDB3/AMI = High

The error signal (ERR) is flagged high for one CTX period if a violation pulse (±V) is received of the same polarity as the last received violation pulse.

A violation pulse (±V) is considered a reception error and does not cause replacement of the last string of 4 bits to zeros, if:

The received 4 data bits previous to reception of the violation pulse have not been the sequence BX00 (where X = don't care). The error signal (ERR) remains low.

NOTES:

The data sequences B000V and BB00V are valid HDB3 codings of the NRZ binary sequence 10000.

The error signal (ERR) count, is the accurate number of all single bit errors.

AMI Signals HDB3/AMI = Low

A coding error (ERR) is signaled when a violation pulse (+V) is received.

In either the HDB3 or AMI mode:

When high levels appear simultaneously on both HDB3 inputs (+ HDB3 IN, -HDB3 IN) a logical one is assumed in the HDB3/AMI input stream and the error signal (ERR) goes high for the duration of the violation.

Alarm Inhibit Signal

The alarm output (AIS) is set high if in two successive periods of the external Reset Alarm Signal, ($\overline{RAIS}$), less than three zeros are received.

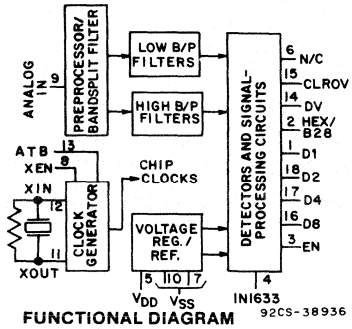
The alarm output (AIS) is reset low when three or more zeros are received during two reset alarm signal periods.

CD22202

Product Preview

5-V Low-Power DTMF Receiver

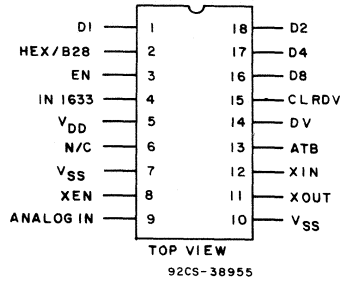
Features:
- *Central-office quality*
- *No front-end band splitting filters required*
- *Single, low-tolerance, 5-V supply*
- *Detects either 12 or 16 standard DTMF digits*
- *Uses inexpensive 3.579545-MHz crystal for reference*
- *Excellent speech immunity*
- *Output in either 4-bit hexadecimal code or binary coded 2-of-8*
- *Synchronous or handshake interface*
- *Three-state outputs*



FUNCTIONAL DIAGRAM

The CD22202E complete dual-tone-multiple-frequency (DTMF) receiver detects a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally-required components are an inexpensive 3.58-MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal-connected CD22202E receiver to drive the time bases of additional receivers. This is a monolithic integrated circuit fabricated with low power, complementary-symmetry CMOS processing. It requires only a single low-tolerance voltage supply and is packaged in a standard 18-pin dual-in-line plastic package (Suffix E).

The CD22202E employs state-of-the-art circuit technology to combine the digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60-Hz reject and band-splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry and are three-state-enabled to facilitate bus-oriented architectures.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{DD}) (Referenced to V_{SS} terminal) ..... 7 V
OPERATING-TEMPERATURE RANGE (T_A) ..... 0° C to 70° C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
POWER DISSIPATION (P_D) @ T_A = 25° C (derate above T_A=25° C @ 6.25 mW/° C) ..... 65 mW
INPUT VOLTAGE RANGE, ALL INPUTS EXCEPT ANALOG IN ..... (V_{DD}+0.5 V) to -0.5 V
ANALOG IN VOLTAGE RANGE ..... (V_{DD}+0.5 V) to (V_{DD}-10 V)
DC CURRENT INTO ANY INPUT ..... ±1 mA
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

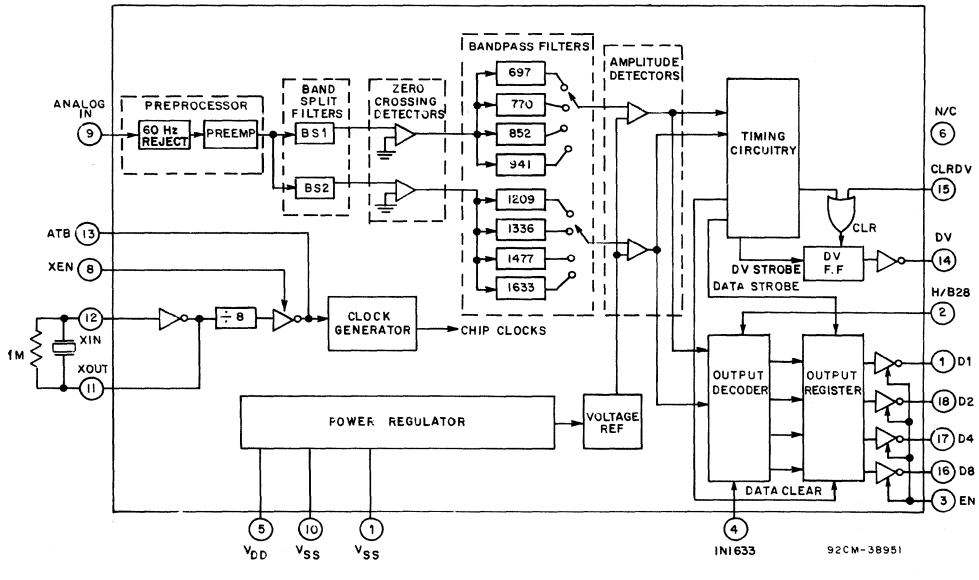
Note: Unused inputs must be connected to V_{DD} or V_{SS} as appropriate.

File Number **1695**

CD22202

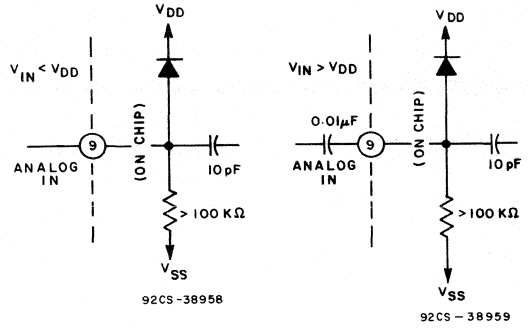
ELECTRICAL CHARACTERISTICS (0° C ≤ T_A ≤ 70° C, V_{DD} = 5 V ± 10%)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of f_t
Amplitude for Detection	each tone	-32		-2	dBm referenced to 600 Ω
Minimum Acceptable Twist	twist= high tone / low tone	-10		+10	dB
60-Hz Tolerance				0.8	V rms
Dial Tone Tolerance	"precise" dial tone			0 dB	dB referenced to lower amplitude tone
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level, 400 μA load "1" level, 200 μA load	0 V_{DD} - 0.5		0.5 V_{DD}	V
Digital Inputs	"0" level "1" level	0 0.7 V_{DD}		0.3 V_{DD} V_{DD}	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25° C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB referenced to lowest amplitude tone
Input Impedance	$V_{DD} \geq V_{IN} \geq V_{DD}$ - 10	100 KΩ// 15pF			



ANALOG IN

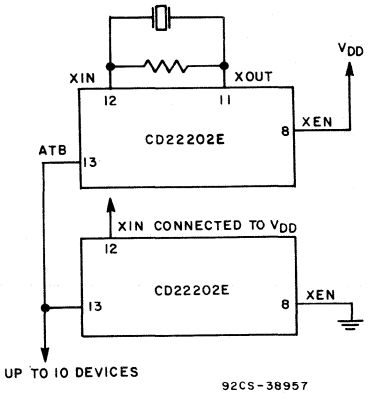
This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



The CD22202E is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

CRYSTAL OSCILLATOR

The CD22202E contains an on-board inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1-MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other CD22202Es may use the same frequency reference by tying their ATB pins to the ATB of a crystal-connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected CD22202E as shown below.



HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The following table describes the two output codes.

Table I - Output Codes

Digit	Hexadecimal				Binary Coded 2-of-8			
	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DTMF DIALING MATRIX

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Note:
Column 3 is for special applications and is not normally used in telephone dialing.

IN1633

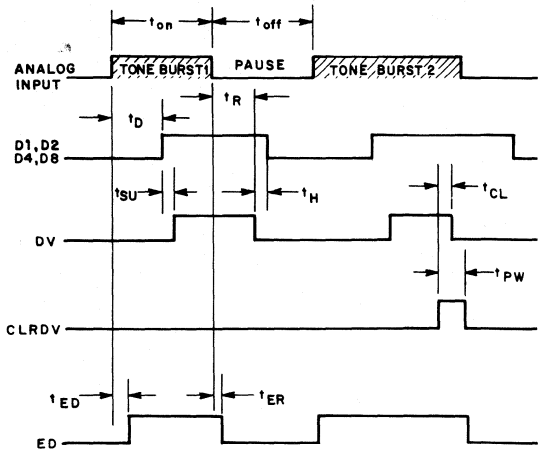
When tied high, this pin inhibits detection of tone pairs containing the 1633-Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

N/C PINS

These pins have no internal connection and may be left floating.

CD22202

TIMING WAVEFORMS



92CS-38956

DETECTION FREQUENCY

Low Group f_O	High Group f_O
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
TONE TIME:					
for detection	t_{ON}	40	—	—	ms
for rejection	t_{ON}	—	—	20	ms
PAUSE TIME:					
for detection	t_{OFF}	40	—	—	ms
for rejection	t_{OFF}	—	—	20	ms
DETECT TIME	t_D	25	—	46	ms
RELEASE TIME	t_R	35	—	50	ms
DATA SETUP TIME	t_{SU}	7	—	—	μs
DATA HOLD TIME	t_H	4.2	—	5	ms
DV CLEAR TIME	t_{CL}	—	160	250	ns
CLRDV pulse width	t_{PW}	200	—	—	ns
ED Detect Time	t_{ED}	7	—	22	ms
ED Release Time	t_{ER}	2	—	18	ms
OUTPUT ENABLE TIME C_L=50 pF, R_L=1 KΩ	—	—	200	300	ns
OUTPUT DISABLE TIME C_L=35 pF, R_L=500 Ω	—	—	150	200	ns
OUTPUT RISE TIME C_L=50 pF	—	—	200	300	ns
OUTPUT FALL TIME C_L=50 pF	—	—	160	250	ns

Product Preview

CD22203

5-V Low-Power DTMF Receiver

For Telecommunications and
Data Transmission Applications

Features:

- *Central-office quality*
- *No front-end band splitting filters required*
- *Single, low-tolerance, 5-V supply*
- *Uses inexpensive 3.579545-MHz crystal for reference*
- *Excellent speech immunity*
- *Output in either 4-bit hexadecimal code or binary coded 2-of-8*
- *Sychronous or handshake interface*
- *Three-state outputs*
- *Additional early detect output available on pin 6.*

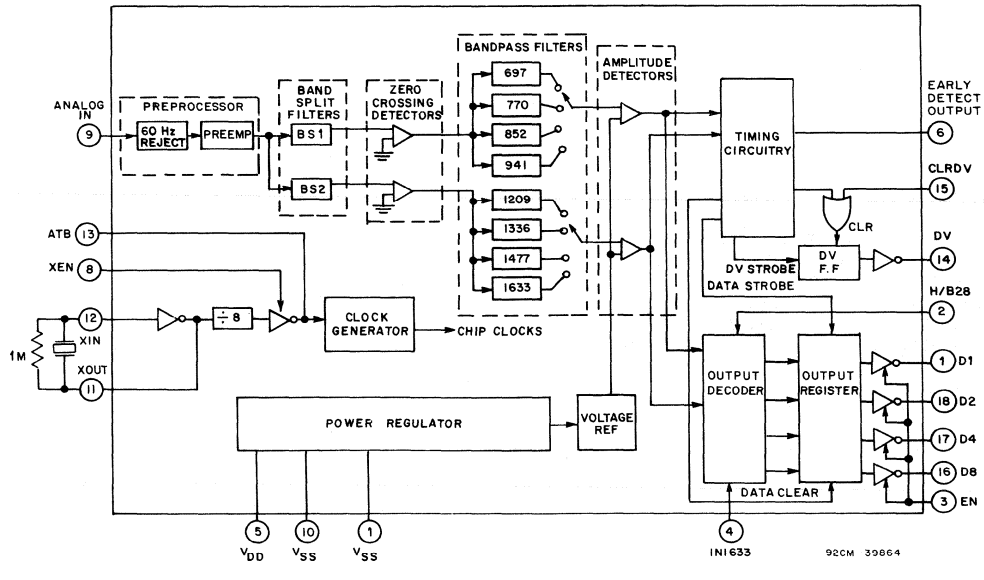
The CD22203 is a complete dual-tone-multiple-frequency (DTMF) receiver that detects a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally-required components are an inexpensive 3.58-MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. The internal clock input can be used to drive additional receivers. The CD22203 has an additional early detect output available on pin 6.

The CD22203 employs state-of-the-art circuit technology to combine the digital and analog functions on the same CMOS chip using a standard digital semiconductor process.

The analog input is preprocessed by 60-Hz reject and band-splitting filters and provides AGC.

Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry and are three-state-enabled to facilitate bus-oriented architectures.

The CD22203 device is available in a 16-lead dual-in-line plastic package (E suffix).



Block digaram for the CD22203.

Preview Data only

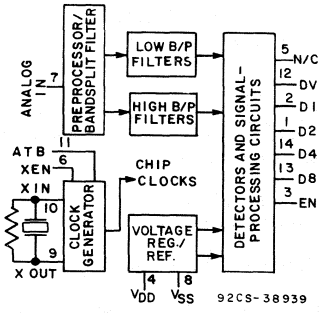
CD22204

Product Preview

5-V Low-Power Subscriber DTMF Receiver

Features:

- *No front-end band-splitting filters required*
- *Single low-tolerance 5-volt supply*
- *Three-state outputs for microprocessor-based systems*
- *Detects all 16 standard DTMF digits*
- *Uses inexpensive 3.579545-MHz crystal*
- *Excellent speech immunity*
- *Output in 4-bit hexadecimal code*



FUNCTIONAL DIAGRAM

The RCA-CD22204E is a complete Dual-Tone Multiple-Frequency (DTMF) receiver that detects all 16 standard digits. No front-end prefiltering is needed. The only externally required components are an inexpensive 3.58-MHz television "color-burst" crystal for frequency reference and a bias resistor. An Alternate Time Base (ATB) is provided to permit operation of up to ten CD22204Es from a single crystal.

The CD22204E employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering, and digital circuitry on the same CMOS chip. The analog input signal is pre-processed by 60-Hz reject and band-split filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to measure the tone and pause durations and to provide output timing and decoding. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus-oriented architectures.

The CD22204E is supplied in 14 lead dual-in-line plastic packages (E Suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{DD}) (Referenced to V_{SS} Terminal) ..... +7 V
OPERATING-TEMPERATURE RANGE (T_A) ..... 0°C to 70°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
POWER DISSIPATION (P_D) @ T_A = 25°C ..... 65 mW
(DERATE ABOVE T_A = 25°C @ 6.25 mW/°C)
INPUT VOLTAGE RANGE, ALL INPUTS EXCEPT ANALOG IN ..... (V_{DD} + 0.5 V) to -0.5 V
ANALOG IN VOLTAGE RANGE ..... (V_{DD} + 0.5 V) to V_{DD} -10 V
DC CURRENT INTO ANY INPUT ..... ± 1 mA
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Note: Unused inputs must be connected to V_{DD} or V_{SS} as appropriate

File Number **1696**

ELECTRICAL CHARACTERISTICS ($0° C \leq T_A \leq 70° C$, $V_{DD} = 5 V \pm 10\%$)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Frequency Detect Bandwidth		±(1.5 ÷ 2 Hz)	±2.3	±3.5	% of f_o
Amplitude for Detection	each tone	-18		-2	dBm referenced to 600 Ω
Minimum Acceptable Twist	twist = high tone / low tone	-8		+4	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB referenced to lower amplitude tone
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs (except XOUT)	"0" level 400 μA load "1" level, 200 μA load	0 V_{DD} -0.5		0.5 V_{DD}	Volts Volts
Digital Inputs	"0" level "1" level	0 0.7 V_{DD}		0.3 V_{DD} V_{DD}	Volts Volts
Power Supply Noise	wide band			10	mV p-p
Supply Current	$T_A = 25° C$		10	20	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB referenced to lowest amplitude tone
Input Impedance	$V_{DD} \geq V_{IN} \geq V_{DD}$ -10	100KΩ//15pF			

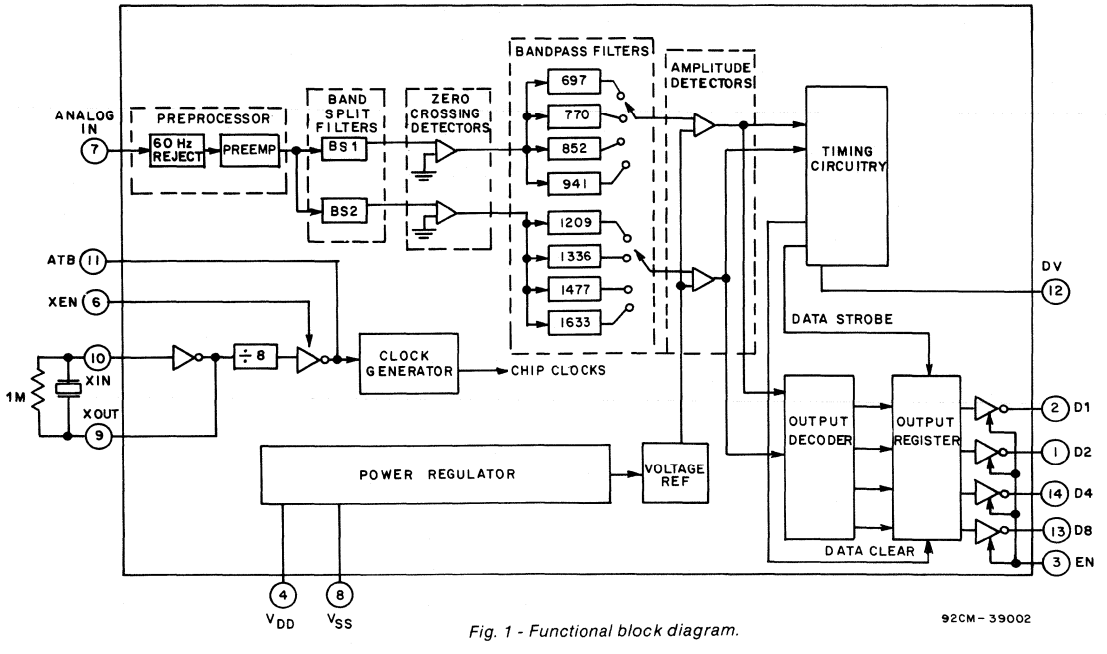
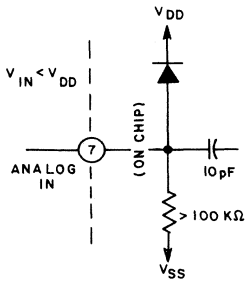


Fig. 1 - Functional block diagram.

CD22204

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated below.



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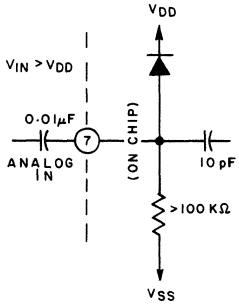
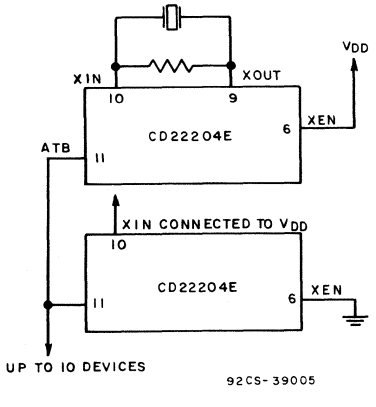


92CS-39007

The CD22204E is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than 20 dB below the fundamental.

CRYSTAL OSCILLATOR

The CD22204E contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other CD22204Es may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected CD22204E as shown below.



92CS-39005

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The table below describes the hexadecimal codes.

	OUTPUT CODE			
Digit	**D8**	**D4**	**D2**	**D1**
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs.

N/C PIN

This pin has no internal connection and may be left floating.

DTMF DIALING MATRIX

	COL 0	COL 1	COL 2	COL 3
ROW 0	1	2	3	A
ROW 1	4	5	6	B
ROW 2	7	8	9	C
ROW 3	*	0	#	D

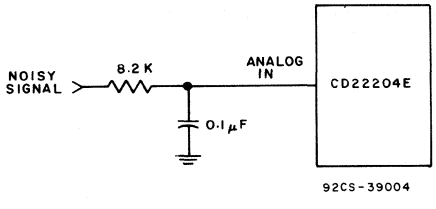
Note: Column 3 is for special applications and is not normally used in telephone dialing.

DETECTION FREQUENCY

Low Group f_o	High Group f_o
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

INPUT FILTER

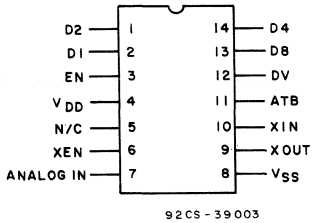
The CD22204E will tolerate total input rms noise up to 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the CD22204E unnecssary. However, noise near the 56 kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28 kHz, the simple RC filter as shown below may be employed to band limit the incoming signal.



Filter for use in extreme high frequency input noise environment.

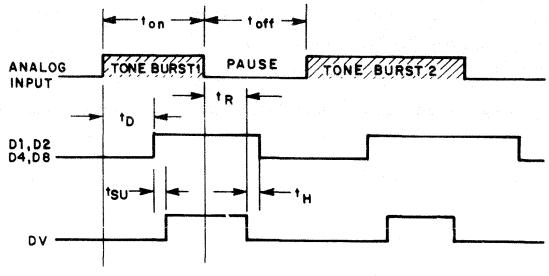
Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case leave XOUT floating.

Top View



TERMINAL ASSIGNMENT

TIMING WAVEFORMS



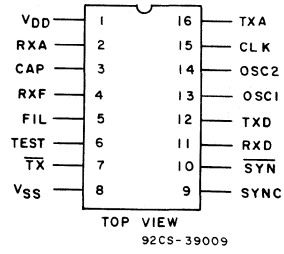
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Tone Time:					
for detection	t_{ON}	40	—	—	ms
for rejection	t_{ON}	—	—	20	ms
Pause Time:					
for detection	t_{OFF}	40	—	—	ms
for rejection	t_{OFF}	—	—	20	ms
Detect Time	t_D	25	—	46	ms
Release Time	t_R	35	—	50	ms
Data Setup Time	t_{SU}	7	—	—	μs
Data Hold Time	t_H	4.2	—	5.0	ms
DV Clear Time	t_{CL}	—	160	250	ns
CLRDV pulse width	t_{PW}	200	—	—	ns
ED Detect Time	t_{ED}	7	—	22	ms
ED Release Time	t_{ER}	2	—	18	ms
Output Enable Time C_L=50pF R_L=1KΩ	—	—	200	300	ns
Output Disable Time C_L=35pF R_L=500Ω	—	—	150	200	ns
Output Rise Time C_L=50pF	—	—	200	300	ns
Output Fall Time C_L=50pF	—	—	160	250	ns

CD22223

1200-Baud FSK Modem

Product Preview

Features:
- *Data rate 1200 baud*
- *CCITT V 0.23 compatible*
- *Built-in loop-back test*
- *Switched capacitor receive filter*
- *Low power CMOS (2 mA @ 5-V typ.)*
- *Single-supply operation*
- *Low error rate (5×10^{-3} @ 8-dB SNR)*



TERMINAL ASSIGNMENT

The RCA-CD22223 1200-baud modem is intended for half-duplex operation over a single-line system or full-duplex operation over a two-line system.

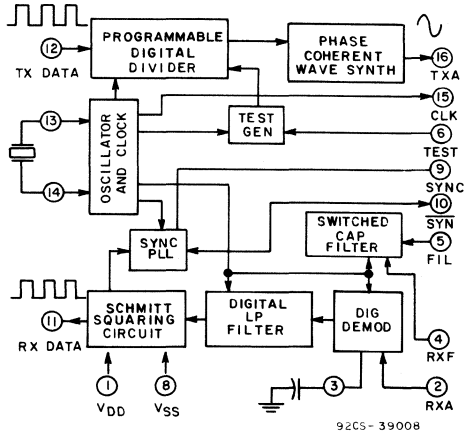
The transmitted data is an analog continuous-phase FSK modulated signal at 1302 Hz and 2097 Hz for Data 1 and 0, respectively. The transmitted signal may be inhibited using the $\overline{TX}$ control line.

The received signal is bandpass filtered to reduce background noise and then sliced using an auto zeroed, offset corrected, zero-crossing detector. This signal is then digitally demodulated and filtered. The output of the receiver is a digital eye pattern. A digital phase-lock loop is synchronized to the received signal and may be used to sample the received eye signal. During high noise periods, the synchronization circuit may be locked using the $\overline{SYN}$ control. A 1200-Hz signal (CLK) is also available for system timing purposes.

The modem features an autotest mode which can facilitate field testing of nearly all of the on-chip functions. When the modem is placed in the autotest mode, Test=Logic 1, the digital data input to the chip is switched to a pseudo-random number generator on chip and the analog transmit output is connected to the receiver input. The digital output of the receiver is compared to the digital input. The modem is determined to be operational if the received data agrees with the transmitted data as indicated by a pass/fail digital output. (RXD, pass=Logic 0, fail=Logic 1).

The CD22223 is supplied in a 16-lead dual-in-line plastic package (E suffix).

Applications:
- *Built-in low-speed modems*
- *Remote data collection*
- *Radio telemetry*
- *Credit verification*
- *Stand-alone modems*
- *Point-of-sale terminals*
- *Tone signaling systems*
- *Remote process control*



FUNCTIONAL DIAGRAM

ABSOLUTE MAXIMUM RATINGS

POWER SUPPLY VOLTAGE (V_{DD}-V_{SS}) ..... 14 V
ANALOG INPUT VOLTAGE AT RXA ..... -0.3 TO V_{DD} V
ANALOG INPUT VOLTAGE AT RXF ..... -3 TO V_{DD} V
DIGITAL INPUT VOLTAGE ..... V_{SS} -0.3 TO V_{DD} +0.3 V
STORAGE TEMPERATURE RANGE ..... -65 TO +150°C
OPERATING TEMPERATURE RANGE ..... -25 TO +70°C
LEAD TEMPERATURE 10 s SOLDERING ..... 260°C

File Number **1702**

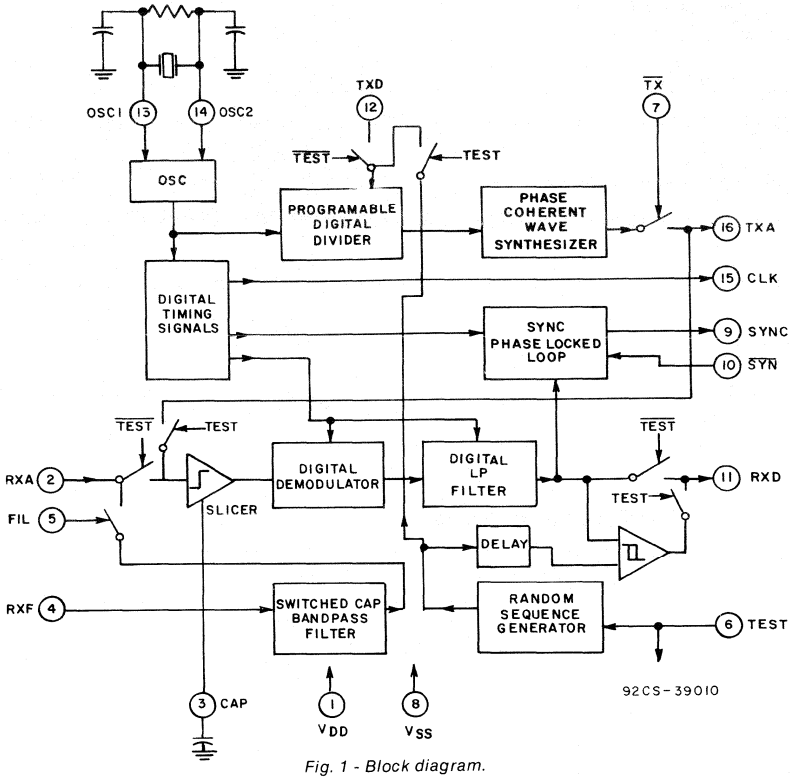


Fig. 1 - Block diagram.

Circuit Operation

The CD22223E has four main functional sections: timing, transmit, receive, and test. Each section of the chip will be individually described below.

Timing

The timing section contains the oscillator (OSC) and random logic which generates digital timing signals used throughout the chip. The time base can be derived from 3.18-MHz crystal or an external digital input. The modem will operate with clock inputs from 330 kHz to 3.3 MHz. Back channel is supplied by selecting the lower frequency clock rate. The digital timing logic divides the oscillator frequency to give a 1200-Hz output that can be used for system timing.

Transmitter

The CD22223E transmitter consists of a programmable divider that drives a programmable coherent-phase frequency synthesizer. The programmable divider is digitally controlled via the Data Input pin (TXD). The output of the divider clocks a 16-segment phase-coherent frequency synthesizer. A sine wave is constructed by eight weighted capacitors which are the inputs to a high pass filter. Proper matching of the capacitors is important in order to suppress the second through fourteenth harmonics. The synthesized signal is outputted directly to the transmit pin TXA. The transmit signal can be disabled by using the digital control pin TX.

Receiver

The CD22223E receiver is comprised of three sections: the input bandpass filter, the synchronization loop, and the demodulator.

The input bandpass filter is a four-pole Butterworth filter, implemented using switched capacitor technology. This filter reduces wideband noise which significantly improves data error rates. The SSI 223 can be configured with the bandpass filter in series with the receiver by setting FIL=1 and inserting the received signal at RXF, or the bandpass filter can be deleted from the system by setting FIL=0 and inputting the received signal through RXA.

The demodulator is used to detect a received mark or space.

The synchronization for sampling the digital output at RXD is derived from a digital phase-locked loop. The phase-locked loop is clocked at 16 times the bit rate with a maximum lock period of 8 clocks and locks on the data output signal.

Self-Test Mode

The CD22223E features an autotest mode which provides easy field test capability of the chip's functionality. The modem is placed in the test mode by taking the test pin high. In the test mode the Data Input pin is disconnected and the programmable divider is driven by a pseudo-random PN sequence generator and the transmitter's output is connected to the receiver's input. The input data to the programmable divider is delayed by the system delay time and compared to the digital output on sync transitions. If the detected data matches the delayed input data from the PN sequence counter, the CD22223E is properly functioning as indicated by RXD low. A high on the RXD pin indicates a functional problem on the CD22223E.

CD22223

PERFORMANCE SPECIFICATIONS

1200-Baud Modem

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Range V_{DD}		4.5	—	13	V
Supply Current	V_{DD} = 5 V @ 25° C 12 V @ 25° C	— —	2 5	— —	mA
Temperature Range		-25	—	70	°C
Modem Frequencies	Crystal = 3.1872 MHz Data = 1 Data = 0	 — —	 1302 2097	 — —	Hz
Input Level at RXA		35	—	—	mV (rms)
Error Rate	S/N = 8 dB	—	—	$5x10^{-3}$	
Output Level at TXA	R_{Load} = 10 KΩ	-	0.25 V_{DD}	—	V
Output Harmonic Suppression	2nd to 14th Harmonic 15th Harmonic	— —	-60 —	-50 -20	dB

PIN DESIGNATIONS

Pin No.	Symbol	Description
1	V_{DD}	+ Supply
2	RXA	Analog Input from Telephone Network
3	CAP	0.1 μF CAP to V_{SS}
4	RXF	Filter Input
5	FIL	Input Control 1 = Filter Input 0 = RXA Input
6	TEST	Test Mode Control 0 = Normal Operation 1 = Test Mode
7	$\overline{TX}$	Transmitter Control 0 = Normal Operation 1 = Block Transmitter
8	V_{SS}	Ground
9	SYNC	Sync Output
10	$\overline{SYN}$	Hold SYNC Control
11	RXD	Digital Output
12	TXD	Digital Input
13	OSC1	Crystal Input (3.1872 MHz)
14	OSC2	Crystal Return
15	CLK	1200-Hz Output
16	TXA	FSK Output

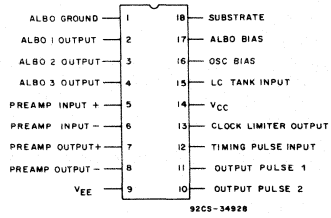
Advance Information/
Preliminary Data

CD22301

PCM Line Repeater

Features:

- *Automatic line buildout*
- *5.1 V supply voltage*
- *Buffered output*



CD22301
TERMINAL ASSIGNMENT

The RCA-CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544 Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37 Mbits/s. The circuit operates from a 5.1 V ± 5 % externally regulated supply.

The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing, and buffered output formation.

The CD22301 is supplied in an 18-lead dual-in-line plastic package (E suffix).

Applications:

- *T1 1.544 Mbits/s bipolar carrier system*
- *T148 2.37 Mbits/s ternary carrier system*

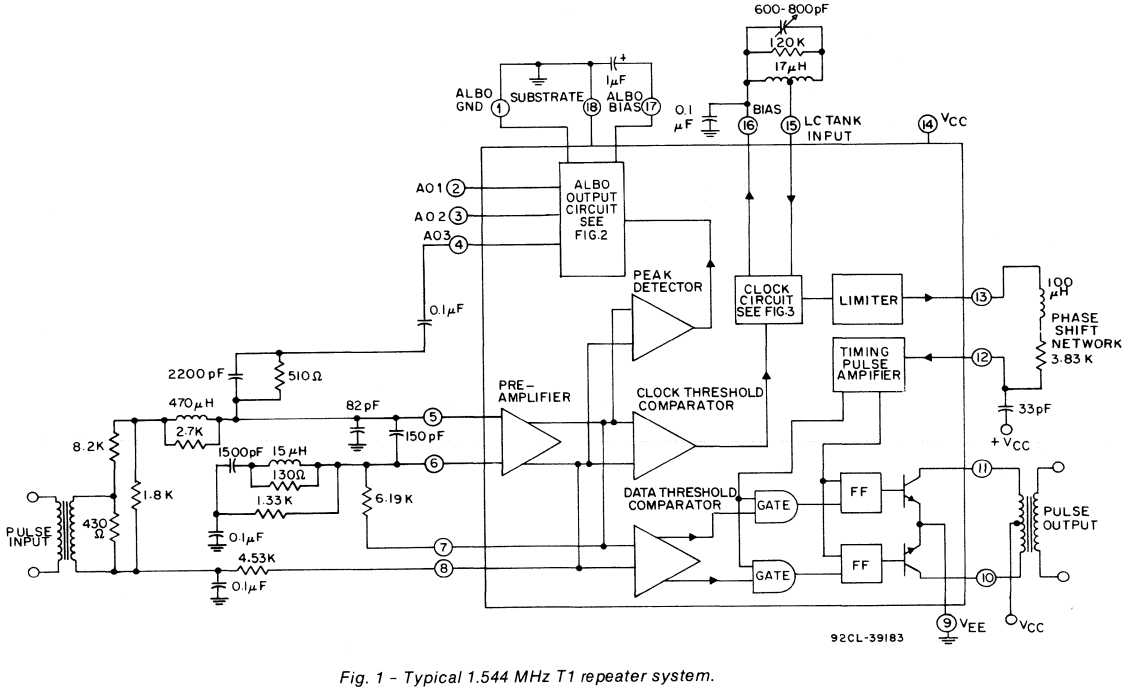


Fig. 1 - Typical 1.544 MHz T1 repeater system.

File Number **1368**

CD22301

MAXIMUM RATINGS, *Absolute Maximum Values:*
At ambient temperature (T_A) = 25° C

DC SUPPLY ..... 10 V
DC CURRENT (Into Pin 9 or 10) ..... 25 mA
PEAK CURRENT (Into Pin 9 or 10) ..... 100 mA
INPUT SURGE VOLTAGE (Between Pins 5 and 6, t = 10 ms) ..... 50 V
OUTPUT SURGE VOLTAGE (Between Pins 10 and 11, t = 1 ms) ..... 50 V
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60° C ..... 500 mW
For T_A = +60° C to +85° C ..... Derate linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING TEMPERATURE RANGE (T_A) ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. ..... +265° C

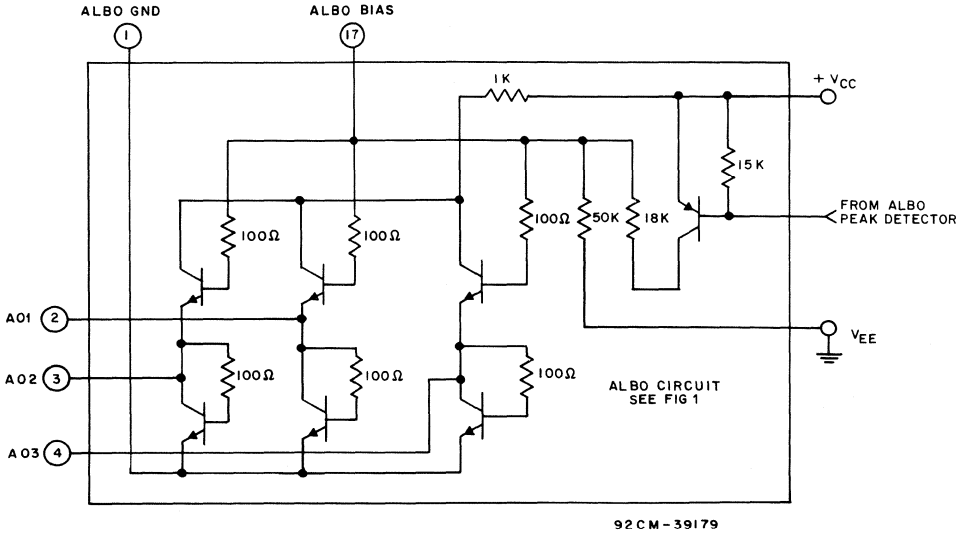


Fig. 2 - ALBO output circuit.

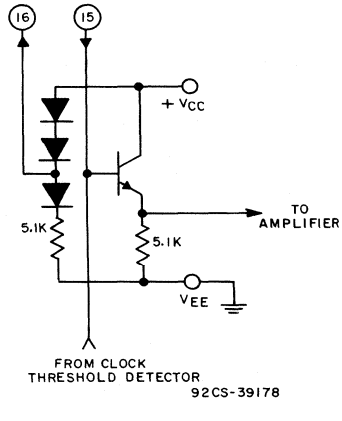


Fig. 3 - Clock interface circuit.

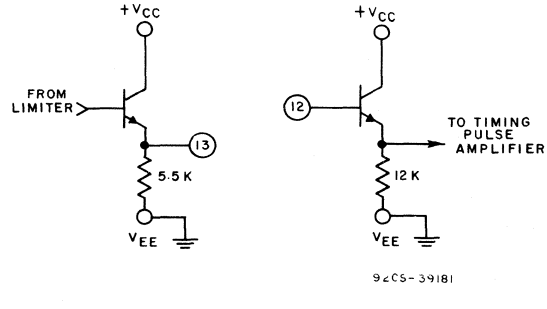


Fig. 4 - Phase-shift interface circuits.

STATIC ELECTRICAL CHARACTERISTICS
T_A = 25° C, V_{CC} = 5.1 V ± 5% (See Fig. 5)

CHARACTERISTIC	LIMITS			UNITS
	Min.	Typ.	Max.	
DC VOLTAGES				
Pins 2, 3, 4 and 17	—	0	0.1	V
Pins 5, 6, 7 and 8	2.4	2.9	3.4	V
Pins 10 and 11	—	5.1	—	V
Pins 12, 13, 15 and 16	3.1	3.6	4.1	V
DC CURRENTS				
Pin 14	—	22	30	mA
Pins 10 and 11	—	0	100	μA

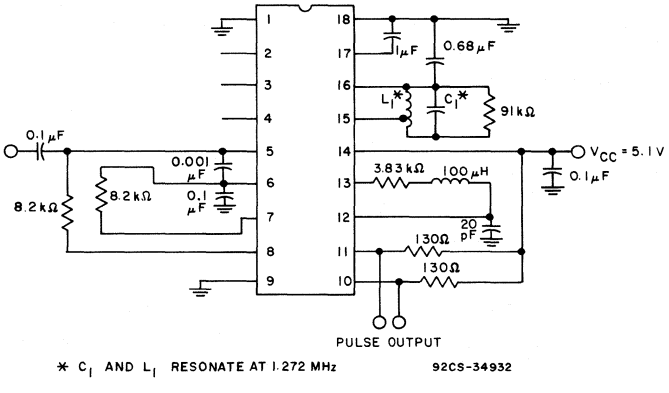


Fig. 5 - DC and output pulse test circuit.

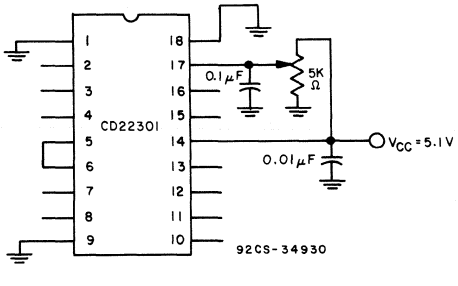


Fig. 6 - Test circuit for impedance measurement.

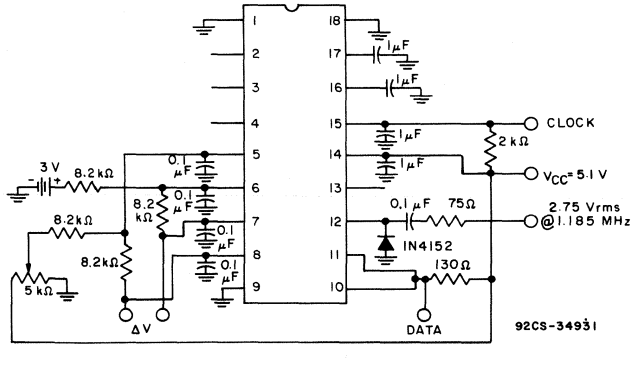


Fig. 7 - Test circuit for threshold voltage measurement.

CD22301

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A = 25° C, V_{CC} = 5.1 V ± 5%

CHARACTERISTIC	SYMBOL	FIG.	NOTE	LIMITS			UNITS
				MIN.	TYP.	MAX.	
Preamplifier Input Imedance	Z_{in}	8		20	—	—	kΩ
Preamplifier Output Impedance	Z_{out}	8		—	—	2	kΩ
Preamplifier Gain @ 2.37 MHz	A_o	8		47	50	—	dB
Preamplifier Output Offset Voltage	ΔV_{out}	8	1	-50	0	50	mW
Clock Limiter Input Impedance	$Z_{in}(CL)$	6	2	10	—	—	kΩ
ALBO Off Impedance	$Z_{ALBO}(off)$	6	3	20	—	—	kΩ
ALBO On Impedance	$Z_{ALBO}(on)$	6	4	—	—	10	Ω
DATA Threshold Voltage	$V_{TH}(D)$	7	5, 8	0.75	0.8	0.85	V
CLOCK Threshold Voltage	$V_{TH}(CL)$	7	6, 8	—	1.12	—	V
ALBO Threshold	$V_{TH}(AL)$	7	7, 8	1.5	1.6	1.7	V
$V_{TH}(D)$ as % of $V_{TH}(AL)$				42	45	49	%
$V_{TH}(CL)$ as % of $V_{TH}(AL)$				65	70	75	%
Buffer Gate Voltage (low)	V_{OL}	5	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	ΔV_{OL}	5	9	-0.15	0	0.15	V
Output Pulse Rise Time	t_r	5, 9	9, 10	—	—	40	ns
Output Pulse Fall Time	t_f	5, 9	9, 10	—	—	40	ns
Output Pulse Width	t_w	5, 9	9, 10	290	324	340	ns
Pulse Width Differential	Δt_W	5, 9	9, 10	-10	0	10	ns
Clock Drive Current	I_{CL}			—	2	—	mA

Notes:

1. No signal input. Measure voltage between pins 7 and 8.
2. Measure clock limiter input impedance at pin 15.
3. Adjust potentiometer for 0 volts. Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
4. Increase potentiometer until voltage at pin 17 = 2 Vdc. Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
5. Adjust potentiometer for ΔV = 0 volts. Then slowly increase ΔV in the positive direction until pulses are observed at the DATA terminal.
6. Continue increasing ΔV until the DC level at the clock terminal drops to 4 volts.
7. Continue increasing ΔV until the ALBO terminal rises to 1 volt.
8. Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
9. Set e_{in} = 2.75 mV(rms) at f ≈ 1.185 MHz. Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
10. Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by three dB.

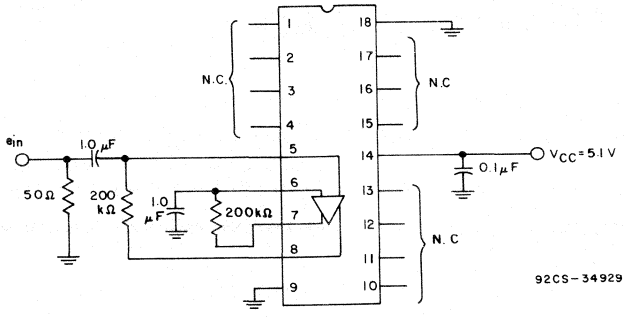


Fig. 8 - Preamplifier gain and impedance measurement circuit.

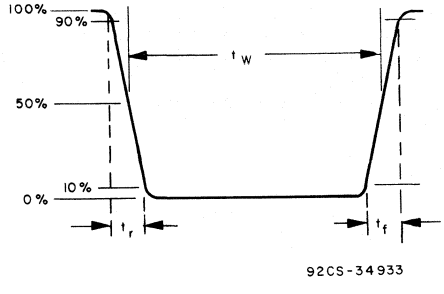


Fig. 9 - Output pulse waveform.

CD22302, CD22303

CMOS Single Chip PCM CODEC with Filters

Features:

- *Low power dissipation:*
  - *50 mW typical operating*
  - *5 mW typical standby*
- *Meets or exceeds all AT&T D3/D4 specifications and CCITT recommendations*
- *Complete CODEC and filtering systems:*
  - *No external components for sample and hold and Auto-Zero functions*
  - *Transmit Input section includes Anti-Aliasing Prefilter*
  - *Receive output filter with SIN X/X correction*
- *Variable Data Clocks-from 64 KHz to 4.1 MHz*
- *Programmable gain for transmit input*
- *CD22302-16-pin μ-law CODEC*
- *CD22303-16-pin A-law CODEC*
- *Synchronous and Asynchronous operation*
- *TTL or CMOS compatible logic*
- *Flexible external reference voltage from −2.5 V to −3.16 V*
- *± 5 V operation*
- *Fast acquisition on power-up*
- *ESD protection on all inputs and outputs*

The RCA CD22302 and CD22303 are monolithic silicon gate double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22302 provides the AT&T μ-law and the CD22303 provides the CCITT A-law companding characteristic.

The primary applications for the CD22302 and CD22303 are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown in Fig. 1.

With the flexible features, including synchronous and asynchronous operations, variable rates and a variable reference voltage, the CD22302 and CD22303 are ideally suited for PABX, Central Office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

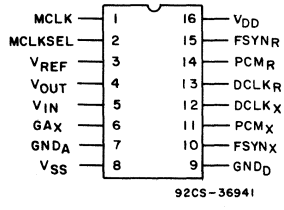
Applications:

- *PABX*
- *Cellular and Mobile Telephones*
- *Central Office Switching Systems*
- *Accurate A/D and D/A conversions*
- *Digital Telephones*

The CD22302 and CD22303 are supplied in 16-lead hermetic dual-in-line ceramic packages (F-suffix) and 16-lead dual-in-line plastic packages (E-suffix).

Table I

Pin Symbol	Pin Names	Pin No.
MCLK	Master Clock	1
MCLKSEL	Master Clock Select	2
V_{REF}	Reference Voltage	3
V_{OUT}	Analog Output	4
V_{IN}	Analog Input	5
GA_X	Analog Input Gain Adjust	6
GND_A	Analog Ground	7
V_{SS}	Power (-5 V)	8
GND_D	Digital Ground	9
$FSYN_X$	Transmit Frame SYNC	10
PCM_X	Transmit PCM Data Output	11
$DCLK_X$	Transmit Data Clock	12
$DCLK_R$	Receive Data Clock	13
PCM_R	Receive PCM Data Input	14
$FSYN_R$	Receive Frame SYNC	15
V_{DD}	Power (5 V)	16



TERMINAL ASSIGNMENT

File Number **1473**

CD22302, CD22303

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE V_{DD} ..... +6 V
DC SUPPLY-VOLTAGE V_{SS} ..... -6 V
OPERATING TEMPERATURE RANGE ..... -25° C to +70° C
STORAGE-TEMPERATURE RANGE ..... -65° C to +150° C
POWER DISSIPATION AT 25° C ..... 500 mW
DIGITAL INPUT ..... -0.5 to V_{DD} +0.5 V

ELECTRICAL CHARACTERISTICS at T_A = 25° C

SYMBOL	CHARACTERISTIC	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
V_{DD}	Positive Supply		4.75	5	5.25	V
V_{SS}	Negative Supply		-4.75	-5	-5.25	V
P_{OPR}	Power Dissipation (Operating)	V_{DD} = 5 V, V_{SS} = -5 V	—	50	—	mW
P_{STBY}	Power Dissipation (Standby)	V_{DD} = 5 V, V_{SS} = -5 V	—	5	—	mW

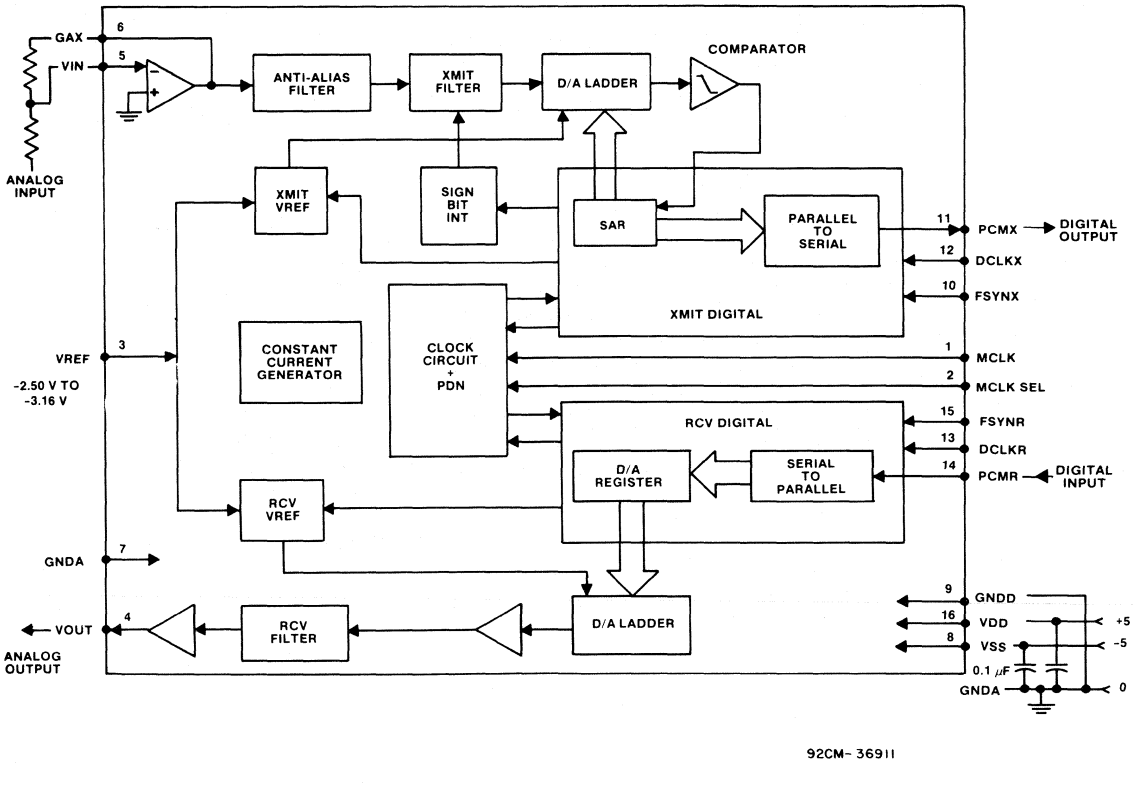


Fig. 1 - Functional block diagram.

CD22302, CD22303

Pin Function and Description

Pin No.	Name	Description
1	MCLK	Master Clock. Input of the master clock can be a 1.536 MHz, 1.544 MHz, or 2.048 MHz clock. Pinstrap the MCLKSEL pin to reflect the proper input master clock frequency. This input is TTL compatible.
2	MCLKSEL	Master clock frequency selection. Input must be pinstrapped to reflect the input master clock frequency. MCLKSEL = V_{SS} for 2.048 MHz MCLKSEL = GND_D for 1.536 MHz MCLKSEL = V_{DD} for 1.544 MHz
3	V_{REF}	External reference voltage input for the coder and decoder. It can range from -2.5 V to -3.16 V as required by different applications.
4	V_{OUT}	Analog output of the receive filter. The analog voltage on this pin is the decoded value of the PCM word received on PCM_R pin.
5	V_{IN}	Analog input to the transmit filter for encoding into PCM data. V_{IN} is the input to a high input impedance Op Amp.
6	GA_X	Gain adiust for transmit input signal. GA_X is the output voltage of the input Op Amp. GA_X and V_{IN} pins allow the user control of the input Op Amp so that it can be connected as an adjustable gain amplifier for facilitating calibration of the transmit channel.
7	GND_A	Analog ground return common to internal analog circuits.
8	V_{SS}	-5 V ± 5% - reference to GND_D.
9	GND_D	Digital ground return common to internal logic circuits.
10	$FSYN_X$	Transmit frame synchronization clock. The rising edge of this 8 KHz input signal defines the start of the transmit time slot on the transmit PCM highway. This input initiates the PCM data output from the transmit buffer. The width of this signal is not critical. Internal logic circuit generates the necessary timing for the PCM data output. The device enters the power-down state whenever $FSYN_X$ and $FSYN_R$ are held low. $FSYN_X$ can be synchronous or asynchronous with $FSYN_R$. $DCLK_X$ must be synchronous with $FSYN_X$. This input is TTL compatible.
11	PCM_X	Transmit PCM data output. The 8-bit PCM data is shifted out on this pin at the time defined by $DCLK_X$ and $FSYN_X$. It is TTL tri-state compatible.
12	$DCLK_X$	Transmit data clock. This input data clock can range from 64 KHz to 4.1 MHz. PCM data is shifted out of the transmit buffer on the rising edges of this clock after receiving a rising edge on the $FSYN_X$ input. This input is TTL compatible.
13	$DCLK_R$	Receive data clock. This input data clock can range from 64 KHz to 4.1 MHz. PCM data is shifted into the receive buffer on the falling edge of this clock after receiving a rising edge on the $FSYN_R$ input. This input is TTL compatible.
14	PCM_R	Receive PCM data input. The 8-bit PCM data is shifted in on this pin at the time defined by $DCLK_R$ and $FSYN_R$. This input is TTL compatible.
15	$FSYN_R$	Receive frame synchronization clock. The rising edge of this 8 KHz input signal defines the start of the receive time slot on the receive PCM highway. This input initiates the PCM data input into the receive buffer. The width of this signal is not critical. Internal logic circuit generates the necessary timing for the PCM data input. The device enters power-down state whenever $FSYN_R$ and $FSYN_X$ are held low. $FSYN_R$ can be synchronous or asynchronous with $FSYN_X$. $DCLK_R$ must be synchronous with $FSYN_R$. This input is TTL compatible.
16	V_{DD}	+5 V ± 5% - reference to GND_D.

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A. C. CHARACTERISTICS

Unless otherwise specified, the following conditions apply:

V_{DD} = 5 V dc ± 5%, V_{SS} = −5 V dc ± 5%, V_{REF} = −2.5 V to −3.16 V dc
GND_A = GND_D = 0 V, F_{FX} = 1020 Hz at 0 dBm0
Transmit input amplifier operating in a unity gain configuration
Temperature = 25° C
Receive output is measured single-ended. All output levels are SIN X/X corrected.

GAIN TRACKING

SYMBOL	CHARACTERISTIC	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
GTX	Transmit Gain Tracking Error	CD22302 μ-Law CD22303 A-Law				
		+3 to −40 dBm0			± 0.25	dB
		−40 to −50 dBm0			± 0.5	dB
		−50 to −55 dBm0			± 1.2	dB
GTR	Receive Gain Tracking Error	+3 to −40 dBm0			± 0.15	dB
		−40 to −50 dBm0			± 0.5	dB
		−50 to −55 dBm0			± 1.2	dB

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25° C, C_L = 50 pF

V_{DD} = 5 V ± 5%, V_{SS} = −5 V ± 5%, GND_A = GND_D = 0 V

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Transmit or Receive:					
Data Clock Pulse Width	t_w	0.120	—	15.6	μs
Set-up Time, Sync Pulse to Clock	t_s	−100	—	100	ns
Sync Pulse Width	t_w	0.120	—	125	μs
Propagation Delay, Clock to PCM Output	t_{PHL}, t_{PLH}	—	—	100	ns
Hold Time, PCM Data to Clock	t_H	100	—	—	ns
Set-up Time, PCM Data to Clock	t_s	100	—	—	ns

DEFINITION

AMPLITUDE RESPONSE
Absolute Levels Definition:
Vref = −2.5 V dc Nominal 0 dBm0 level = 4 dBm into 600 Ω
= 1.2276 V (rms)
Vref = −3.16 V dc Nominal 0 dBm0 level = 6 dBm into 600 Ω
= 1.5517 V (rms)
Maximum Overload Level:
Voltage reference (Vref) of −2.5 V = 2.5 V μ-Law
= 2.49 V A-Law
Voltage reference (Vref) of −3.16 V = 3.16 V μ-Law
= 3.15 V A-Law

CD22302, CD22303

Table II - TRANSMIT FILTER TRANSFER CHARACTERISTICS
(V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, $DCLK_X$ = MCLK = 1.544 MHz, MCLKSEL = V_{DD}, V_{IN} = 0 dBm0 @ T_A = 25° C)

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Transmit Gain					
(Relative to Gain at 1020 Hz)	G_{RX}				
Input Amplifier Set to Unity Gain					
	50 Hz	—	-33	—	dB
	60 Hz	—	-30	—	dB
	200 Hz	—	-1.1	—	dB
	300 to 3000 Hz	—	± 0.1	—	dB
	3400 Hz	—	-0.6	—	dB
	4000 Hz	—	-14.6	—	dB
	4600 Hz	—	-34	—	dB

Table III - RECEIVE FILTER TRANSFER CHARACTERISTICS
(V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, $DCLK_R$ = MCLK = 1.544 MHz, MCLKSEL = V_{DD}, V_{IN} = 0 dBm0 @ T_A = 25° C)

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Receive Gain					
(Relative to Gain at 1020 Hz)	G_{RR}				
0 dBm0 Signal Input at Data Receive					
	100 Hz	—	0.1	—	dB
	400 Hz	—	0.01	—	dB
	2000 Hz	—	0.04	—	dB
	3000 Hz	—	-0.05	—	dB
	3400 Hz	—	-0.07	—	dB
	4000 Hz	—	-14.3	—	dB
	4600 Hz	—	-33	—	dB

LOOP-AROUND FILTER TRANSFER CHARACTERISTICS
(V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, $DCLK_R$ = $DCLK_X$ = MCLK = 1.544 MHz, MCLKSEL = V_{DD}, V_{IN} = 0 dBm0 @ T_A = 25° C)
PCM_X connected to PCM_R

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Frequency Response					
End-to-End Measurement					
(Looparound)					
	50 Hz	—	-33	—	dB
	60 Hz	—	-31	—	dB
	180 Hz	—	-2.7	—	dB
	200 Hz	—	-1.2	—	dB
	300 Hz	—	0.17	—	dB
	1020 Hz	—	0.01	—	dB
	3300 Hz	—	0.19	—	dB
	3400 Hz	—	1.15	—	dB
	4 KHz	—	-30	—	dB
	4.6 KHz	—	-74	—	dB

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = +5 V ± 5%, V_{SS} = -5 V ± 5%

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Analog Input Resistance	R_{INA}		100	—	—	KΩ
Input Capacitance	C_{IN}	All Logic and Analog Inputs	—	5	—	pF
Input Leakage Current	I_I	V_I = 0 V or V_{DD}	—	—	± 1	μA
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Input Voltage	V_{IH}		2	—	—	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.8 mA	—	—	0.4	V
High Level Output Voltage	V_{OH}	I_{OH} = -40 μA	2.6	—	—	V

DISTORTION CHARACTERISTICS

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Signal to Total Distortion XMT or RCV	STD_X, STD_R	Level +3 dBm0	33	—	—	dBC
		0 to -30 dBm0	36	—	—	
		-40 dBm0	29	—	—	
		-45 dBm0	25	—	—	
Single Frequency Distortion XMT or RCV	SFD_X, SFD_R		—	-45	—	dBC
Intermodulation (End-to-End Measurement) 2-Tone	IMD		—	-56	—	dB

ABSOLUTE AND ENVELOPE DELAY DISTORTION CHARACTERISTICS

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Absolute Delay	t_{DAX}	f = 1600 Hz	—	280	—	μs
Transmit Envelope Delay Relative to D_{AX}	t_{DEX}	f = 500-600 Hz	—	170	—	μs
		f = 600-1000 Hz	—	70	—	
		f = 1000-2600 Hz	—	70	—	
		f = 2600-2800 Hz	—	90	—	
Receive Absolute Delay	t_{DAR}	f = 1600 Hz	—	180	—	μs
Receive Envelope Delay Relative to D_{AR}	t_{DER}	f = 500-600 Hz	—	30	—	μs
		f = 600-1000 Hz	—	30	—	
		f = 1000-2600 Hz	—	60	—	
		f = 2600-2800 Hz	—	110	—	

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NOISE CHARACTERISTICS

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Noise C Message Weighted	N_{XC}	V_F = GRD Analog				
		Vref = -2.5 V	—	15	—	dBrnc0
		Vref = -3.16 V	—	13	—	
Transmit Noise Psophometric	N_{XP}	Vref = -2.5 V	—	-74	—	dBm0p
		Vref = -3.16 V	—	-76	—	
Receive Noise C Message Weighted	N_{RC}	Vref = -2.5 V	—	9	—	dBrnc0
		Vref = -3.16 V				
		PCMR = 11111111	—	7	—	
Receive Noise Psophometric	N_{RP}	Vref = -2.5 V	—	-81	—	dBm0p
		Vref = -3.16 V	—	-83	—	
V_{DD} Power Supply Rejection Transmit Channel	PSRR	300 Hz to 10 KHz	—	-30	—	dB
V_{SS} Power Supply Rejection Transmit Channel	PSRR	300 Hz to 10 KHz	—	35	—	dB
V_{DD} Power Supply Rejection Receive Channel	PSRR	300 Hz to 10 KHz	—	-35	—	dB
V_{SS} Power Supply Rejection Receive Channel	PSRR	300 Hz to 10 KHz	—	34	—	dB
Cross Talk Transmit to Receive	CT_{XR}	V_{FX} = 0 dBm0 at 1020 Hz	—	-80	—	dB
Cross Talk Receive to Transmit	CT_{RX}	DR = 0 dBm0, V_{FX} = 0 V 1020 Hz	—	-75	—	dB

Functional Description

The CD22302/CD22303 contains all the analog and digital circuitry necessary for the conversion of voice signal into PCM data and vice versa. All necessary filtering to the standard AT&T D3/D4 specifications and CCITT recommendations is realized by the switched capacitor filters on chip. As shown in the functional block diagram in Fig. 1, this device contains independent circuitry for converting transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting to the voice signal in both conversions.

Transmit Section

The transmit section consists of a gain adjustable input Op Amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input Op Amp drives a RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30-dB attenuation (minimum) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128 KHz, followed by a 3rd order high-pass filter clocked at 32 KHz. The transmit filter characteristics are shown in Table II. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8-KHz sampling rate. The V_{REF} input reference voltage can range from -2.5 volts to -3.16 volts as required by different applications. The $FSYN_X$ Transmit Frame Sync pulse controls the successive approximation analog to digital conversion process. The 8-bit PCM data is clocked out at PCM_X pin by the $DCLK_X$ Transmit Data clock which can be varied from 64 KHz to 4.1 MHz.

Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at PCM_R upon the occurrence of $FSYN_R$, Receive Frame Sync pulse. $DCLK_R$ Receive Data Clock, which can range from 64 KHz to 4.1 MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clocked at 128 KHz to smooth the sample and hold signal as well as to compensate for the SIN X/X distortion. The filter output is available at the V_{OUT} pin which can drive a 20-KΩ resistive load. The receive filter characteristics are shown in Table III.

A.C. Waveforms

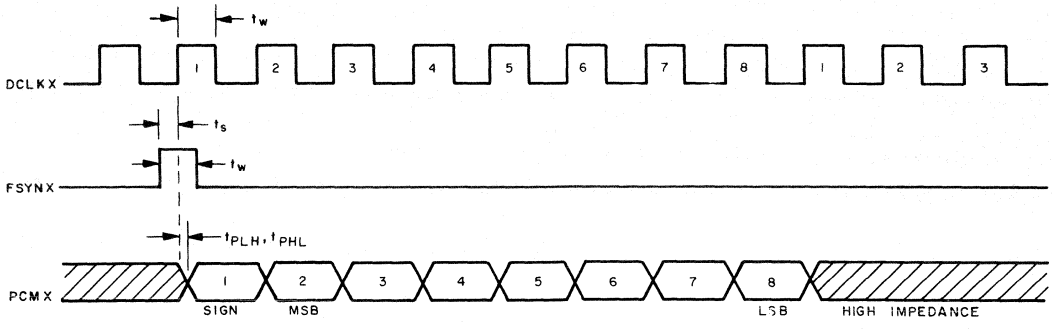
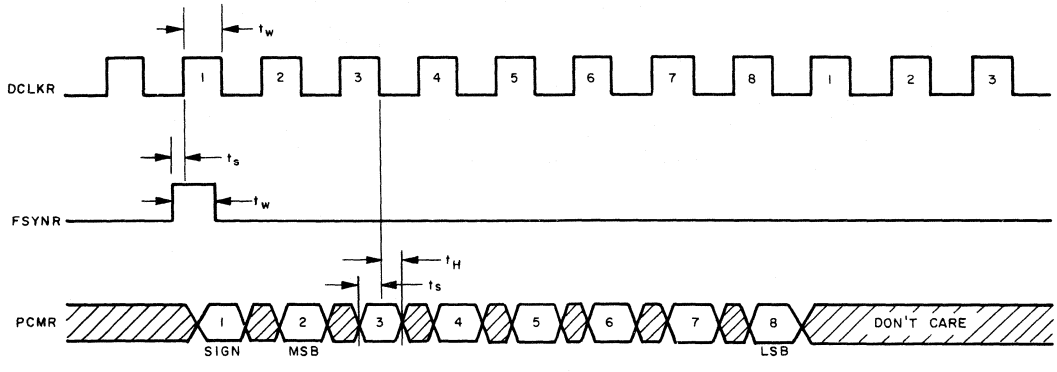


Fig. 2 - Transmit timing diagram.

92CM-36909

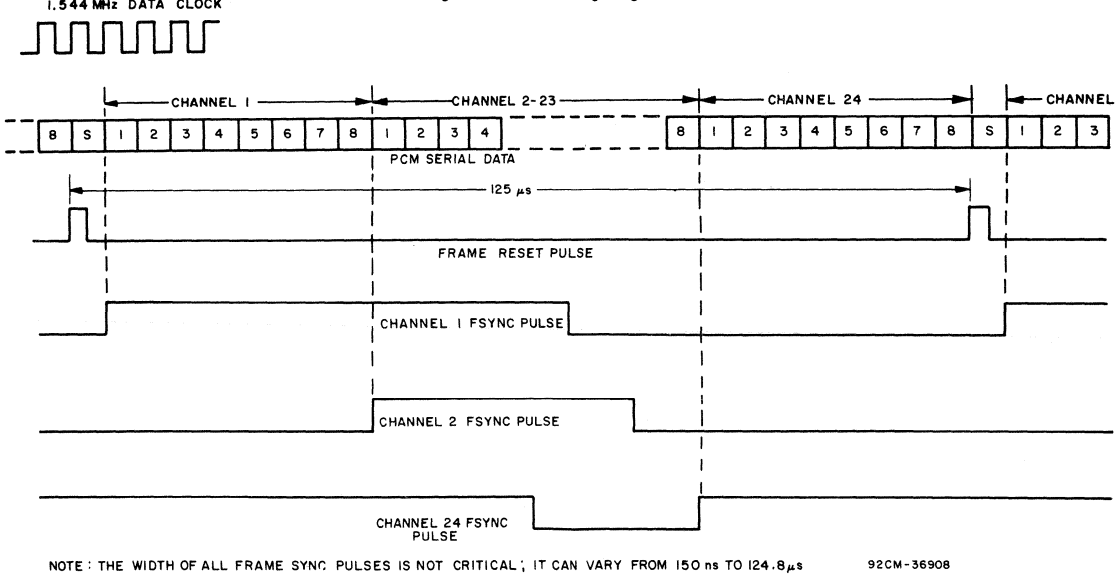


NOTE: 1. DCLKX AND DCLKR CLOCKS SHOULD BE 50% DUTY CYCLE ±20%

2. THE MAXIMUM RISING AND FALLING TIME OF ALL DIGITAL INPUTS SHOULD BE UNDER 100 ns

92CM-36910

Fig. 3 - Receive timing diagram.



NOTE: THE WIDTH OF ALL FRAME SYNC PULSES IS NOT CRITICAL; IT CAN VARY FROM 150 ns TO 124.8 µs

92CM-36908

Fig. 4 - 24-channel PCM system timing diagram.

CD22302, CD22303

Master Clock

The master clock can assume a 1.536 MHz, 1.544 MHz, or 2.048 MHz clock. The input master clock frequency must be reflected by pinstrapping the proper voltage level of the MCLKSEL input pin. This pin is tied to V_{DD} (+5 V) for 2.048 MHz, or to GND_D (0 V) for 1.536 MHz, or to V_{SS} (-5 V) for 1.544 MHz. The master clock is divided down internally to provide the timing and control signals required for the switched capacitor filters and for the CODEC conversions.

Power-Down Mode

When power is first applied, the device is in the power-down standby mode. To power-up the device, a clock signal must be applied to MCLK and either $FSYN_X$ or $FSYN_R$. To power-down the device, $FSYN_X$ and $FSYN_R$ must be held to a low logic level, while a master clock frequency must be applied at MCLK.

Product Preview

CD22352

PCM CODEC with A/B Signaling

Features:

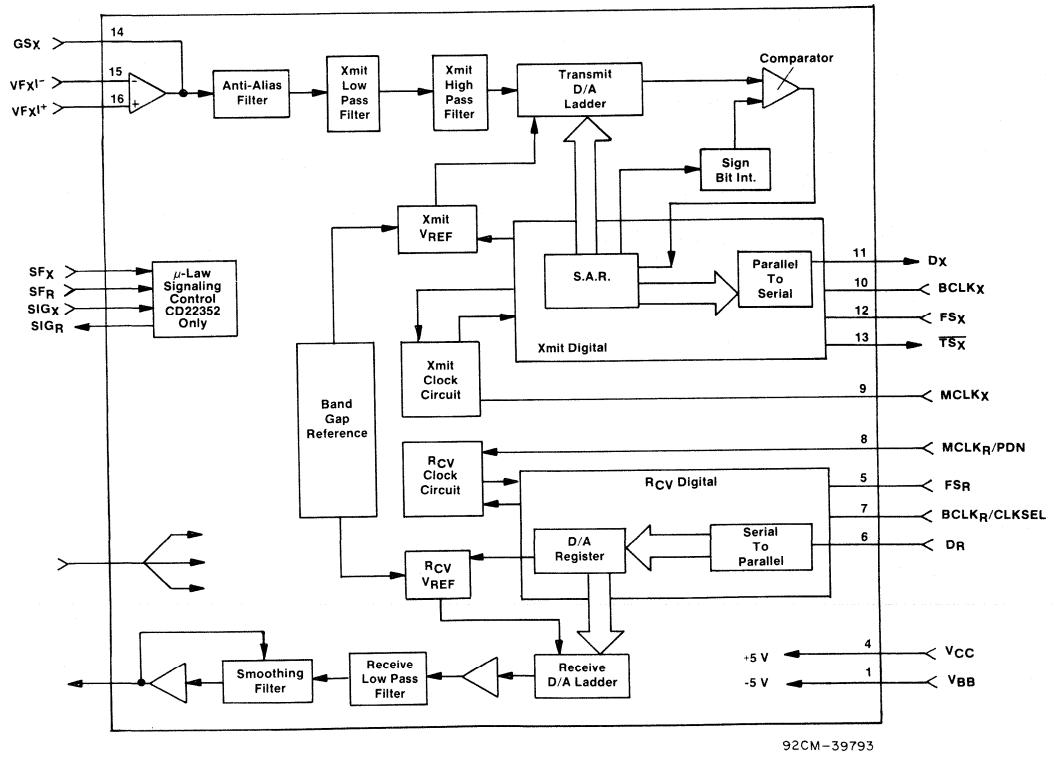
- *μ-Law with signaling*
- *Low power dissipation*
  - *80 mW operating (typical)*
  - *5 mW standby*
- *Meets D3/D4 channel bank specifications*
- *Variable data clock rates*
  - *64KB/s to 4.16 MHz*
- *Automatic power down*
- *TTL/CMOS compatible interfaces*
- *Synchronous/Asynchronous operation*

The RCA CD22352 Combo Chip is a monolithic silicon-gate CMOS integrated circuit which meets the CCITT recommendations and D3/D4 channel bank specifications. This device contains the band-limiting filters and companding A/D and D/A conversion circuits as well as transmit and receive signaling capability, if desired. Without signaling the codec, operates in long and short frame synchronous mode.

However, this device is designed for short-frame sync applications for signaling, that is, the frame sync pulse is 2-bit clock period long.

With FS_X two-bit clock period long, the data present at SIG_X input will be inserted as the LSB in the PCM data stream during that frame. With FS_R two-bit clock period long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame.

The CD22352 is supplied in the 18-lead dual-in-line plastic package (E suffix).



Block diagram of the CD22352.

Preview Data only

Advance Information/
Preliminary Data

CD22354, CD22357

CMOS Single-Chip, Full-Feature PCM CODEC

Features:

- *Low power dissipation:*
  80 mW - typical operating
  5 mW - typical standby
- *Meets or exceeds all AT&T D3/D4 specifications and CCITT recommendations*
- *Complete CODEC and filtering systems:*
  No external components for sample-and-hold and auto-zero functions
  Transmit input section includes anti-aliasing prefilter
  Receive output filter with SIN X/X correction
- *Variable data clocks - from 64 kHz to 4.1 MHz*
- *Programmable gain for transmit input*
- *CD22354 - 16-pin μ-law CODEC*
- *CD22357 - 16-pin A-law CODEC*
- *Synchronous and asynchronous operation*
- *TTL or CMOS-compatible logic*
- *±5-V operation*
- *Fast acquisition on power-up*
- *ESD protection on all inputs and outputs*
- *Automatic power-down by removal of both frame syncs*
- *Internal precision voltage reference*

The RCA-CD22354 and CD22357 are monolithic silicon-gate, double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22354 provides the AT&T μ-law and the CD22357 provides the CCITT A-law companding characteristic.

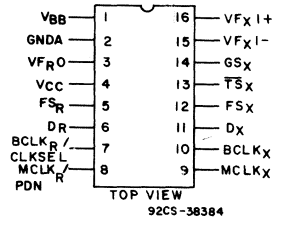
The primary applications for the CD22354 and CD22357 are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown in Fig. 1.

With the flexible features, including synchronous and asynchronous operations and variable data rates, the CD22354 and CD22357 are ideally suited for PABX, central office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

The CD22354 and CD22357 are supplied in 16-lead dual-in-line plastic packages (E suffix).

Applications:

- *PABX*
- *Central office switching systems*
- *Accurate A/D and D/A conversions*
- *Digital telephones*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE V_{CC}	+6 V
DC SUPPLY-VOLTAGE V_{BB}	-6 V
OPERATING TEMPERATURE RANGE	-25 to +85°C
STORAGE TEMPERATURE RANGE	-65 to+150°C
POWER DISSIPATION AT 25°C	500 mW
DIGITAL INPUT	-0.5 to V_{CC} +0.5 V

File Number **1682**

Table I

Pin Symbol	Pin Names	Pin No.
V_{BB}	Negative power supply	1
GNDA	Ground analog	2
VF_RO	Analog output	3
V_{CC}	Positive power supply	4
FS_R	Frame sync. receive	5
D_R	Receive data input	6
$BCLK_R$/CLKSEL	Bit clock receive/Master clock select	7
$MCLK_R$/PDN	Master clock receive/Power down	8
$MCLK_X$	Master clock transmit	9
$BCLK_X$	Bit clock transmit	10
D_X	PCM data output	11
FS_X	Frame sync. transmit	12
$\overline{TS_X}$	Open drain output (Encoder Indicator)	13
GS_X	Transmit gain adjust	14
VF_XI^-	Inverting input of the input amplifier	15
VF_XI^+	Non-inverting input of the input amplifier	16

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Positive Power Supply	V_{CC}		4.75	5	5.25	V
Negative Power Supply	V_{BB}		-4.75	-5	-5.25	
Power Dissipation (Operating)	P_{OPR}	V_{CC} = 5 V	60	80	90	mW
Power Dissipation (Standby)	P_{STBY}	V_{BB} = -5 V	—	5	—	

Table II - TRANSMIT FILTER TRANSFER CHARACTERISTICS
(V_{CC}=5 V ± 5%, V_{BB}=-5 V ± 5%, $BCLK_X$=$MCLK_R$=1.544 MHz, T_A=25°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Gain (Relative to Gain at 1020 Hz) Input Amplifier Set to Unit Gain	G_{RX}	50 Hz	—	-33	—	dB
		60 Hz	—	-30	—	
		200 Hz	—	-1.1	—	
		300 to 3000 Hz	—	±0.1	—	
		3400 Hz	—	-0.6	—	
		4000 Hz	—	-14.6	—	
		4600 Hz	—	-34	—	

Table III - RECEIVE FILTER TRANSFER CHARACTERISTICS
(V_{CC}=5 V ± 5%, V_{BB}=-5 V ± 5%, $BCLK_R$=$MCLK_X$=1.544 MHz, V_{IN} =0 dBmO@T_A=25°C)

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Receive Gain (Relative to Gain at 1020 Hz) (Includes sin X/X Compensation)	G_{RR}	100 Hz	—	0.01	—	dB
		400 Hz	—	0.01	—	
		2000 Hz	—	0.04	—	
		3000 Hz	—	-0.05	—	
		3400 Hz	—	-0.6	—	
		4000 Hz	—	-14.3	—	
		4600 Hz	—	-33	—	

CD22354, CD22357

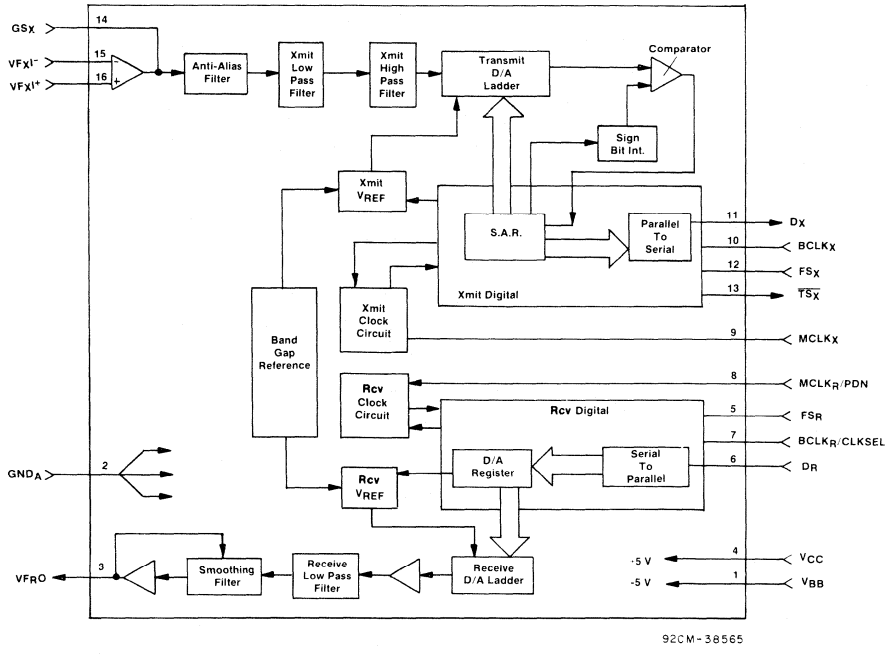


Fig. 1 - Functional block diagram - full-feature PCM CODEC.

LOOP-AROUND FILTER TRANSFER CHARACTERISTICS
(V_{CC}=5 V ± 5%, V_{BB}=-5 V ± 5%, $BCLK_R$=$BCLK_X$=$MCLK_X$=1.544 MHz, V_{IN}=0 dBmO @T_A=25° C)
D_X connected to D_R

CHARACTERISTIC	CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Frequency Response End-to-End Measurement (Loop-around)	50 Hz	—	-33	—	dB
	60 Hz	—	-30	—	
	180 Hz	—	-2.7	—	
	200 Hz	—	-1.1	—	
	300 Hz	—	0.17	—	
	1020 Hz	—	0.01	—	
	3300 Hz	—	0.19	—	
	3400 Hz	—	-1.12	—	
	4 kHz	—	-30	—	
	4.6 kHz	—	-74	—	

DISTORTION CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Signal to Total Distortion Xmit or R_{CV}	STD_X, STD_R	Level +3 dBmO	33	—	—	dBC
		0 to -30 dBmO	36	—	—	
		-40 dBmO	29	—	—	
		-45 dBmO	25	—	—	
Single Frequency Distortion Xmit or R_{CV}	SFD_X, SFD_R		—	-45	—	dBC
Intermodulation (End-to-End Measurement) 2-Tone	IMD		—	-56	—	dB

ABSOLUTE AND ENVELOPE DELAY DISTORTION CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Absolute Delay	t_{DAX}	f = 1600 Hz	—	280	—	μs
Transmit Envelope Delay Relative to D_{AX}	t_{DEX}	f = 500-600 Hz	—	170	—	
		f = 600-1000 Hz	—	70	—	
		f = 1000-2600 Hz	—	70	—	
		f = 2600-2800 Hz	—	90	—	
Receive Absolute Delay	t_{DAR}	f = 1600 Hz	—	180	—	
Receive Envelope Delay Relative to D_{AR}	t_{DER}	f = 500-600 Hz	—	30	—	
		f = 600-1000 Hz	—	30	—	
		f = 1000-2600 Hz	—	60	—	
		f = 2600-2800 Hz	—	110	—	

PIN FUNCTION AND DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1	V_{BB}	Negative power supply, V_{BB} = -5 V ± 5%
2	GND_A	Analog ground. All signals referenced to this pin.
3	VF_RO	Analog output of RECEIVE FILTER
4	V_{CC}	Positive power supply, V_{CC} = +5 V ± 5%
5	FS_R	Receive Frame Sync Pulse which enables $BCLK_R$ to shift PCM Data into D_R. FS_R is an 8-kHz PULSE TRAIN.
6	D_R	Receive Data Input. PCM Data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLKSEL	The Bit Clock which shifts data into D_R after the Frame sync leading edge, may vary from 64 kHz to 4.16 MHz. Alternatively, the leading edge may be a logic input which selects either 1.536 MHz or 1.544 MHz or 2.048 MHz for Master Clock in synchronous mode and $BCLK_X$ is used for both Transmit and Receive directions.
8	$MCLK_R$/PDN	Receive Master Clock. Must be 1.536 MHz or 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$ but should be synchronous with $MCLK_X$ for best performance. When this pin is continuously connected low, $MCLK_X$ is selected for all internal timing. When this pin is continuously connected high, the device is power down.
9	$MCLK_X$	Transmit Master Clock. Must be 1.536 MHz or 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
10	$BCLK_X$	The Bit Clock which shifts out the PCM Data on D_X. May vary from 64 kHz to 4.16 MHz but must be synchronous with $MCLK_X$.
11	D_X	The TRI-STATE PCM Data Output which is enabled by FS_X.
12	FS_X	Transmit Frame Sync Pulse input which enables $BCLK_X$ to shift out the data on D_X. FS_X is an 8-kHz PULSE TRAIN.
13	$\overline{TS}_X$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Transmit gain adjust
15	VF_XI^-	Inverting input of the transmit input amplifier
16	VF_XI^+	Non-inverting input of the transmit input amplifier

CD22354, CD22357

FUNCTIONAL DESCRIPTION

CD22354 is pin- and function-compatible to TP3054.

CD22357 is pin- and function-compatible to TP3057.

Power-Up

When power is first applied, the Power-On reset circuitry initializes the CODEC and places it in a Power-Down mode.

To power up the device, there are two modes available.

1. A logical zero at pin 8 will power up the device provided FS_X or FS_R pulses are present.
2. Alternatively, a clock ($MCLK_R$) must be applied to pin 8 and FS_X or FS_R pulses must be present.

Power-Down

Two power-down modes are available.

1. A logical 1 at pin 8 after 1 ms will power down the device.
2. Alternatively, hold both FS_X and FS_R continuously low, the device will power down approximately 1 ms after the last FS_X or FS_R pulse.

Synchronous Operation

The same master clock and bit clock should be used for the receive and transmit sections. $MCLK_X$ (pin 9) is used to provide the master clock for the transmit section. The receive section will use the same master clock if the $MCLK_R$/PDN (pin 8) is grounded (synchronous operation), or at V_{CC} (power-down mode).

The $BCLK_X$ (pin 10) is used to provide the bit clock to the transmit section. In synchronous operation, this bit clock is used for the receive section if $MCLK_R$/PDN (pin 8) is grounded. $BCLK_R$/CLKSEL (pin 7) is then used to select the proper internal frequency division for 1.544 MHz, 1.536 MHz or 2.048 MHz operation. See Table IV for 1.544 MHz operation. The device automatically compensates for the 193rd clock pulse each frame.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the leading edge of the $BCLK_X$. After 8 bit-clock periods, the tristate D_X output is returned to a high impedance state. With a FS_R pulse PCM data is latched via the D_R input on the negative edge of the $BCLK_X$.

FS_X and FS_R must be synchronous with $MCLK_X$. For 1.544-MHz operation, the device automatically compensates for 193rd clock pulse each frame.

Table IV - CLOCKING OPTIONS

$BCLK_R$/ CLKSEL	Master Clock Frequency Selected		$MCLK_R$/ PDN
	CD22354	CD22357	
Clocked	1.536 MHz or 1.544 MHz	2.048 MHz	Clocked/0
0	2.048 MHz	1.536 MHz or 1.544 MHz	0
1(or open circuit)	1.536 MHz or 1.544 MHz	2.048 MHz	0

Asynchronous Operation

For asynchronous operation separate transmit and receive clocks may be applied.

For CD22357, the $MCLK_X$ and $MCLK_R$ must be 2.048 MHz and for CD22354 must be 1.536 MHz or 1.544 MHz. These clocks may not be synchronous. However, for best transmission performance it is recommended that $MCLK_X$ and $MCLK_R$ should be synchronous.

For 1.544-MHz operation the device automatically compensates for the 193rd clock pulse each frame. FS_X must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R must be synchronous with $BCLK_R$.

Short-Frame Synchronous Operation

When the power is first applied, the power initialization circuitry places the CODEC in a short-frame synchronous mode. In this mode both frame sync pulses must be 1 bit-clock period long, with timing relationship shown in Fig. 2.

With FS_X high during falling edge of the $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X tristate output buffer, which will output the sign bit. The following rising seven edges clock out the remaining seven bits, and the next falling edge disables the D_X output.

With FS_R high during the falling edge of the $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge latches in the sign bit. The following seven edges latch in the seven remaining bits.

Long-Frame Synchronous Operation

In this mode of operation, both the frame sync pulses must be three or more bit-clock periods long with timing relationship shown in Fig. 3.

Based on the transmit frame sync FS_X, the CODEC will sense whether short- or long-frame synchronous pulses are being used.

For 64-kHz operation the frame sync pulse must be kept low for a minimum of 160 ns.

The D_X tristate output buffer is enabled with the rising edge of FS_X or the rising edge of the $BCLK_X$, whichever comes later and the first bit clocked out is the sign bit. The following seven rising edges of the $BCLK_X$ clock out the remaining seven bits. The D_X output is disabled by the next falling edge of the $BCLK_X$ following the 8th rising edge or by FS_R going low whichever comes later.

A rising edge on the receive frame sync, FS_R, will cause the PCM data at D_R to be latched in on the next falling edge of the $BCLK_R$. The remaining seven bits are latched on the successive seven falling edges of the bit-clock ($BCLK_X$ in synchronous mode).

Transmit Section

The transmit section consists of a gain-adjustable input op-amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input op-amp drives a RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30-dB attenuation (minimum) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128 kHz, followed by a 3rd order high-pass filter clocked at 32 kHz. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8-kHz sampling rate. A precision voltage reference is trimmed in manufacturing to provide an input overload of nominally 2.5-V peak. Transmit frame sync pulse, FS_X, controls the succesive approximation analog to digital conversion process. The 8-bit PCM data is clocked out at D_X by the $BCLK_X$.

$BCLK_X$ can be varied from 64 kHz to 4.1 MHz.

Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at D_R upon the occurrence of FS_R, Receive Frame sync pulse. $BCLK_R$, Receive Data Clock, which can range from 64 kHz to 4.1 MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clocked at 128 kHz to smooth the sample-and-hold signal as well as to compensate for the SIN X/X distortion.

The filter is then followed by a second order Sallen and Key active filter capable of driving a 600-Ω load to a level of 7.2 dBm.

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+5 V ± 5%, V_{BB}=-5 V ± 5%

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Analog Input Resistance	R_{INA}		100	—	—	kΩ
Input Capacitance	C_{IN}	All Logic and Analog Inputs	—	5	—	pF
Input Leakage Current	I_I	V_I = 0 V or V_{CC}	—	—	±1	μA
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Input Voltage	V_{IH}		2	—	—	
Low Level Output Voltage	V_{OL}	I_{OL} = 0.8 mA	—	—	0.4	
High Level Output Voltage	V_{OH}	I_{OH} = -40 μA	2.6	—	—	

A.C. CHARACTERISTICS
Unless otherwise specified, the following conditions apply:

V_{CC} = 5 V dc ± 5%, V_{BB} = -5 V dc ± 5%
GND_A, GND_D = 0 V, F_{FX} = 1020 Hz at 0 dBmO
Transmit input amplifier operating in a unity gain configuration
Temperature = 25°C
Receive output is measure single-ended. All output levels are SIN X/X corrected.

DEFINITION

AMPLITUDE RESPONSE
Absolute Levels Definition:
V_{REF} = -2.5 V dc Nominal 0 dBmO level = 4 dBm into 600 Ω
= 1.2276 V (rms)
Maximum Overload Level:
Voltage reference (V_{REF}) of -2.5 V = 2.5 V μ-Law
= 2.49 V A-Law

ENCODING FORMAT AT D_X OUTPUT

	CD22354 μ-LAW								CD22357 A-LAW (INCLUDES EVEN BIT INVERSION)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0 V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = -Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

CD22354, CD22357

GAIN TRACKING

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Gain Tracking Error	GTX	+3 to -40 dBmO	—	—	±0.25	dB
		-40 to -50 dBmO	—	—	±0.5	
		-50 to -55 dBmO	—	—	±1.2	
Receive Gain Tracking Error	GTR	+3 to -40 dBmO	—	—	±0.15	
		-40 to -50 dBmO	—	—	±0.5	
		-50 to -55 dBmO	—	—	±1.2	

NOISE CHARACTERISTICS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Transmit Noise	N_X	$VF_XI^-=GND_A$	—	12	16	dBrncO
		$VF_XI^+=GND_A$	—	-74	-68	dBmOp
Receive Noise	N_R	D_R=1111111	—	7	11	dBrncO
			—	-81	—	dBmOp
V_{CC} Power Supply Rejection Transmit	PSRR	$VF_XI^+=0$ V_{CC}=5 V + (100 mV RMS) f=0 to 50 kHz	35	40	—	dBc
V_{BB} Power Supply Rejection Transmit	PSRR	$VF_XI^-=0$ V V_{BB}=-5 V + (100 mV RMS) f=0 to 50 kHz	35	40	—	dBc
V_{CC} Power Supply Rejection Receive	PSRR	PCM Code ≡ All 1 Code V_{CC}=5 V + (100 mV RMS) f=0 to 4 kHz	35	40	—	dBc
		=4 to 25 kHz	35	40	—	dB
		=25 to 50 kHz	35	36	—	
V_{BB} Power Supply Rejection Receive	PSRR	PCM Code ≡ All 1 Code V_{BB}=-5 V + (100 mV RMS) f=0 to 4 kHz	35	40	—	dBc
		=4 to 25 kHz	35	40	—	dB
		=25 to 50 kHz	35	36	—	
Cross Talk Transmit to Receive	CT_{XR}	$VF_XI^-=0$ dBmO @ 1020 Hz	—	-80	—	dB
Cross Talk Receive to Transmit	CT_{RX}	D_R ≡ 0 dBmO @ 1020 Hz, $VF_XI^-=0$ V	—	-75	—	

TIMING SPECIFICATIONS

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Frequency of Master Clocks	$1/t_{PM}$	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin	—	1.536	—	MHz
		$MCLK_X$ and $MCLK_R$	—	1.544	—	
			—	2.048	—	
Width of Master Clock High	t_{WMH}	$MCLK_X$ and $MCLK_R$	160	—	—	ns
Width of Master Clock Low	t_{WML}	$MCLK_X$ and $MCLK_R$	160	—	—	
Rise Time of Master Clock	t_{RM}	$MCLK_X$ and $MCLK_R$	—	—	50	
Fall Time of Master Clock	t_{FM}	$MCLK_X$ and $MCLK_R$	—	—	50	
Set-up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	t_{SBFM}	First Bit Clock after the Leading Edge of FS_X	100	—	—	
Period of Bit Clock	t_{PB}		485	488	15,725	
Width of Bit Clock High	t_{WBH}	V_{IH} = 2.2 V	160	—	—	
Width of Bit Clock Low	t_{WBL}	V_{IL} = 0.6 V	160	—	—	
Rise Time of Bit Clock	t_{RB}	t_{PB} = 488 ns	—	—	50	
Fall Time of Bit Clock	t_{FB}	t_{PB} = 488 ns	—	—	50	
Holding Time from Bit Clock Low to Frame Sync	t_{HBF}	Long Frame Only	0	—	—	
Holding Time from Bit Clock High to Frame Sync	t_{HOLD}	Short Frame Only	0	—	—	
Set-up Time from Frame Sync to Bit Clock Low	t_{SFB}	Long Frame Only	80	—	—	
Delay Time from $BCLK_X$ High to Data Valid	t_{DBD}	Load=150 pF plus 2 LSTTL Loads	0	—	180	
Delay Time to TS_X Low	t_{XDP}	Load=150 pF plus 2 LSTTL Loads	—	—	140	
Delay Time from $BCLK_X$ Low to Data Output Disabled	t_{DZC}		50	—	165	
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	t_{DZF}	C_L = 0 pF to 150 pF	20	—	165	
Set-up Time from D_R Valid to $BCLK_{R/X}$ Low	t_{SDB}		50	—	—	
Hold Time from $BCLK_{R/X}$ Low D_R Invalid	t_{HBD}		50	—	—	
Set-up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	t_{SF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50	—	—	
Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	t_{HF}	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100	—	—	
Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	t_{HBFI}	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100	—	—	
Minimum Width of the Frame Sync Pulse (Low Level)	t_{WFL}	64k Bit/s Operating Mode	160	—	—	

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

CD22354, CD22357

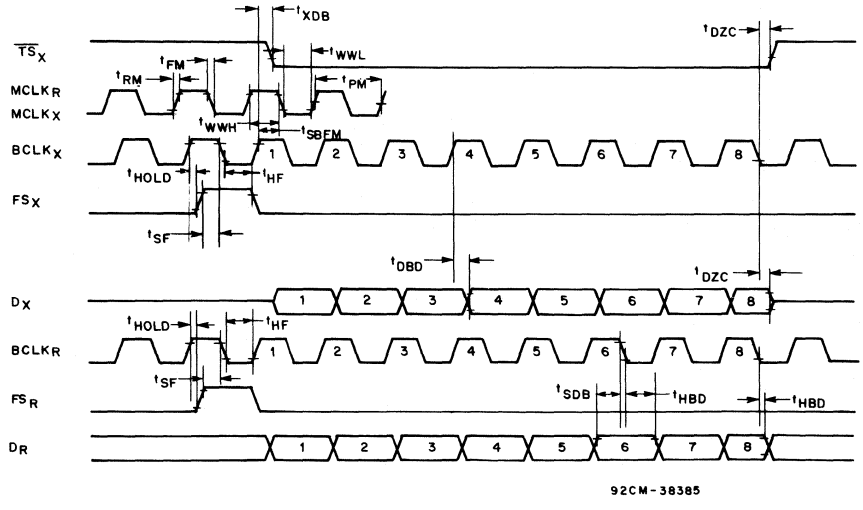


Fig. 2 - Short frame-sync timing.

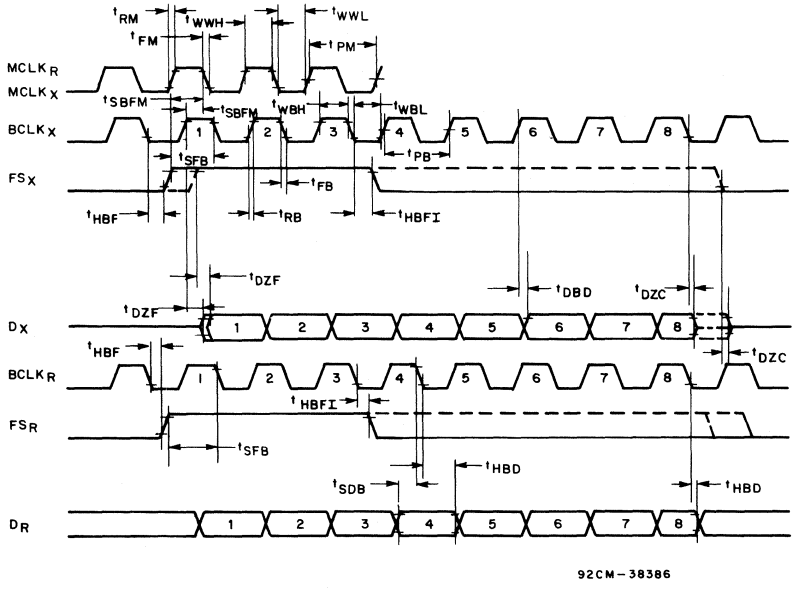


Fig. 3 - Long frame-sync timing.

Advance Information/
Preliminary Data

CD22859

COS/MOS Dual-Tone Multifrequency Tone Generator

For Use in Dual-Tone Telephone Dialing Systems

Features

- *Mute drivers on chip*
- *Device power can either be regulated dc or telephone loop current*
- *Use of an inexpensive 3.579545-MHz TV crystal provides high accuracy and stability for all frequencies*

General Description

The RCA-CD22859 is a CMOS dual-tone multifrequency (DTMF) tone generator for use in dual-tone telephone dialing systems. The device can easily be interfaced to a standard pushbutton telephone keyboard, to provide enabling operation directly with the telephone lines.

The CD22859 generates standard DTMF sinusoidal dialing tones from an on-chip reference crystal oscillator. The reference oscillator uses an inexpensive 3.579545-MHz color TV crystal to create highly stable and accurate tones. The sinusoidal tones are digitally synthesized by a stair-step approximation.

One of four low-frequency band row tones and one of four high-frequency band column tones are selected by driving one of the four row inputs and one of the four column inputs low. Simultaneous selection of more than one row input and/or more than one column input will inhibit tone generation, or generate a single-tone sinusoid. These operating modes are described in the functional truth table.

Control logic is included to allow easy interface to standard K500-type telephones. Two CMOS outputs Tx, Rx, capable of driving external p-n-p receiver and transmitter muting transistors are provided. A low input to the CD pin, inhibits tone generation, turns off the reference oscillator, and causes Tx and Rx outputs to logic '0'. During tone generation mode, $\overline{CD} = 1$ and Tx, Rx = logic 1.

All row, column, and $\overline{CD}$ inputs are provided with pull-up resistors to allow the use of SPST switch matrixes.

The CD22859 type is supplied in a 16-lead hermetic dual-in-line side-brazed ceramic package (D suffix), and a 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$)	−0.5 to +12 V
INPUT VOLTAGE RANGE	−0.5 to V_{DD} + 0.5 V
POWER DISSIPATION, P_D:	
At T_A = −40 °C to +60 °C	500 mW
At T_A = +60 °C to +85 °C	Derate Linearly at 12 mW/ °C to 200 mW
POWER DISSIPATION PER OUTPUT	100 mW
OPERATING TEMPERATURE RANGE	−40 °C to +85 °C
LEAD TEMPERATURE DURING SOLDERING:	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

File Number **1257**

CD22859

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -25°C$ to $+60°C$
All voltages referenced to $V_{SS} = 0$ V.

CHARACTERISTIC	V_{DD}	LIMITS		UNITS
		Min.	Max.	
DC Supply Voltage				
Tone Generation Mode with Valid Input*		2.5	10	V
Non-Tone Generation**		1.7	10	
Operating Current				
Tone Generation Mode (Outputs Unloaded)	3.7 V		1.7	mA
	9.3 V		13	
No Keydown Mode	3.7 V		100	μA
	9.3 V		200	
Input Pull-Up Current	3-10 V		400	μA
Input Low Voltage (V_{IL}) Max.	3-10 V		0.2 V_{DD}	V
Input High Voltage (V_{IH}) Min.	3-10 V	0.8 V_{DD}		V

*All logic and counters functional.
**Mute switches remain open.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -25°C$ to $+60°C$

CHARACTERISTIC	V_{DD} (V)	V_O (V)	LIMITS		UNITS
			Min.	Max.	
Tone Outputs (R_L = 82)					
V_O; Dual-Tone Output	3.7-9.3		350	700	mV rms
$V_O(C_L)$; Single-Tone Output, Column*	3.7-9.3		300	—	mV rms
$V_O(R_L)$; Single-Tone Output, Row**	3.7-9.3		260	—	mV rms
Distortion (Note 1)	3.9-9.3		—	10	%
Rise and Fall Time (Dual-Tone Out) (Note 2)	3.9-9.3		—	5	ms
Pre-Emphasis (Note 3)	3.9-9.3		1	3	dB
Output Frequency (Note 4)	3.9-9.3		(Nom. − 1%)	(Nom. + 1%)	Hz
Mute Output Current					
Transmitter					
I_{OH} (Source)	1.7	1.2	−0.5	—	mA
	10	9.5	−3.4	—	
I_{OL} (Sink)	10	2.5	—	10	μA
Receiver					
I_{OH} (Source)	1.7	1.2	−0.5	—	mA
	10	9.5	−3.4	—	
I_{OL} (Sink)	10	2.5	—	10	μA

*Two or more row inputs low, and one column input low.
**Two or more column inputs low, and one row input low.

Notes:

1. Distortion is defined as: The ratio of all extraneous frequency components generated in the voiceband 0.5 kHz to 3 kHz, to the power of the dual-tone signal, measure across R_L.

$$= \frac{(V_1^2 + V_2^2 = \ldots + V_n^2)}{V_L^2 + V_H^2}$$

where $V_1, V_2, \ldots V_n$ are extraneous frequency components in the voiceband 0.5 kHz to 3 kHz, V_L is the low-band frequency tone, and V_H is the high-band frequency tone.

2. Tone rise time is defined as the time for each of the 2 DTMF frequencies to attain 90% of full amplitude, measured from the time when a row and column signal are driven low.
3. Pre-emphasis is the ratio of the high-group level to the low-group level.
4. Refer to Fig. 1 for standard DTMF frequencies.

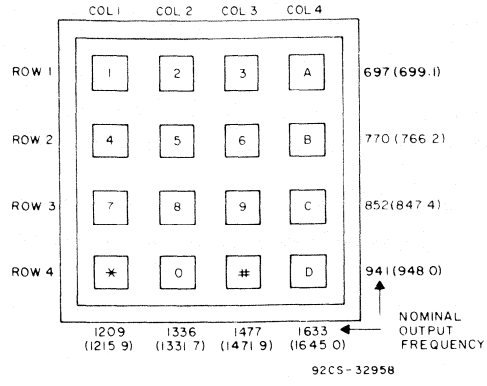


Fig. 1 - Bell and nominal output frequencies (in parenthesis) for 3.579545-MHz crystal.

DTMF Generator Functional Truth Table

	Inputs				Outputs		
Keyboard Mode	**Number of Column Inputs Activated "Low"**	**Number of Row Inputs Activated Low**	$\overline{CD}$	**Tone**	**OSC Running**	**RX**	**TX**
X	X	X	"0"	None	No	"0"	"0"
No key depressed	0	0	"1"	None	No	"0"	"0"
	0	1	"1"	Dual Tone R_a,C_1	Yes	"1"	"1"
	1,2,3, or 4	0	"1"	None	No	"0"	"0"
Normal Dialing One Key Depressed (See Note 1)	1	1	"1"	Dual Tone R_a,C_b	Yes	"1"	"1"
Two or More Keys In Same Row (See Note 2)	2,3, or 4	1	"1"	Single Row Tone R_a	Yes	"1"	"1"
Two or More Keys In Same Column	1	2,3, or 4	"1"	Single Column Tone C_b	Yes	"1"	"1"
Two or More Keys In Different Rows & Columns	2,3 or 4	1	"1"	None	Yes	"1"	"1"
	1		1	None	Yes	"1"	"1"

Where:
X = Do Not Care
R_a,C_b refers to Tone Output frequencies corresponding to Row 1, Row 2, Row 3, Row 4, Column 1, Column 2, Column 3, Column 4
a = 1,2,3,4 b = 1,2,3,4 a = b, or a ≠b

1. Corresponds to normal dual-tone operation.
2. Corresponds to single-tone generation mode.

CD22859

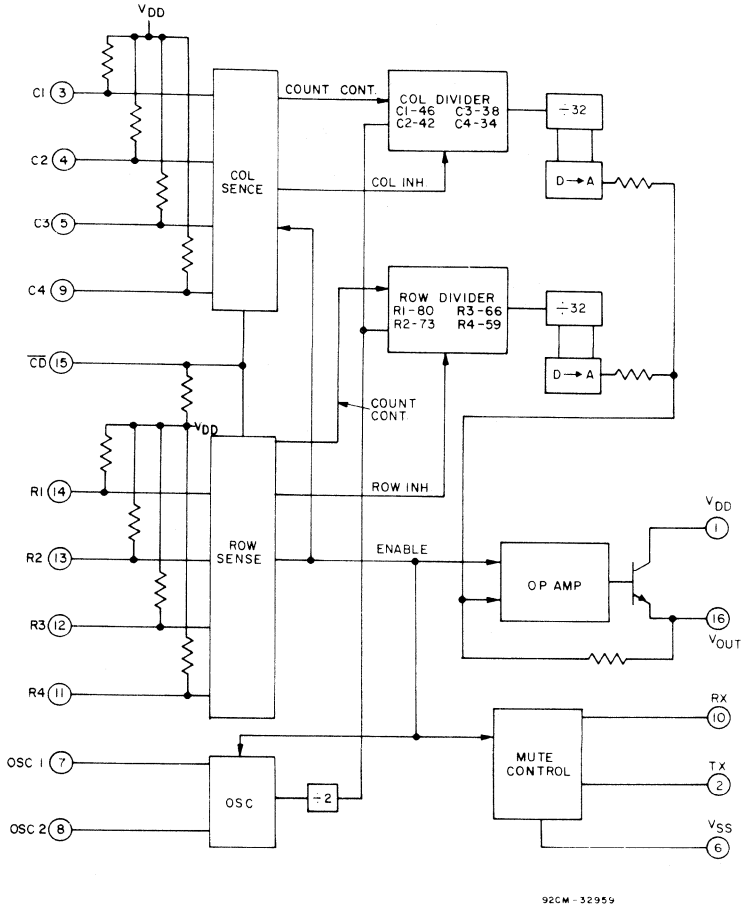


Fig. 2 - Touch-tone generator.

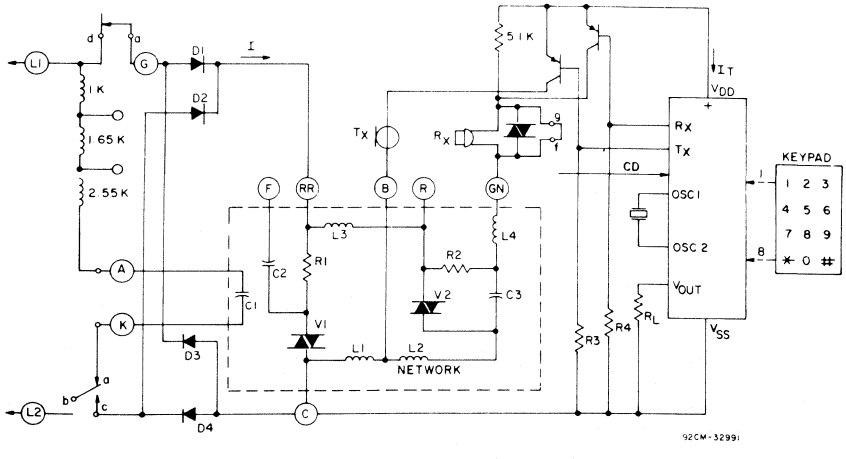
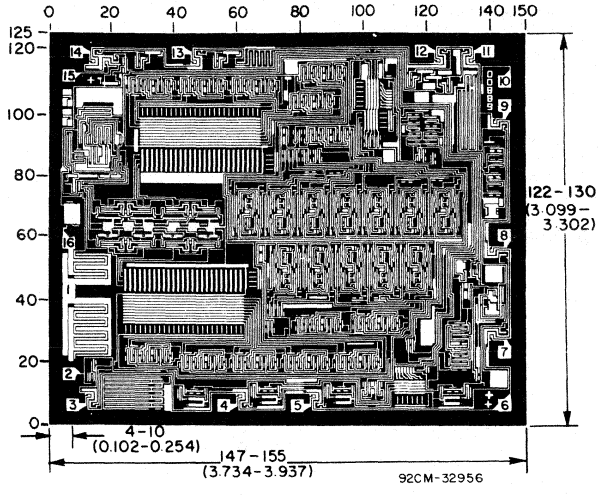


Fig. 3 - Interface with standard K500 telephone network.

CD22859



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CD22859CH chip.

CD54/74HC22106, CD54/74HCT22106

Advance Information/
Preliminary Data

QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control

Type Features:

- *64 analog switches in an 8 x 8 x 1 array*
- *On-chip line decoder and control latches*
- *Automatic power-up reset by using a 0.1 μF capacitor at the $\overline{MR}$ pin*
- *R_{on} resistance 95 ohms @ V_{CC} = 4.5 V*
- *CD54HC/CD74HC types: 2 to 10 V operation*
- *CD54HCT/CD74HCT types: 4.5 to 5.5 V operation*
- *Analog signal capability: V_{CC}*

The RCA-CD54/74HC22106 and CD54/74HCT22106 are digitally controlled analog switches which utilize silicon-gate CMOS technology. The CD54HC/74HC22106 types feature CMOS input-voltage-level compatibility and the CD54HCT/74HCT22106 feature LSTTL input-voltage-level compatibility.

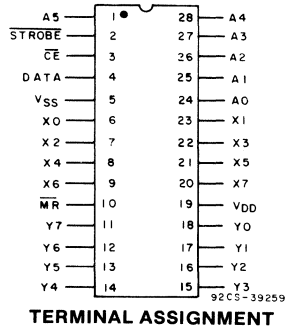
The Master Reset has an internal pull-up resistor and is normally used with a 0.1 μF capacitor. During power-up all switches are automatically reset. The crosspoint switches will reset with $\overline{MR}$ = 0 even if $\overline{CE}$ is high. A 6-bit address through a 6-line-to-64-line decoder selects the transmission gate which can be turned on by applying a logical ONE to the DATA input and logical ZERO to the STROBE. Similarly, any transmission gate can be turned OFF by applying a logical ZERO to the DATA input while strobing the STROBE with a logical ZERO.

The $\overline{CE}$ pin allows the crosspoint array to be cascaded for matrix expansion in both the X and Y directions.

The CD54HC and CD54HCT devices are supplied in the 28-lead dual-in-line frit-seal ceramic packages (F-suffix). The CD74HC and CD74HCT devices are supplied in the 28-lead dual-in-line plastic packages (E-suffix).

Family Features:

- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *CD54HC/CD74HC types:*
  2 to 10 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} =30% of V_{CC}; @ V_{CC} = 5 V and 10 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS input compatibility
  $I_I \leq 1$ μA @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

File Number **1719**

CD54/74HC22106, CD54/74HCT22106

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages reference to ground) ..... -0.5 to +11 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V or $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC TRANSMISSION GATE CURRENT ..... ±25 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A =60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For T_A =100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 12 mW/° C to 200 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING) FOR 10 s MAX.:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:			
CD54/74HC22106	2	10	V
CD54/74HCT22106	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V

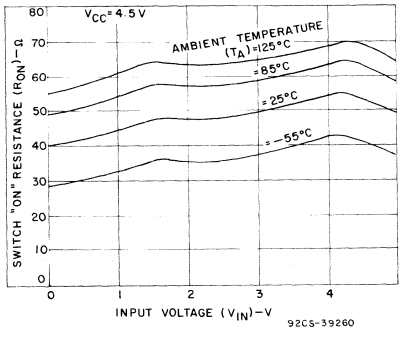


Fig. 1 - Typical "ON" resistance as a function of input signal voltage.

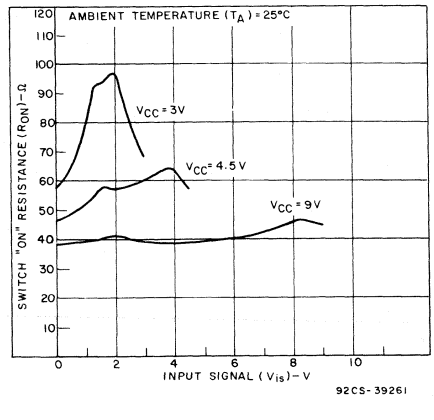


Fig. 2 - Typical "ON" resistance as a function of input signal voltage.

CD54/74HC22106, CD54/74HCT22106

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC22106/CD54HC22106										CD74HCT22106/CD54HCT22106										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES			
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C			
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max		
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5									
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—		V
			9	6.3	—	—	6.3	—	6.3	—		5.5									
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5									
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8		V
			9	—	—	2.7	—	2.7	—	2.7		5.5									
Input Leakage Current I_I (Any Control)	V_{CC} or Gnd		10	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1		μA
Quiescent Device Current I_{CC} (with $\overline{MR}$ = 1)	V_{CC} or Gnd		10	—	—	5	—	50	—	100	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40		μA
Off Leakage Current I_L (with $\overline{MR}$ = 1)	All Switches OFF		10	—	—	0.1	—	1	—	1	—	5.5	—	—	0.1	—	1	—	1		μA
"On" Resistance R_{on}	V_{CC} to Gnd		2	—	470	700	—	875	—	1050											
			4.5	—	64	95	—	120	—	140	—	4.5	—	64	95	—	120	—	140		Ω
			9	—	45	70	—	90	—	100											
			—	—	—	—	—	—	—	—											
	$V_{CC/2}$		4.5	—	58	85	—	110	—	130	—	4.5	—	58	85	—	110	—	130		Ω
			9	—	40	60	—	80	—	90											
"On" Resistance Between Any Two Channels ΔR_{on}	V_{CC} to Gnd		—	—	—	—	—	—	—	—	V_{CC} to Gnd	4.5	—	25	—	—	—	—	—		Ω
			4.5	—	25	—	—	—	—	—											
			9	—	23	—	—	—	—	—											

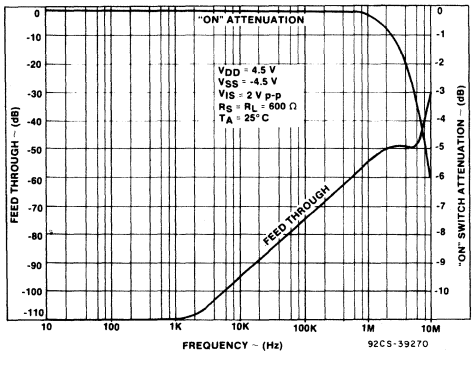


Fig. 3 - Typical "ON" resistance and crosstalk as a function of frequency.

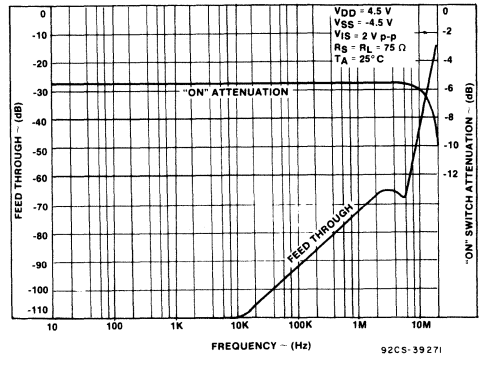


Fig. 4 - Typical "ON" switch attenuation and "OFF" switch feed through as a function of frequency.

CD54/74HC22106, CD54/74HCT22106

SWITCHING CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	V_{SS}	V_{CC}	LIMITS												UNITS
				25°C				-40°C to +85°C				-55°C to +125°C				
				HC		HCT		74HC		74HCT		54HC		54HCT		
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CONTROLS																
Propagation Delay Time: t_{PZH}		0	2	—	370	—	—	—	385	—	—	—	400	—	—	
Strobe to Output		0	4.5	—	110	—	120	—	125	—	135	—	135	—	150	ns
(Switch Turn-on to		0	9	—	65	—	—	—	70	—	—	—	75	—	—	
High Level)																
Data-in to Output t_{PZH}		0	2	—	240	—	—	—	255	—	—	—	270	—	—	
(Turn-on to High Level)		0	4.5	—	75	—	85	—	85	—	95	—	90	—	100	ns
		0	9	—	50	—	—	—	55	—	—	—	60	—	—	
Address to Output t_{PZH}		0	2	—	380	—	—	—	400	—	—	—	420	—	—	
(Turn-on to High Level)		0	4.5	—	110	—	120	—	125	—	135	—	135	—	150	ns
		0	9	—	65	—	—	—	75	—	—	—	80	—	—	
Propagation Delay Times: t_{PHZ}		0	2	—	400	—	—	—	420	—	—	—	400	—	—	
Strobe to Output		0	4.5	—	135	—	150	—	155	—	170	—	160	—	180	ns
(Switch Turn-off)		0	9	—	90	—	—	—	100	—	—	—	110	—	—	
Data-in to Output t_{PZL}		0	2	—	240	—	—	—	255	—	—	—	270	—	—	
(Turn-on to Low Level)	R_L = 10 kΩ	0	4.5	—	75	—	85	—	85	—	95	—	90	—	100	ns
	C_L = 50 pF	0	9	—	50	—	—	—	55	—	—	—	60	—	—	
Address to Output t_{PHZ}	t_r, t_f = 6 ns	0	2	—	420	—	—	—	440	—	—	—	460	—	—	
(Turn-off)		0	4.5	—	140	—	150	—	155	—	170	—	165	—	180	ns
		0	9	—	95	—	—	—	100	—	—	—	105	—	—	
Minimum Set-up Time t_{SU}		0	2	35	—	—	—	40	—	—	—	45	—	—	—	
Data-in to Strobe, Address		0	4.5	20	—	20	—	20	—	20	—	20	—	20	—	ns
		0	9	15	—	—	—	15	—	—	—	15	—	—	—	
Minimum Hold Time t_H		0	2	85	—	—	—	90	—	—	—	95	—	—	—	
Data-in to Strobe, Address		0	4.5	25	—	25	—	25	—	25	—	25	—	25	—	ns
		0	9	20	—	—	—	20	—	—	—	20	—	—	—	
Minimum Strobe Pulse Width t_W		0	2	200	—	—	—	210	—	—	—	220	—	—	—	
		0	4.5	45	—	55	—	55	—	65	—	60	—	—	70	ns
		0	9	25	—	—	—	30	—	—	—	35	—	—	—	
Maximum Switching F_0		0	2	0.7	—	—	—	0.6	—	—	—	0.5	—	—	—	
Frequency		0	4.5	3.0	—	2.8	—	2.8	—	2.6	—	2.7	—	2.5	—	MHz
		0	9	7	—	—	—	6.5	—	—	—	6.0	—	—	—	
Input (Control) C_I		—	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
Capacitance																

CD54/74HC22106, CD54/74HCT22106

ANALOG CHANNEL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS	V_{IS}	V_{SS}	V_{CC}	LIMITS												UNITS
					25°C				-40°C to +85°C				-55°C to +125°C				
					HC		HCT		74HC		74HCT		54HC		54HCT		
					Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay Time t_{PHL}	R_L = 10 kΩ	—	0	2	—	30	—	—	—	33	—	—	—	35	—	—	
Signal Input to Output t_{PLH}	C_L = 50 pF	—	0	4.5	—	20	—	20	—	22	—	22	—	25	—	25	ns
	t_r, t_f = 6 ns	—	—	9	—	15	—	—	—	17	—	—	—	19	—	—	
Switch Frequency					Typ.		Typ.										
Response @ -3dB	R_S = R_L = 600 Ω	2Vp-p	-2.25	2.25	5		5										MHz
		2Vp-p	-4.5	4.5	6		6										
Crosstalk Between	R_S = R_L = 600 Ω				Typ.		Typ.										
Any Two Channels	f = 1 KHz	2Vp-p	-2.25	2.25	-110		-110										dB
	f = 1 MHz	2Vp-p	-2.25	2.25	-53		-53										
		2Vp-p	-4.5	4.5	-55		-55										
Switch "OFF"					Typ.		Typ.										
-40dB Feed Through	R_S = R_L = 600 Ω	2Vp-p	-2.25	2.25	7		7										MH
-Frequency		2Vp-p	-4.45	4.45	8		8										
Total Harmonic					Typ.		Typ.										
Distortion T_{HD}	R_L = 10 kΩ	4Vp-p	-2.25	2.25	.05		.05										
	f = 1 kHz sinewave	8Vp-p	-4.5	4.5	.05		.05										%
	R_L = 600 Ω	4Vp-p	-2.25	2.25	0.25		0.25										
	f = 1 kHz sinewave	7Vp-p	-4.5	4.5	0.12		0.12										
Control to Switch					Typ.		Typ.										
Feed-thru Noise	R_L = 10 kΩ	5	0	5	35		35										
(DATA IN, Strobe,	t_r, t_f = 6 ns	10	0	10	65		65										mV
Address)																	
Capacitance C_o					Typ.		Typ.										
X_n to Gnd	f = 1 MHz		0	10	48		48										pF
Y_n to Gnd	f = 1 MHz		0	10	44		44										

CD54/74HC22106, CD54/74HCT22106

TRUTH TABLE

A_5	A_4	A_3	A_2	A_1	A_0	SWITCH SELECT	A_5	A_4	A_3	A_2	A_1	A_0	SWITCH SELECT
0	0	0	0	0	0	$X_0\ Y_0$	1	0	0	0	0	0	$X_0\ Y_4$
0	0	0	0	0	1	$X_1\ Y_0$	1	0	0	0	0	1	$X_1\ Y_4$
0	0	0	0	1	0	$X_2\ Y_0$	1	0	0	0	1	0	$X_2\ Y_4$
0	0	0	0	1	1	$X_3\ Y_0$	1	0	0	0	1	1	$X_3\ Y_4$
0	0	0	1	0	0	$X_4\ Y_0$	1	0	0	1	0	0	$X_4\ Y_4$
0	0	0	1	0	1	$X_5\ Y_0$	1	0	0	1	0	1	$X_5\ Y_4$
0	0	0	1	1	0	$X_6\ Y_0$	1	0	0	1	1	0	$X_6\ Y_4$
0	0	0	1	1	1	$X_7\ Y_0$	1	0	0	1	1	1	$X_7\ Y_4$
0	0	1	0	0	0	$X_0\ Y_1$	1	0	1	0	0	0	$X_0\ Y_5$
0	0	1	0	0	1	$X_1\ Y_1$	1	0	1	0	0	1	$X_1\ Y_5$
0	0	1	0	1	0	$X_2\ Y_1$	1	0	1	0	1	0	$X_2\ Y_5$
0	0	1	0	1	1	$X_3\ Y_1$	1	0	1	0	1	1	$X_3\ Y_5$
0	0	1	1	0	0	$X_4\ Y_1$	1	0	1	1	0	0	$X_4\ Y_5$
0	0	1	1	0	1	$X_5\ Y_1$	1	0	1	1	0	1	$X_5\ Y_5$
0	0	1	1	1	0	$X_6\ Y_1$	1	0	1	1	1	0	$X_6\ Y_5$
0	0	1	1	1	1	$X_7\ Y_1$	1	0	1	1	1	1	$X_7\ Y_5$
0	1	0	0	0	0	$X_0\ Y_2$	1	1	0	0	0	0	$X_0\ Y_6$
0	1	0	0	0	1	$X_1\ Y_2$	1	1	0	0	0	1	$X_1\ Y_6$
0	1	0	0	1	0	$X_2\ Y_2$	1	1	0	0	1	0	$X_2\ Y_6$
0	1	0	0	1	1	$X_3\ Y_2$	1	1	0	0	1	1	$X_3\ Y_6$
0	1	0	1	0	0	$X_4\ Y_2$	1	1	0	1	0	0	$X_4\ Y_6$
0	1	0	1	0	1	$X_5\ Y_2$	1	1	0	1	0	1	$X_5\ Y_6$
0	1	0	1	1	0	$X_6\ Y_2$	1	1	0	1	1	0	$X_6\ Y_6$
0	1	0	1	1	1	$X_7\ Y_2$	1	1	0	1	1	1	$X_7\ Y_6$
0	1	1	0	0	0	$X_0\ Y_3$	1	1	1	0	0	0	$X_0\ Y_7$
0	1	1	0	0	1	$X_1\ Y_3$	1	1	1	0	0	1	$X_1\ Y_7$
0	1	1	0	1	0	$X_2\ Y_3$	1	1	1	0	1	0	$X_2\ Y_7$
0	1	1	0	1	1	$X_3\ Y_3$	1	1	1	0	1	1	$X_3\ Y_7$
0	1	1	1	0	0	$X_4\ Y_3$	1	1	1	1	0	0	$X_4\ Y_7$
0	1	1	1	0	1	$X_5\ Y_3$	1	1	1	1	0	1	$X_5\ Y_7$
0	1	1	1	1	0	$X_6\ Y_3$	1	1	1	1	1	0	$X_6\ Y_7$
0	1	1	1	1	1	$X_7\ Y_3$	1	1	1	1	1	1	$X_7\ Y_7$

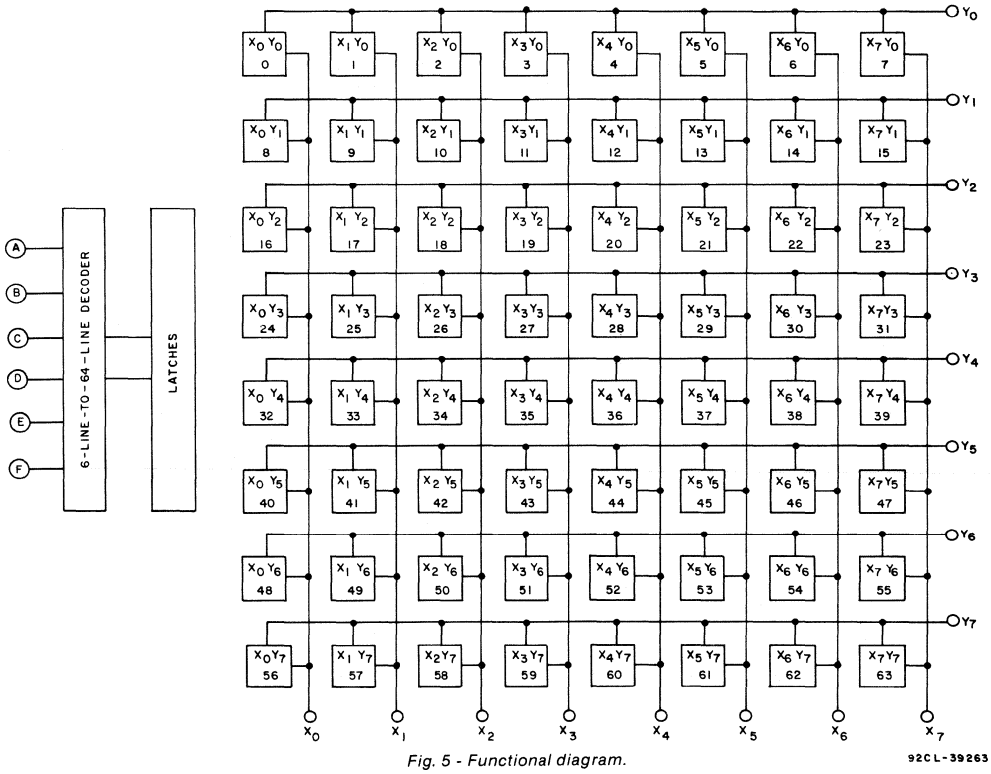


Fig. 5 - Functional diagram.

CD54/74HC22106, CD54/74HCT22106

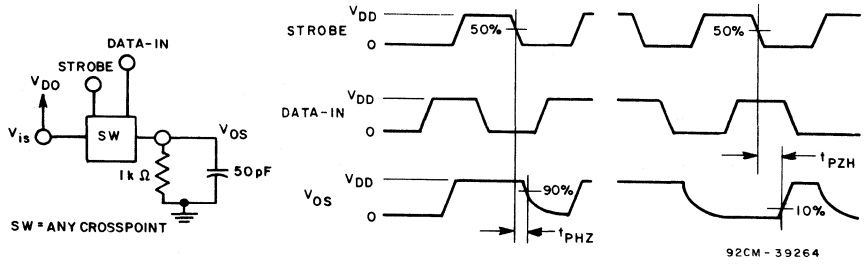


Fig. 6 - Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

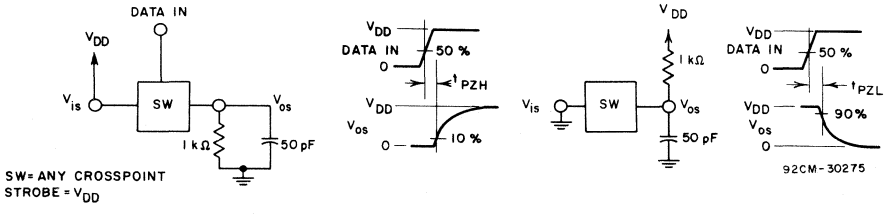


Fig. 7 - Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

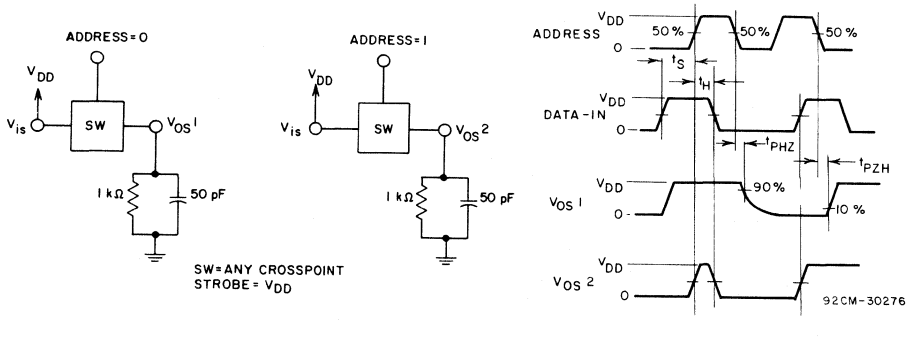


Fig. 8 - Propagation delay time test circuit and waveforms (address signal output, switch Turn-ON or Turn-OFF).

CD54/74HC22106, CD54/74HCT22106

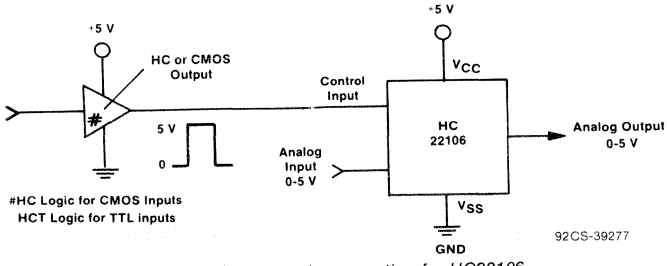


Fig. 9 - Typical single-supply connection for HC22106.

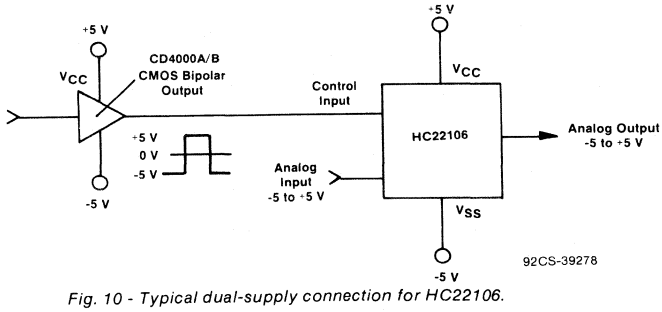


Fig. 10 - Typical dual-supply connection for HC22106.

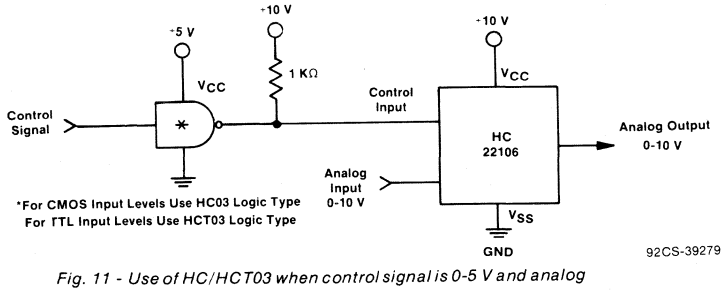


Fig. 11 - Use of HC/HCT03 when control signal is 0-5 V and analog signal is 0-10 V.

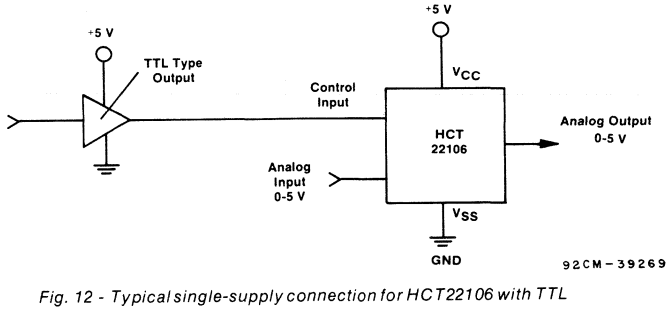


Fig. 12 - Typical single-supply connection for HCT22106 with TTL input.

Interface Circuits

Interface Circuits — Technical Data

Interface Circuits (Cont'd)

Type No.	Description	Page No.
Quad Analog Switches		
CD4016	Quad Bilateral Switch	—
CD54/74HC/HCT4016	High Speed, Low R_{ON} Version of the CD4016B	—
CD4066B	Improved Linearity Version of CD4016B	—
CD54/74HC/HCT4066	High Speed, Low R_{ON} Version of CD4066B	—
CD54/74HC/HCT4316	Quad Bilateral Switch	—
Analog Multiplexers/Demultiplexers		
CD4051B	Single 8 Channel	—
CD54/74HC/HCT4051	High Speed, Low R_{ON} Version of CD4051B	—
CD54/74HC/HCT4351	Similar to HC/HCT4051 with Latch	—
CD4052B	Differential 4 Channel	—
CD54/74HC/HCT4052	High Speed, Low R_{ON} Version of CD4052B	—
CD54/74HC/HCT4352	Similar to HC/HCT4051 with Latch	—
CD4053B	Triple 2 Channel	—
CD54/74HC/HCT4053	High Speed, Low R_{ON} Version of CD4053B	—
CD54/74HC/HCT4353	Similar to HC/HCT4053 with Latch	—
CD4067B	Single 16 Channel	—
CD4097B	Differential 8 Channel	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290,* QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices.*

CA570

Product Preview

2-Channel Floppy Disk Read/Write Circuit

Features:

- *Single chip read/write amplifier and read data processing function*
- *Compatible with 8—, 5¼—, and 3½—inch drives*
- *Internal write and erase current sources, externally set*
- *Internal center tap voltage source*
- *Control signals are TTL compatible*
- *Schmitt trigger inputs for higher noise immunity on bussed control signals*
- *TTL selectable write current boost*
- *Operates on +12 volt and +5 volt power supplies*
- *High gain, low noise, low peak shift (0.3% typ) read processing circuits*

The RCA-CA570E is an integrated circuit which performs the functions of generating write signals and amplifying and processing read signals required for a double sided floppy disk drive. The write data circuitry includes switching differential current drivers and erase head drive with programmable delay and hold times.

Applications:

- *Single channel floppy disk drive read/write controller*
- *Dual channel floppy disk drive read/write controller*

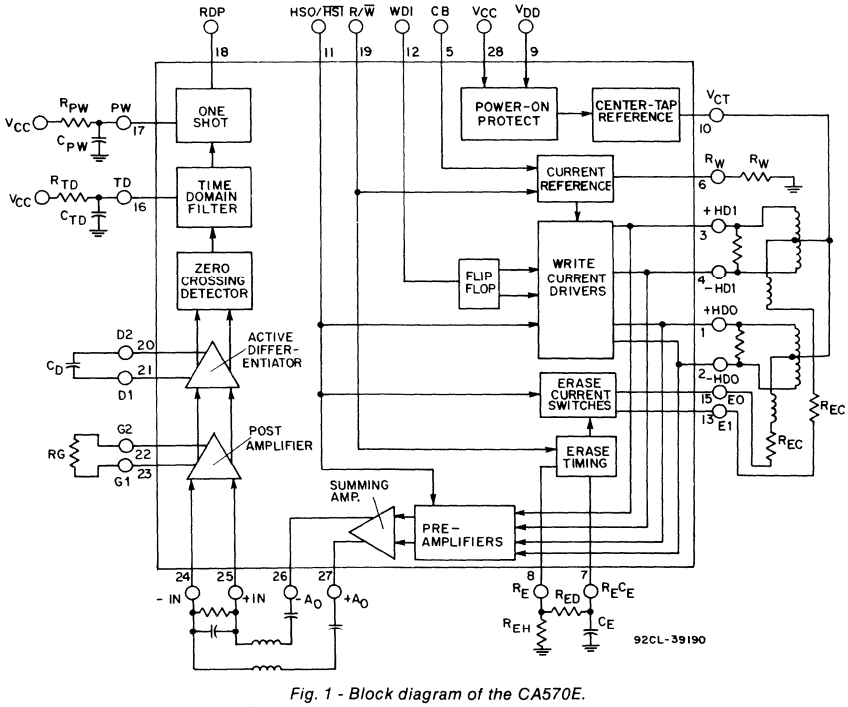


Fig. 1 - Block diagram of the CA570E.

File Number **1706**

The read data circuitry includes low noise amplifiers for each channel as well as a programmable gain stage and necessary equalization and filtering capability using external passive components. All logic inputs and outputs are TTL compatible and all timing is externally programmable for maximum design flexibility. The circuit operates on +12 volt and +5 volt power supplies and has an operating temperature range of 0° C to 70° C.

The CA570E is available in a 28-lead dual-in-line plastic package (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE, V_{CC} (5 V SUPPLY VOLTAGE) ..... 7 V
DC SUPPLY VOLTAGE, V_{DD} (12 V SUPPLY VOLTAGE) ..... 14 V
LOGIC INPUT VOLTAGE ..... -0.5 V_{DC} to 7 V_{DC}
POWER DISSIPATION ..... 800 mW
STORAGE TEMPERATURE ..... -65° C to +130° C
AMBIENT OPERATING TEMPERATURE ..... 0° C to +70° C
JUNCTION OPERATING TEMPERATURE ..... 0° C to +130° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 260° C

CIRCUIT OPERATION

Write Mode Circuitry

In Write Mode (R/$\overline{W}$ low), the circuit provides controlled write and erase currents to either of two magnetic heads. The Write-Erase circuitry consists of two differential Write Current Drivers, a Center Tap Voltage Reference, two Erase Current Switches and control circuits for head selection and erase timing.

Write current is toggled between opposing sides of the head on each negative transition of the Write Data Input (WDI) and is set externally by a single resistor, R_W, connected between the R_W terminal and ground. Since driver output impedance is large, proper damping resistors must be provided across each head. A signal at the CB terminal provides write current boost.

Erase current is also set externally through resistors R_{EC} connected in series with each erase coil. Erase can be activated by, but delayed from, selection of the write mode, and is held active after mode deselection. The turn-on delay is determined by the charging of C_E through R_{ED}, while the hold time is determined by the discharge of C_E through the series combination of R_{ED} and R_{EH} (see connection diagram). The R_EC_E mode may be driven directly by a logic gate, with external resistors per fig. 4, if the erase period is to be controlled separately from the write mode selection. For applications where no delays are required, C_E is omitted.

The Center Tap Voltage Reference supplies both write and erase currents. A Power Turn-On protection circuit prevents undesired writing or erasure by holding the voltage reference off until the supply voltages are within their operating ranges.

Read Mode Circuitry

In the Read Mode (R/$\overline{W}$ high), the circuit performs the functions of amplifying and detecting the selected head output pulses which correspond to magnetic transitions in the media. The Read circuitry consists of two differential Preamplifiers, a Summing Amplifier, a Postamplifier, an Active Differentiator, a Zero-Crossing Detector, a Time Domain Filter, and an Output One-Shot.

The selected Preamplifier drives the Summing Amplifier whose outputs are AC coupled to the Postamplifier through an external filter network. The Postamplifier adjusts signal amplitudes prior to application of signals to the Active Differentiator. Postamplifier gain is set as requirecd by connecting a resistor across the gain terminals, G1 and G2. If desired, an additional frequency/phase compensation network may also be connected across these gain terminals.

The Differentiator, driven by the Postamplifier, provides zero-crossing output voltages in response to input signal peaks. Differentiator response characteristics are set by an external capacitor or more complex series network connected between the D1 and D2 terminals.

The Zero-Crossing Detector provides a unipolar output for each positive or negative zero-crossing of the Differentiator output. To enhance signal peak detection, the Time Domain Filter inhibits the detection of zero-crossings if they are not sufficiently separated in time. The filter period is set by an external RC network connected to the TD pin.

The Time Domain Filter drives the output One-Shot which generates uniform output data pulses. The pulse width is set by an external RC network connected to the PW pin. The Output One-Shot is inhibited while in the Write Mode.

CA570

ELECTRICAL CHARACTERISTICS, Unless Otherwise Specified, 4.75 V ≤ V_{CC} ≤ 5.25 V; 11.4 V ≤ V_{DD} ≤ 12.6 V; 0°C ≤ T_A ≤ 70°C; R_W = 430 Ω; R_{ED} = 62 kΩ; C_E = 0.012 μF; R_{EH} = 62 kΩ; R_{EC} = 220Ω

POWER SUPPLY

CHARACTERISTIC	TEST CONDITIONS	MIN.	MAX.	UNITS
POWER SUPPLY CURRENTS				
I_{CC}—5-V Supply Current	Read Mode	—	35	mA
	Write Mode	—	38	
I_{DD}—12-V Supply Current	Read Mode	—	26	
	Write Mode (excluding Write & Erase currents)	—	24	
LOGIC SIGNALS - READ/$\overline{\text{WRITE}}$ (R/$\overline{\text{W}}$), CURRENT BOOST (CB)				
Input Low Voltage (V_{IL})		—	0.8	V
Input Low Current (I_{IL})	V_{IL} = 0.4 V	—	-0.4	mA
Input High Voltage (V_{IH})		2	—	V
Input High Current (I_{IH})	V_{IH} = 2.4 V	—	20	μA
LOGIC SIGNALS - WRITE DATA INPUT (WDI), HEAD SELECT (HS0/$\overline{\text{HS1}}$)				
Threshold Voltage, V_T^+ Positive-going		1.4	1.9	V
Threshold Voltage, V_T^- Negative-going		0.6	1.1	V
Hysteresis, V_T^+ to V_T^-		0.4	—	V
Input High Current, I_{IH}	V_{IH} = 2.4 V	—	20	μA
Input Low Current, I_{IL}	V_{IL} = 0.4 V	—	-0.4	mA
CENTER TAP VOLTAGE REFERENCE				
Output Voltage (V_{CT})	I_{WC} + I_E = 3 mA to 60 mA	V_{DD}-1.5	V_{DD}-0.5	V
V_{CC} Turn-Off Threshold	(See Note 1)	4	—	
V_{DD} Turn-Off Threshold	(See Note 1)	9.6	—	
V_{CT} Disabled Voltage		—	1	
ERASE OUTPUTS (E1, E0)				
Unselected Head Leakage	V_{E0}, V_{E1} = 12.6 V	—	100	μA
Output on Voltage (V_{E1}, V_{E0})	I_E = 50 mA	—	0.5	V
WRITE CURRENT				
Unselected Head Leakage	V_{E1}, V_{E0} = 12.6 V	—	25	μA
Write Current Range	R_W = 820 Ω to 180 Ω	3	10	mA
Current Reference Accuracy	I_{WC} = 2.3/R_W V_{CB} (current boost) = 0.5 V	-5	+5	%
Write Current Unbalance	I_{WC} = 3 mA to 10 mA	—	1	%
Differential Head Voltage Swing	Δ I_{WC} ≤ 5%	12.8	—	V_{peak}
Current Boost	V_{CB} = 2.4 V	1.25 I_{WC}	1.35 I_{WC}	—
ERASE TIMING				
Erase Delay Range	R_{ED} = 39 kΩ to 82 kΩ; C_E = 0.0015 μF to 0.043 μF	0.1	1	ms
Erase Delay Accuracy $\frac{\Delta T_{ED}}{T_{ED}} \times 100\%$	T_{ED} = 0.69 R_{ED} C_E R_{ED} = 39 kΩ to 82 kΩ; C_E = 0.0015 μF to 0.043 μF	-15	+15	%
Erase Hold Range	R_{EH} + R_{ED} = 78 kΩ to 164 kΩ; C_E = 0.0015 μF to 0.043 μF	0.2	2	ms
Erase Hold Accuracy $\frac{\Delta T_{EH}}{T_{EH}} \times 100\%$	T_{EH} = 0.69 (R_{EH} + R_{ED}) C_E R_{EH} + R_{ED} = 78 kΩ to 164 kΩ; C_E = 0.0015 μF to 0.043 μF	-15	+15	%

CA570

ELECTRICAL CHARACTERISTICS, Unless Otherwise Specified: V_{IN} (Preamplifier) = 10mVp-p sine wave, dc coupled to center tap. (See Figure 2). Summing Amplifier Load = 2 kΩ line-line, ac coupled. V_{IN} **(Postamplifier)** = 0.2 Vp-p sine wave, ac coupled; R_G = **open; Data Pulse Load = 1 kΩ to V_{CC}; C_D = 240 pF; C_{TD} = 100 pF; R_{TD} = 7.5 kΩ; C_{PW} = 47 pF; R_{PW} = 7.5 kΩ.**

READ MODE

CHARACTERISTIC	TEST CONDITIONS	MIN.	MAX.	UNITS
PREAMPLIFIER - SUMMING AMPLIFIER				
Differential Voltage Gain	Freq. = 250 kHz	85	115	V/V
Bandwidth (-3 dB)		3	—	MHz
Gain Flatness	Freq. = dc to 1.5 MHz	—	±1	dB
Differential Input Impedance	Freq. = 250 kHz	20	—	kΩ
Max. Differential Output Voltage Swing	V_{IN} = 250 kHz sine wave, THD ≤ 5%	2.5	—	V_{p-p}
Small-Signal Differential Output Resistance	$I_O \leq 1\ mA_{p-p}$	—	75	Ω
Common Mode Rejection Ratio	V_{IN} = 300 mV_{p-p} @ 500 kHz. Inputs shorted	50	—	dB
Power Supply Rejection Ratio	ΔV_{DD} = 300 mV_{p-p} @ 500 kHz Inputs shorted to V_{CT}	50	—	dB
Channel Isolation	Unselected Channel V_{IN} = 100 mV_{p-p} @ 500 kHz Selected channel input connected to V_{CT}	40	—	dB
Equivalent Input Noise	Power BW = 10 kHz to 1 MHz Inputs shorted to V_{CT}	—	10	μV rms
Center Tap Voltage, V_{CT}		1.5 (typ.)		V
POSTAMPLIFIER - ACTIVE DIFFERENTIATOR				
A_O, Differential Voltage Gain +IN, -IN to D1, D2	Freq. = 250 kHz (See Fig. 3)	8.5	11.5	V/V
Bandwidth (-3 dB) +IN, -IN to D1, D2	C_D = 0.1 μF, R_D = 2.5 kΩ	3	—	MHz
Gain Flatness +IN, -IN to D1, D2	Freq. = dc to 1.5 MHz C_D = 0.1 μF, R_D = 2.5 kΩ	—	±1	dB
Max. Differential Output Voltage Swing	V_{IN} = 250 kHz sine wave, ac coupled. ≤ 5% THD in voltage across C_D. (See Fig. 3)	5	—	V_{p-p}
Max. Differental Input Voltage	V_{IN} = 250 kHz sine wave, ac coupled. ≤ 5% THD in voltage across C_D. R_G = 1.5 kΩ	2.5	—	V_{p-p}
Differential Input Impedance		10	—	kΩ
Gain Control Accuracy $\frac{\Delta A_R}{A_R} \times 100\%$	$A_R = A_O R_G/(8 \times 10^3 + R_G)$ R_G = 2 kΩ	-25	+25	%
Threshold Differential Input (See Note 2)	Min. differential input voltage at post amp that results in a change of state at RDP V_{IN} = 250 kHz square wave, C_D = 0.1 μF, R_D = 500 Ω, $t_r, t_f \leq 0.2\ \mu s$ No overshoot; Data Pulse from each V_{IN} transition. (See Fig. 4)	—	3.7	mV_{p-p}
Peak Differentiator Network Current		1	—	mA
TIME DOMAIN FILTER				
Delay Accuracy $\frac{\Delta T_{TD}}{T_{TD}} \times 100\%$	$T_{TD} = 0.58\ R_{TD} \times (C_{TD} + 10^{-11}) + 50$ ns R_{TD} = 5 kΩ to 10 kΩ, $C_{TD} \geq 56$ pF V_{IN} = 50 mV_{p-p} @ 250 kHz square wave, $t_r, t_f \leq 20$ ns, ac coupled. Delay measured from 50% input amplitude to 1.5 V Data Pulse	-15	+15	%
Delay Range	$T_{TD} = 0.58\ R_{TD} \times (C_{TD} + 10^{-11}) + 50$ ns R_{TD} = 5 kΩ to 10 kΩ C_{TD} = 56 pF to 240 pF	240	2370	ns

CA570

ELECTRICAL CHARACTERISTICS (Continued)

CHARACTERISTIC	TEST CONDITIONS	MIN.	MAX.	UNITS
DATA PULSE				
Width Accuracy $\frac{\Delta T_{PW}}{T_{PW}} \times 100\%$	$T_{PW} = 0.58\ R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20$ ns R_{PW} = 5 kΩ to 10 kΩ $C_{PW} = \geq 36$ pF width measured at 1.5 V amplitudes	-20	+20	%
Active Level Output Voltage	I_{OH} = 400 μA	2.7	—	V
Inactive Level Output Leakage	I_{OL} = 4 mA	—	0.5	V
Pulse Width	$T_{PW} = 0.58\ R_{PW} \times (C_{PW} + 8 \times 10^{-12}) + 20$ ns R_{PW} = 5 kΩ to 10 kΩ C_{PW} = 36 pF to 200 pF	145	1225	ns

NOTES:
1. Voltage below which center tap voltage reference is disabled.
2. Threshold Differential Input Voltage can be related to peak shift by the following formula:

$$\text{Peak Shift} = \frac{3.7\ \text{mV}}{\pi V_{in}} \times 100\%$$

where V_{in} = peak-to-peak input voltage at post amplifier.
Note that this formula demonstrates an inverse relationship between the input amplitude and the Peak Shift.

TEST SCHEMATICS

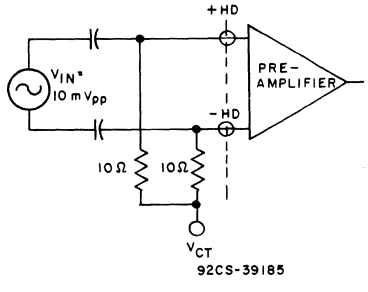


Fig. 2 - Preamplifier characteristics.

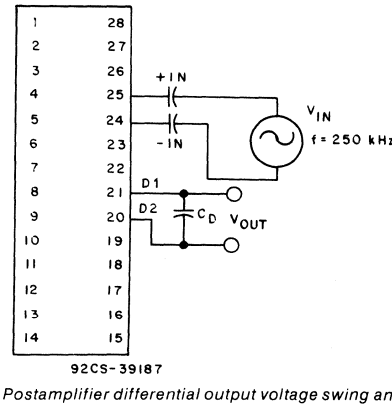


Fig. 3 - Postamplifier differential output voltage swing and voltage gain.

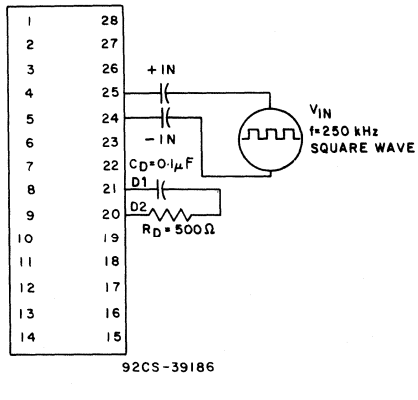


Fig. 4 - Postamplifier threshold differential input voltage.

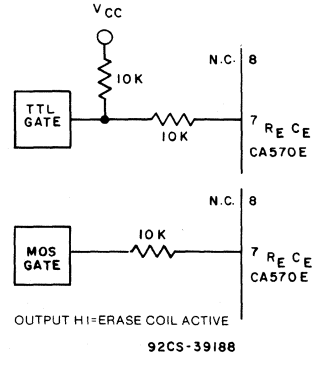


Fig. 5 - External erase control connections.

Product Preview

CA575

4-Channel Floppy Disk

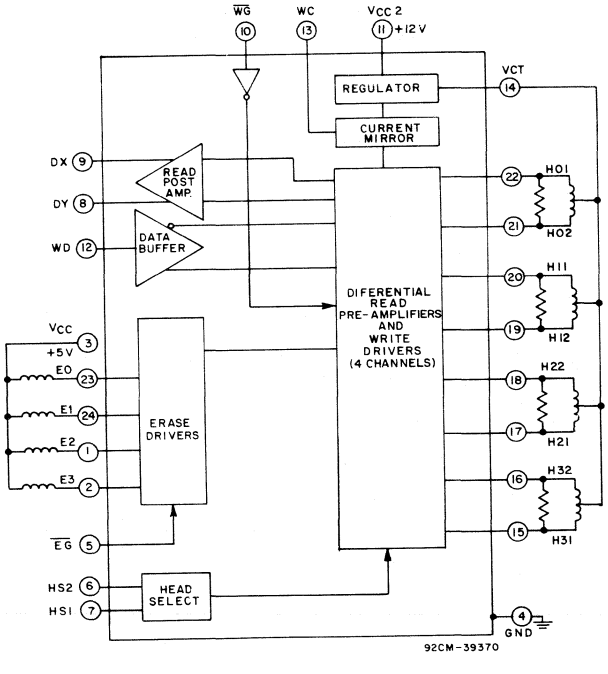
Read/Write Amplifier

Features:

- *Operates on +5 V, +12 V power supplies*
- *Four-channel capability*
- *TTL-compatible control inputs*
- *Read/Write functions on one chip*
- *Internal center-tap voltage source*
- *Supports all disk sizes*
- *Applicable to tape systems*

The CA575 device is a bipolar monolithic integrated circuit used in floppy disc systems for head control and write, erase, and read select functions. The device has four discrete read, write, and erase channels. Channel inputs are TTL compatible. The CA575 device requires +5 V and +12 V power supplies and has an operating range of 0° C to 70° C.

The CA575 is available in a 24-lead dual-in-line plastic package (E suffix).



Block diagram of the CA575.

File Number **1729**

CA575

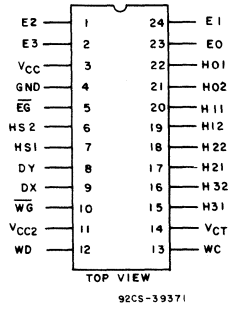
ABSOLUTE-MAXIMUM RATINGS*

DC SUPPLY VOLTAGE:
- V_{CC} ..... 6 V
- V_{CC2} ..... 14 V

WRITE CURRENT ..... 10 mA
HEAD PORT VOLTAGE ..... 18 V
DIGITAL INPUT VOLTAGES:
- DX, DY, HS2, HS1, WD ..... -0.3 to +10 V
- $\overline{EG}$, $\overline{WG}$ ..... -0.3 to V_{CC} +0.3 V

DX, DY OUTPUT CURRENT ..... -5 mA
VCT OUTPUT CURRENT ..... -10 mA
STORAGE-TEMPERATURE RANGE ..... -65 to +150°C
JUNCTION TEMPERATURE ..... 125°C
LEAD TEMPERATURE (10 sec solder) ..... 260°C

*Operation above these ratings may cause permanent damage to the device.



TERMINAL ASSIGNMENT

TERMINAL DESCRIPTIONS

PIN 1 PIN 2	E2 E3	Erase head driver connections.
PIN 3	V_{CC}	+5 V power-supply input.
PIN 4	GND	Ground.
PIN 5	EG	Erase gate: allows erasure by selected head.
PIN 6	HS2	Head select input - when high select head 2,
PIN 7	HS1	when low head 1 is selected.
PIN 8 PIN 9	DY DX	X, Y Read Data: Differential read signal out.
PIN 10	WG	Write gate: sets write mode operation.
PIN 11	V_{CC2}	+12 V power-supply input.
PIN 12	WD	Write data input for encoded data to be written to media.
PIN 13	WC	Write current: current mirror used to drive floppy disk heads - is set by connecting a resistor between this pin and V_{CC}.
PIN 14	VCT	Center tap voltage source.
PIN 15	H31	
PIN 16	H32	
PIN 17	H21	
PIN 18	H22	Appropriate head windings are attached to these ports. The first number is the port or
PIN 19	H12	head number, the second differentiates between the sides of the winding.
PIN 20	H11	
PIN 21	H02	
PIN 22	H01	
PIN 23 PIN 24	E0 E1	Erase head driver connections.

RECOMMENDED OPERATING CONDITIONS $0°C < T_A < 50°C$, $4.7\ V < V_{CC} < 5.3\ V$, $11\ V < V_{DD} < 13\ V$

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
V_{CC} Supply Current:					
Read Mode	V_{CC} Max.	—	—	15	mA
Write Mode		—	—	35	
Read Mode	V_{CC2} Max.	—	—	25	mA
Write Mode		—	—	15	
Write Current		—	5.5	—	mA
ERASE OUTPUT					
Erase On Voltage	IE = 80 mA	0.7	—	1.3	V dc
Erase Off Leakage		—	—	100	μA
LOGIC SIGNALS - HEAD SELECT (HS2, HS1) AND WRITE DATA (WD)					
Low-Level Voltage		-0.3	—	0.8	V dc
High-Level Voltage		2	—	6	V dc
Low-Level Current	V_{IN} = 0 volts	-1.6	—	—	mA
High-Level Current	V_{IN} = 2.7 volts	—	—	40	μA
LOGIC SIGNALS - WRITE GATE (WG) AND ERASE GATE (EG)					
Low-Level Voltage		-0.3	—	0.81	V dc
High-Level Input Current		-300	—	—	μA
Low-Level Current	V_{IN} = 0 volts	-2	—	—	mA
READ MODE					
Differential Gain	f = 100 kHz, V_{IN} = 5 mV rms, R_L = 10 kΩ	80	100	120	V/V
Bandwidth	V_{IN} = 5 mV rms, R_L = 10 kΩ, C_L = 15 pF	9	—	—	MHz
Input Voltage Range for 95% Linearity	f = 100 kHz, R_L = 10 kΩ	25	—	—	mV_{p-p}
Differential Input Resistance	f = 1 MHz	100	—	—	kΩ
Differential Input Capacitance	f = 1 MHz	—	—	10	pF
Input Bias Current		—	—	25	μA
Input Offset Voltage		—	—	12	mV
Output Voltage, Common Mode		—	8	—	V dc
Output Resistance		—	—	35	Ω
Output Current Sink		2	—	—	mA
Output Current Source		3	—	—	mA
Common-Mode Rejection Ratio	f = 1 MHz (input referred)	50	—	—	dB
Power-Supply Rejection Ratio	f = 1 MHz (input referred)	50	—	—	dB
Channel Separation	f = 1 MHz (input referred)	50	—	—	dB
Input Noise	BW = 100 Hz to 1 MHz, Z Source = 0	—	7	—	μV rms
WRITE MODE					
Write Current Gain	IW = 5.5 mA	0.97	—	1.05	A/A
Write Current Voltage Level	IW = 5.5 mA	1.2	—	2.1	V dc
Differential Head Voltage	IW = 5.5 mA	12.5	—	—	V dc
Unselected Head Current	IW = 5.5 mA, DC Condition	—	—	0.1	mA
Write Current Unbalance	IW = 5.5 mA	—	—	1	%
Write Current Time Symmetry	IW = 5.5 mA	—	—	±10	ns
Read Amplifier Output Level		—	10.5	—	V dc
Center-Tap Voltage (Read and Write Modes)		—	8.5	—	V dc
SWITCHING CHARACTERISTICS					
Write and Erase Gate Switching Delay	Delay to 90% of Write Current	—	—	1	s
Head Select Switching Delay		—	—	1	s
Head Current Switching Delay	T1 in Fig. 1	—	10	—	ns
Head Current Switching Time	IW = 5.5 mA Shorted Head	—	10	30	ns
Write-to-Read Recovery Time		—	—	2	s

CA575

Circuit Operation

The CA575 functions as a write and erase driver or as a read amplifier for the selected head. Two TTL-compatible inputs are decoded to select the desired read/write and erase heads. Both the erase gate ($\overline{EG}$) and write gate ($\overline{WG}$) lines have internal pull-up resistors to prevent an accidental write or erase condition.

Mode Selection

The read or write mode is determined by the write gate ($\overline{WG}$) line. The input is open collector TTL compatible. With the input low, the circuit is in the write mode. With the input high (open), the circuit is in the read mode. In the read mode, or with the +5 V supply off the circuit will not pass write current.

Erase

The erase operation is controlled by an open-collector TTL-compatible input. With erase gate ($\overline{EG}$) input high (open) or the +5 V supply off, the circuit will not pass erase current. With $\overline{EG}$ low, the selected open-collector erase output will be low and current will be pulled through the erase heads.

Read Mode

With the $\overline{WG}$ line high, the read mode is enabled. In the read mode the circuit functions as a differential amplifier. The state of the head-select input determines which amplifier is active. When the mode or head is switched, the read output will have a voltage level shift. External reactive elements must be allowed to recover before proper reading can commence. A current diverting circuit prevents any possible write current from appearing on a head line.

Write Mode

With the $\overline{WG}$ line low, externally generated write current is mirrored to the selected head and is switched between head windings by the state of the write data (WD) signal.

CA3081, CA3082

General-Purpose High-Current N-P-N Transistor Arrays

CA3081 — Common-Emitter Array
CA3082 — Common-Collector Array

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features:

- *7 transistors permit a wide range of applications in either a common-emitter [CA3081] or common-collector [CA3082] configuration*
- *High I_C: 100 mA max.*
- *Low V_{CE} sat (at 50 mA): 0.4 V typ.*

RCA-CA3081 and CA3082 consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, and light-emitting diode (LED) displays. These types are also well-suited for a variety of other drive applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design. Both types are also available in chip form.

Applications:

- *Drivers for:*
  - *Incandescent display devices*
  - *LED displays*
  - *Relay control*
  - *Thyristor firing*

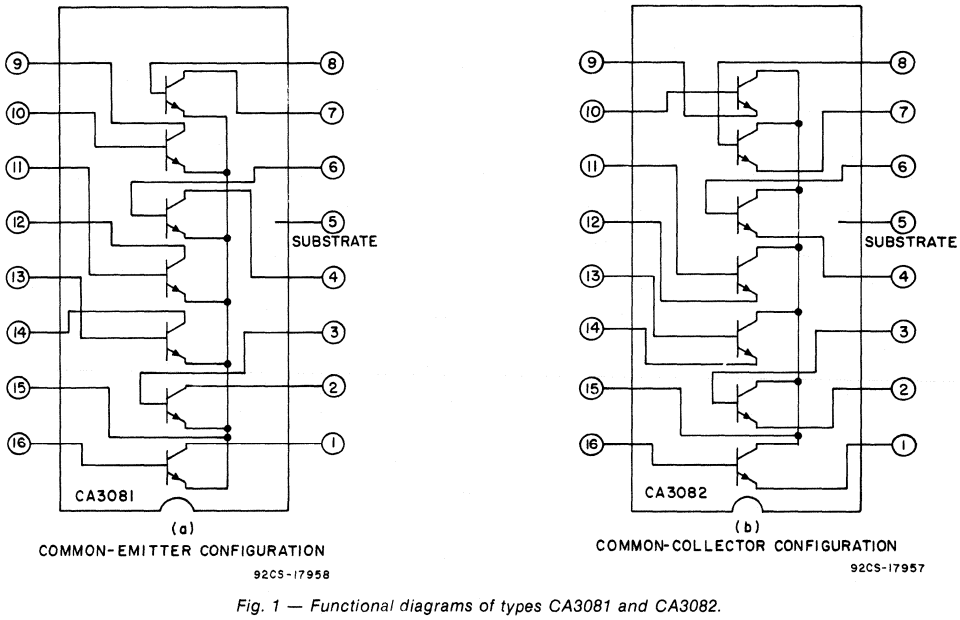


Fig. 1 — Functional diagrams of types CA3081 and CA3082.

File Number **480**

CA3081, CA3082

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to + 150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max. ..... 265 °C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

* The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

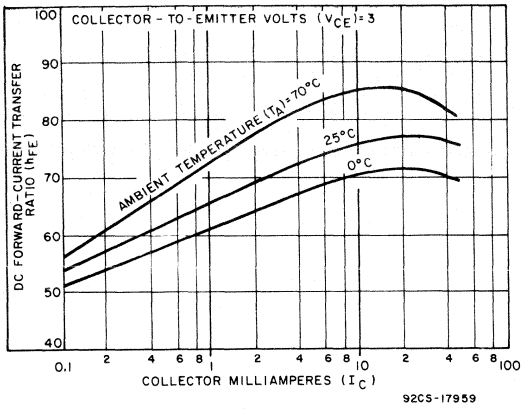


Fig.2–h_{FE} vs. I_C

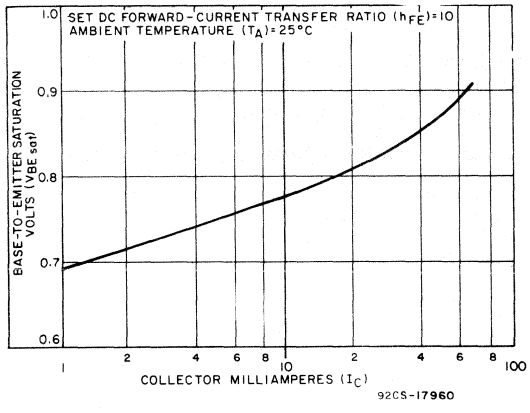


Fig.3–V_{BEsat} vs. I_C

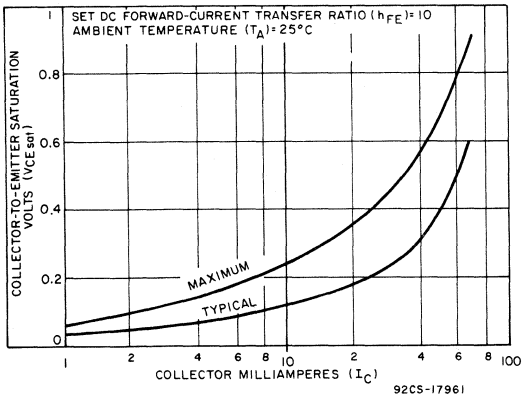


Fig.4–V_{CEsat} vs. I_C at T_A = 25°C.

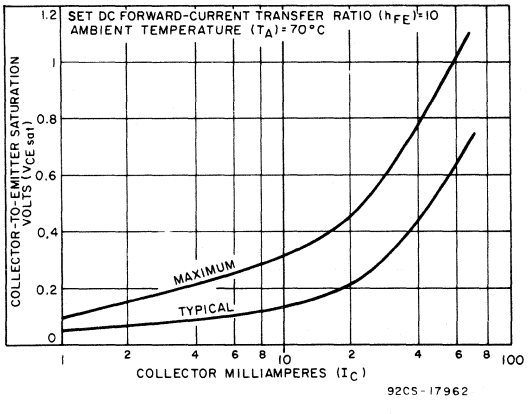


Fig.5–V_{CEsat} vs. I_C at T_A = 70°C.

TYPICAL READ-OUT DRIVER APPLICATIONS

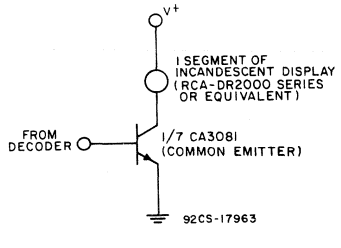
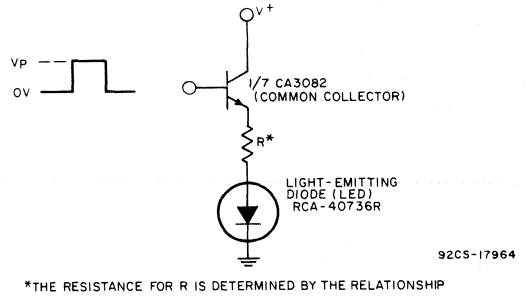


Fig.6–Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I\,(LED)}$$

$R = 0$ FOR $V_P = V_{BE} + V_F(LED)$

WHERE: V_P = INPUT PULSE VOLTAGE

V_F = FORWARD VOLTAGE DROP ACROSS THE DIODE

Fig.7–Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

CA3161

BCD-to-Seven-Segment Decoder/Driver

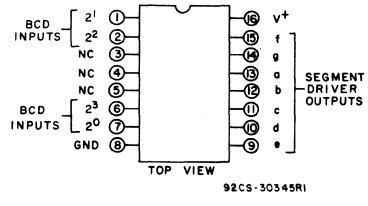
Features:

- *TTL-compatible input logic levels*
- *25-mA [typ.] constant-current segment outputs*
- *Eliminates need for output current-limiting resistors*
- *Pin compatible with other industry standard decoders*
- *Low standby power dissipation - 18 mW (typ.)*

The RCA-CA3161E is a monolithic intergrated circuit that performs the BCD-to-seven-segment decoding function and features constant-current segment drivers. When used with the CA3162E A/D Converter* the CA3161E provides a complete digital readout system with a minimum number of external parts.

The CA3161 is supplied in the 16-lead dual-in-line plastic package (E suffix). The CA3161 is also available in chip form (H suffix).

*The CA3162E is described in RCA data bulletin File No. 1080.



TERMINAL ASSIGNMENT
CA3161E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 1 and 10) ..... +7 V

INPUT VOLTAGE (terminals 1, 2, 6, 7) ..... +5.5 V

OUTPUT VOLTAGE:

Output "Off" ..... +7 V

Output "On" (See note 1) ..... +10 V

DEVICE DISSIPATION:

Up to T_A = +55°C ..... 1 W

Above T_A = +55°C ..... derate linearly at 10.5 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to +75°C

Storage ..... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

NOTE 1: This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst-case conditions. Example: All segments "on", 100% duty cycle.

File Number **1079**

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	H	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	—
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

CA3161

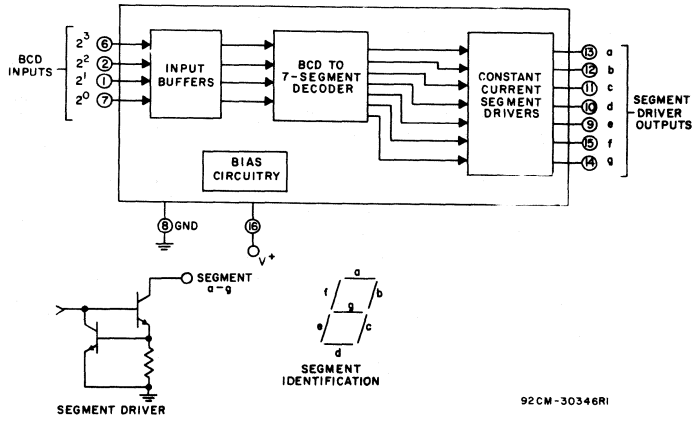
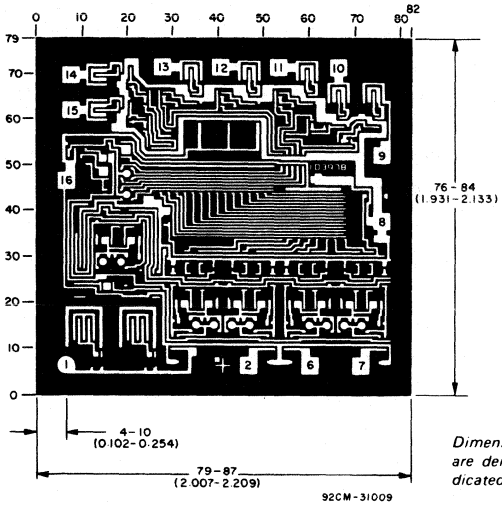


Fig. 1-Functional block diagram of the CA3161E.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage Operating Range, V^+		4.5	5	5.5	V
Supply Current, I^+ (all inputs high)		–	3.5	8	mA
Output Current Low ($V_O = 2$ V)		18	25	32	mA
Output Current High ($V_O = 5.5$ V)		–	–	250	μA
Input Voltage High (logic "1" level)		2	–	–	V
Input Voltage Low (logic "0" level)		–	–	0.8	V
Input Current High (logic "1")	2 V	–30	–	–	μA
Input Current Low (logic "0")	0 V	–40	–	–	μA
Propagation Delay Time	t_{PHL}	–	2.6	–	μs
	t_{PLH}	–	1.4	–	



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for the CA3161H.

CA3168

2-Digit BCD-to-7-Segment Decoder/Driver

For Common-Anode LED Displays

Features

- *Separate BCD inputs and segment outputs for each digit*
- *Input loading less than 15 μA*
- *I^2L logic with buffered inputs and outputs*
- *Internal input overrange protection circuit*
- *5-V supply operation*
- *Internal biasing circuits*
- *Output drive capability of 25 mA per segment*
- *Open collector outputs drive indicators directly*

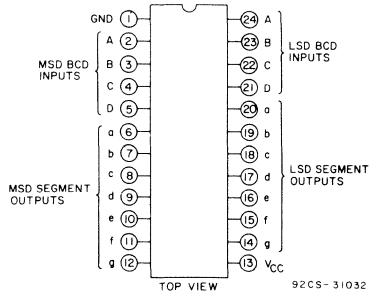
The RCA-CA3168E•is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications. It consists of two independent BCD-to-7-segment decoder/drivers. Two sets of BCD inputs are buffered with p-n-p differential amplifier stages internally referenced to 1.7 V. Each of the eight input terminals draws less than 15 μA and is provided with an internal protection circuit.

Decoding is accomplished with I^2L ROM's. The fourteen output terminals are buffered with Darlington pairs driving common-emitter output transistors. Each output is capable of sinking 25 mA for an LED common-anode display device. The supply-voltage range (V_{CC}) is intended to be 4.5 V to 6 V. The output voltage (V_O) must not exceed 12 V, which provides for a wide range of common-anode voltage sources.

The CA3168E is supplied in the 24-lead dual-in-line plastic package.

•Formerly RCA Dev. Type No. TA10337

CA3168E
TERMINAL ASSIGNMENT



MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE, V_{CC} ..... 6 V
INPUT-VOLTAGE (MIN./MAX.) ..... $-0.3/V_{CC}$ V
INPUT CURRENT (PROTECTION CIRCUIT) ..... ±10 mA
OUTPUT VOLTAGE, V_O ..... 12 V
OUTPUT SEGMENT CURRENT, $I_{DISPLAY}$ ..... 25 mA
AMBIENT TEMPERATURE RANGE:
  Operating ..... 0 to +70° C
  Storage ..... -55 to +150° C
POWER DISSIPATION:
  Up to +70° C ..... 400 mW
  Above +70° C ..... derate linearly at 8.7 mW/° C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for
  10 seconds max. ..... +265° C

File Number **1140**

TYPICAL ELECTRICAL CHARACTERISTICS at V_{CC} = 5 V, V_1 = GND, $V_{DISP.}$ = 12 V, and T_A = 25°C, See Fig. 2
Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Voltage High, V_{IH}		2.4	5	V_{CC}	V
Input Voltage Low, V_{IL}		0	–	0.6	V
Input Current High, I_{IH}	All BCD Inputs = 5 V	–	–	15	μA
Input Current Low, I_{IL}	All BCD inputs = 0 V	–10	–	–	μA
On-State Output Voltage, V_{OL}	$I_{O(Sink)}$ = 25 mA	–	–	1	V
Off-State Output Current, I_{OH}		–	5	50	μA
Power Supply Drain Current, I_{CC}	V_{CC} = 6 V	–	17	25	mA
Input Capacitance, C_I		–	5	–	pF

TRUTH TABLES

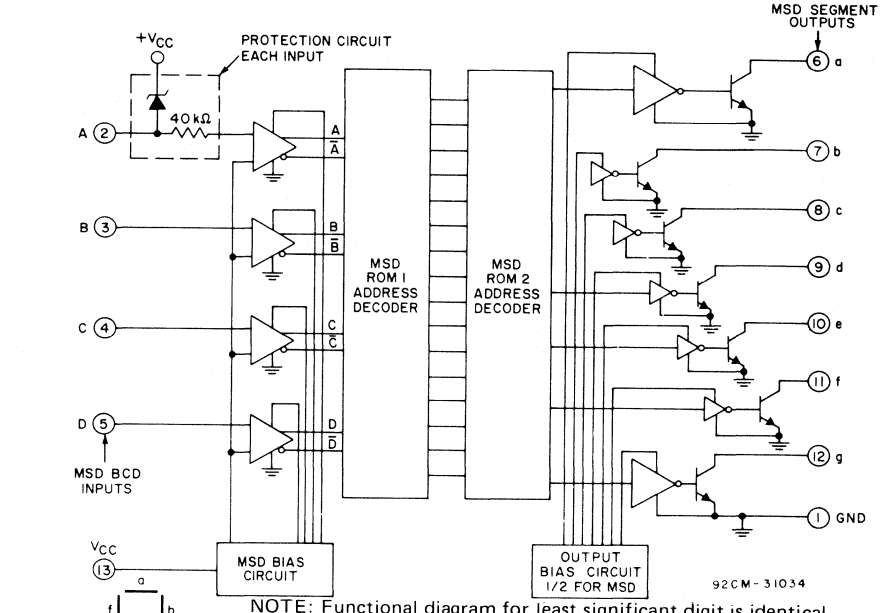
Most Significant Digit (MSD)

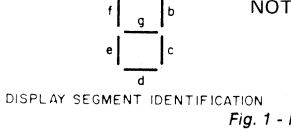
INPUTS				OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	0	1	1	0	0	0	1	C
1	0	1	1	0	0	0	1	0	0	0	A
1	1	0	0	0	0	1	1	0	0	0	P
1	1	0	1	0	1	1	0	0	0	0	E
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

Least Significant Digit (LSD)

INPUTS				OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	1	0	0	1	0	0	0	H
1	0	1	1	1	0	0	0	0	1	1	J
1	1	0	0	1	1	1	0	0	0	1	L
1	1	0	1	0	1	1	1	0	0	0	F
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

CA3168

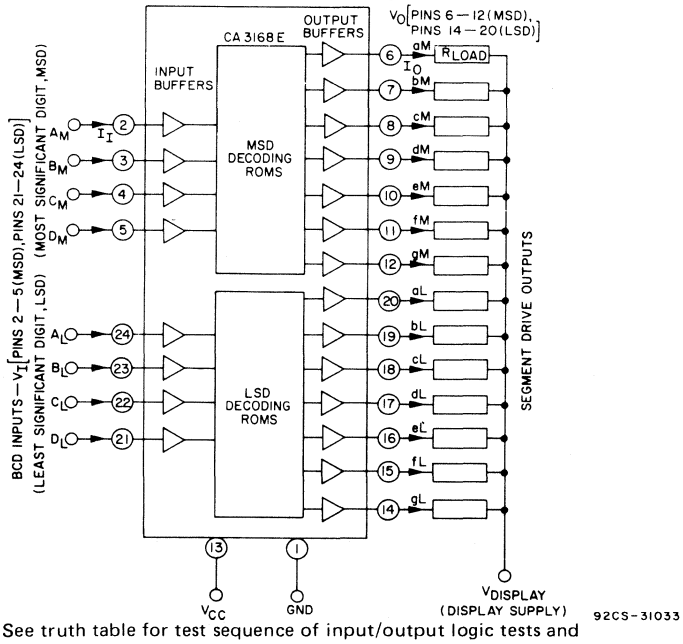




DISPLAY SEGMENT IDENTIFICATION

NOTE: Functional diagram for least significant digit is identical to functional diagram used for MSD with the exception of Terminal Assignments (see Terminal Assignment diagram). A separate LSD Bias circuit, and ½ of the Output Bias Circuit is used for LSD.

Fig. 1 - Functional diagram for Most Significant Digit (MSD).



NOTE: See truth table for test sequence of input/output logic tests and

Minimum $R_{LOAD} = \frac{V_{DISPLAY} - V_{OL}}{\text{Max. } I_{DISPLAY}}$ **for each of the 14 segment** drive output terminals. (LED is not used in test circuit)

Fig. 2 - Test circuit.

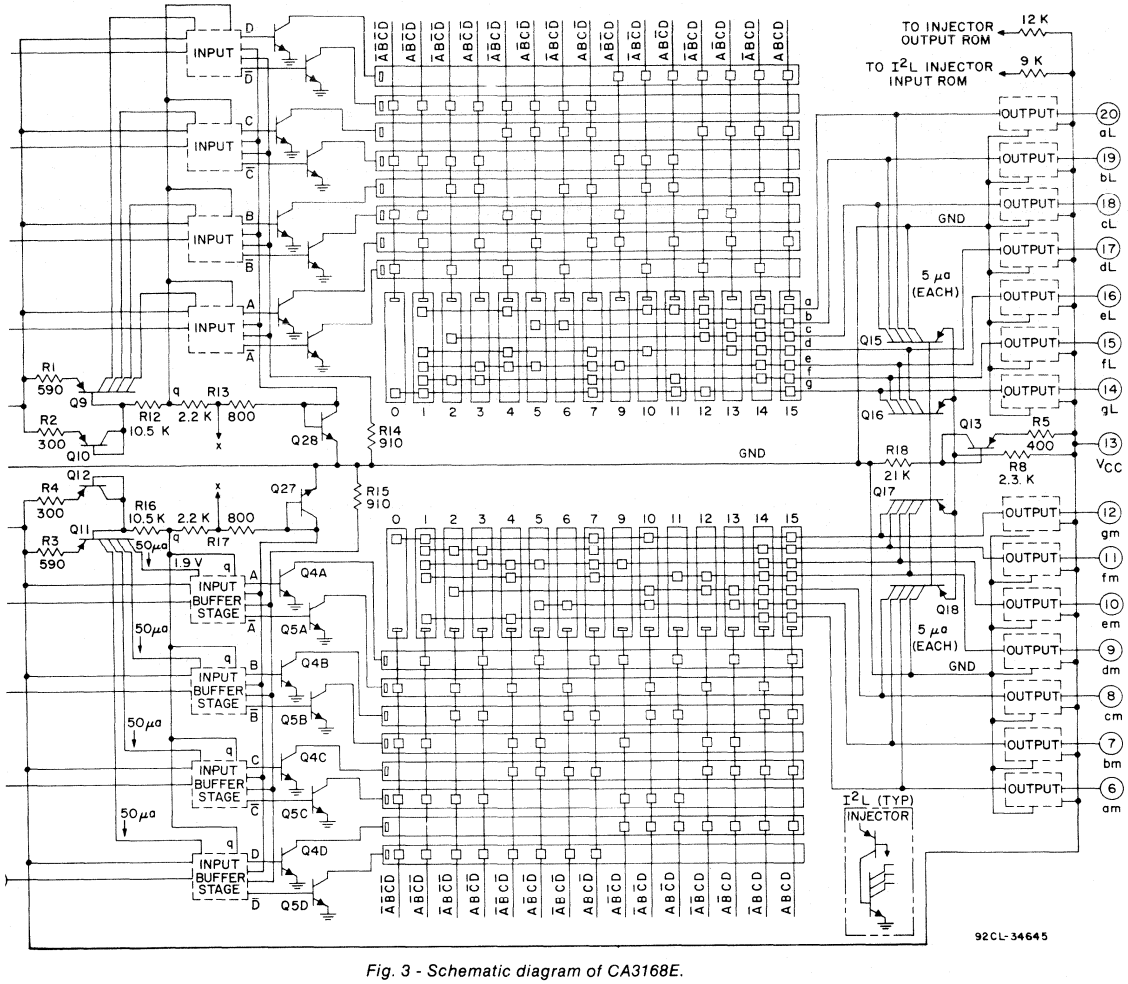


Fig. 3 - Schematic diagram of CA3168E.

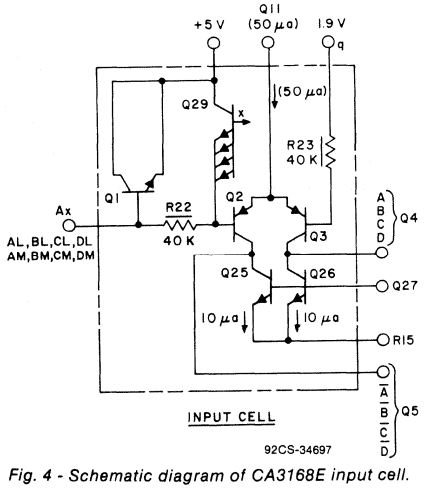


Fig. 4 - Schematic diagram of CA3168E input cell.

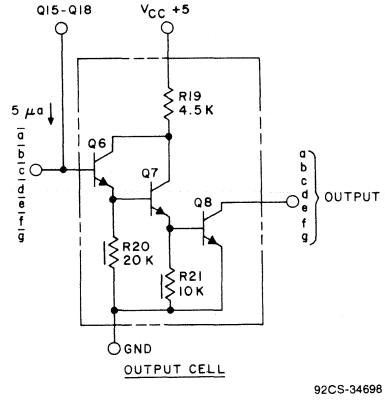


Fig. 5 - Schematic diagram of CA3168E output cell.

CA3207, CA3208

BiMOS Sequencer Driver and Segment Latch-Driver for Vacuum Fluorescent Displays

Features:
- *Serial input, parallel output*
- *Total of 14 outputs*
- *CMOS and T^2L compatible inputs*
- *Low-power CMOS Logic–Bipolar high-voltage output BiMOS process*
- *Use with vacuum fluorescent display*
- *Will operate in an output voltage range of 35 V to 55 V*

Sequencer Driver (CA3207E)
- *Sequentially turns on 1 of 14 characters (or 2 of 28 when used with 2 CA3208E's)*
- *Signal dimming through Gates 1 or 2*

Latch Driver (CA3208E)
- *Drives any combination of 14 outputs selected by DATA input*
- *Two or more devices may be interconnected by means of the CE and $\overline{CE}$ inputs to drive more than 14 characters*

The RCA-CA3207E and CA3208E★, sequence-driver and segment latch-driver, respectively, are used in combination to drive vacuum fluorescent display devices of up to 14 segments with up to 14 characters of display. The CA3207E selects the digit or character to be displayed in sequence and the CA3208E turns on the required number of segments of the character selected.

Each sequencer-driver will sequentially activate 14 characters. The sequencer-driver clock line may be used to drive the cross-coupled $\overline{CE}$ and CE inputs of 2 segment-latch drivers to provide for the display of up to 28 characters (see Fig. 12). The logic portion of both circuits use CMOS technology operating at 5 volts. The output drivers use bipolar technology and operate at supply voltages up to 55 volts. The CA3207E will source 40-mA per character and the CA3208E will source 7.5-mA per segment.

Both types are supplied in the 22-lead dual-in-line plastic package (E suffix), and they are also available in chip form (H suffix).

★Formerly Dev. Type No. TA10563 and TA10564, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:

V_{CC}, Pin 3 to GND, Pin 10 ..... 55 V

V_{DD}, Pin 4 to GND, Pin 10 ..... 6 V

DEVICE DISSIPATION:

Up to T_A=+85°C ..... 750 mW

Above T_A=+85°C ..... 13 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... -40 to +85°C

Storage ..... -55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... 265°C

File Number **132**

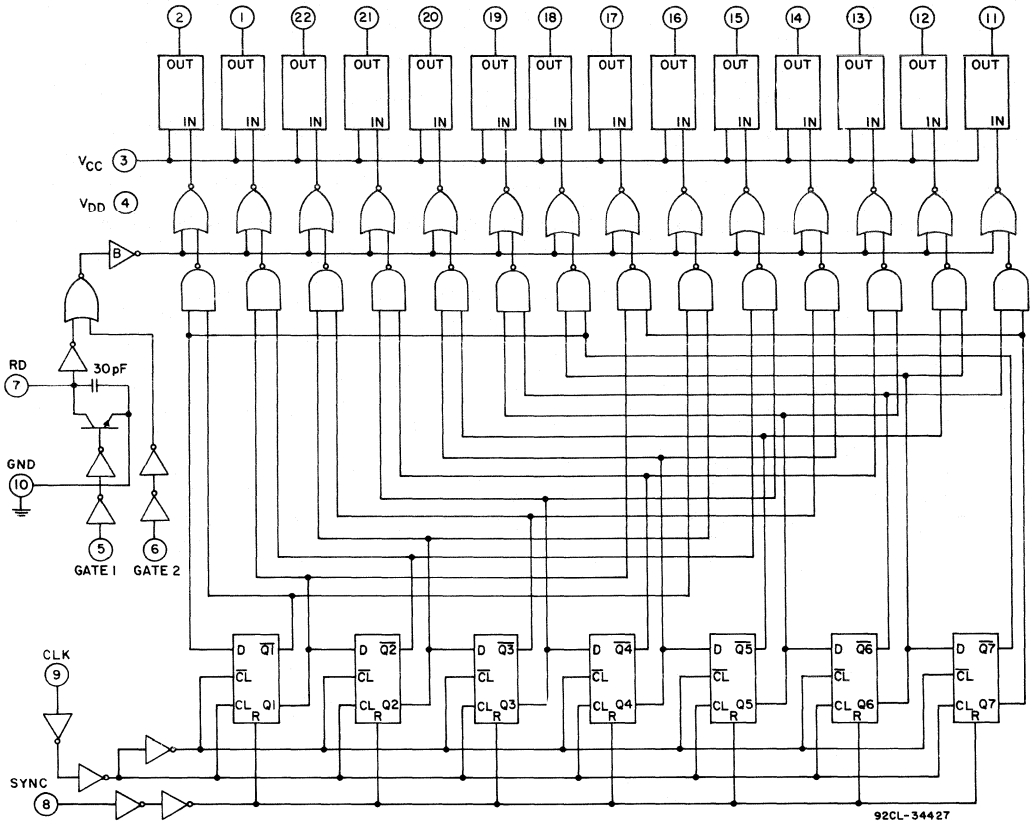
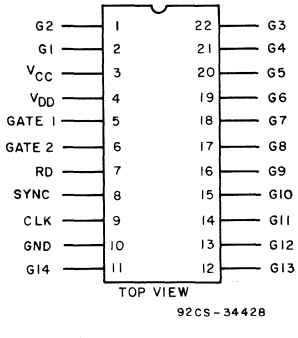


Fig. 1 – Sequencer-driver (CA3207E) logic diagram.



TERMINAL ASSIGNMENT
CA3207E

CA3207, CA3208

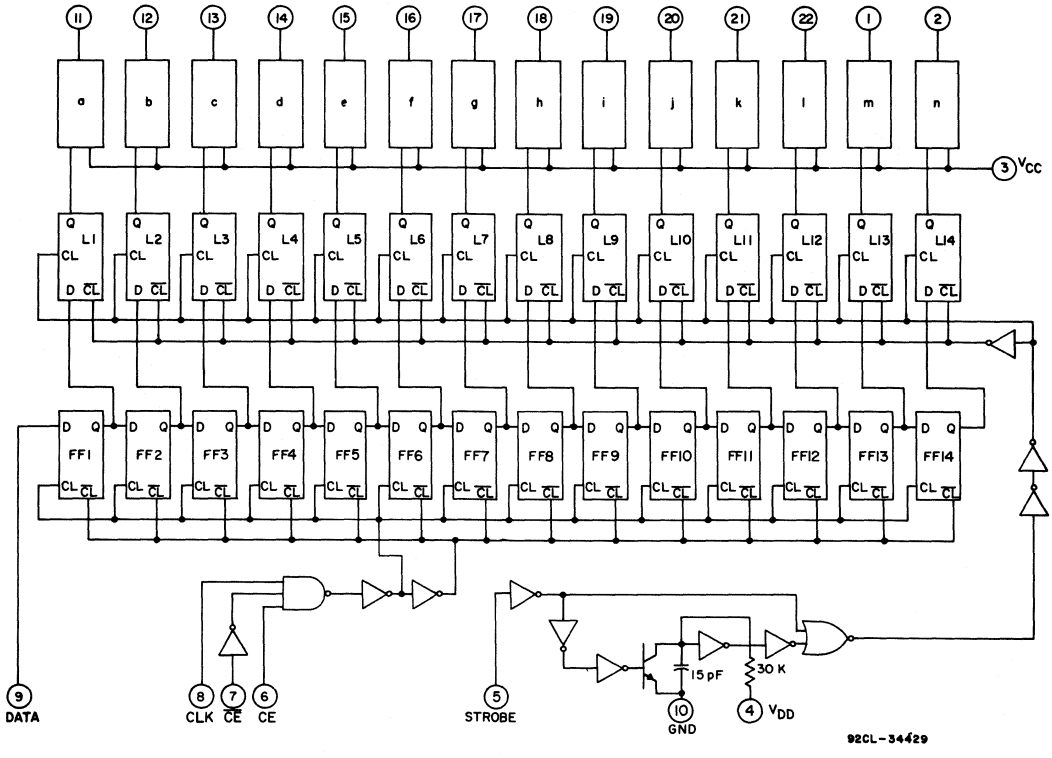
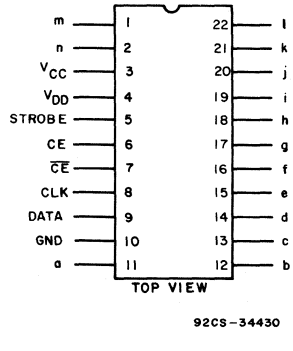


Fig. 2 - Segment-latch driver (CA3208E) logic diagram.

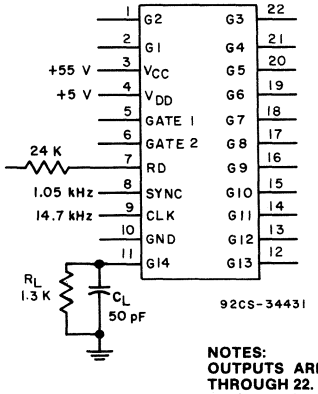


TERMINAL ASSIGNMENT
CA3208E

CA3207, CA3208

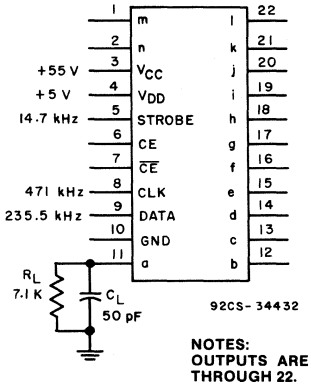
STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, See Fig. 3 and Fig. 4.

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			CA3207E		CA3208E		
			Min.	Max.	Min.	Max.	
V_{CC} Supply Current	I_{CC}	No outputs "ON"	—	10	—	—	mA
		Half outputs HIGH "ON"	—	—	—	65	
V_{DD} Supply Current	I_{DD}	All inputs HIGH	—	1	—	—	mA
		All inputs LOW	—	—	—	800	μA
		All inputs HIGH	—	—	—	1	
Input Current, Low-Level	I_{IL}	V_{IN}=0 V	—	1	—	1	μA
Input Current, High-Level	I_{IH}	V_{IN}=5 V	—	1	—	1	μA
Output Voltage, Low-Level	V_{OL}	R_L=1.3K	—	1	—	—	V
		R_L=7.1K	—	—	—	1	
Output Voltage, High-Level	V_{OH}	I_{OH}=40 mA	53	—	—	—	
		I_{OH}=7.5 mA	—	—	53	—	
Input Low Voltage	V_{IL}		—	1.5	—	1.5	V
Input High Voltage	V_{IH}		3.5	—	3.5	—	



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (1.3 K) AND C_L (50 pF) WHICH RESULTS IN A 40-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V and 5 V.

Fig. 3 - Sequencer-driver (CA3207E) test circuit.



NOTES:
OUTPUTS ARE PINS 1, 2 AND 11 THROUGH 22.
OUTPUT LOADS ARE R_L (7.1 K) AND C_L (50 pF) WHICH RESULTS IN A 7.5-mA LOAD CURRENT.
INPUT VOLTAGE LEVELS ARE 0 V AND 5 V.

Fig. 4 - Segment-latch driver (CA3208E) test circuit.

CA3207, CA3208

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L=50 pF, R_L=1.3K

CHARACTERISTIC		LIMITS CA3207E Min.	LIMITS CA3207E Max.	UNITS
Sequencer-Driver, See Fig. 5				
Sync Pulse Width	t_{SW}	2	—	μs
Time Delay Gate 1:				
Input-to-Output Inhibit	t_{GI}	—	1.5	μs
Input-to-Output Enable	t_{GE}	—	2.3	μs
Lead Time Sync to Gate	t_{SG}	0.5	—	
Lead Time Clock to Gate	t_{CG}	0.5	—	
Clock Frequency	f_{CL}	—	14	kHz

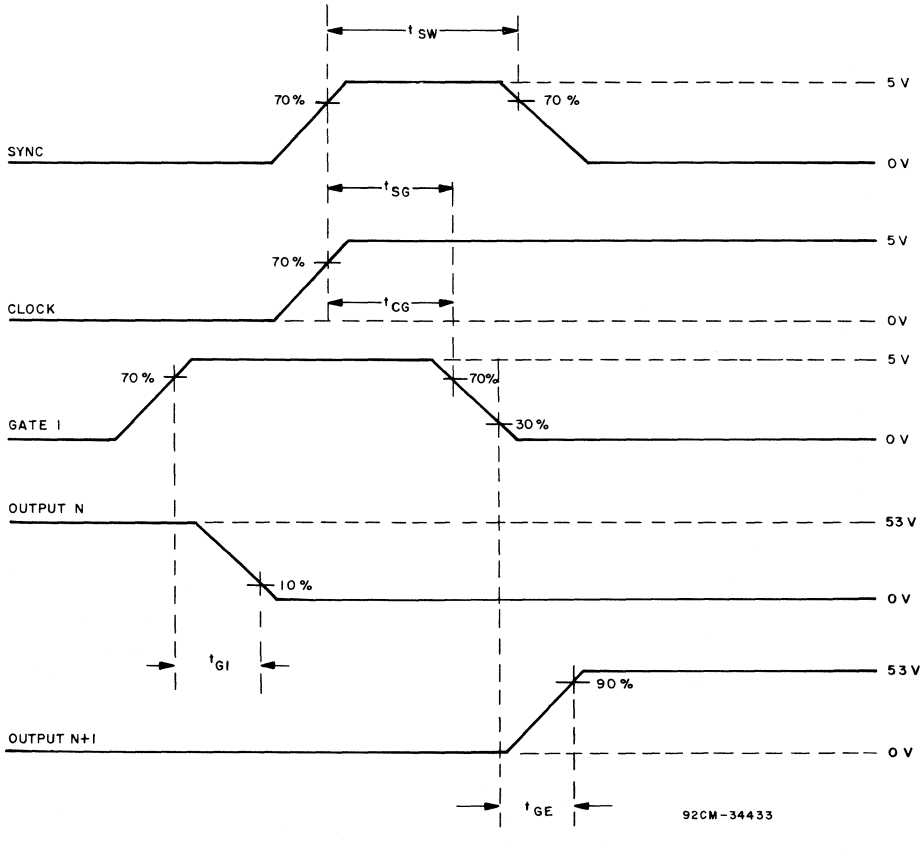


Fig. 5 - Sequencer-driver (CA3207E) timing waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=+55 V, V_{DD}=+5 V, C_L= 50 pF, R_L=7.1 K

CHARACTERISTIC		LIMITS CA3208E Min.	LIMITS CA3208E Max.	UNITS
Segment-Latch Driver, See Fig. 6				
Time Delay:				
Strobe to Output	t_{PLH}	0.4	1.8	μs
Strobe to Output	t_{PHL}	—	2.6	μs
CE or $\overline{CE}$ to Clock	t_{CE}	0.8	—	μs
Input Data Set-Up Time	t_{SU}	0.5	—	μs
Input Data Hold Time	t_H	0.5	—	μs
Clock Frequency	f_{CL}	—	448	kHz
Data Frequency	f_D	—	224	kHz

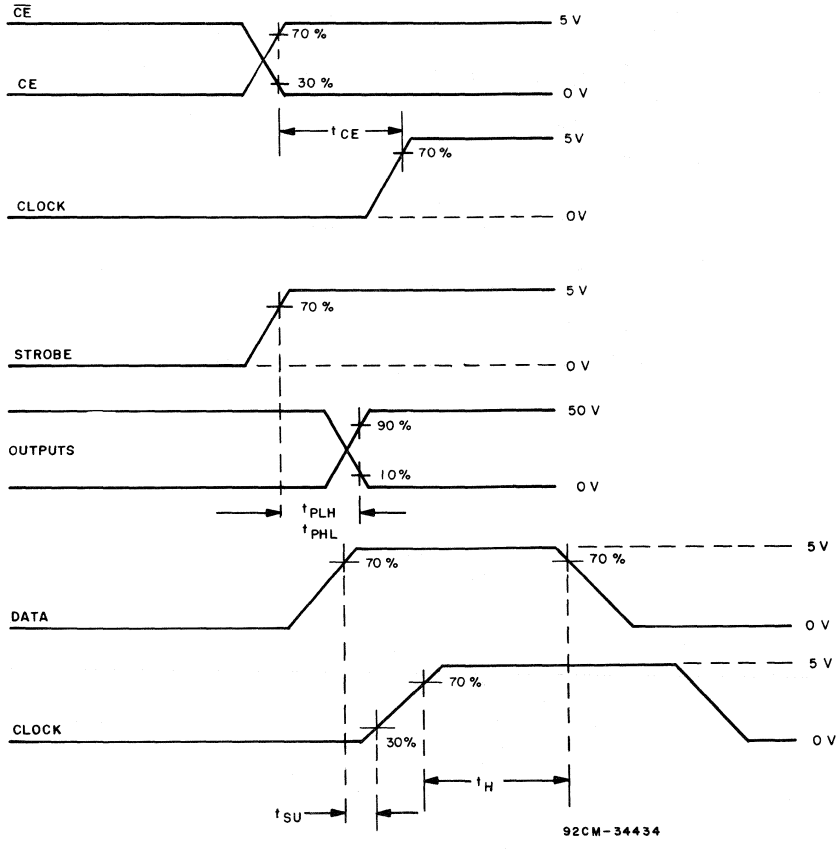


Fig. 6 - Segment-latch driver (CA3208E) timing waveforms.

CA3207, CA3208

Circuit Descriptions

Sequencer-Driver (CA3207E)

The CA3207E circuit consists of a 7-stage Johnson counter, which is reset by the positive transition of the sync pulse and which is clocked on the positive transitions of the clock pulse. The outputs of the counter are decoded to turn on one output driver at a time in sequence, for the period of one clock pulse (normally 70 μs). The 14 output drivers are each capable of sourcing 40 mA of current and in a typical application will be connected to the grids of a vacuum fluorescent display, thereby performing a digit select function on a display of up to 14 characters. All outputs are set to zero by the application of a positive "1" level to either of the gate terminals, 5 and 6. The action of the 7-stage counter is unaffected by the presence of inhibit levels on the gate terminals. The gate terminals can be used for a controlled power down or for chopping where display dimmer is desired. The only difference between the two terminals is that gate 1, pin 5, has a delayed falling edge, which delays the release of the output drivers for a time determined by the value of the resistor connected between pin 7 and V_{DD}.

Segment-Latch Driver (CA3208E)

This circuit consists of a 14-bit shift register accepting serial data at pin 9 at a typical rate of 224 kHz and being clocked on the rising edge of the 448-kHz clock signal.

The leading edge of a 14-kHz strobe signal generates an internal strobe pulse through the one shot, which shifts the data, in parallel, from the shift register to the output latches, which in turn set the output drivers to the corresponding state. There are 14 output drivers, each capable of driving 7.5-mA at 55 volts, simultaneously. The drivers are normally connected to the anodes or segments of the vacuum fluorescent display. In a multi-character display, all corresponding segments in each character would be linked together. Activation of a particular character is made by the CA3207E Sequencer-Driver turning on the appropriate output and raising the grid of the display to a positive value.

Clock Enable (CE) and Clock Enable Not ($\overline{CE}$) pins are available for use in system applications. The first enables the chip with a logic level "1" and the second with a logic level"0".

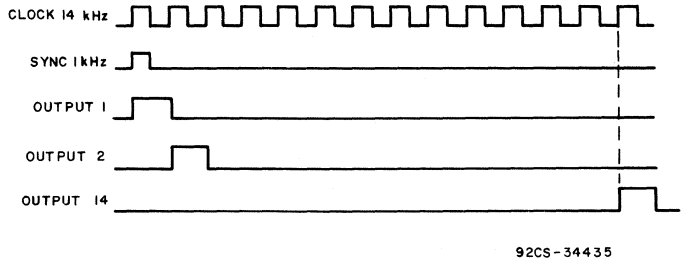


Fig. 7 - Sequencer driver (CA3207E) timing waveforms.

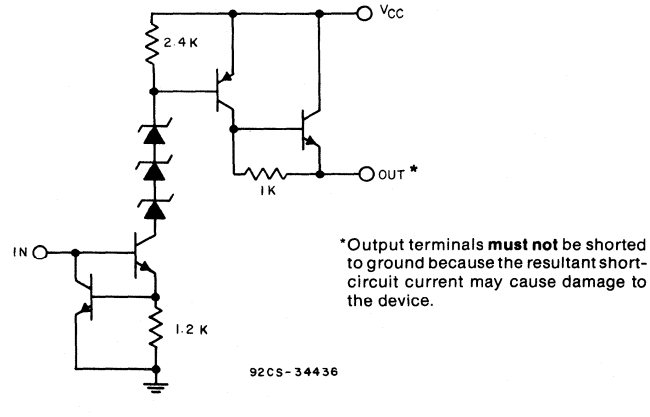


Fig. 8 - Sequencer driver (CA3207E) output circuit.

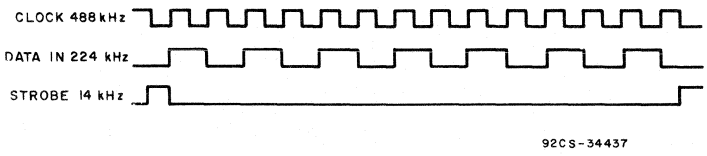
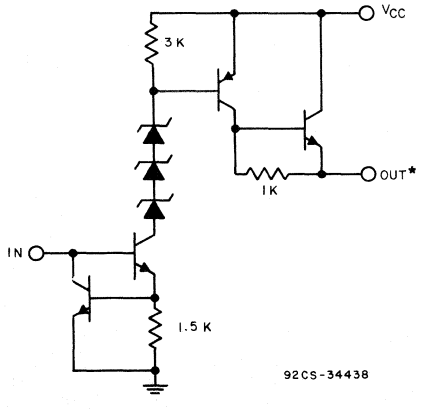


Fig. 9 - Segment-latch driver (CA3208E) timing waveforms.



*Output terminals **must not** be shorted to ground because the resultant short-circuit current may cause damage to the device.

Fig. 10 - Segment latch-driver (CA3208E) output circuit.

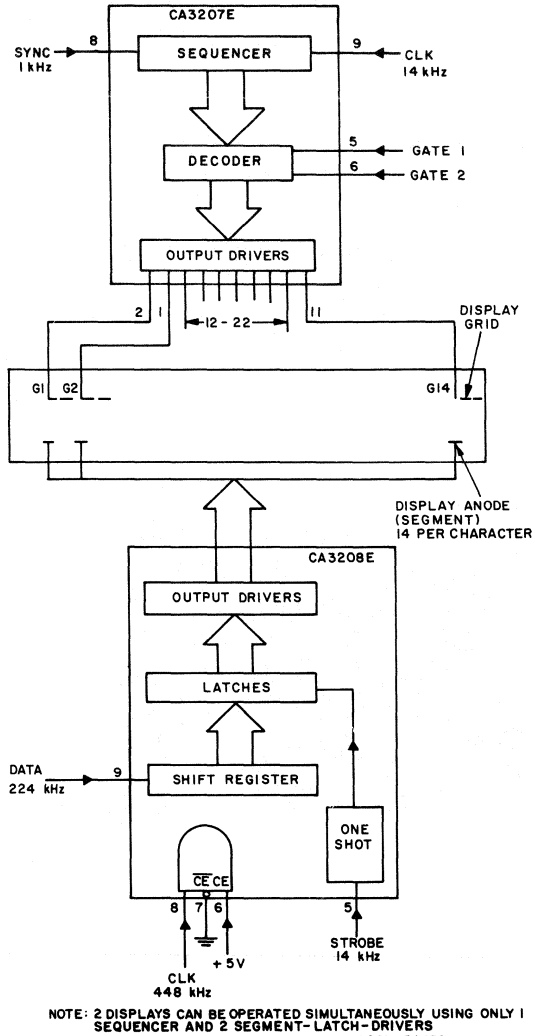


Fig. 11 - Typical systems application of the CA3207E and CA3208E display circuits.

CA3207, CA3208

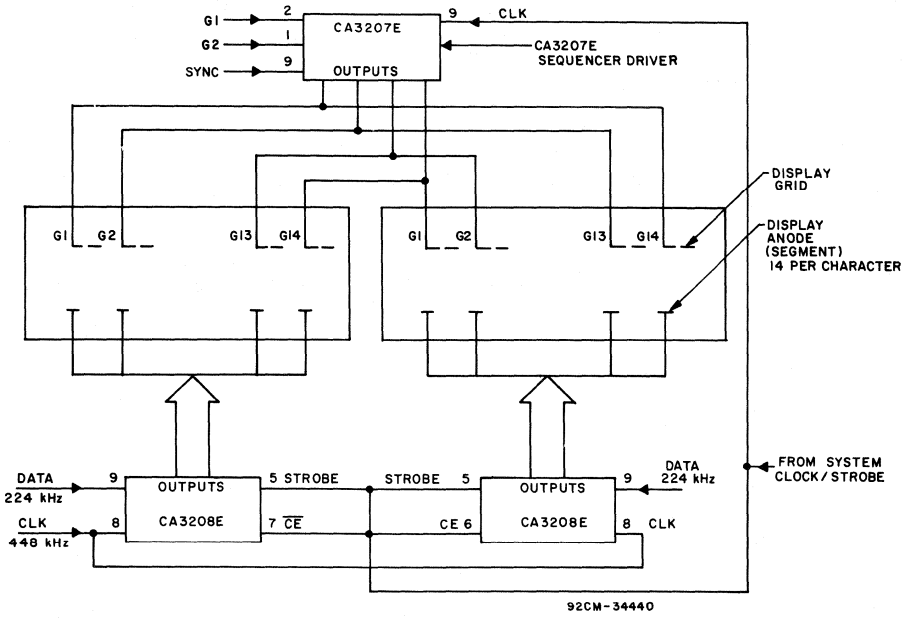
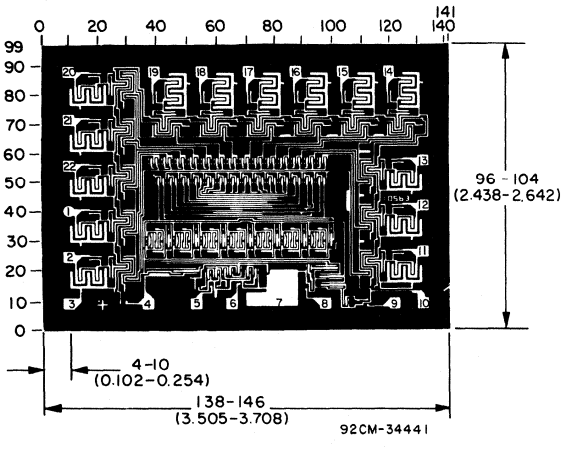
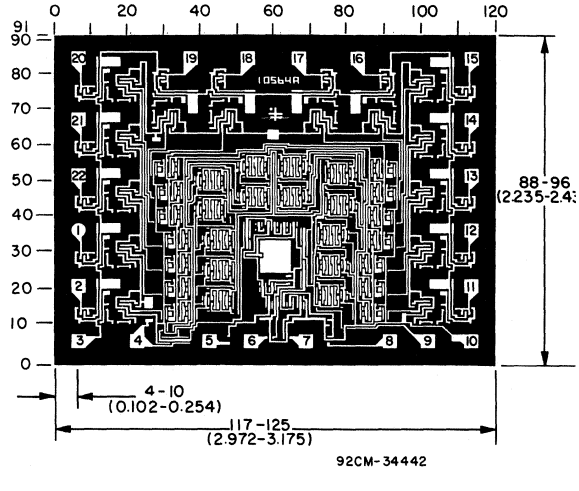


Fig. 12 - Typical systems application of the CA3207E and 2 CA3208E circuits for a total 28-character display.



Dimensions and pad layout for the CA3207H.



Dimensions and pad layout for the CA3208H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Advance Information/
Preliminary Data

CA3250, CA3251

General-Purpose High-Current N-P-N Transistor Arrays

CA3251 - Common-Emitter Array
CA3250 - Common-Collector Array

Features:

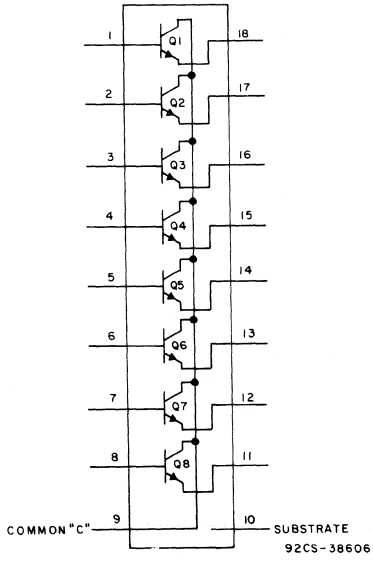
- *8 transistors permit a wide range of applications in either a common-emitter (CA3251) or common-collector (CA3250) configuration*
- *High I_C: 100 mA max.*
- *Low V_{CEsat} (at 50 mA): 0.4 V typ.*

RCA-CA3250• and CA3251• consist of eight high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3251 is connected in a common-emitter configuration and the CA3250 is connected in a common-collector configuration.

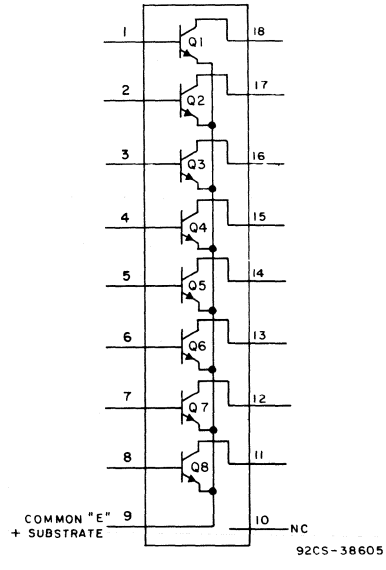
•Formerly RCA Development Type Nos. TA11550 and TA11551.

Applications:

- *Drivers for:*
  Incandescent display devices
  LED (e.g. RCA-40736R GaAs High-Efficiency Emitting Diode)
  Relay control
  Thyristor firing



(a)
COMMON-COLLECTOR CONFIGURATION



(b)
COMMON-EMITTER CONFIGURATION

Fig. 1 - Functional diagrams of types CA3250 and CA3251.

File Number **1684**

CA3250, CA3251

The CA3250 and CA3251 are capable of directly driving seven-segment and decimal point displays such as incandescent and light-emitting diode (LED). These types are also well-suited for a variety of other drive applications, including relay control and thyristor firing.

In some applications, the CA3250 is functionally compatible with the higher power UDN2580A. The CA3251 is functionally compatible with the ULN2800A series and the TD62081AP series. It may be necessary, however, to insert in each base a series resistance to limit the I_B to 20 mA.

The CA3250 and CA3251 are supplied in an 18-lead dual-in-line plastic package (E suffix), and in an 18-lead dual-in-line frit seal ceramic package (F suffix), which includes a separate substrate connection (CA3250 only) for maximum flexibility in circuit design. Both types are also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

The following ratings apply for each transistor in the device:

COLLECTOR-TO-EMITTER VOLTAGE (V_{CEO}) ..... 16 V
COLLECTOR-TO-BASE VOLTAGE (V_{CBO}) ..... 20 V
COLLECTOR-TO-SUBSTRATE VOLTAGE (V_{CIO})* ..... 20 V
EMITTER-TO-BASE VOLTAGE (V_{EBO}) ..... 5 V
COLLECTOR CURRENT (I_C) ..... 100 mA
BASE CURRENT (I_B) ..... 20 mA
POWER DISSIPATION:
  Any one transistor ..... 500 mW
  Total Package ..... 750 mW
  Above 55° C ..... Derate Linearly 6.67 mW/° C
AMBIENT TEMPERATURE RANGE:
  Operating ..... -55 to +125° C
  Storage ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 seconds max. ..... 265° C

* The collector of each transistor of the CA3250 and CA3251 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (10) of the CA3250 should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

The substrate of the CA3251 is internally connected to the common-emitter terminal No. 9 to make it more compatible with existing industry types.

ELECTRICAL CHARACTERISTICS AT T_A = 25° C FOR EQUIPMENT DESIGN

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA	20	60	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	20	60	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	16	24	—	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500 μA	5	6.9	—	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	30	68	—	—
		V_{CE} = 3 V, I_C = 50 mA	40	70	—	—
Base-to-Emitter Saturation Voltage	V_{BEsat}	I_C = 30 mA, I_B = 1 mA	—	0.87	1.0	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 30 mA, I_B = 1 mA	—	0.27	0.5	V
		I_C = 50 mA, I_B = 5 mA	—	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	—	—	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	—	—	1	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3250 AND CA3251

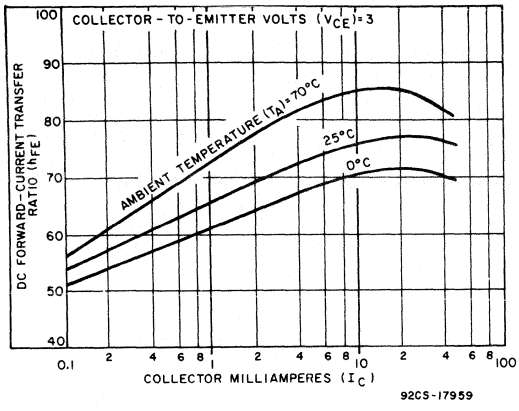


Fig. 2 - DC Forward-current transfer ratio as a function of collector current.

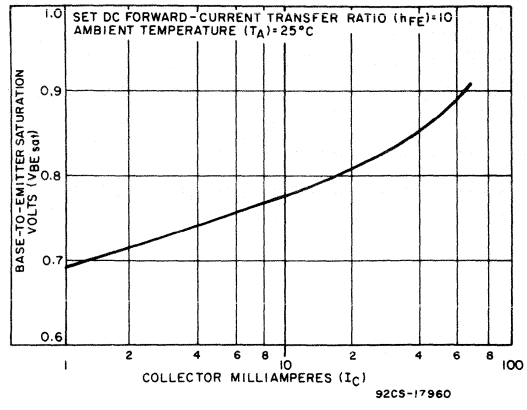


Fig. 3 - Base-to-emitter saturation voltage as a function of collector current.

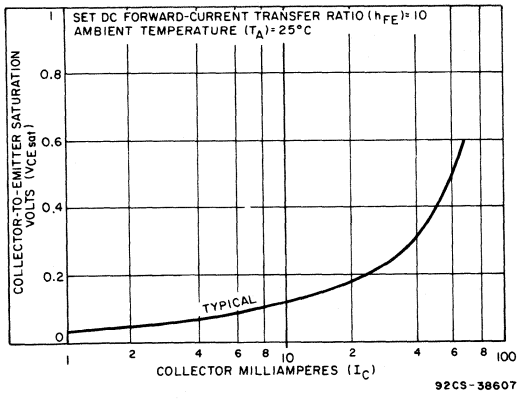


Fig. 4 - Collector-to-emitter saturation voltage as a function of collector current at T_A = 25° C.

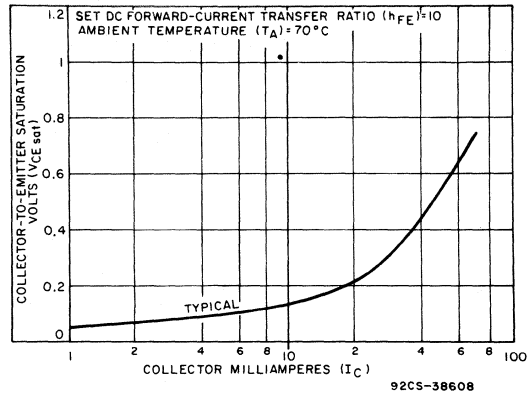


Fig. 5 - Collector-to-emitter saturation voltage as a function of collector current at T_A = 70° C.

TYPICAL READ-OUT DRIVER APPLICATIONS

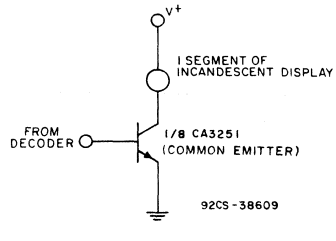


Fig. 6 - Schematic diagram showing one transistor of the CA3251 driving one segment of an incandescent display.

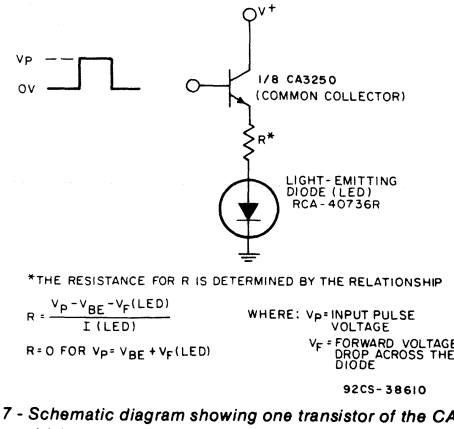


Fig. 7 - Schematic diagram showing one transistor of the CA3250 driving a light-emitting diode (LED).

CD7211, CD7211A

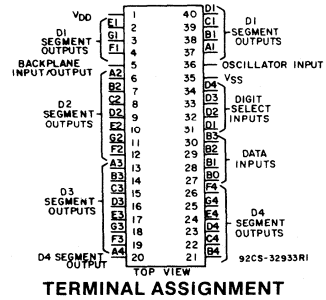
Advance Information/
Preliminary Data

CMOS Four-Digit LCD Decoders-Drivers

6-V Rating

Features:

- *6-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Decodes multiplexed binary to hexadecimal (CD7211) and decimal (CD7211A) outputs*



TERMINAL ASSIGNMENT
CD7211, CD7211A

The RCA-CD7211 and CD7211A are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

They contain all the circuitry necessary to drive conventional LCD displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four-digit displays.

The backplane and segment drives are designed so that p and n channels have the same ON resistance and thus equal rise and fall times. This equality eliminates any DC component, thereby maximizing display life. In addition to feeding the internal display drivers, the backplane signal can also be used as a master to drive a number of slave devices. The number of slaved devices should be limited to the load that keeps the backplane rise and fall times from exceeding 5 μs. If this limit is to be exceeded the master backplane drivers should be disabled (by connecting pin 36, the oscillator input, to V_{SS}) and pin 5 should be fed from an external oscillator and all devices slaved to it. The maximum frequency of the external signal should be 125 MHz at room temperatures.

The on-board oscillator, which operates at 16 kHz when free-running (pin 36 floating), provides a backplane signal whose frequency is approximately 125 Hz. This frequency can be reduced by connecting an external capacitor to pin 36. Plots of backplane frequency vs. supply voltage at various values of external capacitance are shown in Fig. 3. The oscillator may be overdriven by an external signal but care must be taken to keep the lower voltage level above V_{SS} by at least 20 per cent of V_{DD} (for V_{DD}=5 V the signal should oscillate between +1 and +5 volts). This precaution prevents the backplane driver from being disabled, a condition that would present a DC component to the LCD display. A signal swinging from rail-to-rail can also be used to overdrive the oscillator but in this case the duty cycle should be such that the lower portion of the signal must be less than one-microsecond duration (the backplane disable sensing circuit will not respond to signals of this duration).

Applications:

- *Digital meters and calculators*
- *General-purpose displays*
- *Wall and table clocks*
- *Automobile dashboard displays*
- *Appliance control panels*

There are four data inputs and four digit-select inputs. The four-bit binary input is decoded by means of a PROM into seven-segment hexadecimal outputs for the CD7211 and into decimal seven-segment display outputs for the CD7211A. These devices are pin-compatible with the Intersil ICM7211 and ICM7211A, respectively.

The CD7211 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.

File Number **1725**

CD7211, CD7211A

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.3 to +6.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to V_{DD} +0.3 V
DC INPUT CURRENT, ANY ONE INPUT* ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-20 to +60° C ..... 500 mW
For T_A=+60 to +70° C ..... Derate Linearly at 12 mW/° C to 380 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -20 to +70° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +125° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

*Pin 36 limited to ±5 mA.

STATIC ELECTRICAL CHARACTERISTICS
T_A=25° C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Operating Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3	5	6	V
Operating Current	I_{op}	Display Operating	—	10	50	μA
Oscillator Input Current	I_{OL}, I_{OH}	Pin 36	—	±2	±10	μA
Segment Rise and Fall Time	t_{rs}, t_{fs}	C_L = 200 pF	—	0.5	—	μs
Backplane Rise and Fall Time	t_{rB}, t_{fB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz
Input High Voltage	V_{IH}		3.5	—	—	V
Input Low Voltage	V_{IL}		—	—	1.5	V
Input Leakage Current	I_{IL}	Pins 27-34	—	±0.01	±1	μA
Input Capacitance	C_I	Pins 27-34	—	5	—	pF
Backplane Input Leakage	$I_{IL(BP)}$	Pin 5 with Pin 36 @ V_{SS}	—	±0.01	±1	μA
Backplane Input Capacitance	$C_{I(BP)}$		—	200	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS
T_A=25° C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	TYP. VALUES	UNITS
Digit-Select Active Pulse Width	t_{sa}	See Timing Diagram	0.5	μs
Data Setup Time	t_{ds}	See Timing Diagram	250	ns
Data Hold Time	t_{dh}	See Timing Diagram	100	ns
Inter-Digit Select Time	t_{ids}	See Timing Diagram	1	μs

CD7211, CD7211A

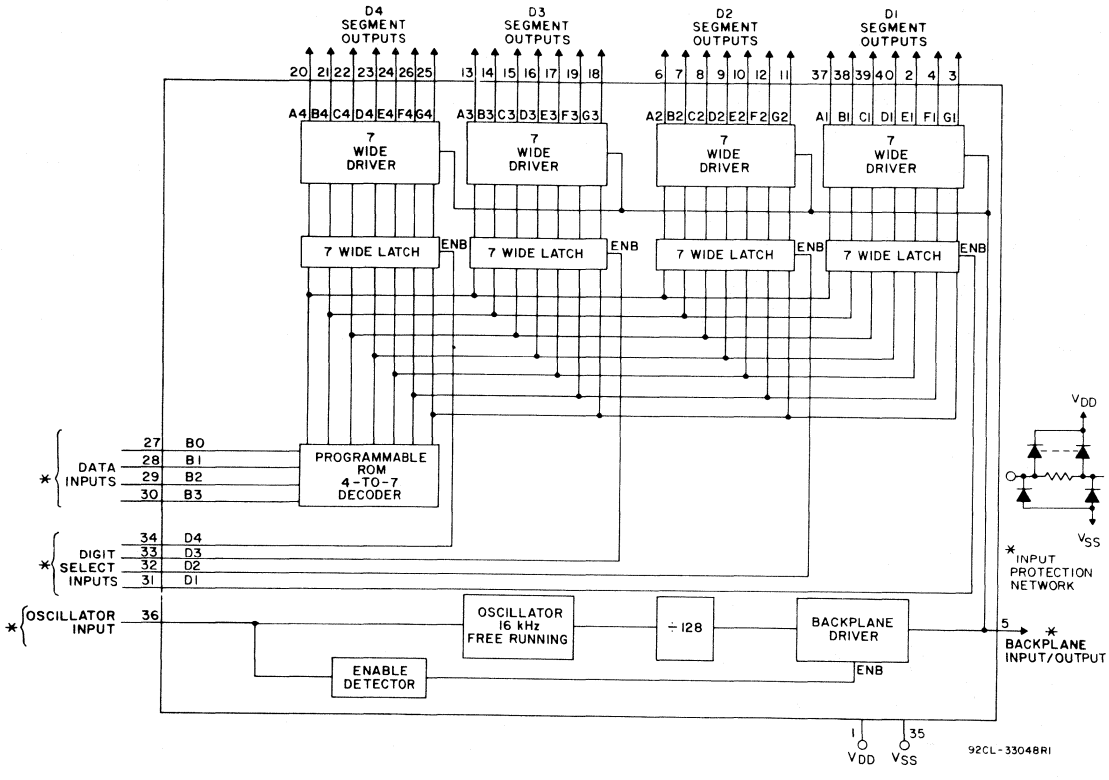


Fig. 1 - Block diagram of CD7211 and CD7211A.

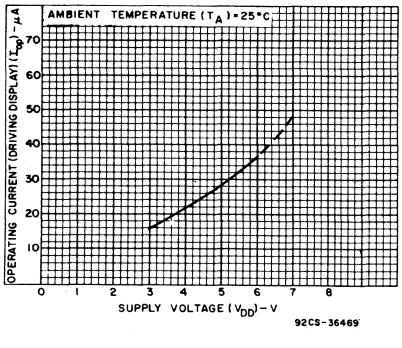


Fig. 2 - Typical operating current as a function of supply voltage.

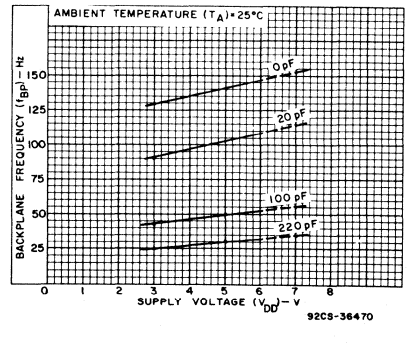


Fig. 3 - Typical backplane frequency as a function of supply voltage and external capacitance on pin 36.

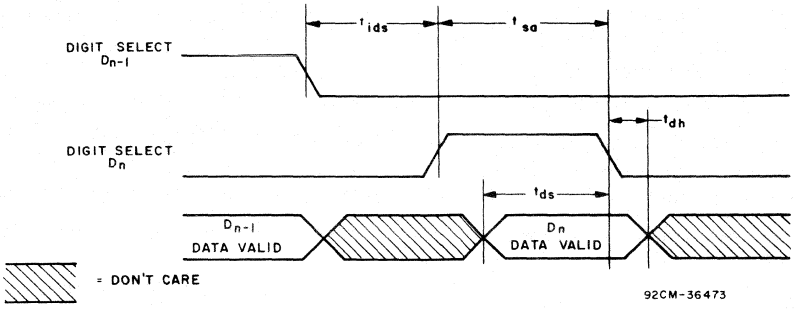


Fig. 4 - CD7211, CD7211A timing diagram.

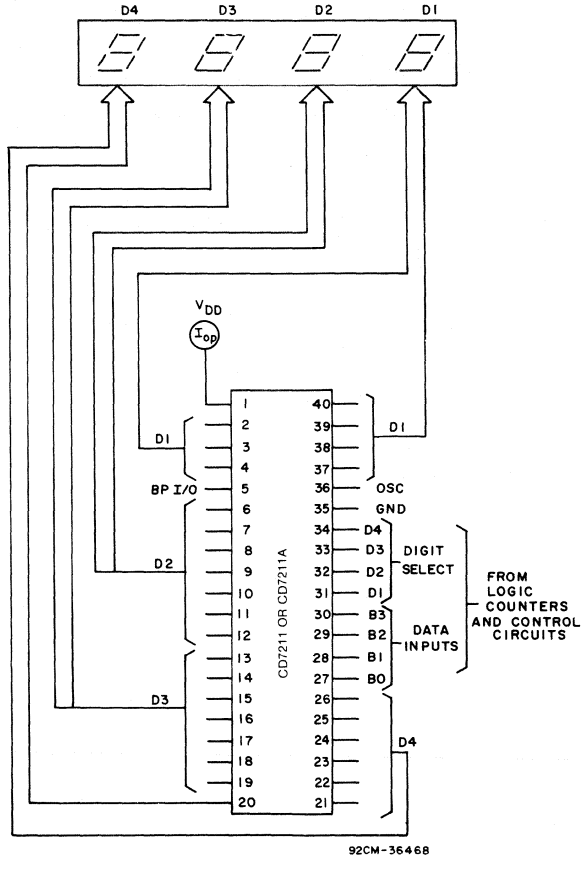


Fig. 5 - Test circuit.

CD7211, CD7211A

Table I — Output Codes

Binary Input B3 B2 B1 B0	Display Hexadecimal CD7211	Display Decimal CD7211A
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	A	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

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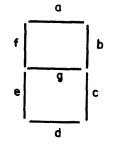
DIGIT SELECTION TRUTH TABLE

Pins 31	32	33	34	Digit Selected
1	0	0	0	D1 (LSD)
0	1	0	0	D2
0	0	1	0	D3
0	0	0	1	D4 (MSD)

DISPLAY SEGMENTS



92CS-31376

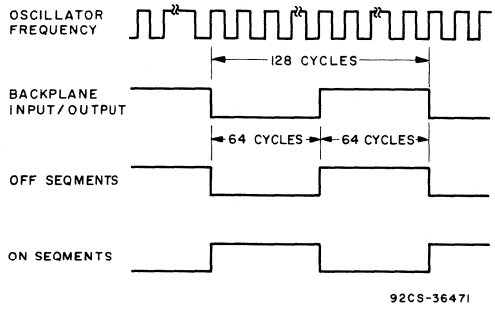


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Fig. 6 - Display waveforms.

Advance Information/
Preliminary Data

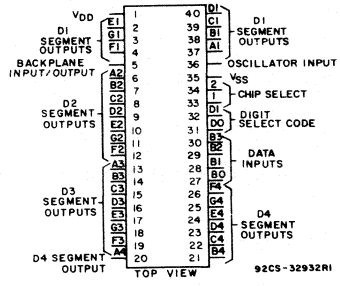
CD7211M, CD7211AM

CMOS Four-Digit LCD Decoders-Drivers

6-V Rating

Features:

- *6-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Direct microprocessor interface*
- *Decodes binary into hexadecimal (CD7211M) and decimal (CD7211AM) outputs*



TERMINAL ASSIGNMENT
CD7211M, CD7211AM

The RCA-CD7211M and CD7211AM are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

They contain all the circuitry necessary to drive conventional liquid-crystal displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four-digit displays.

The backplane and segment drives are designed so that p and n channels have the same ON resistance and thus equal rise and fall times. This equality eliminates any DC component, thereby maximizing display life. In addition to feeding the internal display drivers, the backplane signal can also be used as a master to drive a number of slave devices. The number of slaved devices should be limited to the load that keeps the backplane rise and fall times from exceeding 5 μs. If tnis limit is to be exceeded the master backplane drivers should be disabled (by connecting pin 36, the oscillator input, to V_{SS}) and pin 5 should be fed from an external oscillator and all devices slaved to it. The maximum frequency of the external signal should be 125 Hz at room temperatures.

The on-board oscillator, which operates at 16 kHz when free-running (pin 36 floating), provides a backplane signal whose frequency is approximately 125 Hz. This frequency can be reduced by connecting an external capacitor to pin 36. Plots of backplane frequency vs. supply voltage at various values of external capacitance are shown in Fig. 3. The oscillator may be overdriven by an external signal but care must be taken to keep the lower voltage level above V_{SS} by at least 20 per cent of V_{DD} (for V_{DD}=5 V the signal should oscillate between +1 and +5 volts). This precaution prevents the backplane driver from being disabled, a condition that would present a DC component to the LCD display. A signal swinging from rail-to-rail can also be used to overdrive the oscillator but in this case the duty cycle should be such that the lower portion of the signal must be less than one-microsecond duration (the backplane disable sensing circuit will not respond to signals of this duration).

Applications:

- *Microprocessor-controlled digital meters and calculators*
- *General-purpose displays*
- *Microprocessor-controlled automotive dashboard displays*
- *Microprocessor applicance control panels*

A four-bit data-input latch and a two-bit select-code latch under the control of two chip-select inputs permit interfacing with a microprocessor. This device simplifies designing a seven-segment display into a microprocessor system, without requiring extensive ROM or CPU time for decoding and display updating. The four-bit binary input is decoded by means of a PROM into a seven-segment hexadecimal output for the CD7211M type and into a decimal display for the CD7211AM type. These types are pin-compatible with the Intersil ICM7211 and ICM7211A, respectively.

The CD7211 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.

File Number **1726**

CD7211M, CD7211AM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.3 to +6.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to V_{DD} +0.3 V
DC INPUT CURRENT, ANY ONE INPUT* ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-20 to +60°C ..... 500 mW
For T_A=+60 to +70°C ..... Derate Linearly at 12 mW/°C to 380 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -20 to +70°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

*Pin 36 limited to ±5 mA.

STATIC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Operating Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3	5	6	V
Operating Current	I_{op}	Display Operating	—	10	50	μA
Oscillator Input Current	I_{OL}, I_{OH}	Pin 36	—	±2	±10	μA
Segment Rise and Fall Time	t_{rs}, t_{fs}	C_L = 200 pF	—	0.5	—	μs
Backplane Rise and Fall Time	t_{rB}, t_{fB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz
Input High Voltage	V_{IH}		3.5	—	—	V
Input Low Voltage	V_{IL}		—	—	1.5	V
Input Leakage Current	I_{IL}	Pins 27-34	—	±0.01	±1	μA
Input Capacitance	C_I	Pins 27-34	—	5	—	pF
Backplane Input Leakage	$I_{IL(BP)}$	Pin 5 with Pin 36 @ V_{SS}	—	±0.01	±1	μA
Backplane Input Capacitance	$C_{I(BP)}$		—	200	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	TYP. VALUES	UNITS
Chip-Select Active Pulse Width	t_{csa}	See Timing Diagram	100	ns
Data Setup Time	t_{dsm}	See Timing Diagram	50	ns
Data Hold Time	t_{dhm}	See Timing Diagram	25	ns
Inter-Chip Select Time	t_{ics}	See Timing Diagram	1	μs

CD7211M, CD7211AM

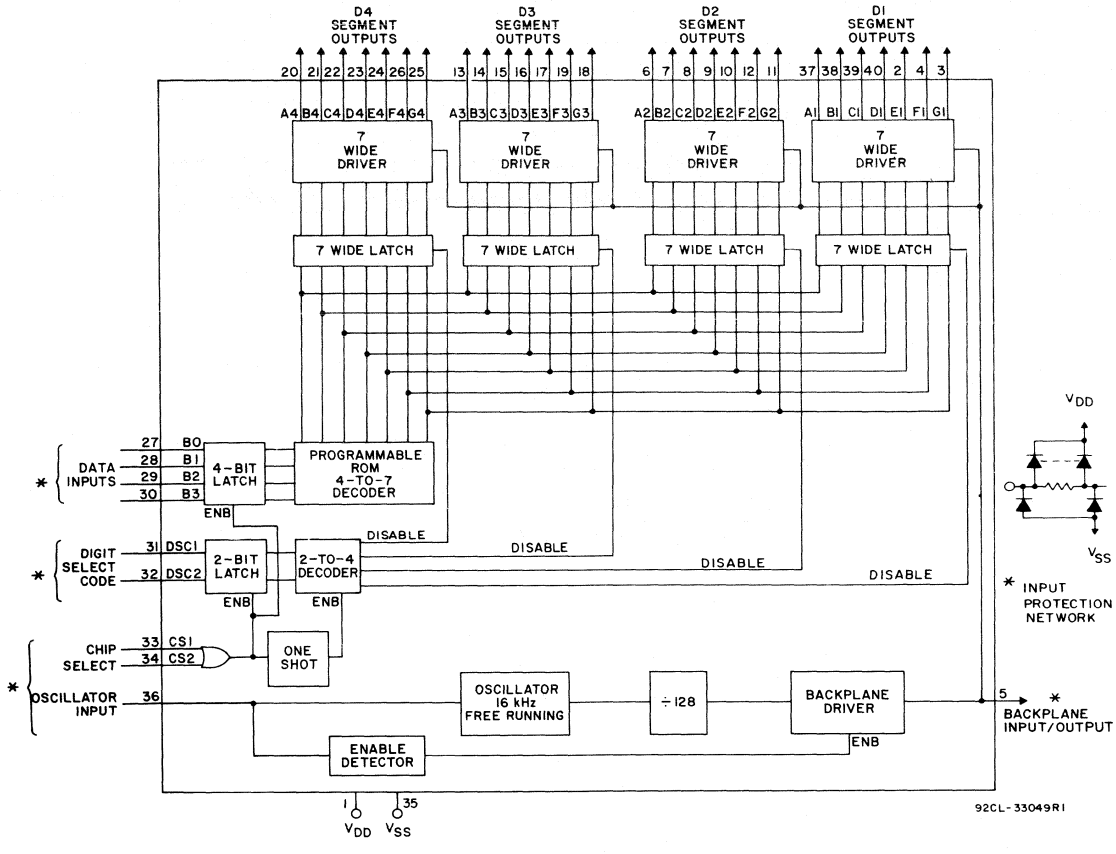


Fig. 1 - Block diagram of CD7211M and CD7211AM.

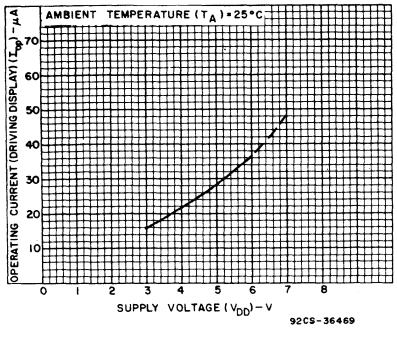


Fig. 2 - Typical operating current as a function of supply voltage.

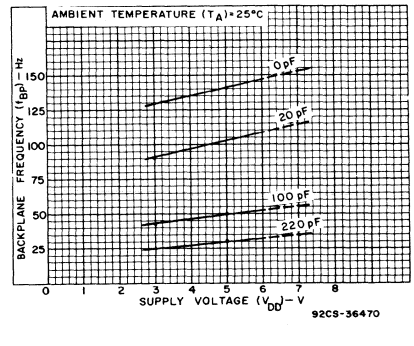


Fig. 3 - Typical backplane frequency as a function of supply voltage and external capacitance on pin 36.

CD7211M, CD7211AM

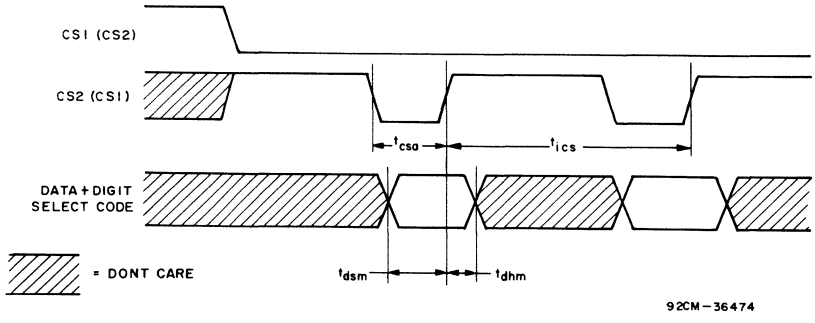


Fig. 4 - CD7211M, CD7211AM timing diagram.

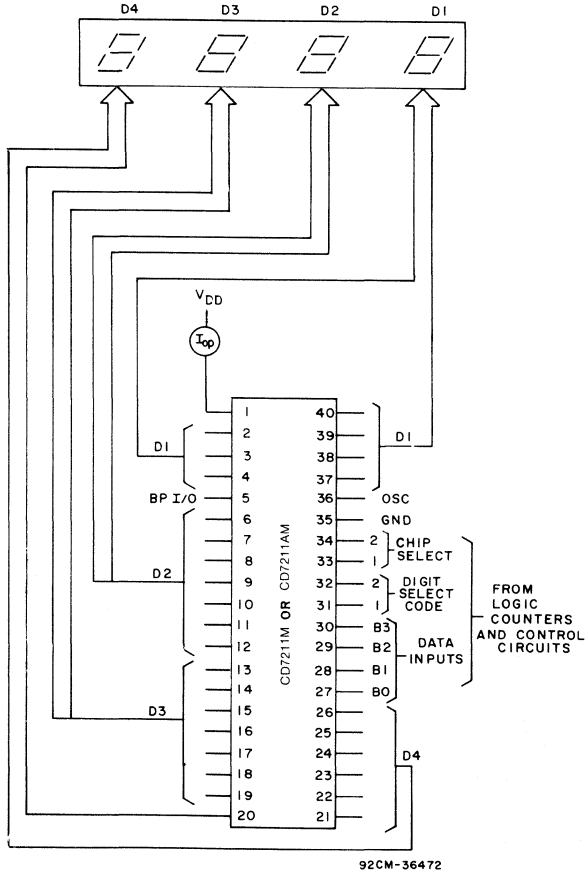


Fig. 5 - Test circuit.

CD7211M, CD7211AM

Table I — Output Codes

Binary Inout B3 B2 B1 B0	Display: Hexadecimal CD7211M	Display: Decimal CD7211AM
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	A	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

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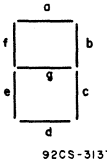
CHIP-SELECT TRUTH TABLE

Pins 33	Pins 34	Function
0	0	New inputs from μP are written into input latches
0	1	Inputs from μP are latched in input latches, decoded, and passed through selected (1 of 4) output latch to update selected digit
1	0	
1	1	

DIGIT SELECTION TRUTH TABLE

Pins 31	Pins 32	Digit Selected
1	1	D1 (LSD)
0	1	D2
1	0	D3
0	0	D4 (MSD)

DISPLAY SEGMENTS



92CS-31376

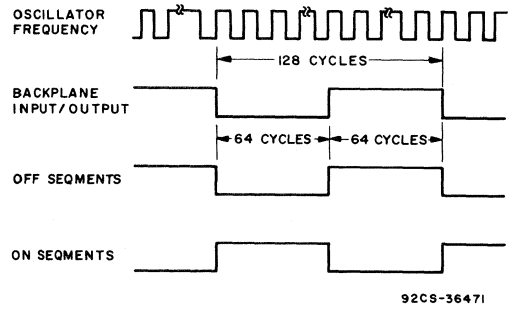


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Fig. 6 - Display waveforms.

Operational Amplifiers

Operational Amplifiers — Technical Data

Operational Amplifiers (Cont'd)

Op-Amp, OTA, and Comparator Selection Chart

Type	V_{IO} (Max) mV	I_{IO}(Max) nA	I_I Max nA	I^+ Max Ma	Max V^+ V^-	A_{OL} (Min) V/V	A_{OL} (Min) dB	BW MHz	SR (Typ) V/μs	Compensation	Package Plastic/Ceramic	Package TO-5 Metal CAN
Wideband Single-Unit Types Cont'd.												
CA3030A	2	1600	0.06	30	±16	2K	66	0.2	7	External	14E	—
CA3037	5	5000	0.012	30	±8	700	57	0.2	3	External	14D	—
CA3037A	2	1500	0.04	30	±8	700	57	0.2	3	External	14D	—
CA3038	5	5000	0.024	30	±16	2K	66	0.2	7	External	14D	—
CA3038A	2	1600	0.06	30	±16	2K	66	0.2	7	External	14D	—
CA3100 BiMOS	5	400	0.02	10.5	±18	630	56	38*	70	External	8E	8T, 8S
CA3130 BiMOS	15	0.03	0.05	15	±8	50K	94	4.5*	9	External	8E	8T, 8S
CA3130A BiMOS	5	0.02	0.03	15	±8	50K	94	4.5*	9	External	8E	8T, 8S
CA3140 BiMOS	15	0.03	0.05	6	±18	20K	86	4.5*	9	Internal	8E	8T, 8S
CA3140A BiMOS	5	0.02	0.03	6	±18	20K	86	4.5*	9	Internal	8E	8T, 8S
CA3160 BiMOS	15	0.03	0.05	15	±8	50K	94	4*	10	Internal	8E	8T, 8S
CA3160A BiMOS	5	0.02	0.03	15	±8	50K	94	4*	10	Internal	8E	8T, 8S
CA3450 (3 GHz)	15	150	350	35	±8.5	1K	60	170[4]	330[5]	External	16E	—
Wideband Dual-Unit Types												
CA3240 BiMOS	15	0.03	0.05	12	±18	20K	86	4.5*	9	Internal	8E, 14E1	8T, 8S
CA3240A BiMOS	5	0.02	0.04	12	±18	20K	86	4.5*	9	Internal	8E, 14E1	8T, 8S
CA3260 BiMOS	15	0.03	0.05	15.5	±8	50K	94	4*	10	Internal	8E	8T, 8S
CA3260A BiMOS	5	0.02	0.03	15.5	±8	50K	94	4*	10	Internal	8E	8T, 8S
Wideband High-Slew Rate Types (> 50V/μs)												
CA3080	5	600	5000	1.2	±18	gm=9600μmho		2	50	External	8E	8T, 8S
CA3080A	2	600	5000	1.2	±18	gm=9600μmho		2	50	External	8E	8T, 8S
CA3100 BiMOS	5	400	0.02	10.5	±18	630	56	38*	70	External	8E	8T, 8S
CA3280	3	700	5000	4.8	±18	50K	44	9	125	External	16E	—
CA3280A	0.5	700	5000	4.8	±18	50K	94	9	125	External	16E	—
CA3450 (3 GHz)	15	150	350	35	±8.5	1K	60	170[4]	330[5]	External	16E	—
5-Volt BiMOS Logic Types for Low-Supply Voltage, Low-Input-Current Applications												
CA5130	10	0.01	0.015	0.1	±8	17.8K	85	4*	10	External	8E	8T, 8S
CA5130A	4	0.005	0.01	0.1	±8	31.6K	90	4*	10	External	8E	8T, 8S
CA5160	10	0.01	0.015	0.1	±8	17.8K	85	4*	10	Internal	8E	8T, 8S
CA5160A	4	0.005	0.01	0.1	±8	31.6K	90	4*	10	Internal	8E	8T, 8S
CA5260	15	0.01	0.015	1.4	±8	10K	80	4*	10	Internal	8E	8T, 8S
CA5260A	4	0.01	0.015	1.4	±8	14.1K	83	4*	10	Internal	8E	8T, 8S
CA5420	10	0.001	0.002 0.0250	0.55	±18	17.8K	85	0.5*	0.5	Internal	8E	8T, 8S
CA5420A	5	0.05	0.001 0.0150	0.55	±18	17.8K	85	0.5*	0.5	Internal	8E	8T, 8S
CA5422 Ampl. A	10	0.001	0.005	0.7	±22	1K	60	160•	0.25	External	14E	—
CA5422 Ampl. B	10	0.015	0.025	0.7		316	50	1•	1	External		
OTA's (Programmable, Variable) Micropower (Single-Unit Types)												
CA3060 (Triple Unit)	5	1000	5000	3.6	±18	gm=30μmho		0.11	8	External	16E	—
CA3078	4.5	32	170	0.13	±7	25K	88	0.002	1.5	External	14D	—
CA3078A	3.5	2.5	12	0.02	±18	40K	92	0.0003	0.5	External	14D	—
CA3080	5	600	5000	1.2	±18	gm = 9600 μmho		2	50	External	8E	8T, 8S
CA3080A	2	600	5000	1.2	±18			2	50	External	8E	8T, 8S
CA3440 BiMOS	10	0.03	0.05	0.017	±12.5	10K	80	0.063*	0.03	Internal	8E	8T, 8S
CA3440A BiMOS	5	0.02	0.04	0.017	±12.5	10K	80	0.063*	0.03	Internal	8E	8T, 8S
CA6078A	Low-Noise Version of CA3078A	"Popcorn" (Burst) Noise. Device rejected if total noise voltage (burst and 1/f) referred to input exceeds 20μV peak during 30-second test period.										
Dual-Unit Types												
CA3280	3	700	5000	4.8	±18	50K	94	9	125	External	16E	—
CA3280A	0.5	700	5000	4.8	±18	50K	94	9	125	External	16E	—

Op-Amp, OTA, and Comparator Selection Chart

Type	V_{IO} (Max) mV	I_{IO} (Max) nA	I_I Max nA	I^+ Max Ma	Max V^+, V^-	A_{OL} (Min) V/V	A_{OL} (Min) dB	BW MHz	SR (Typ) V/μs	Compensation	Package Plastic/Ceramic	Package TO-5 Metal CAN
General Purpose Types Single-Unit Types												
CA081	15	0.030	0.050	2.8	±18	25K	88	5	13	Internal	8E	—
CA081A	6	0.020	0.040	2.8	±18	50K	94	5	13	Internal	8E	—
CA101	5	200	0.05	2.5	±44	50K	94	1	—	External	8E	8T, 8S
CA201, LM201†	7.5	500	0.15	3	±44	20K	85	1	—	External	8E	8T, 8S
CA301A, LM301A†	7.5	50	0.025	8	±36	25K	88	1	.10	External	8E	8T, 8S
CA307, LM307†	7.5	50	250	3	±36	25K	88	1	—	Internal	8E	8T, 8S
CA741, LM741†	5	200	500	2.8	±44	50k	94	1	0.5	Internal	8E	8T, 8S
CA741C, LM741C†	6	200	500	2.8	±36	20K	86	1	0.5	Internal	14E	10T
CA748, LM748†	5	200	500	2.8	±44	50K	94	1	0.5	External	8E	8T, 8S
CA748C, LM748C†	6	200	500	2.8	±35	20K	86	1	0.5	External	8E	8T, 8S
CA3193 BiMOS	0.5	10	40	3.5	±18	100K	100	1.2	0.25	Internal	8E	8T, 8S
CA3193A BiMOS	0.2	5	20	3.5	±18	316K	110	1.2	0.25	Internal	8E	8T, 8S
CA3420 BiMOS	10	4 pA	0.05	0.65	±22	10K	80	0.5*	0.5	Internal	8E	8T, 8S
CA3420A BiMOS	5	4pA	0.05	0.65	±22	20K	86	0.5*	0.5	Internal	8E	8T, 8S
CA3440† BiMOS	10	0.03	0.05	0.017	±12.5	10K	80	0.063*	0.03	Internal	8E	8T, 8S
CA3440A BiMOS	5	0.02	0.04	0.017	±12.5	10K	80	0.063*	0.03	Internal	8E	8T, 8S
CA3450 (3 GHz)	15	150	350	35	±8.5	1K	60	170[4]	330[5]	External	16E	—
CA3493 BiMOS	0.5	10	40	3.5	±18	100K	100	1.2*	0.25	Internal	8E	8T, 8S
CA3493A BiMOS	0.2	5	20	3.5	±18	316K	110	1.2*	0.25	Internal	8E	8T, 8S
CA6741	Low-Noise Version of CA741	"Popcorn" (Burst) Noise - Dence rejected if total noise voltage (burst & 1/f) referred to input exceeds 20μV during 30-second test period.										
Dual Unit Types												
CA082 BiMOS	15	0.03	0.05	2.8	±18	50K	94	5	13	Internal	8E	—
CA082A BiMOS	6	0.02	0.04	2.8	±18	50K	94	5	13	Internal	8E	—
CA158	5	30	150	1.2	±13	50K	94	1	—	Internal	8E	8T, 8S
CA158A	2	10	50	1.2	±13	50K	94	1	—	Internal	8E	8T, 8S
CA258	5	30	150	1.2	±13	50K	94	1	—	Internal	8E	8T, 8S
CA258A	3	15	80	1.2	±13	50K	94	1	—	Internal	8E	8T, 8S
CA358, LM358†	7	50	250	1.2	±13	25K	88	1	—	Internal	8E	8T, 8S
CA358A	3	30	100	1.2	±13	25K	88	1	—	Internal	8E	8T, 8S
CA747	5	200	500	2.8	±44	50K	94	1	0.5	Internal	14E	10T
CA747C	6	200	500	2.8	±36	20K	86	1	0.5	Internal	14E	10T
CA1458, LM1458†	6	200	500	2.8	±36	20K	86	1	0.5	Internal	8E	8T, 8S
CA1558, LM1558†	5	200	500	2.8	±44	50K	94	1	0.5	Internal	8E	8T, 8S
CA2904, LM2904†	7	50	250	1.2	±13	100K	100•	1	—	Internal	8E	8T, 8S
CA5422 BiMOS Ampl A	10	0.001	0.005	0.7	±22	1K	60	6.16*	0.25	External	14E	—
CA5422 BiMOS Ampl B	10	0.015	0.025	0.7		316	50	0.001*	1			
Quad Unit Types												
CA084 BiMOS	15	0.03	0.05	2.8	±18	50K	94	5	13	Internal	8E	—
CA084A BiMOS	6	0.02	0.04	2.8	±18	50K	94	5	13	Internal	8E	—
CA124	5	30	150	2	±16	50K	94	1	—	Internal	14E	—
CA224	7	50	250	2	±16	25K	88	1	—	Internal	14E	—
CA324, LM324†	7	50	250	2	±16	20K	86	1	—	Internal	14E	—
CA3401	—	—	300	10	±18	1000	60	5	0.6	Internal	14E	—
CA3410	15	0.03	0.04	12	±36	20K	86	5.4*	10	Internal	16E	—
CA3410A	8	0.01	0.01	10	±36	20K	86	5.4*	10	Internal	16E	—
Wideband Single-Unit Types												
CA3010	5	5000	0.012	30	±8	700	57	0.2	3	External	14	14T
CA3010A	2	1500	0.04	30	±8	700	57	0.2	3	External	—	14T
CA3015	5	5000	0.024	30	±16	2K	66	0.2	7	External	—	14T
CA3015A	2	1600	0.06	30	±16	2K	66	0.2	7	External	—	14T
CA3029	5	5000	0.012	30	±8	700	57	0.2	3	External	14E	—
CA3029A	2	1500	0.04	30	±8	700	57	0.2	3	External	14E	—
CA3030	5	5000	0.024	30	±16	2K	66	0.2	7	External	14E	—

Op-Amp, OTA, and Comparator Selection Chart

Type	V_{IO} (Max) mV	I_{IO}(Max) nA	I_t Max mA	I^+ Max Ma	Max V^+, V^-	A_{OL} (Min) V/V	A_{OL} (Min) dB	BW MHz	SR (Typ) V/μs	Compen-sation	Package Plastic/Ceramic	Package TO-5 Metal CAN
High Current Types												
CA3094	5	2000	5000	0.4	±12	20K	86	30	50	External	8E	8T, 8S
CA3094A	5	2000	5000	0.4	±18	20K	86	30	50	External	8E	8T, 8S
CA3049B	5	2000	5000	0.4	±22	20K	86	30	50	External	8E	8T, 8S
Comparators Single Unit												
CA111	7.5	50	250	8	±18	200K	106	Response Time[1]		—	8E	8T, 8S
Dual Unit												
CA3290	20	0.03	0.05	3	±18	25K	88	Response Time[2]		—	8E, 14E1	8T, 8S
CA3290A	10	0.025	0.04	3	±18	25K	88	Response Time[2]		—	8E, 14E1	8T, 8S
Quad Unit												
CA139	5	25	100	8	±18	—	—	Response Time		—	14E	—
CA139A	2	25	100	8	±18	50K	94	Response Time		—	14E	—
CA239	5	50	250	2‡	±18	—	—	Response Time		—	14E	—
CA239A	2	50	250	2‡	±18	50K	94	Response Time		—	14E	—
CA339	5	50	250	2‡	±18	50K	94	Response Time		—	14E	—
CA339A	2	50	250	2‡	±18	50K	94	Response Time[3]		—	14E	—

Note:
1 = 200 ns
2 = t_r = 1.2 μs, t_f = 200 ns
3 = t_r = 1.3 μs, t_f = 200 ns
4 = A_V = 1; R_L = 50 Ω // 20 pF, C_C = 5 pF
5 = $A_V \geq 10$; R_L = 50 Ω // 20 pF, C_C = 0 pF

†T_A = 85°C •kHz ‡Total supply current *f_t

CA081, CA082, CA084

BiMOS Operational Amplifiers

With MOS/FET Input, Composite Bipolar/MOS Output

Single Amplifier: CA081 Dual Amplifier: CA082, Quad Amplifier: CA084

Features:

- *Very low input bias and offset currents*
- *Input impedance typically 1.5 x 10^{12} Ω*
- *Low input offset voltage*
- *Wide common-mode input voltage range*
- *Low power consumption*
- *Fast slew rate*
- *Unity-gain bandwidth = 5 MHz [typ.]*
- *Wide output voltage swing*
- *Low distortion*
- *Continuous short circuit protection*
- *Direct replacement for industry type TL080 series in most applications*

The RCA-CA081, CA082, and CA084 BiMOS operational amplifiers combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range. The bipolar and MOS output transistors allow a wide output voltage swing and provide a high output current capability.

The CA081, CA082, and CA084 are internally phase-compensated. All types except the CA082 have provisions for external offset nulling.

These types have an operating-temperature range of 0 to +70° C.

Applications:

- *Inverters*
- *High-Q notch filters*
- *IC preamplifiers*
- *Unity Gain Absolute Value Amplifiers*
- *Sample and hold amplifiers*
- *Active filters*

The CA081 and CA082 types are supplied in the 8-lead dual-in-line plastic package (E suffix). The CA084 types are supplied in the 14-lead dual-in-line plastic package (E suffix). They are also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY VOLTAGE V±	±18 V
DIFFERENTIAL INPUT VOLTAGE	±16 V
INPUT VOLTAGE RANGE	±15 V
INPUT CURRENT	1 mA
OUTPUT SHORT-CIRCUIT DURATION	UNLIMITED*
POWER DISSIPATION, P_D:	
At T_A = 25° C	625 mW
Derating Factors:	
Mini-DIP	Derate linearly at 6.67 mW/° C above 56° C
14-Lead DIP	Derate linearly at 6.67 mW/° C above 56° C
AMBIENT TEMPERATURE RANGE:	0 to +70° C
STORAGE TEMPERATURE RANGE, ALL TYPES	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max.	+265° C

*The output may be shorted to ground or either supply if the maximum temperature and dissipation ratings are observed.

File Number **1238**

CA081, CA082, CA084

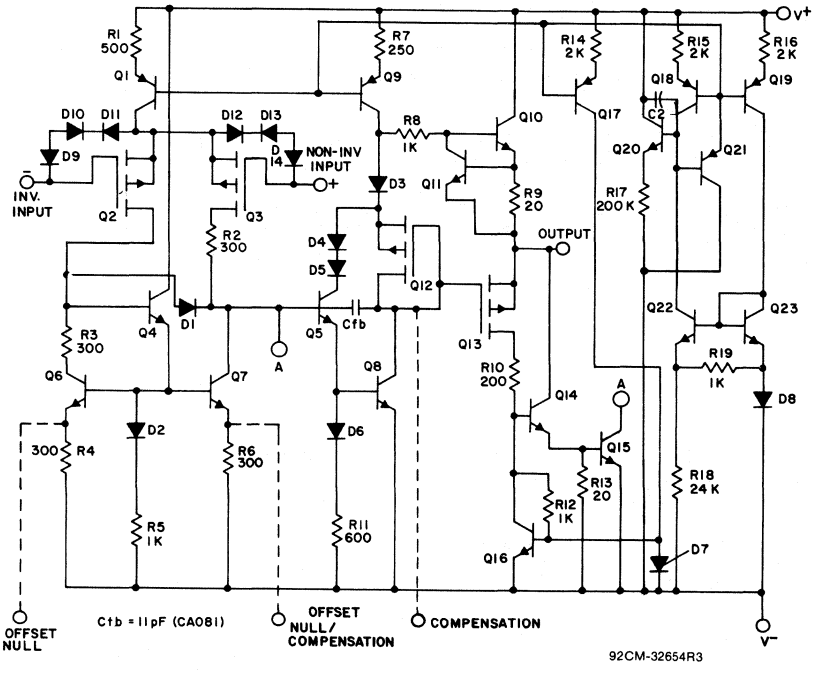
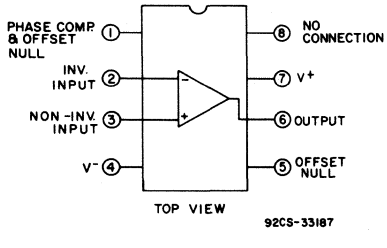
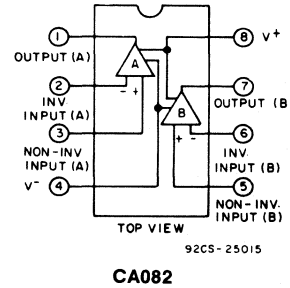


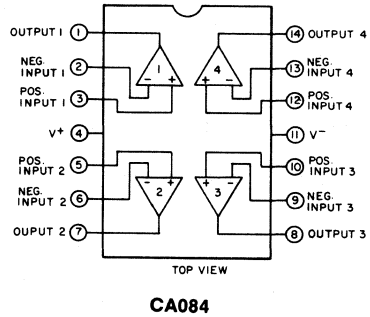
Fig. 1 - Schematic diagram of the CA081, CA082, and CA084.



CA081
E Suffix



CA082
E Suffix



CA084
E Suffix

Fig. 2 - Terminal assignments.

CA081, CA082, CA084

TYPICAL OPERATING CHARACTERISTICS at $V\pm = 15\ V, T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS	VALUE	UNITS
Slew Rate at Unity Gain, SR	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1	13	V/μs
Rise Time, t_r	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, A_{VD} = 1	0.1	μs
Overshoot Factor		10	%
Equivalent Input Noise Voltage, e_n	R_S = 100 Ω, f = 1 kHz	40	nV/√Hz

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, T_A = 0 to +70°C $V\pm = \pm 15\ V$

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA081AE CA082AE CA084AE Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	3	6	mV
			X	—	—	7.5	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	20	pA
			X	—	—	0.6	nA
Input Current		X		—	15	40	pA
			X	—	—	1	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	V
	$R_L \geq$ 10 kΩ		X	24	—	—	
	$R_L \geq$ 2 kΩ		X	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq$ 2 kΩ, V_O = ±10V	X		50	200	—	V/mV
			X	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	X		80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V+/\pm\Delta V_{IO}$)	$R_S \leq$ 10 kΩ	X		80	86	—	dB
Supply Current, I+ (per ampl., CA082, CA084)	No load, No Signal	X		—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between ampl., CA082)	A_{VD} = 100	X		—	120	—	dB

CA081, CA082, CA084

ELECTRICAL CHARACTERISTICS at T_A = 25°C, T_A = 0 to 70°C $V\pm$ = ±15 V

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA081E CA082E CA084E Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	5	15	mV
			X	—	—	20	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	30	pA
			X	—	—	1	nA
Input Current		X		—	15	50	pA
			X	—	—	2	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±10	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	V
	$R_L \geq$ 10 kΩ		X	24	—	—	
	$R_L \geq$ 2 kΩ		X	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq$ 2 kΩ, V_O = ±10V	X		25	200	—	V/mV
			X	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	X		70	76	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V+/\pm\Delta V_{IO}$)	$R_S \leq$ 10 kΩ	X		70	76	—	dB
Supply Current, $I+$ (per ampl., CA082, CA084)	No load, No Signal	X		—	1.4	2.8	mA
Channel Separation, V_{01}/V_{02} (between ampl., CA082)	A_{VD} = 100	X		—	120	—	dB

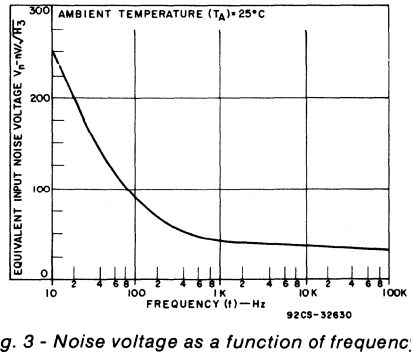


Fig. 3 - Noise voltage as a function of frequency.

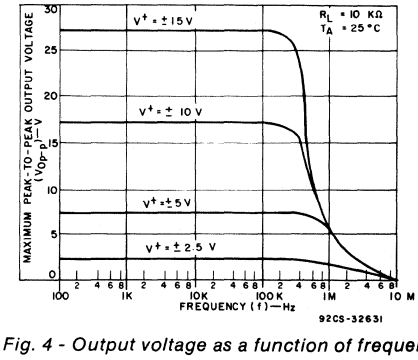


Fig. 4 - Output voltage as a function of frequency.

CA081, CA082, CA084

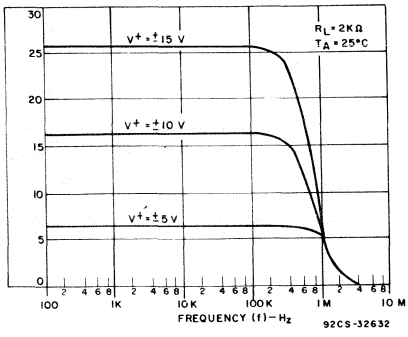


Fig. 5 - Output voltage as a function of frequency.

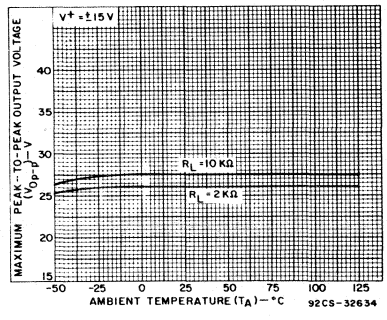


Fig. 6 - Output voltage as a function of ambient temperature.

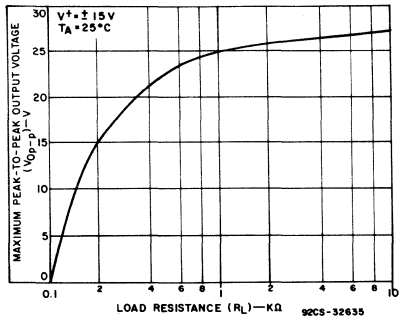


Fig. 7 - Output voltage as a function of load resistance.

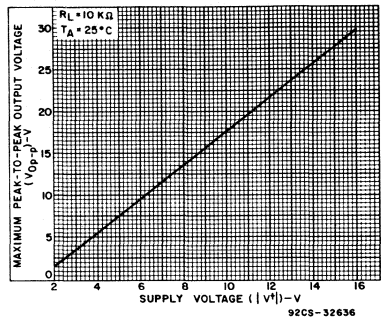


Fig. 8 - Output voltage as a function of supply voltage.

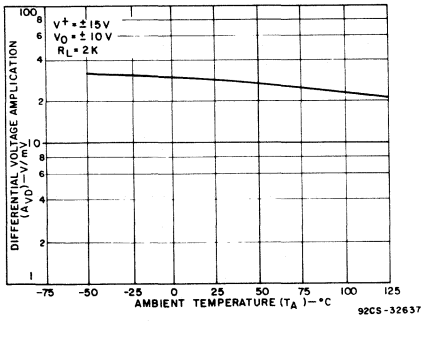


Fig. 9 - Differential voltage amplification as a function of ambient temperature.

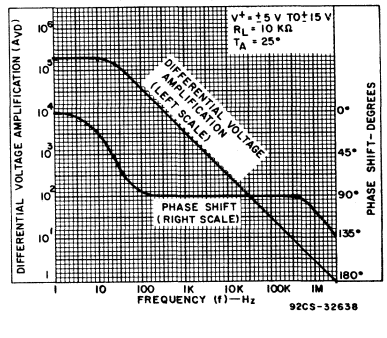


Fig. 10 - Differential voltage amplification as a function of frequency.

CA081, CA082, CA084

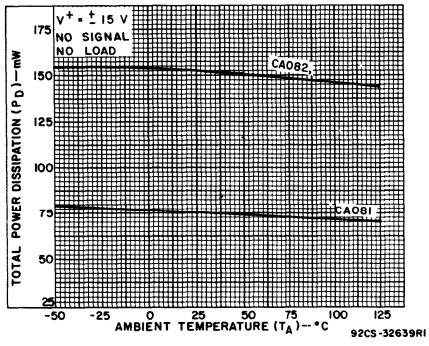


Fig. 11 - Total power dissipation as a function of ambient temperature.

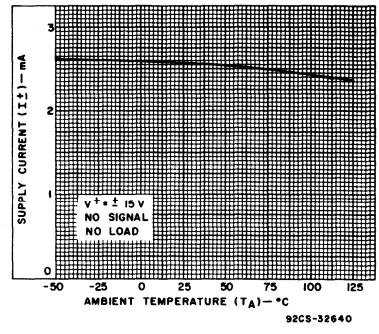


Fig. 12 - Supply current as a function of ambient temperature.

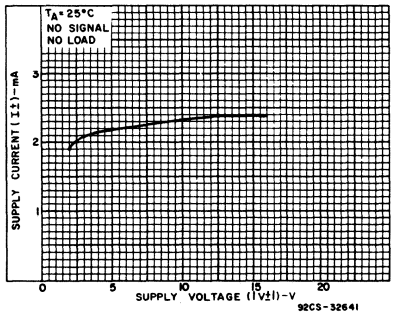


Fig. 13 - Supply current as a function of supply voltage.

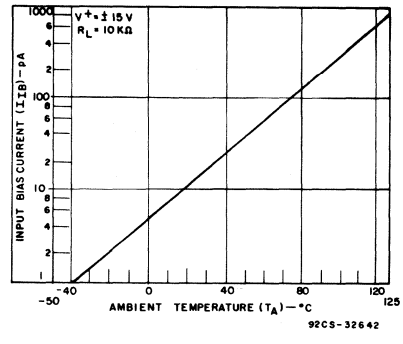


Fig. 14 - Input bias current as a function of ambient temperature.

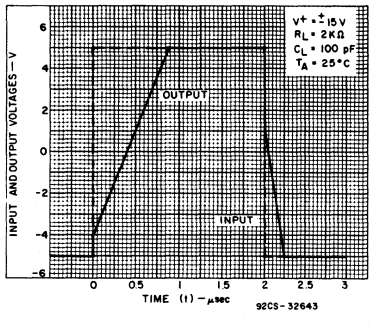


Fig. 15 - Voltage follower large-signal pulse response.

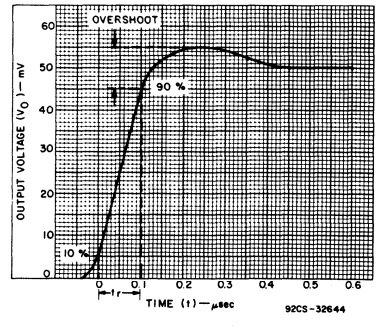


Fig. 16 - Output voltage as a function of elapsed time.

CA081, CA082, CA084

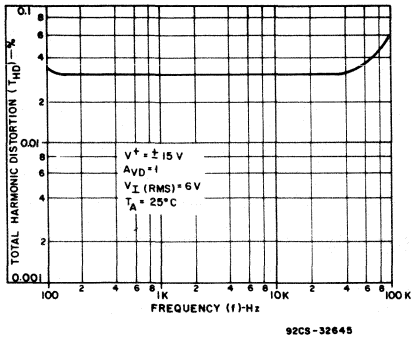


Fig. 17 - Total harmonic distortion as a function of frequency.

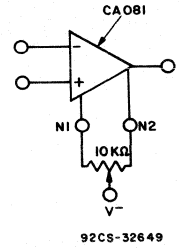


Fig. 18 - Input offset voltage null circuit.

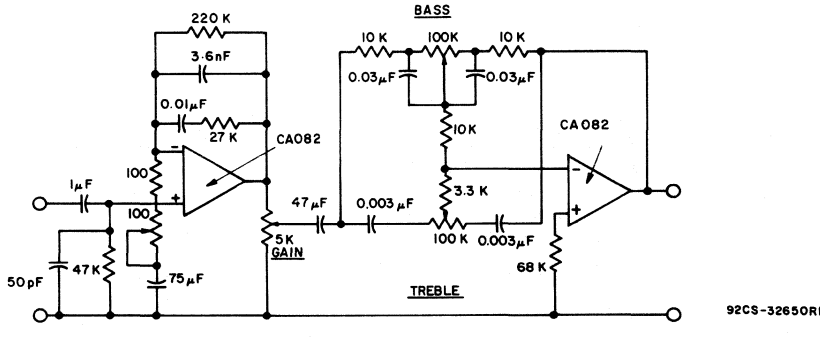


Fig. 19 - IC preamplifier.

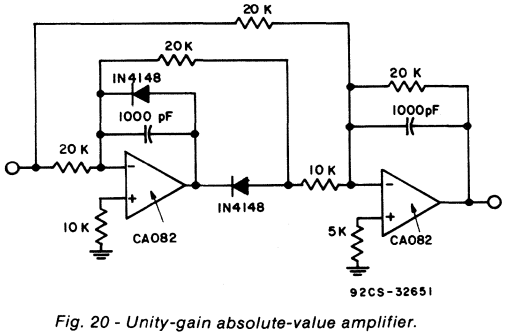


Fig. 20 - Unity-gain absolute-value amplifier.

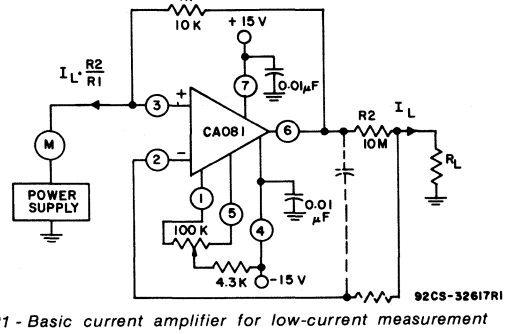


Fig. 21 - Basic current amplifier for low-current measurement systems.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA081 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 21. In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

CA101, CA201, CA301A, LM201*, LM301A*

Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- *Short-circuit protection and latch-free operation*
- *Unity-gain phase compensation with a single 30-pF capacitor*
- *Replacement for industry types 101, 201, 301A*
- *CA301A Slew Rate (Summing ampl.) 10 V/μs*

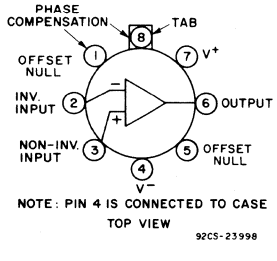
The RCA-CA101, CA201, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commerical applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

All types are available in 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA301A is also available in the 8-lead dual-in-line plastic package ("MINI-DIP" , E suffix), and in chip form (H suffix).

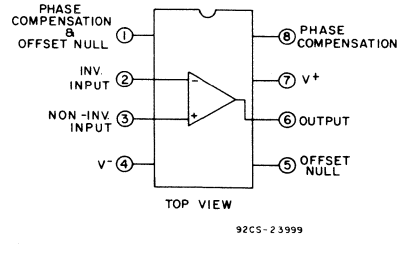
Applications:

- *Long-interval integrator*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*
- *Comparators*
- *Instrumentation*
- *AC/DC converters*
- *Inverting amplifiers*
- *Sine- & square-wave generators*
- *Capacitance multipliers & simulated inductors*



a — TO-5 Style package for all types

T-Suffix
S-Suffix



b — Plastic package for CA301A

E-Suffix

Fig. 1 - Functional diagrams.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **786**

CA101, CA201, CA301A, LM201, LM301A

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
- CA101, CA201 ..... 44 V
- CA301A ..... 36 V

DC INPUT VOLTAGE ..... ±15 V
(For supply voltages less than ±15 V, the Input Voltage rating is equal to the DC Supply Voltage)
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT SHORT-CIRCUIT DURATION ..... Indefinite*
DEVICE DISSIPATION:
- UP TO T_A = 75° C ..... 500 mW
- Above T_A = 75° C Derate linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating —
  - CA101 ..... -55 to +125° C
  - CA201, CA301A ..... 0 to +70° C
- Storage (All types) ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

* At $T_A \leq 70°$ C and $T_C \leq 125°$ C (CA101); $T_A \leq 55°$ C and $T_C \leq 70°$ C (CA201, CA301A).

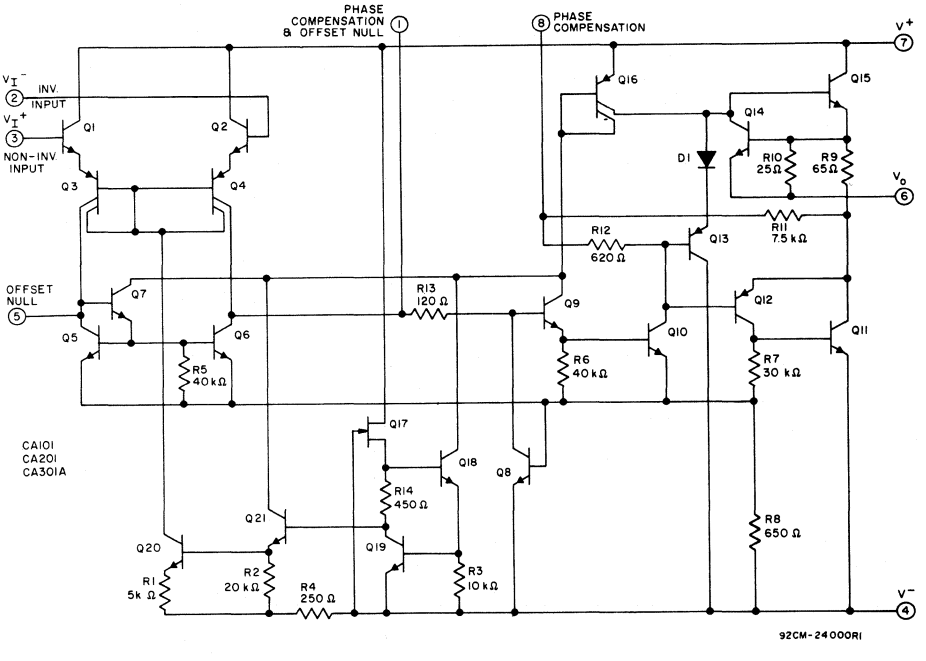


Fig. 2 - Schematic diagram.

CA101, CA201, CA301A, LM201, LM301A

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS Δ	LIMITS									UNIT
	Supply Voltage (V±) = 5 to 15 V	CA101			CA201			CA301A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_{IO}	T_A=25°C $R_S \leq 10k\Omega$	—	1	5	—	2	7.5	—	—	—	mV
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	2	7.5	
	$R_S \leq 10k\Omega$	—	—	6	—	—	10	—	—	—	
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	—	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}	$R_S \leq 10k\Omega$	—	6	—	—	10	—	—	—	—	μV/°C
	$R_S \leq 50\Omega$	—	3	—	—	6	—	—	—	—	
		—	—	—	—	—	—	—	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	-55°C to +25°C	—	—	—	—	—	—	—	—	—	nA/°C
	0°C to +25°C	—	—	—	—	—	—	—	0.02	0.6	
	+25°C to +70°C	—	—	—	—	—	—	—	0.01	0.3	
	+25°C to +125°C	—	—	—	—	—	—	—	—	—	
Input Offset Current I_{IO}	T_A = 0°C	—	—	—	—	150	750	—	—	—	nA
	T_A = 25°C	—	40	200	—	100	500	—	3	50	
	T_A = 70°C	—	—	—	—	50	400	—	—	—	
	T_A = 125°C	—	10	200	—	—	—	—	—	—	
		—	—	—	—	—	—	—	—	70	
	T_A = -55°C	—	100	500	—	—	—	—	—	—	
Input Bias Current I_{IB}	T_A = -55°C	—	0.28	1.5	—	—	—	—	—	—	μA
	T_A = 0°C	—	—	—	—	0.32	2	—	—	—	
	T_A = 25°C	—	0.12	0.5	—	0.25	1.5	—	0.07	0.25	
		—	—	—	—	—	—	—	—	0.3	
Supply Current $I_\pm$	T_A=25°C $V_\pm$=15V	—	—	—	—	—	—	—	1.8	3	mA
	$V_\pm$=20V	—	1.8	3	—	1.8	3	—	—	—	
	T_A=125°C $V_\pm$=20V	—	1.2	2.5	—	—	—	—	—	—	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C $V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	50	160	—	20	150	—	25	160	—	V/mV
	$V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	25	—	—	15	—	—	15	—	—	
Input Resistance R_I	T_A=25°C	0.3	0.8	—	0.1	0.4	—	0.5	2	—	MΩ
Output Voltage Swing V_{OPP}	$V_\pm$=15V R_L=10kΩ	±12	±14	—	±12	±14	—	±12	±14	—	V
	$V_\pm$=15V R_L=2kΩ	±10	±13	—	±10	±13	—	±10	±13	—	
Common-Mode Input-Voltage Range V_{ICR}	$V_\pm$=15V	±12	—	—	±12	—	—	±12	—	—	V
	$V_\pm$=20V	—	—	—	—	—	—	—	—	—	
Common-Mode Rejection Ratio CMRR	$R_S \leq 10k\Omega$	70	90	—	65	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	
Supply-Voltage Rejection Ratio PSRR	$R_S \leq 10k\Omega$	70	90	—	70	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	

Δ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified:
CA101: -55 to +125°C; CA201, CA301A: 0 to 70°C

CA101, CA201, CA301A, LM201, LM301A

TYPICAL STATIC CHARACTERISTICS
TYPE CA101

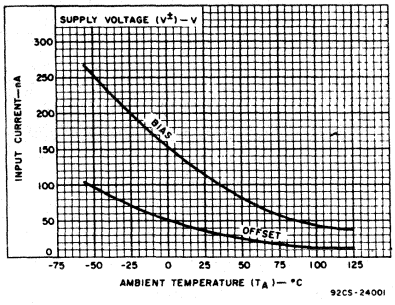


Fig. 3 - Input current (I_{IO}, I_{IB}) vs. temperature.

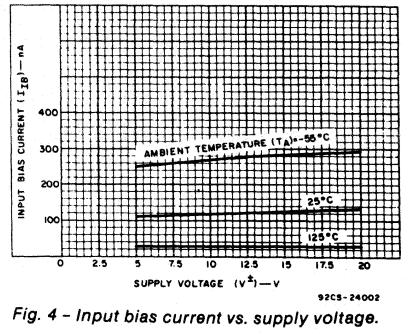


Fig. 4 - Input bias current vs. supply voltage.

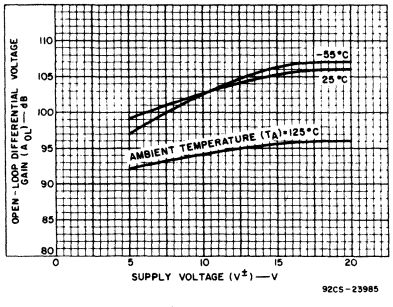


Fig. 5 - Voltage gain vs. supply voltage.

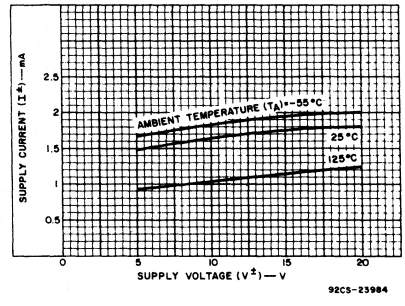


Fig. 6 - Supply characteristics.

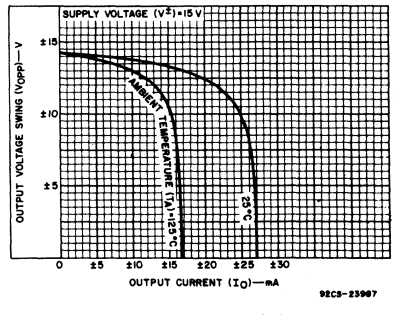


Fig. 7 - Output characteristics.

TYPE CA201

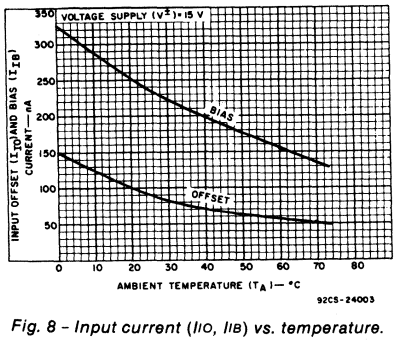


Fig. 8 - Input current (I_{IO}, I_{IB}) vs. temperature.

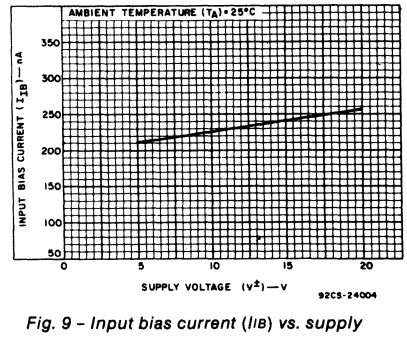


Fig. 9 - Input bias current (I_{IB}) vs. supply voltage.

CA101, CA201, CA301A, LM201, LM301A

TYPICAL STATIC CHARACTERISTICS (Cont'd)

TYPE CA201

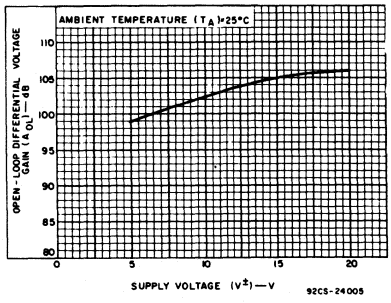


Fig. 10 – Voltage gain vs. supply voltage.

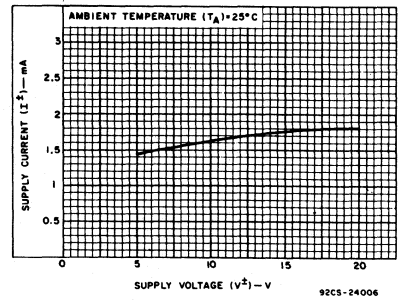


Fig. 11 – Supply characteristics.

TYPE CA301A

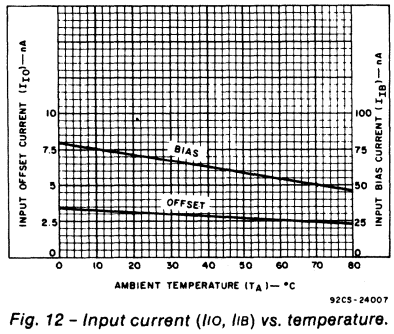


Fig. 12 – Input current (I_{IO}, I_{IB}) vs. temperature.

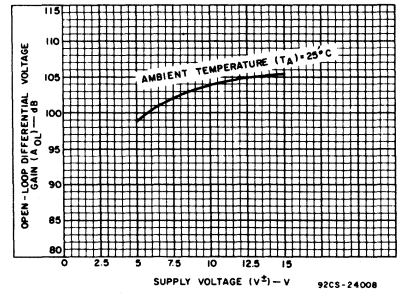


Fig. 13 – Voltage gain vs. supply voltage.

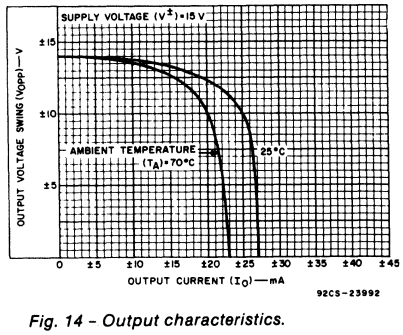


Fig. 14 – Output characteristics.

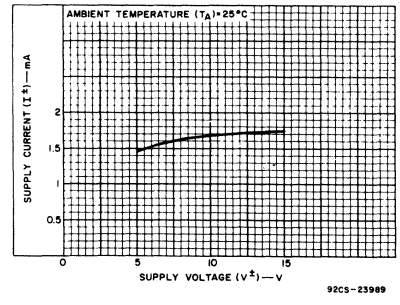


Fig. 15 – Supply characteristics.

TYPICAL DYNAMIC CHARACTERISTICS
TYPES CA101, CA201, CA301A

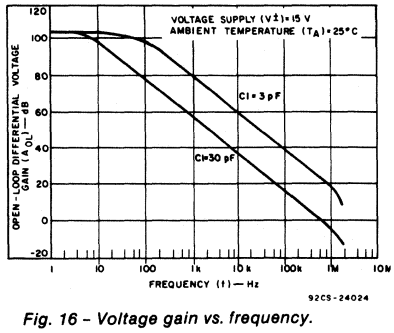


Fig. 16 – Voltage gain vs. frequency.

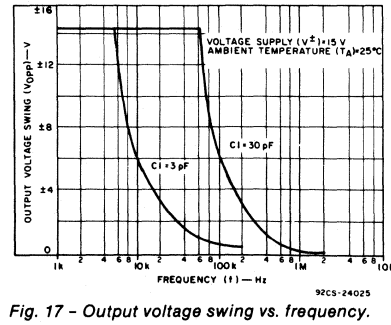


Fig. 17 – Output voltage swing vs. frequency.

CA101, CA201, CA301A, LM201, LM301A

TYPICAL DYNAMIC CHARACTERISTICS (Cont'd) FOR TYPES CA101, CA201 AND CA301A

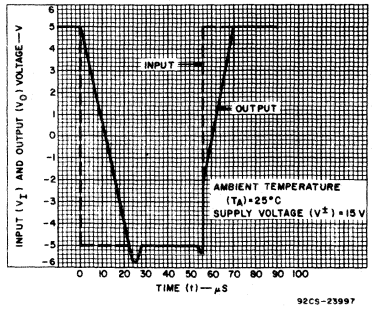


Fig. 18 - Voltage follower pulse response.

TYPE CA301A

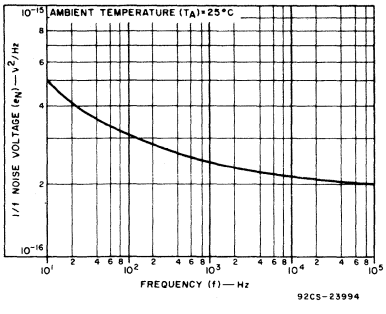


Fig. 19 - 1/f noise voltage vs. frequency.

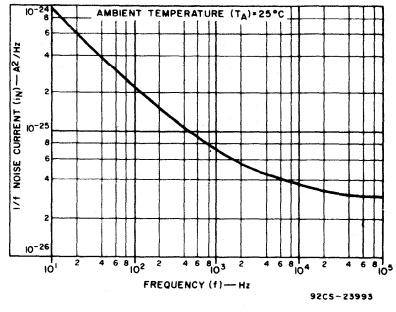
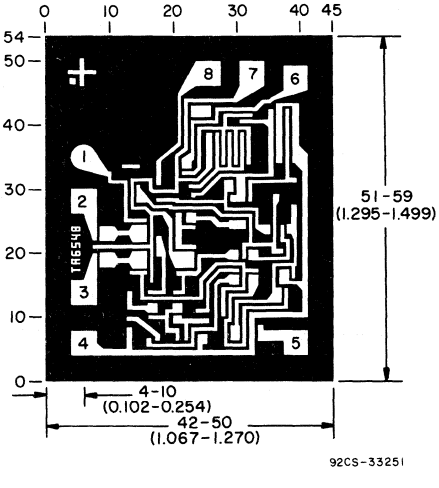


Fig. 20 - 1/f noise current vs. frequency.



Dimensions and pad layout for CA301H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA124, CA224, CA324, LM324*

Quad Operational Amplifiers

For Commerical, Industrial, and Military Applications

Features:

- *Operation from single or dual supplies*
- *Unity-gain bandwidth - 1 MHz (typ.)*
- *DC voltage gain - 100 dB (typ.)*
- *Input bias current - 45 nA (typ.)*
- *Input offset voltage - 2 mV (typ.)*
- *Input offset current -*
  5 nA (typ.) for CA224, CA324
  3 nA (typ.) for CA124
- *Replacement for industry types 124, 224, 324*

The RCA-CA124, CA224, and CA324 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range of from 0 V to V+ -1.5 V (single-supply operation) make the CA124, CA224, and CA324 suitable for battery operation.

The CA124, CA224, and CA324 are supplied in a 14-lead dual-in-line plastic package (E suffix) and is also available in chip form (H suffix).

Applications:

- *Summing amplifiers*
- *Mulivibrators*
- *Oscillators*
- *Transducer amplifiers*
- *DC gain blocks*

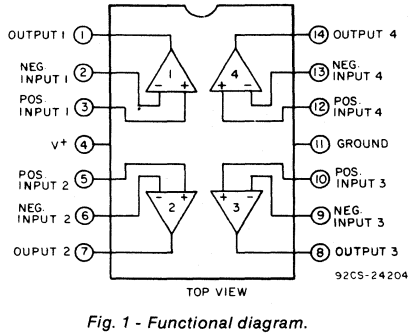


Fig. 1 - Functional diagram.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **796**

CA124, CA224, CA324, LM324

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	−0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

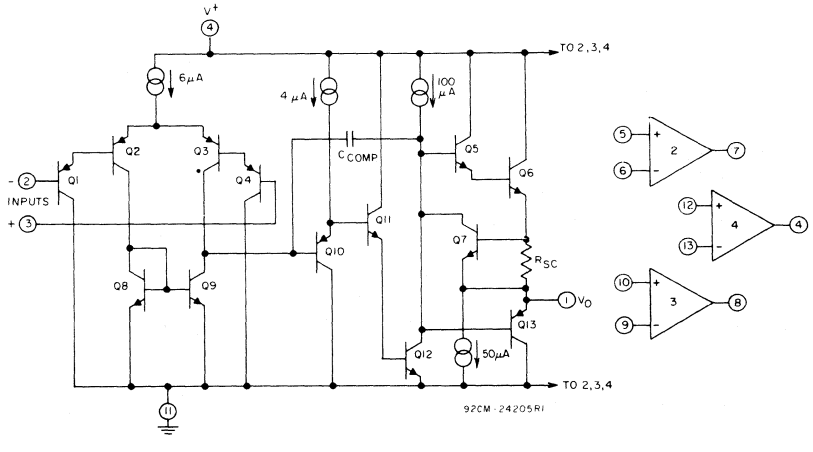


Fig. 2—Schematic diagram—one of four operational amplifiers.

CA124, CA224, CA324, LM324

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA124 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+=30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	94	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f=1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to +125°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	300	nA
Total Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L=2 kΩ, V^+=30 V	26	–	–	V
	R_L=10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L=10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

CA124, CA224, CA324, LM324

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA224, CA324 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+= 30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –40 to +85°C (CA224), T_A = 0 to 70°C (CA324)					
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	500	nA
Total Supply Current, I^+	R_L =∞ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	83	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L = 2 kΩ, V^+ = 30 V	26	–	–	V
	R_L = 10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L = 10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

CA124, CA224, CA324, LM324

TYPICAL CHARACTERISTICS CURVES

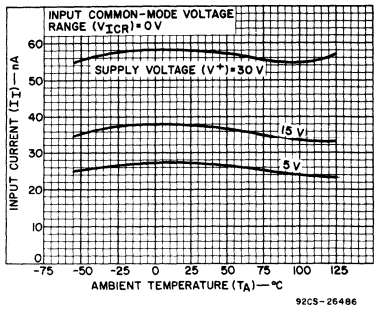


Fig. 3—Input current vs. ambient temperature.

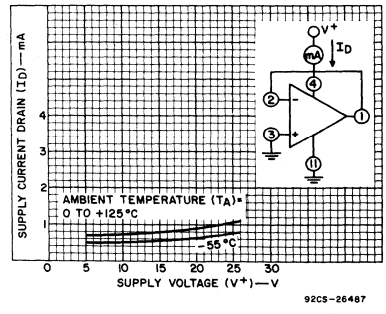


Fig. 4—Supply current drain vs. supply voltage.

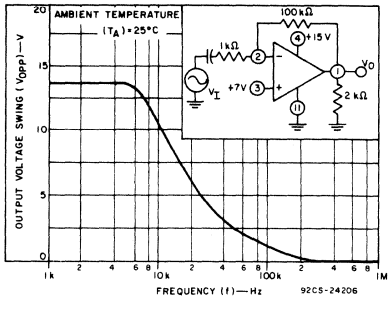


Fig. 5—Large-signal frequency response.

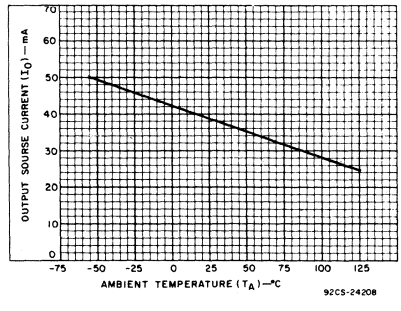


Fig. 6—Output current vs. ambient temperature.

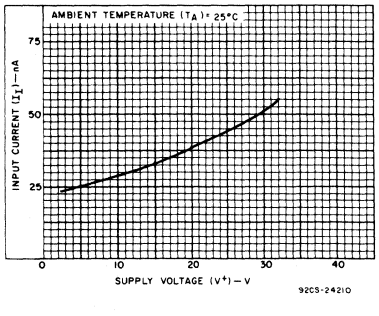


Fig. 7—Input current vs. supply voltage.

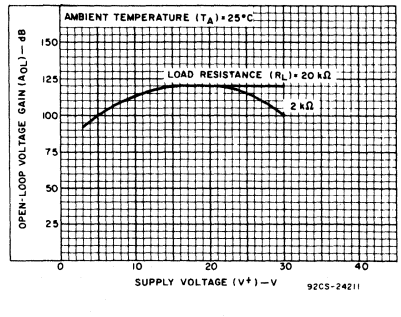


Fig. 8—Voltage gain vs. supply voltage.

TYPICAL CHARACTERISTICS CURVES (CONT'D)

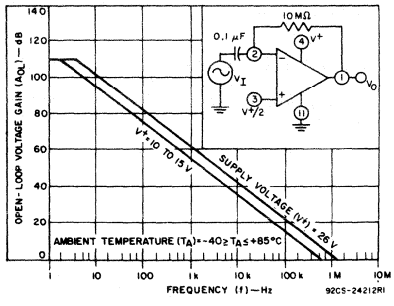


Fig. 9—Open-loop frequency response.

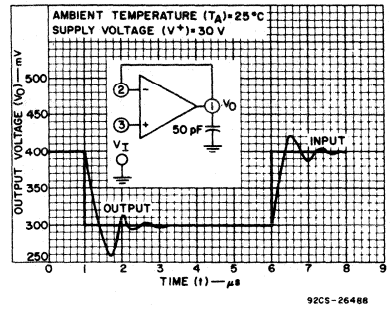


Fig. 10—Voltage follower pulse response (small signal).

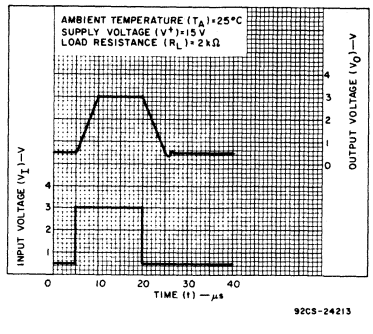


Fig. 11—Voltage follower pulse response.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358*, LM2904*

Dual Operational Amplifiers

For Commerical, Industrial, and Military Applications

Features:

- *Internal frequency compensation for unity gain*
- *High dc voltage gain - 100 dB typ.*
- *Wide bandwidth at unity gain - 1 MHz typ.*
- *Wide power supply range:*
  Single supply 3 to 30 V
  Dual supplies ± 1.5 to ± 15 V
- *Low supply current - 1.5 mA typ.*
- *Low input bias current*
- *Low input offset voltage and current*
- *Input common-mode voltage range includes ground*
- *Differental input voltage range equal to V+ range*
- *Large output voltage swing - 0 to V+ -1.5 V*

The RCA-CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from th single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types are supplied in 8-lead dual-in-line plasti packages (MINI-DIP, E suffix), 8-lead TO-5 style package with standard leads (T suffix), and with dual-in-line formec leads (DIL-CAN, S suffix). The CA358 is also supplied ir chip form (H suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types are an equivalent to or a replacement fo the industry types 158, 158A, 258, 258A, 358, 358A, anc CA2904.

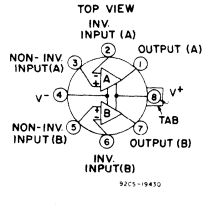


Fig. 1 - Functional diagram for CA158, CA258, and CA358 S- and T-suffix types.

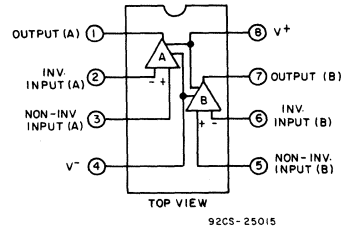


Fig. 2 - Functional diagram for CA158, CA258, CA358, and CA2904 E-suffix types.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **1019**

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE, V^+:	
CA2904	26 V or ± 13 V
Other Types	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE:	
All Types	±32 V
INPUT VOLTAGE	−0.3 V to V^+ V
INPUT CURRENT ($V_I < -0.3$ V) [+]	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leqslant 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	630 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/^{o}C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to + 125^{o}C
Storage	−65 to + 150^{o}C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 300 ^{o}C

[+] This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

* The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

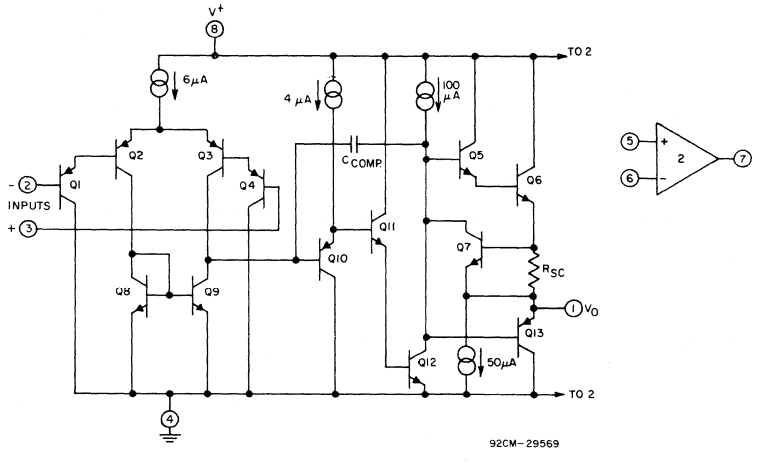


Fig.3 – Schematic diagram – one of two operational amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	1	2	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	10	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	20	50	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = –55 to +125°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA258A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	1	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	15	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	40	80	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –25 to +85°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, $\propto V_{IO}$	R_S = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, $\propto I_{IO}$		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358A (E. T. S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	100	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	5	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	20	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	75	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	300	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	200	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS Supply Voltage (V^+) = 5 V Unless Otherwise Specified	LIMITS CA158 (E, T, S) CA258 (E, T, S) Min.	Typ.	Max.	UNITS
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to + 125°C (CA158); T_A = –25 to +85°C (CA258)				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	300	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA2904E			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
T_A = 25°C					
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 10 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+ = 15 V	10	20	–	mA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq 2$ kΩ, V^+ = 15 V (For large V_O swing)	—	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	50	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	50	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
T_A = -40 to +85°C					
Input Offset Voltage, V_{IO}	Note 3	–	–	10	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	45	200	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is $V^+ - 1.5$ V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to $V^+ - 1.5$ V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

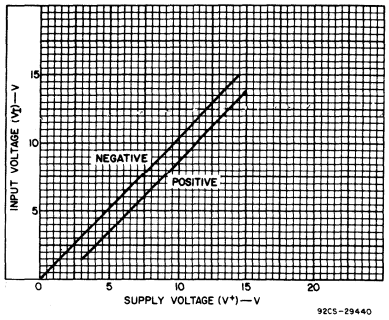


Fig.4 — Input voltage range as a function of supply voltage.

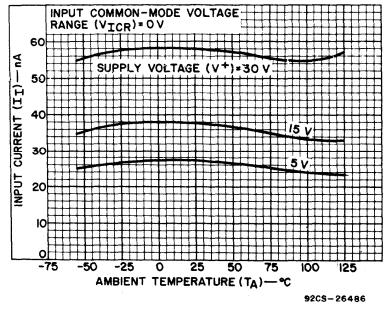


Fig.5 — Input current as a function of ambient temperature.

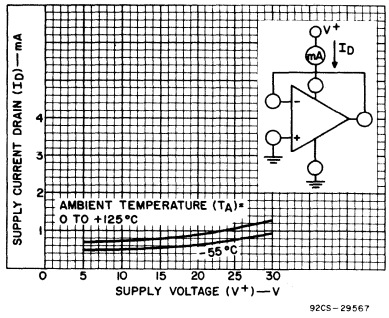


Fig.6 — Supply current drain as a function of supply voltage.

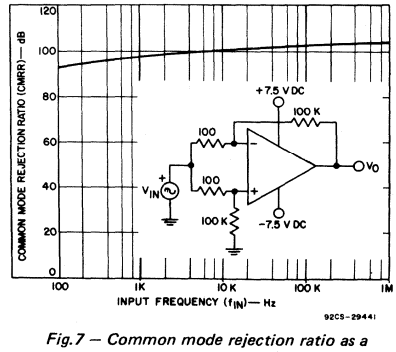


Fig.7 — Common mode rejection ratio as a function of input frequency.

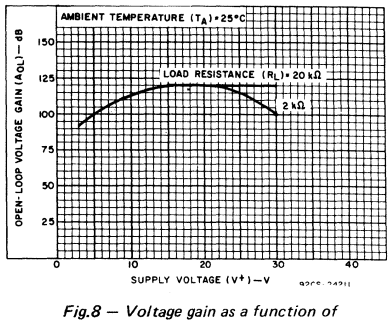


Fig.8 — Voltage gain as a function of supply voltage.

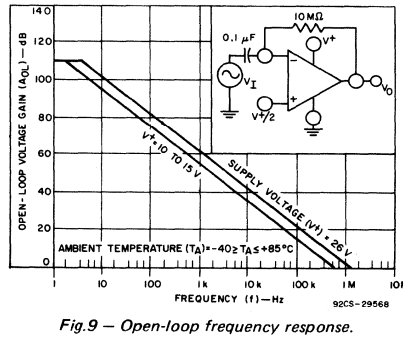


Fig.9 — Open-loop frequency response.

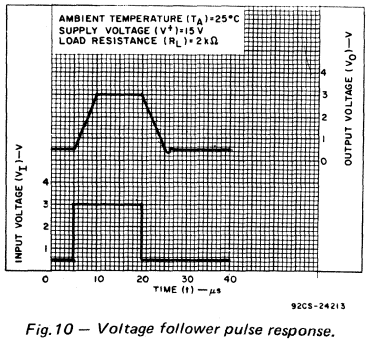


Fig.10 — Voltage follower pulse response.

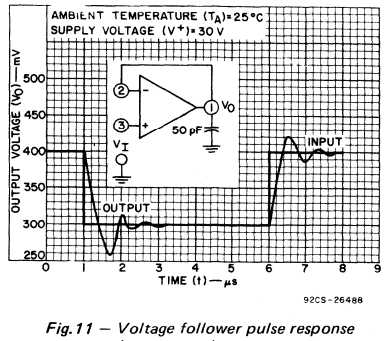


Fig.11 — Voltage follower pulse response (small signal).

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904

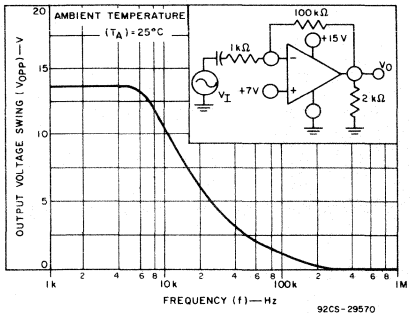


Fig. 12 — Large-signal frequency response.

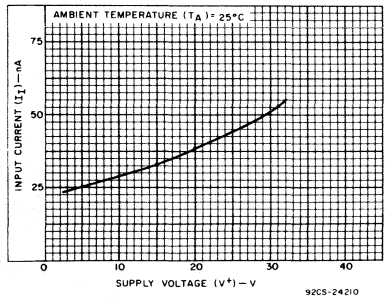


Fig. 13 — Input current as a function of supply voltage.

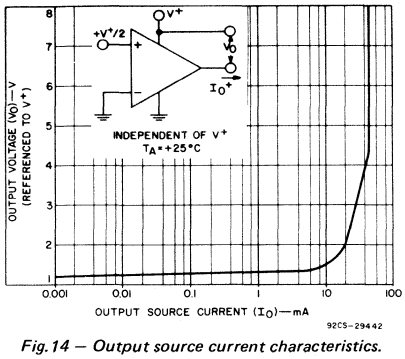


Fig. 14 — Output source current characteristics.

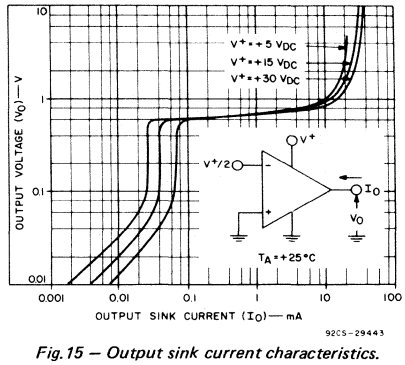


Fig. 15 — Output sink current characteristics.

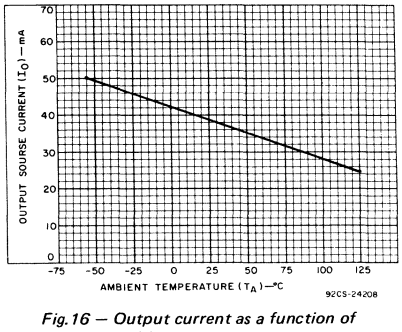


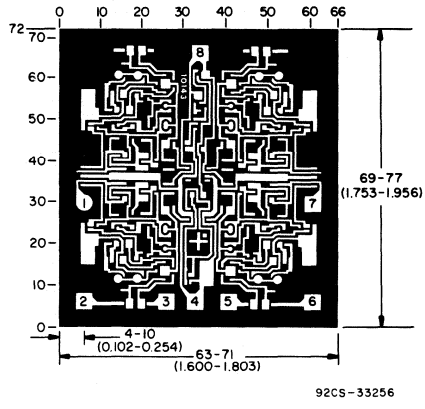
Fig. 16 — Output current as a function of ambient temperature.

ORDERING INFORMATION

These packages are identified by Suffix Letters indicated in the chart shown below. When ordering these devices, it is important that the appropriate suffix letter be affixed to the type number of the device required.

PACKAGE	SUFFIX LETTERS	TYPES
8-Lead Dual-In-Line Plastic with	E	CA158, A CA258, A CA358, A CA2904
8-Lead TO-5 Style with Standard Leads	T	CA158, A CA258, A CA358, A
8-Lead TO-5 Style with Dual-In-Line Formed Leads	S	

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358, LM2904



Dimensions and pad layout for CA358H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA307, LM307*

Operational Amplifier

For Military, Industrial, and Commerical Applications

Applications:

- *Long-interval integrators*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*

The RCA CA307 is a general-purpose operational amplifier intended for use in military, industrial, and commerical applications. A 30-pF on-chip capacitor provides internal frequency compensation.

The CA307 is available in 8-lead TO-5 style packages with standard leads (T suffix), with dual-in-line formed leads ("DIL-CAN", S suffix), in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

The CA307 is a direct replacement for industry type 307 in packages with similiar terminal arrangements.

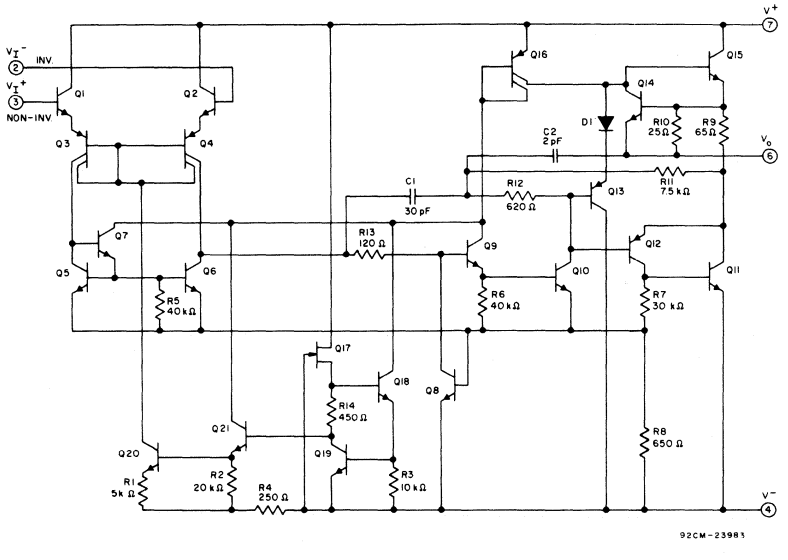


Fig. 1 - Schematic diagram of CA307.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **785**

CA307, LM307

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
CA307 36
DC INPUT VOLTAGE ..... ±15
(For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage)
DIFFERENTIAL INPUT VOLTAGE ..... ±30
OUTPUT SHORT-CIRCUIT DURATION* ..... Indefinit
DEVICE DISSIPATION UP TO T_A = 70° C ..... 500 mV
Above T_A = 70° C Derate linearly at ..... 6.67 mW/° C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0° C to +70° C
Storage ..... -65° C to +150° C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

*For type CA307 continuous short circuit is allowed for Case Temperature to +70° C and ambient temperature to +55° C.
†Types CA307 E, S, and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrica specifications apply only over the temperature range of 0 to 70° C.

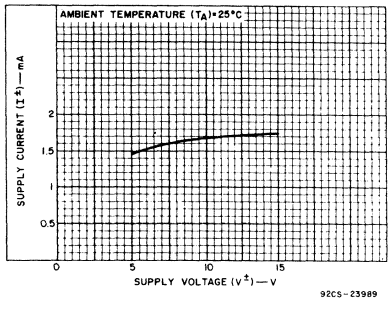


Fig. 2 - Supply current vs. supply voltage.

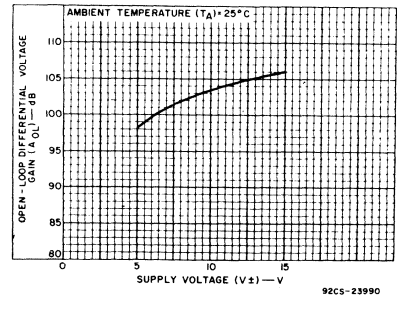


Fig. 3 - Open-loop differential voltage gain vs. supply voltage.

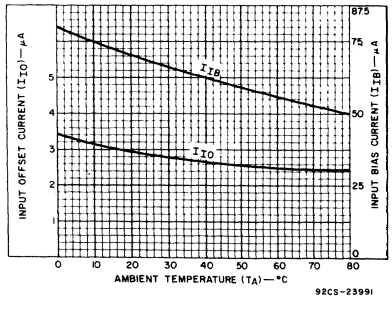


Fig. 4 - Input offset and input bias current vs. ambient temperature.

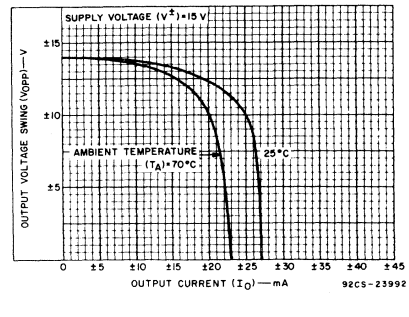
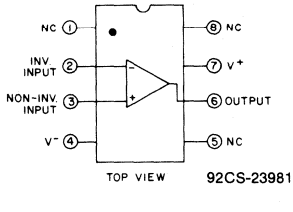


Fig. 5 - Output voltage swing vs. output current.

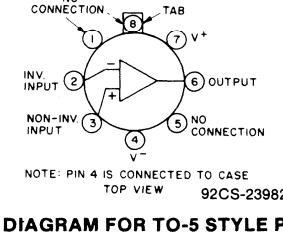
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS△	LIMITS			UNITS
		Supply Voltage (V±) = 5 V to 15 V	CA307			
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	T_A = 25° C, $R_S \leq$ 50 kΩ	—	2	7.5	mV
		$R_S \leq$ 50 kΩ	—	—	10	
Average Temperature Coefficient of Input Offset Voltage	αV_{IO}		—	6	30	μV/° C
Input Offset Current	I_{IO}		—	—	70	nA
		T_A = 25° C	—	3	50	
Average Temperature Coefficient of Input Offset Current	αI_{IO}	+25 to 70° C	—	0.01	0.3	nA/° C
		0 to +25° C	—	0.02	0.6	
Input Bias Current	I_{IB}		—	—	300	nA
		T_A = 25° C	—	70	250	
Supply Current	$I_\pm$	T_A = +125° C, V± = 20 V	—	—	—	mA
		T_A = 25° C, V± = 15 V	—	1.8	3	
Open-Loop Differential Voltage Gain	A_{OL}	V± = 15 V, V_O = ±10V, $R_L \geq$ 2kΩ	15	—	—	V/mV
		V±=15V, V_O=±10 V, R_L≥2kΩ, T_A=25° C	25	160	—	
Input Resistance	R_I	T_A = 25° C	0.5	2	—	MΩ
Output Voltage Swing	V_{OPP}	V± = 15 V, R_L = 10 kΩ	±12	±14	—	V
		V± = 15 V, R_L = 2 kΩ	±10	±13	—	
Input Voltage Range	V_{ICR}	V± = 15 V	±12	—	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq$ 50 kΩ	70	90	—	dB
Supply-Voltage Rejection Ratio	PSRR	$R_S \leq$ 50 kΩ	70	96	—	dB

△Characteristics applicable over operating temperature range T_A = 0 to 70° C unless otherwise specified.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGES

CA307, LM307

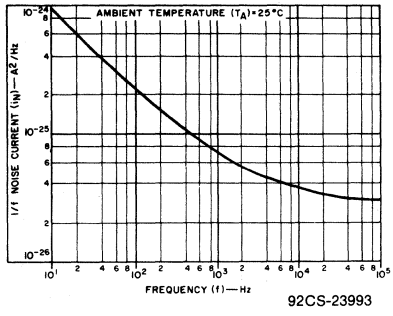


Fig. 6 - 1/f noise current vs. frequency.

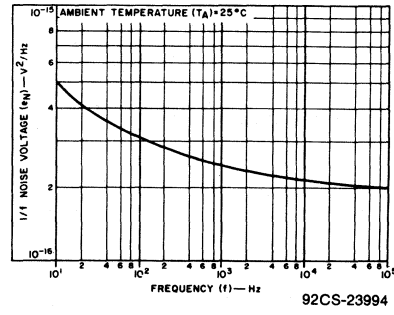


Fig. 7 - 1/f noise voltage vs. frequency.

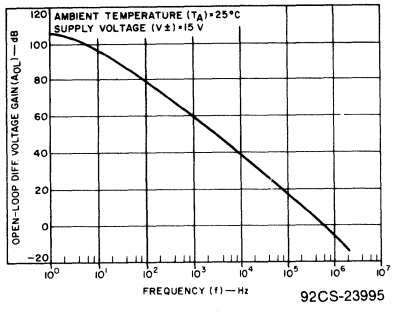


Fig. 8 - Open-loop differential voltage gain vs. frequency.

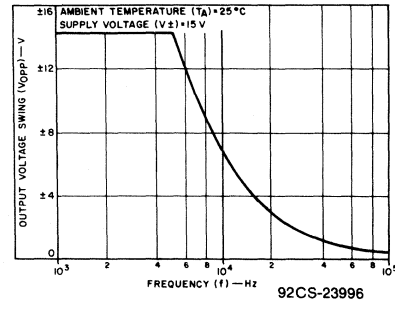


Fig. 9 - Output voltage swing vs. frequency.

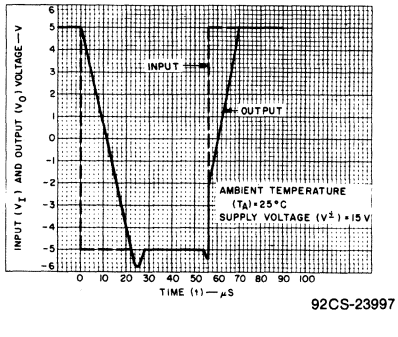
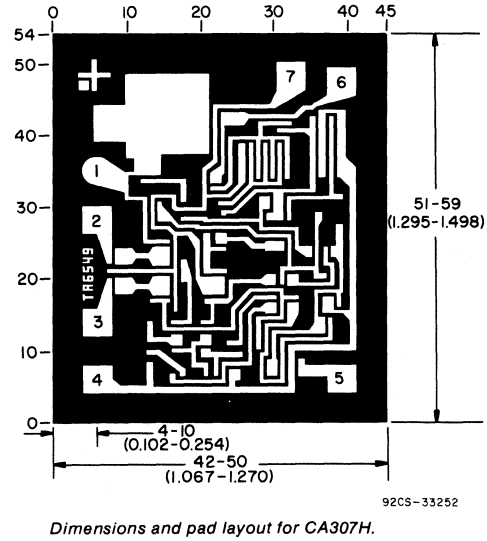


Fig. 10 - Input and output voltage vs. time.



Dimensions and pad layout for CA307H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA741, CA747, CA748, CA1458, CA1558, LM741*, LM748*, LM1458*, LM1558*

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commerical Applications

Features:

- *Input bias current (all types):* *500 nA max.*
- *Input offset current (all types):* *200 nA max.*

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

RCA's manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

Applications:

- *Comparator*
- *DC amplifier*
- *Integrator or differentiator*
- *Multivibrator*
- *Narrow-band or band-pass filter*
- *Summing amplifier*

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

TYPE NO.	PACKAGE TYPE AND SUFFIX LETTER							FIG. NO.
	TO-5 STYLE			PLASTIC		CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L			
CA1458	T		S	E		H		1d, 1h
CA1558	T		S	E				1d, 1h
CA741C	T		S	E		H		1a, 1e
CA741	T		S	E			L	1a, 1e
CA747C		T			E	H		1b, 1f
CA747		T			E			1b, 1f
CA748C	T		S	E		H		1c, 1g
CA748	T		S	E				1c, 1g

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^\circ C$:

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . . . 44 V

Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . . . 500 mW
- Up to 75°C (CA741, CA748) . . . . . 500 mW
- Up to 30°C (CA747) . . . . . 800 mW
- Up to 25°C (CA747C) . . . . . 800 mW
- Up to 30°C (CA1558) . . . . . 680 mW
- Up to 25°C (CA1458) . . . . . 680 mW

For Temperatures Indicated Above . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . . . ±0.5 V
Ambient Temperature Range:
- Operating – CA741, CA747E, CA748, CA1558 . . . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . . . 0 to +70 °C†
- Storage . . . . . −65 to +150 °C

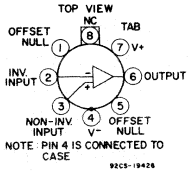
Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265 °C

* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

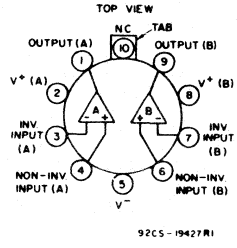
▲ Voltage values apply for each of the dual operational amplifiers.

† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

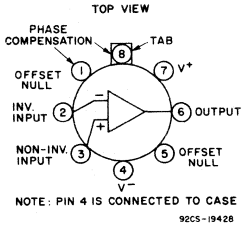
CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558



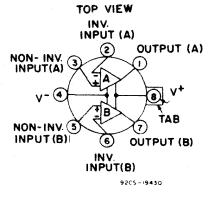
1a.–CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation.



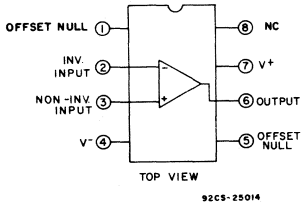
1b.–CA747CT and CA747T with internal phase compensation.



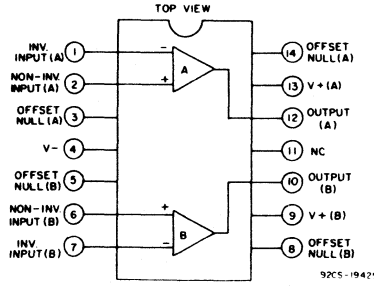
1c.–CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.



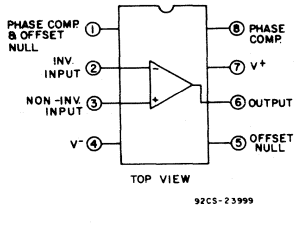
1d.–CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



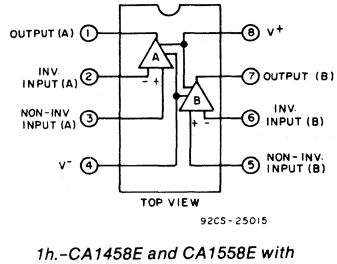
1e.-CA741C and CA741E with internal phase compensation.



1f.-CA747CE and CA747E with internal phase compensation.



1g.-CA748CE and CA748E with external phase compensation.



1h.-CA1458E and CA1558E with internal phase compensation.

Fig. 1 – Functional diagrams.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

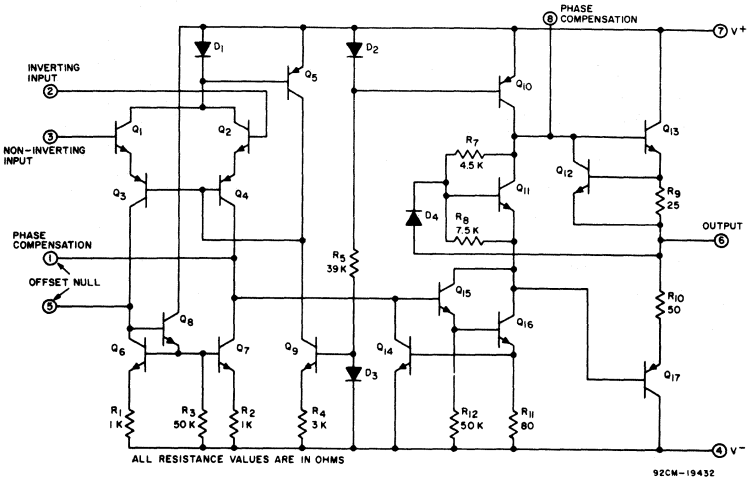


Fig.2–Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

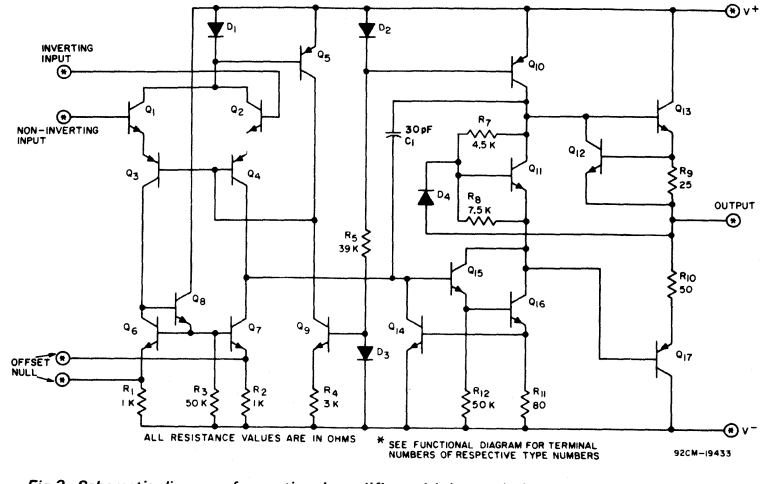


Fig.3–Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V\pm$ = ±15 V *	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, V_I = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq$ 2 kΩ	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	

▲ Open-loop slew rate applies only for types CA748C and CA748.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V	Ambient Temperature, T_A	LIMITS CA741C, CA747C*, CA748C, CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq$ 10 kΩ	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V_O = ±10 V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq$ 10 kΩ	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq$ 10 kΩ	25 °C	±12	±14	–	V
	$R_L \geq$ 2 kΩ	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V	Ambient Temperature, T_A	LIMITS CA741 CA747* CA748 CA1558*			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio , CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

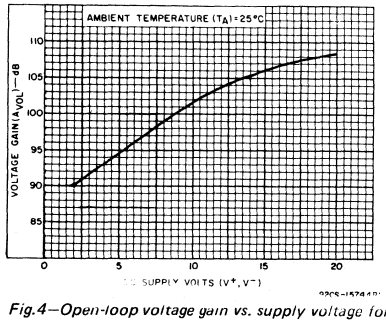


Fig.4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

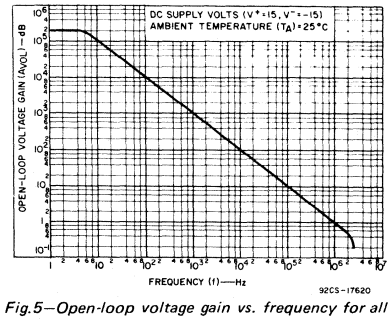


Fig.5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

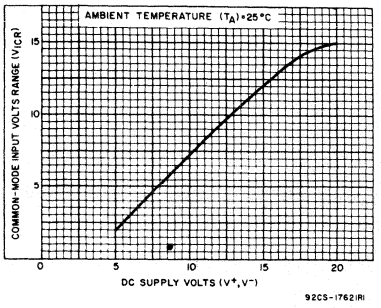


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

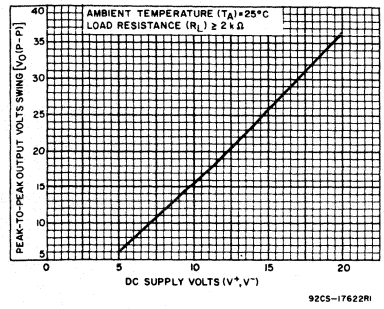


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

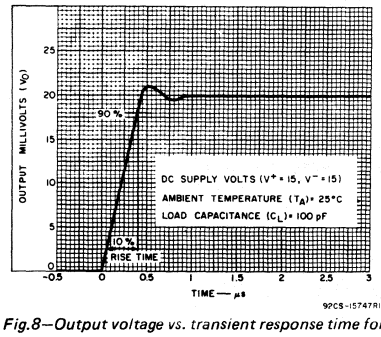


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

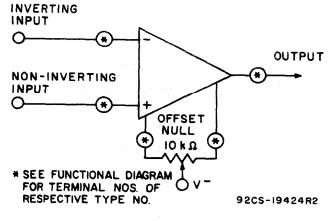


Fig.9—Voltage offset null circuit for CA741C, CA741, CA747CE, and CA747E.

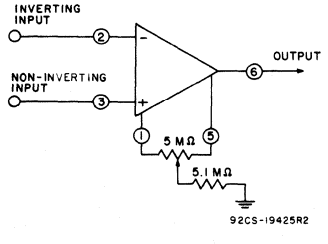


Fig.10—Voltage-offset null circuit for CA748C and CA748.

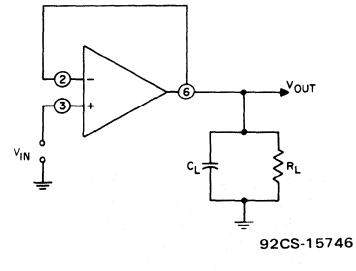


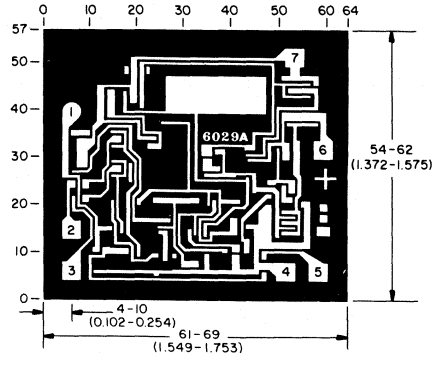
Fig.11—Transient response test circuit for all types.

CA741, CA747, CA748, CA1458, CA1558, LM741, LM748, LM1458, LM1558

CHIP PHOTOS

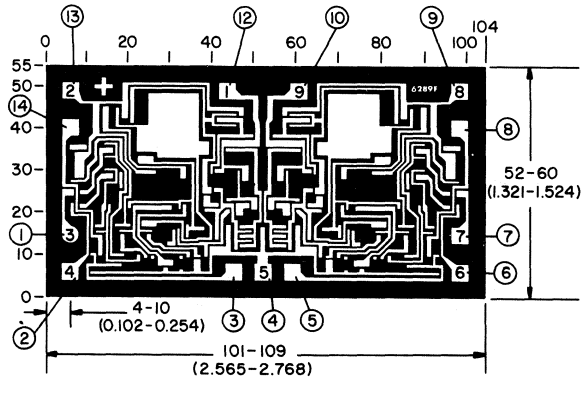
Dimensions and Pad Layouts

CA741CH



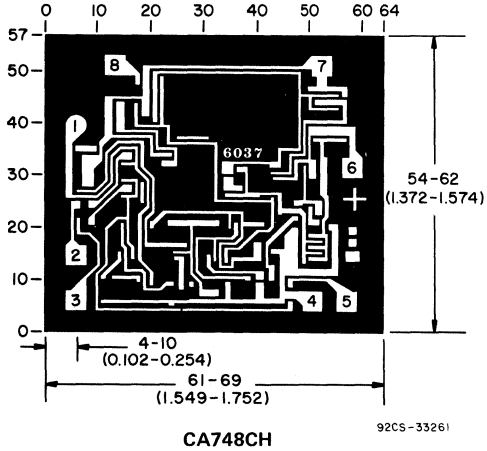
92CS-33259

CA747CH



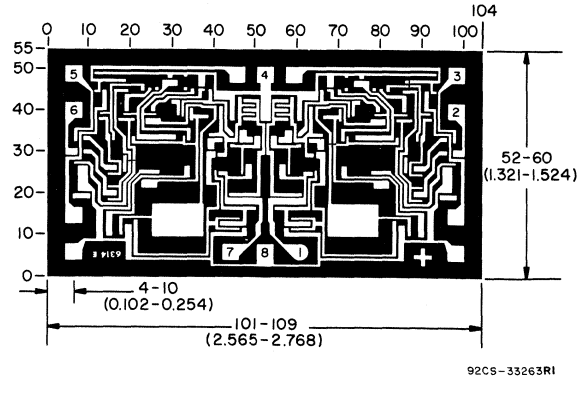
NOTE: NOS. IN PADS ARE FOR 10-LEAD TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-33260



92CS-33261

CA748CH



92CS-33263R1

CA1458H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

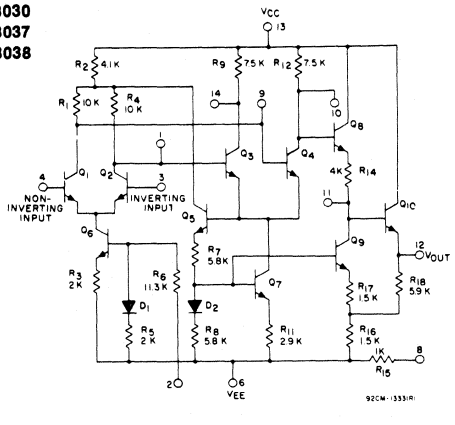
Operational Amplifiers

Features:
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from -55° C to +125° C for TO-5 style, and ceramic dual-in-line packages; 0° C to +70° C for plastic dual-in-line packages*

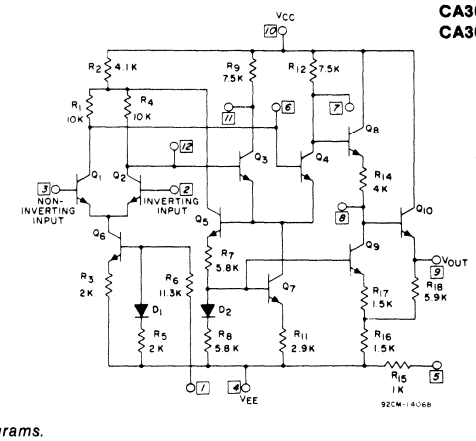
6-Volt Types	12-Volt Types	Package
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3030	14-Lead Plastic Dual-In-Line
CA3037	CA3038	14-Lead Ceramic Dual-In-Line

Applications:
- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Balanced modulator-driver*

CA3029
CA3030
CA3037
CA3038



CA3010
CA3015



Schematic diagrams.

File Number **316**

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3029 CA3037	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010	CA3029 CA3037	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 CA3029, CA3037) 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3030 CA3038	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015	CA3030 CA3038	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 CA3030, CA3038) 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015 (Substrate DO NOT GROUND				

	CA3010 CA3037 CA3015 CA3038	CA3029 CA3030
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C	-65°C to +150°C

	CA3030 CA3038	CA3015	CA3029	CA3010 CA3037
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V		-4 V to +1 V	
MAXIMUM DEVICE DISSIPATION	600 mW		300 mW	

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 CA3029, CA3030, CA3037, CA3038), Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3010 CA3029 CA3037 Min.	CA3010 CA3029 CA3037 Typ.	CA3010 CA3029 CA3037 Max.	CA3015 CA3030 CA3038 Min.	CA3015 CA3030 CA3038 Typ.	CA3015 CA3030 CA3038 Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMRR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	0.5 to -4 -	- -	- -	- 0.65 to -8	- -	- -	V	none

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015.

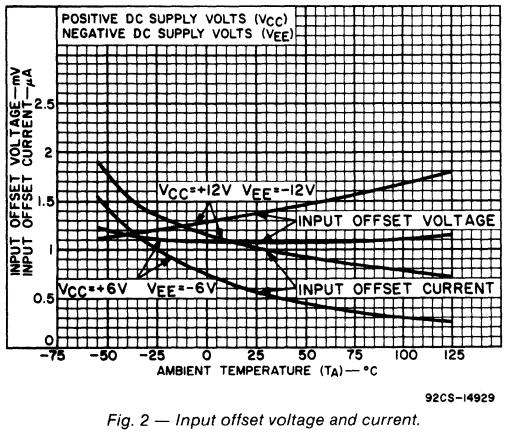


Fig. 2 — Input offset voltage and current.

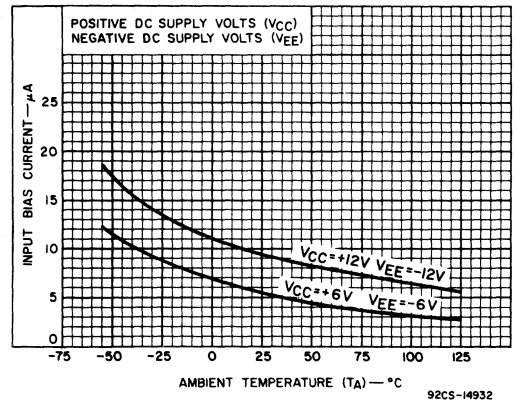


Fig. 3 — Input bias current.

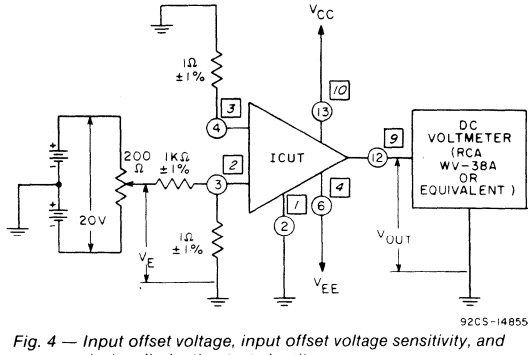


Fig. 4 — Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit

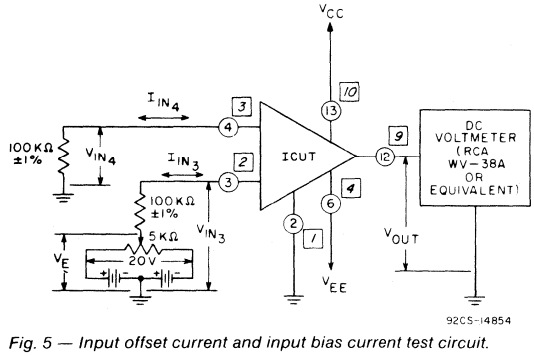


Fig. 5 — Input offset current and input bias current test circuit.

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal (13) or [10]

I_E = Direct Current out of Terminal (6) or [4]

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015.

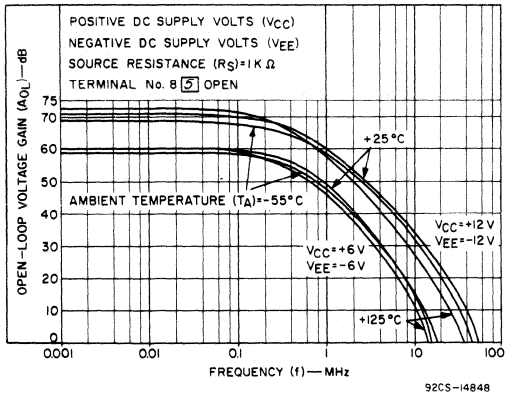


Fig. 6 — Open-loop voltage gain vs. frequency for CA3010, CA3015, CA3037, CA3038

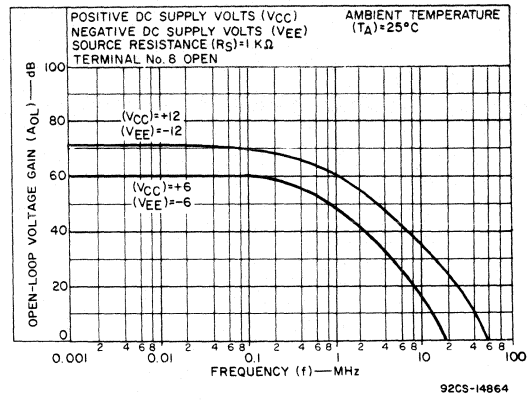
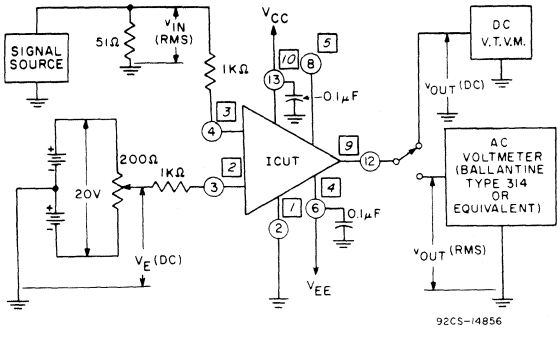


Fig. 7 — Open-loop voltage gain vs. frequency for CA3029 and CA3030



Procedure:

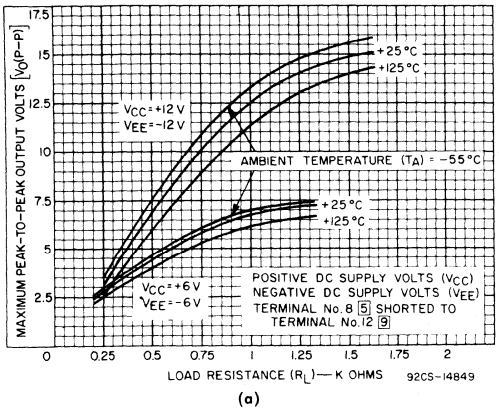
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

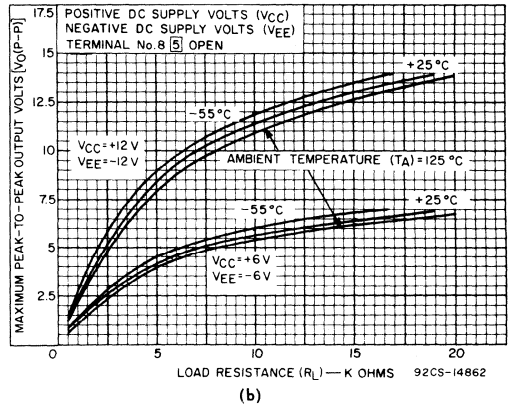
3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.
   Reference Level = A_{OL} at 1 kHz.

Fig.8

Fig. 8 — Open-loop differential voltage gain, maximum peak-to-peak output voltage, and open-loop bandwidth at -3 dB point test circuit



(a)



(b)

Fig. 9 — Maximum peak-to-peak output voltage vs. load resistance for CA3010, CA3015, CA3037, CA3038

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015.

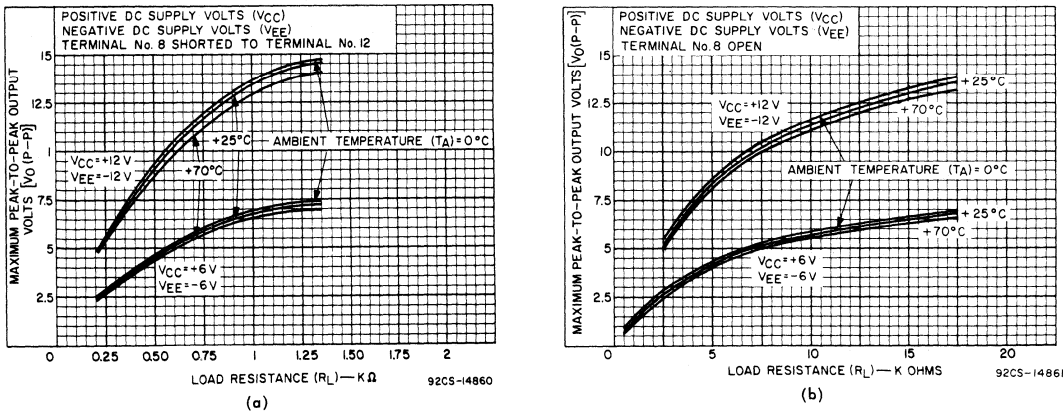
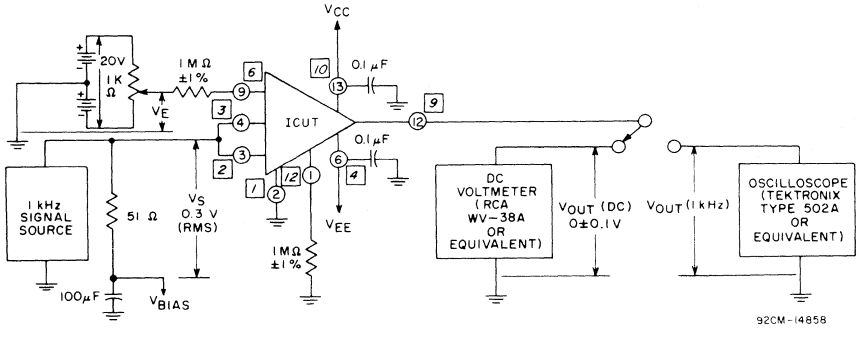


Fig. 10 — Maximum peak-to-peak output voltage vs. load resistance for CA3029 and CA3030



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for $V_{OUT}(DC)$ = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig. 11 — Common-mode rejection ratio and common-mode input-voltage-range test circuit.

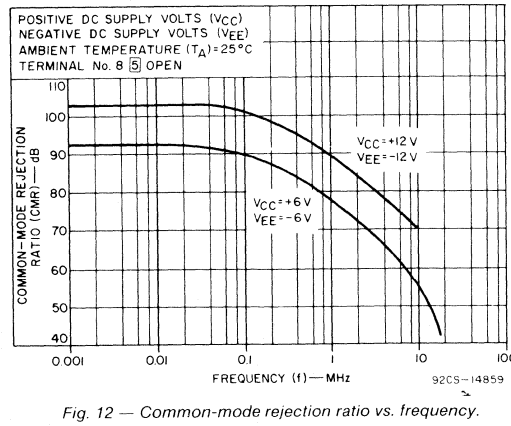


Fig. 12 — Common-mode rejection ratio vs. frequency.

CA3010, CA3015, CA3029, CA3030, CA3037, CA3038

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030, CA3037, CA3038;
Italic Numbers in Square Boxes are for CA3010, CA3015.

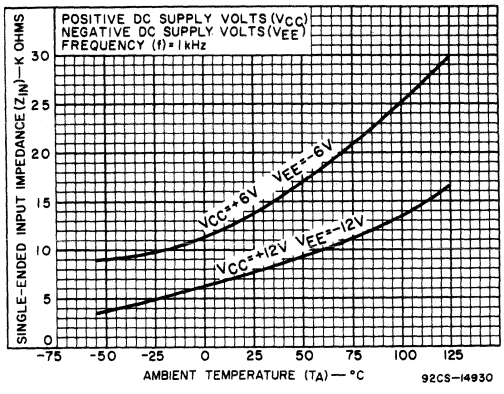


Fig. 13 — Single-ended input impedance vs. temperature.

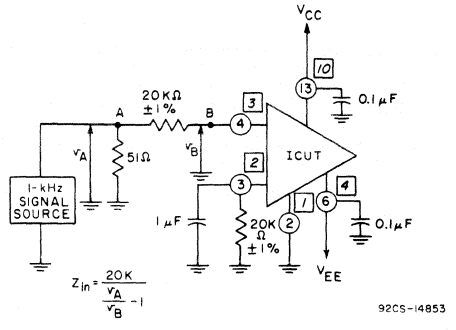
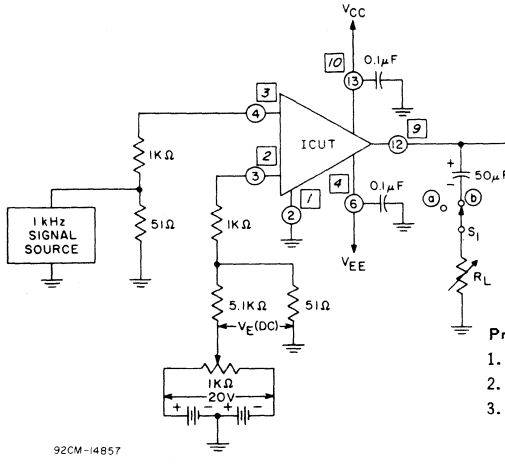
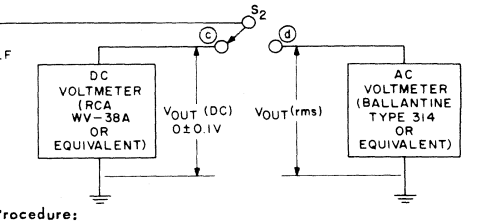


Fig. 14 — Single-ended input impedance test circuit.





Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

Fig. 15 — Output impedance test circuit.

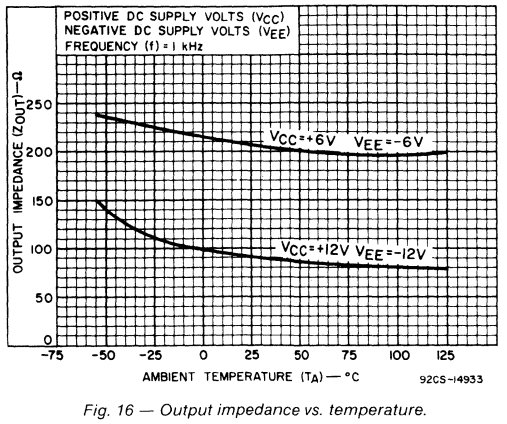


Fig. 16 — Output impedance vs. temperature.

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

Operational Amplifiers

Features:

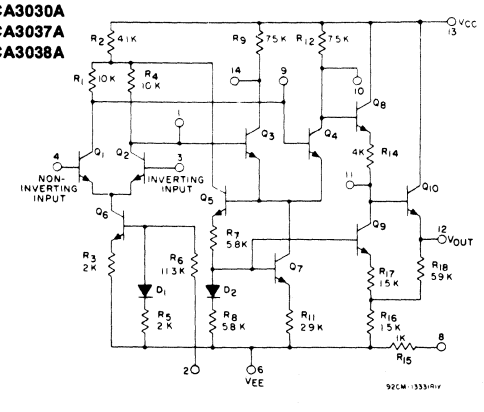
- *These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance*
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from -55° C to +125° C for flat pack, TO-5 style, and ceramic dual-in-line packages; 0° C to +70° C for plastic dual-in-line packages*

6-Volt Types	12-Volt Types	Package
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual-In-Line (TO-116)
CA3037A	CA3038A	14-Lead Ceramic Dual-In-Line (TO-116)

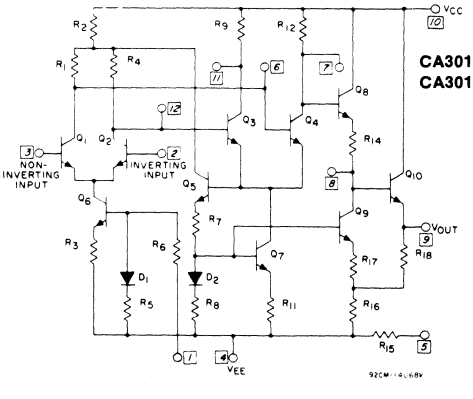
Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Scaling adder*
- *Balanced modulator-driver*

CA3029A
CA3030A
CA3037A
CA3038A



CA3010A
CA3015A



Schematic diagrams.

File Number **310**

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3029A CA3037A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3029A CA3037A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 CA3029A, CA3037A) 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3030A CA3038A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3030A CA3038A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 CA3030A, CA3038A) 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3010A CA3015A CA3037A CA3038A	CA3029A CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +80°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C

	CA3030A CA3038A	CA3029A CA3037A CA3010A CA3015A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A, CA3037A, CA3038A;
Italic Numbers in Square Boxes are for CA3010A, CA3015A.

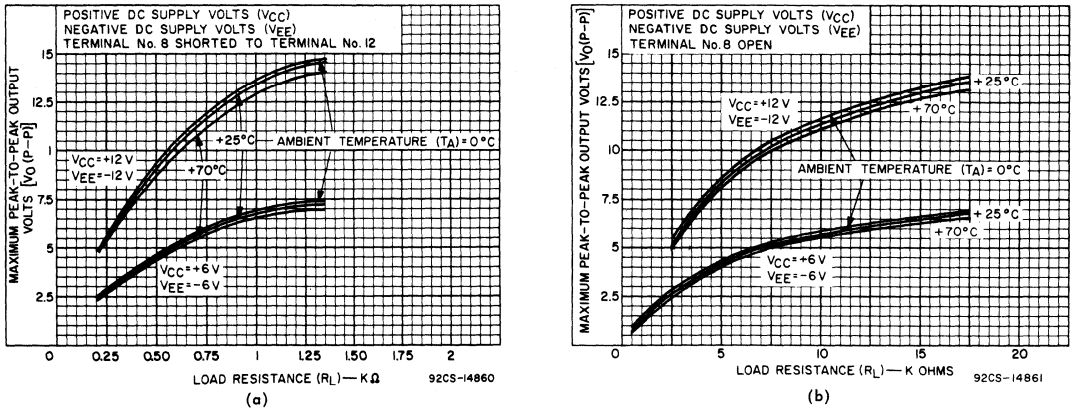
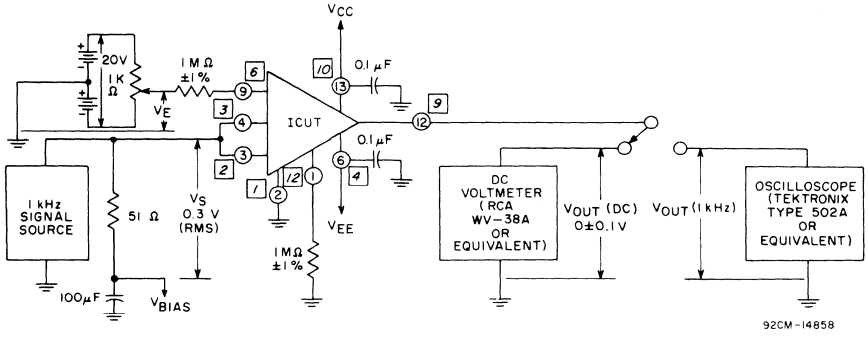


Fig. 10 — Maximum peak-to-peak output voltage vs. load resistance for CA3029A and CA3030A.



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig. 11 — Common-mode rejection ratio and common-mode input-voltage-range test circuit.

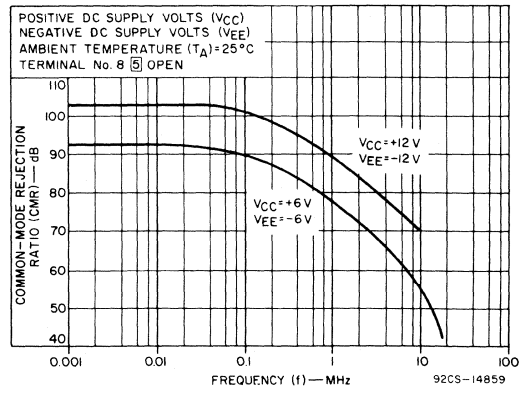


Fig. 12 — Common-mode rejection ratio vs. frequency.

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

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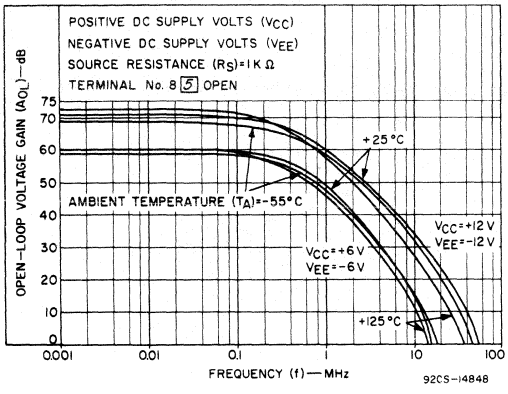


Fig. 6 — Open loop voltage gain vs. frequency for CA3015A, CA3016A, CA3037A, CA3038A.

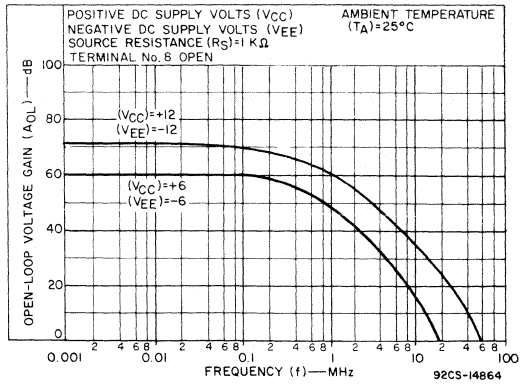
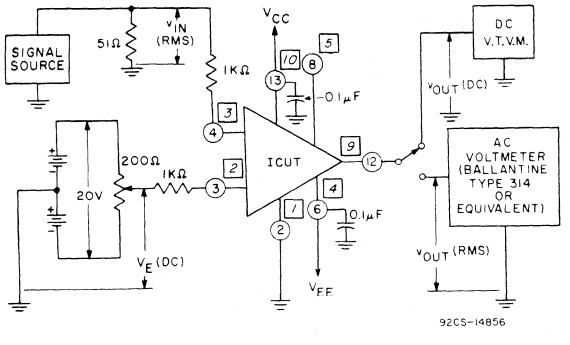


Fig. 7 — Open loop voltage gain vs. frequency for CA3029A and CA3030A.



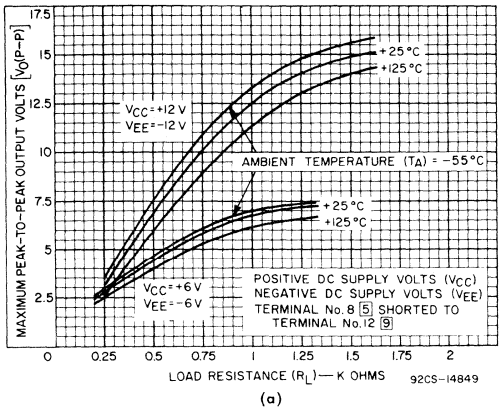
Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point
   Reference Level = A_{OL} at 1 kHz

Fig. 8 — Open-loop differential voltage gain, maximum peak-to-peak output voltage, and open-loop bandwidth at -3 point test circuit.



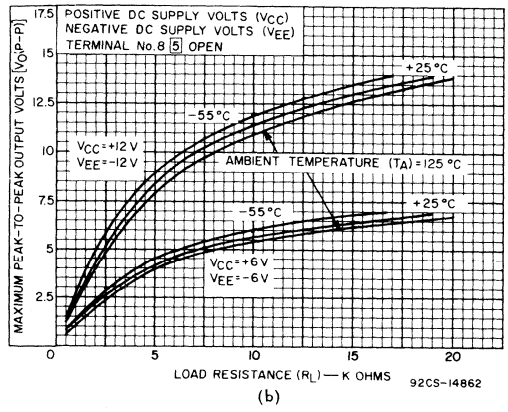


Fig. 9 — Maximum peak-to-peak output voltage vs. load resistance for CA3010A, CA3015A, CA3037A, CA3038A.

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A, CA3037A, CA3038A;
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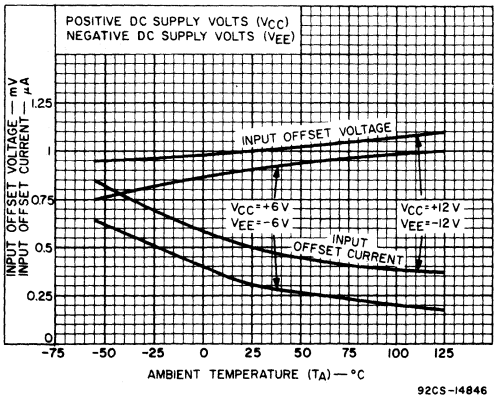


Fig. 2 — Input offset voltage and current

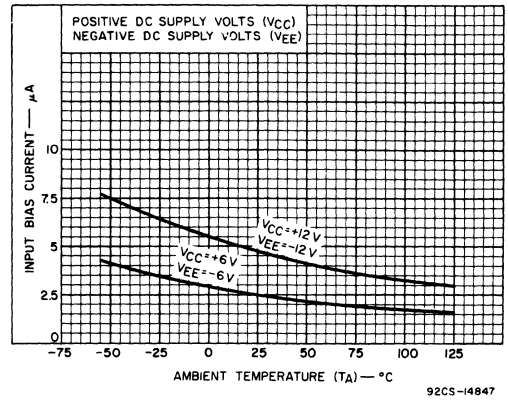


Fig. 3 — Input bias current

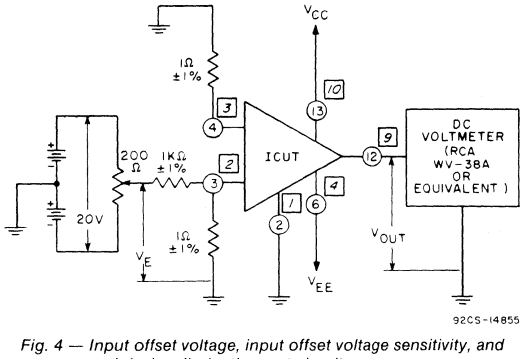


Fig. 4 — Input offset voltage, input offset voltage sensitivity, and and device dissipation test circuit.

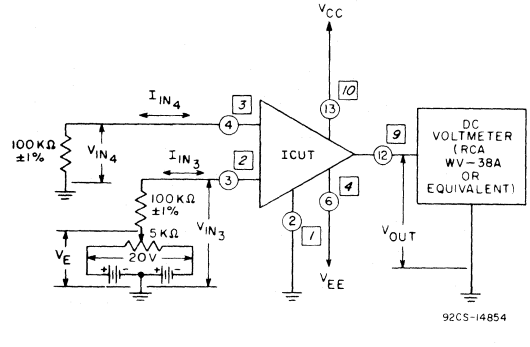


Fig. 5 — Input offset current and input bias current test circuit.

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or *10*

I_E = Direct Current out of Terminal 6 or *4*

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 CA3029A, CA3030A, CA3037A, CA3038A), Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3010A CA3029A CA3037A Min.	CA3010A CA3029A CA3037A Typ.	CA3010A CA3029A CA3037A Max.	CA3015A CA3030A CA3038A Min.	CA3015A CA3030A CA3038A Typ.	CA3015A CA3030A CA3038A Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V		-	102	-	-	-	-		
		8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	500	-		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V R_S = 1 kΩ = +12V = -12V	none	- -	3 -	- -	- -	- 7	- -	V/μs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	+0.5 to -4 -	- -	- -	- +0.65 to -8	- -	- -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V = +6V = -6V = +9V = -9V = +12V = -12V R_S = 1 kΩ	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

LEAD TEMPERATURE (During Soldering): ALL TYPES

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

CA3010A, CA3015A, CA3029A, CA3030A, CA3037A, CA3038A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A, CA3037A, CA3038A;
Italic Numbers in Square Boxes are for CA3010A, CA3015A.

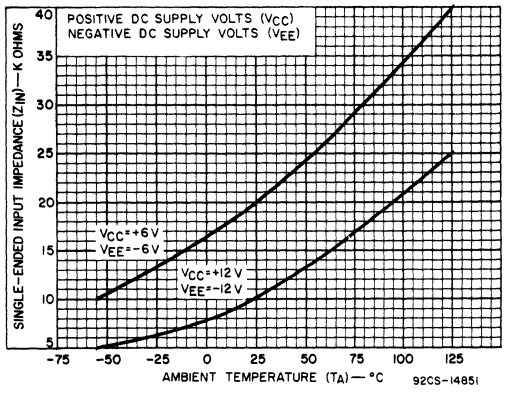


Fig. 13 — Single-ended input impedance vs. temperature.

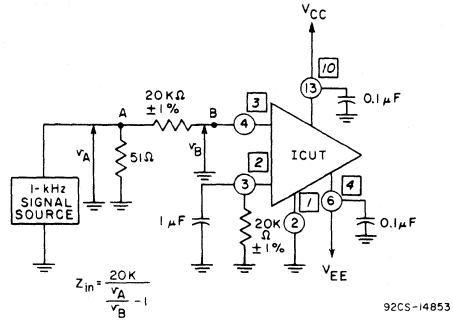
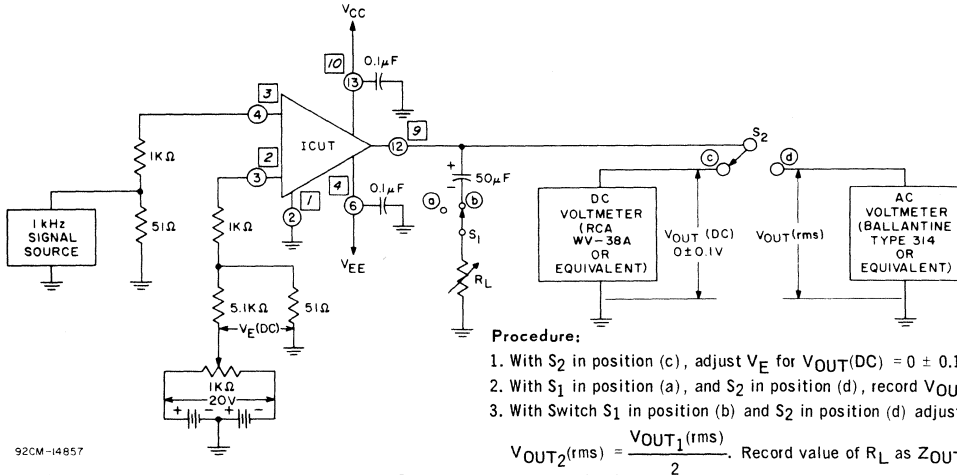


Fig. 14 — Single-ended input impedance test circuit.



Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

Fig. 15 — Output impedance test circuit.

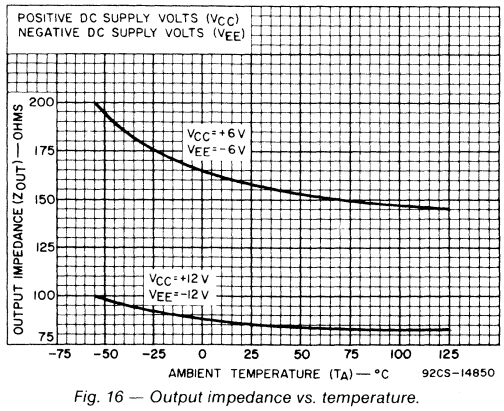


Fig. 16 — Output impedance vs. temperature.

CA3060

Operational Transconductance Amplifier Arrays

Features:
- *Low power consumption — as low as 100 μW per amplifier*
- *Independent biasing for each amplifier*
- *High forward transconductance*
- *Programmable range of input characteristics*
- *Low input bias and input offset current*
- *High input and output impedance*
- *No effect on device under output short-circuit conditions*
- *Zener diode bias regulator*

The RCA CA3060 monolithic integrated circuit consists of an array of three independent Operational Transconductance Amplifiers.* This type of amplifier has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, g_mR_L). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filter.

The three amplifiers in the CA3060 are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current(I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition; the CA3060 incorporates a unique Zener diode regulator system that permits current regulation below supply voltages normally associates with such systems.

The CA3060 is supplied in a 16-lead dual-in-line plastic package (E suffix) and in chip form (H suffix). This device is operational from -40° C to +85° C.

*Generic applications of the OTA are described in ICAN-6668. For improved input operating ranges, refer to CA3080 and CA3280 data bulletins (File Nos. 475 and 1174) and application notes ICAN-6668 and ICAN-6818.

Applications:
- *For low power conventional operational amplifier applications*
- *Active filters*
- *Comparators*
- *Gyrators*
- *Mixers*
- *Modulators*
- *Multiplexers*
- *Multipliers*
- *Strobing and gating functions*
- *Sample and hold functions*

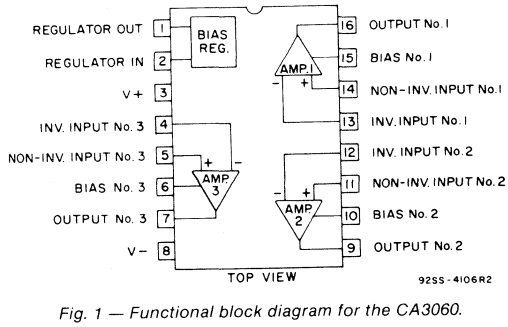


Fig. 1 — Functional block diagram for the CA3060.

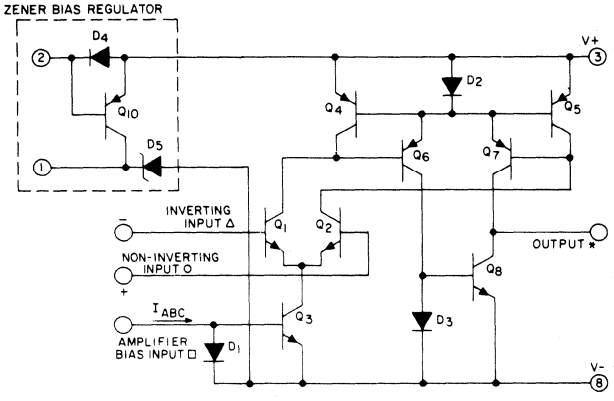
File Number **537**

CA3060

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C.:*

DC SUPPLY VOLTAGE (BETWEEN V+ and V- TERMINALS)	36V (±18V)
DIFFERENTIAL INPUT VOLTAGE (EACH AMPLIFIER)	±5V
DC INPUT VOLTAGE	V+ to V-
INPUT SIGNAL CURRENT (EACH AMPLIFIER)	±1mA
AMPLIFIER BIAS CURRENT (EACH AMPLIFIER)	2 mA
Bias Regulator Input Current	-5mA
OUTPUT SHORT-CIRCUIT DURATION*	No limitation
DEVICE DISSIPATION	
Up to T_A = 75° C	490mW
Above T_A ' 75° C	Derate linearly 6.67 mW/° C
TEMPERATURE RANGE	
Operating	-55° C to +125° C
Storage	-65 to +150° C
LEAD TEMPERATURE (During Soldering)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+300° C

*Short circuit may be applied to ground or to either supply



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY

○ NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY

* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY

□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

92CS-15860RI

Fig. 2 — Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for the CA3060.

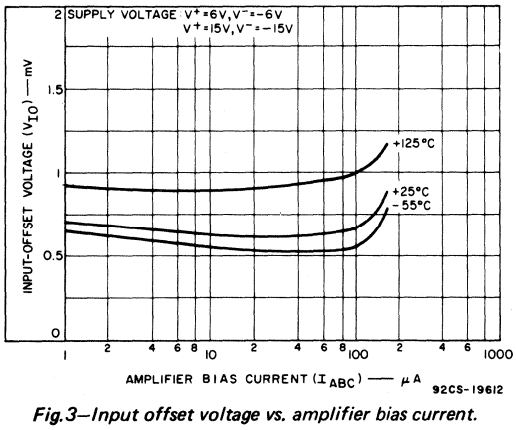


Fig.3—Input offset voltage vs. amplifier bias current.

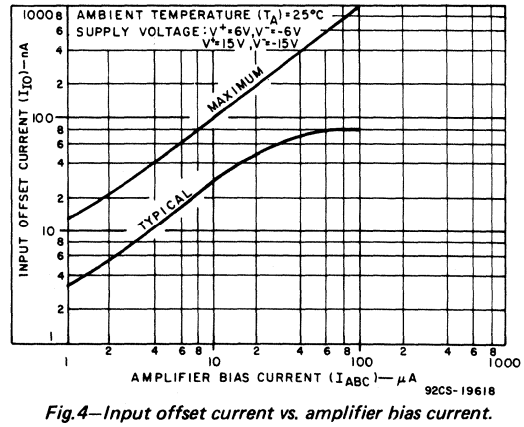


Fig.4—Input offset current vs. amplifier bias current.

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V+ = 15 V, V- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS Amplifier Bias Current I_{ABC} = 1 A TYP.	I_{ABC} = 10 A TYP.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS								
Input Offset Voltage	V_{IO}	3	1	1	—	1	5	mV
Input Offset Current	I_{IO}	4	3	30	—	250	1000	nA
Input Bias Current	I_{IB}	5a,b	33	300	—	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	2.3	26	150	240	—	μA
Peak Output Voltage:								
Positive	V_{OM+}	7	13.6	13.6	12	13.6	—	V
Negative	V_{OM-}		14.7	14.7	12	14.7	—	
Amplifier Supply Current (each amplifier)	I_A	8a,b	8.5	85	—	850	1200	μA
Power Consumption (each amplifier)	P	—	0.26	2.6	—	26	36	mW
Input Offset-Voltage Sensitivity■:								
Positive	$\Delta V^{IO}/\Delta V+$	—	1.5	2	—	2	150	uV/V
Negative	$\Delta V^{IO}/\Delta V-$		20	20	—	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	0.54	0.60	—	0.66	—	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)								
Forward Transconductance (large signal)	921	10a,b	1.55	18	30	102	—	mmho
Common-Mode Rejection Ratio	CMRR	—	110	110	70	90	—	dB
Common-Mode Input Voltage Range	V_{ICR}	—	+12 to -12 min. +13 to -14 typ.	+12 to -12 min. +13 to -14 typ.	+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	—	0.1	1	—	*	—	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	20	45	—	110	—	kHz
Input Impedance Components:								
Resistance	R_I	12	1600	170	10	20	—	kΩ
Capacitance at 1 MHz	C_I	—	2.7	2.7	—	2.7	—	pF
Output Impedance Components:								
Resistance	R_O	14	200	20	—	2	—	MΩ
Capacitance at 1 MHz	C_O	—	4.5	4.5	—	4.5	pF	

ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25° C, I_Z = 0.1 mA)

				MIN.	TYP.	MAX.	
Voltage	V_Z	15	Temp. Coeff. = 3mV/°C	6.2	6.7	7.9	V
Impedance	Z_Z	—			200	300	

*Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test — V+ is reduced to 13 volts for V+ sensitivity
V- is reduced to -13 volts for V- sensitivity

(b) V+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +13 V and -15 V supplies}}{\text{1 volt}}$

V- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +13 V and -15 V supplies}}{\text{1 volt}}$

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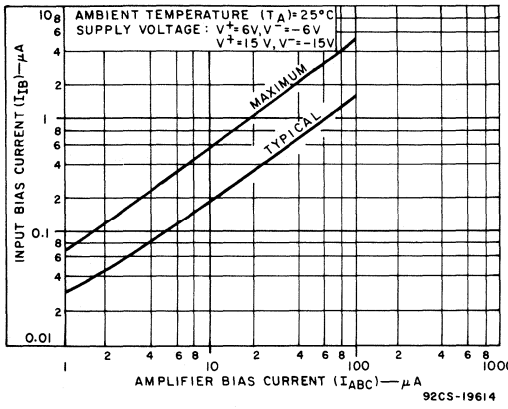


Fig.5a—Input bias current vs. amplifier bias current

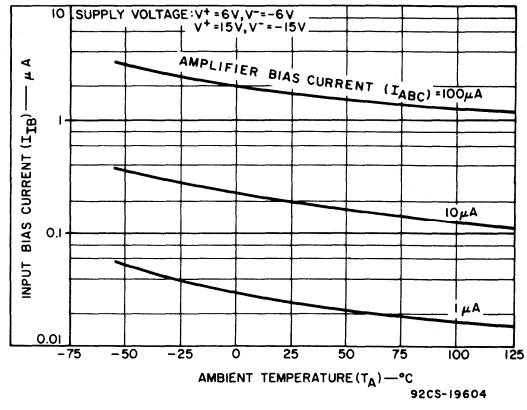


Fig.5b—Input bias current vs. ambient temperature.

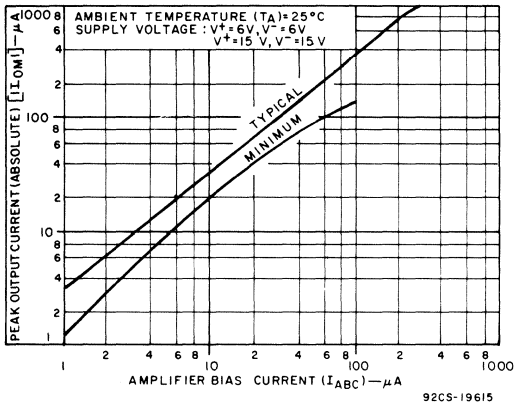


Fig.6a—Peak output current vs. amplifier bias current.

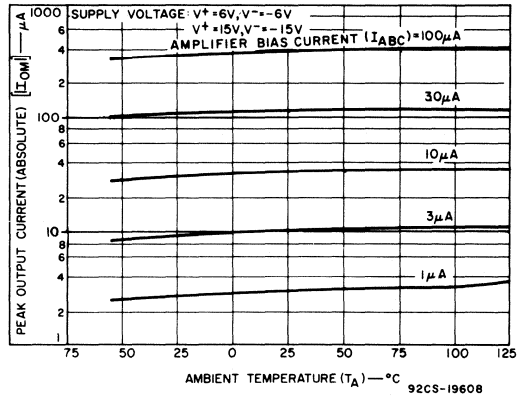


Fig.6b—Peak output current vs. ambient temperature.

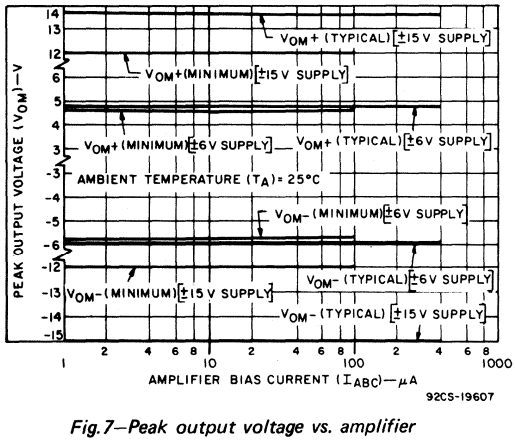


Fig.7—Peak output voltage vs. amplifier bias current.

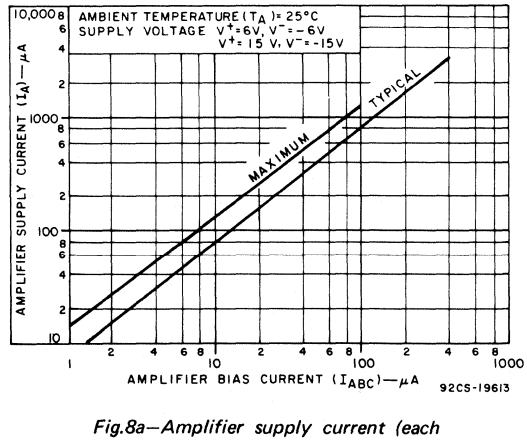


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

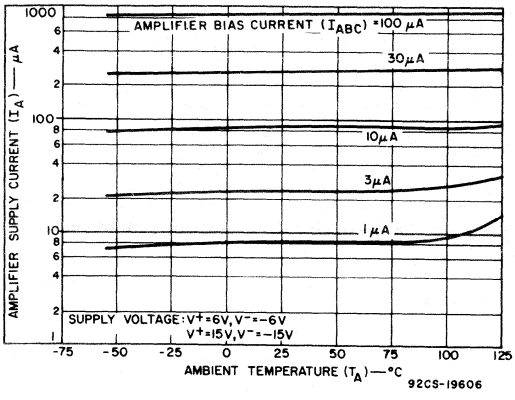


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

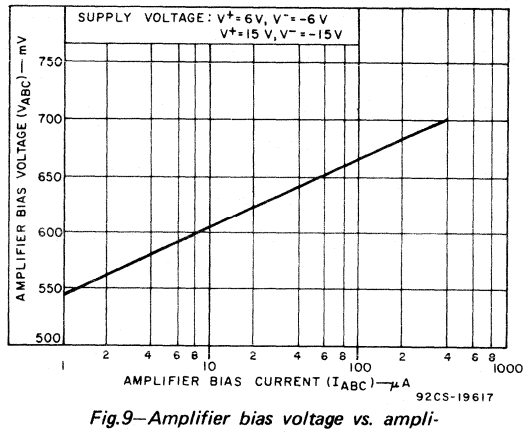


Fig.9—Amplifier bias voltage vs. amplifier bias current.

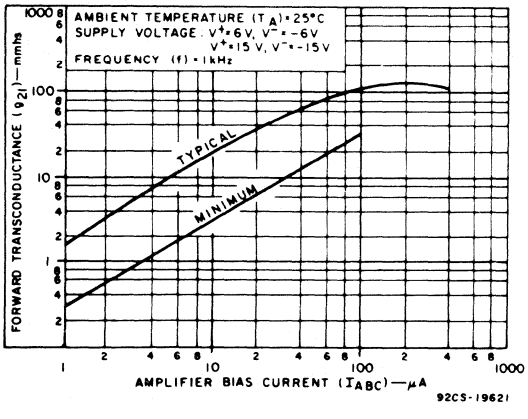


Fig.10a—Forward transconductance vs. amplifier bias current.

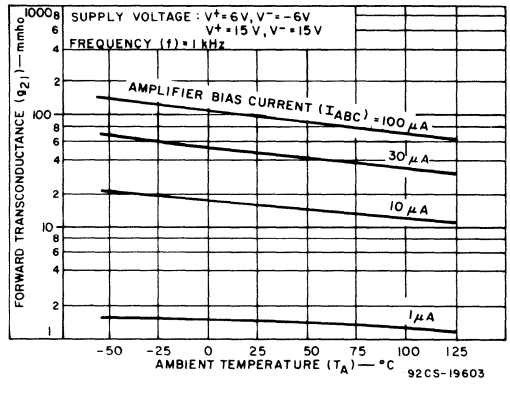


Fig.10b—Forward transconductance vs. ambient temperature.

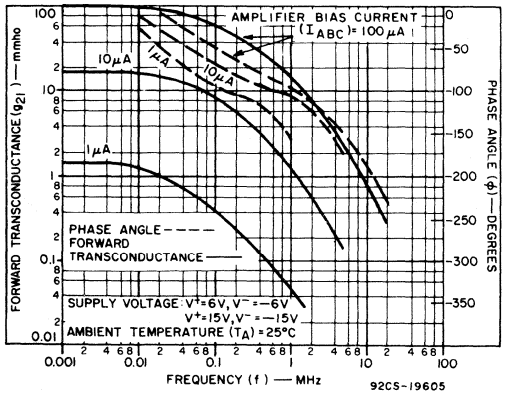


Fig.11—Forward transconductance vs. frequency.

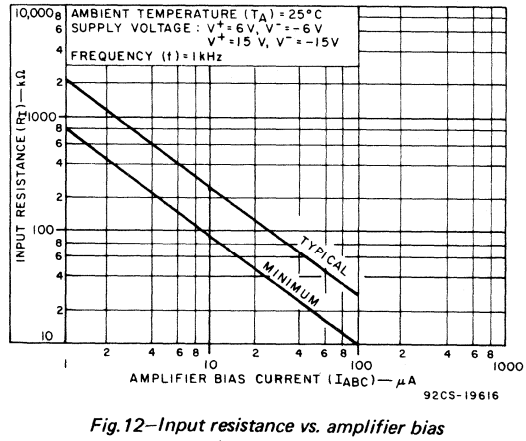
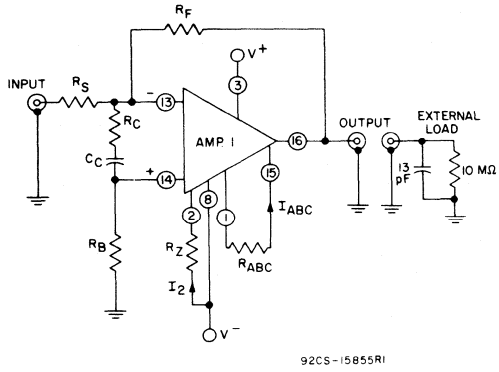


Fig.12—Input resistance vs. amplifier bias current.

CA3060



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.

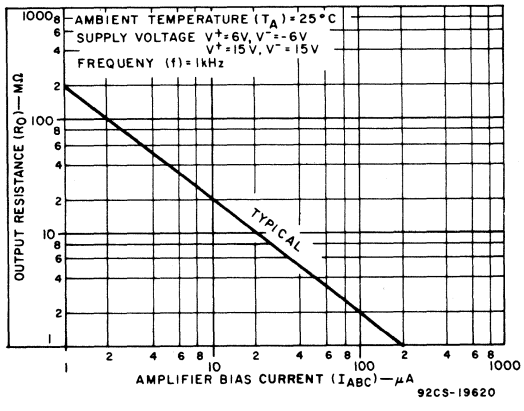


Fig. 14—Output resistance vs. amplifier bias current.

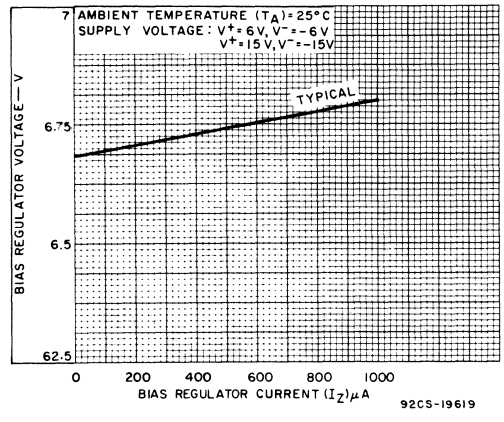


Fig. 15—Bias regulator voltage vs. bias regulator current.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

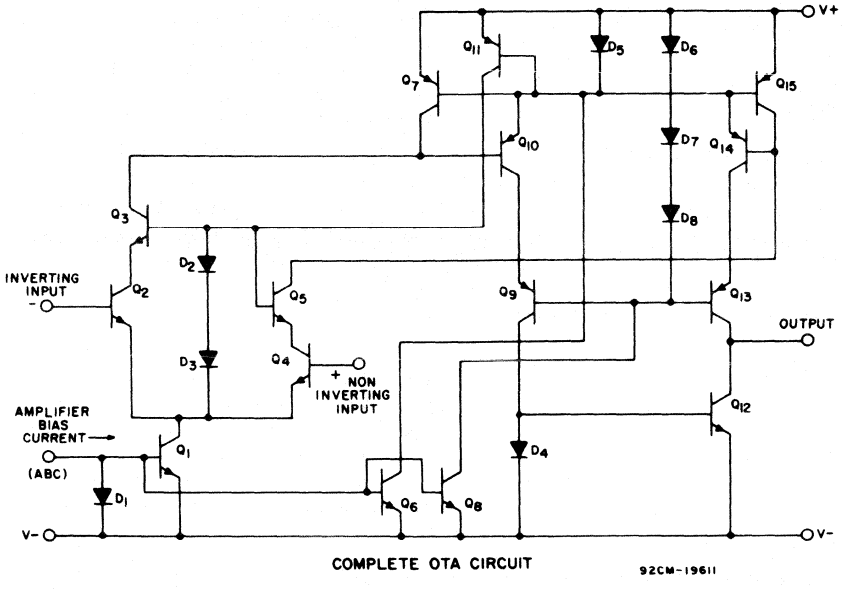


Fig. 16—Complete schematic diagram showing bias regulator and one of the three operational transconductance amplifiers.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

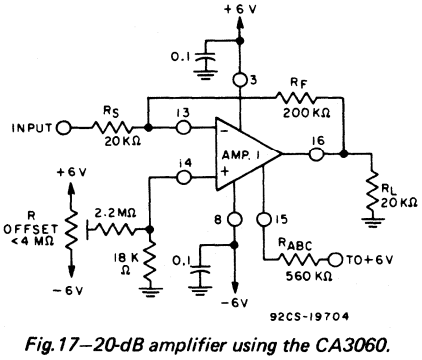


Fig. 17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

≅ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

CA3060

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or } \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

   i.e. $\frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

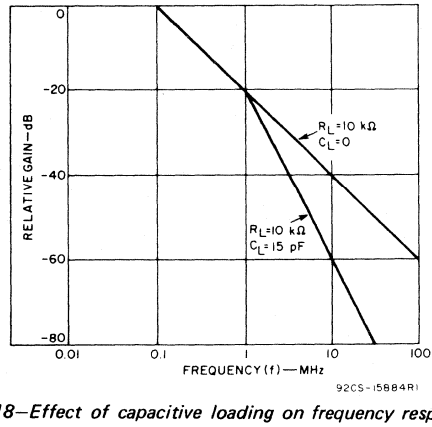


Fig. 18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

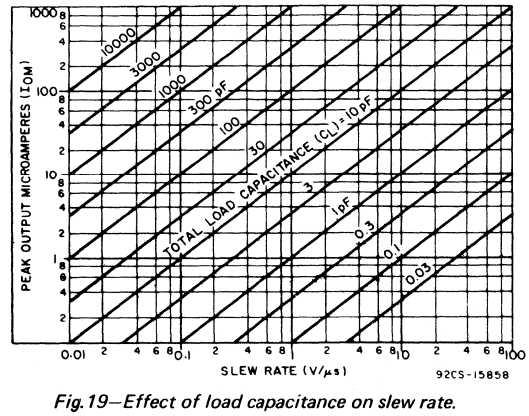


Fig. 19—Effect of load capacitance on slew rate.

CA3060

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-

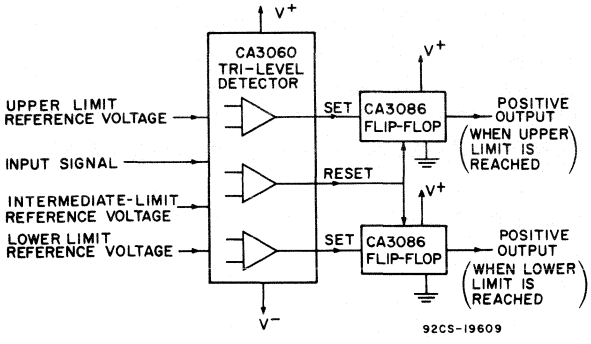


Fig.20—Functional block diagram of a tri-level comparator.

limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V⁻, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

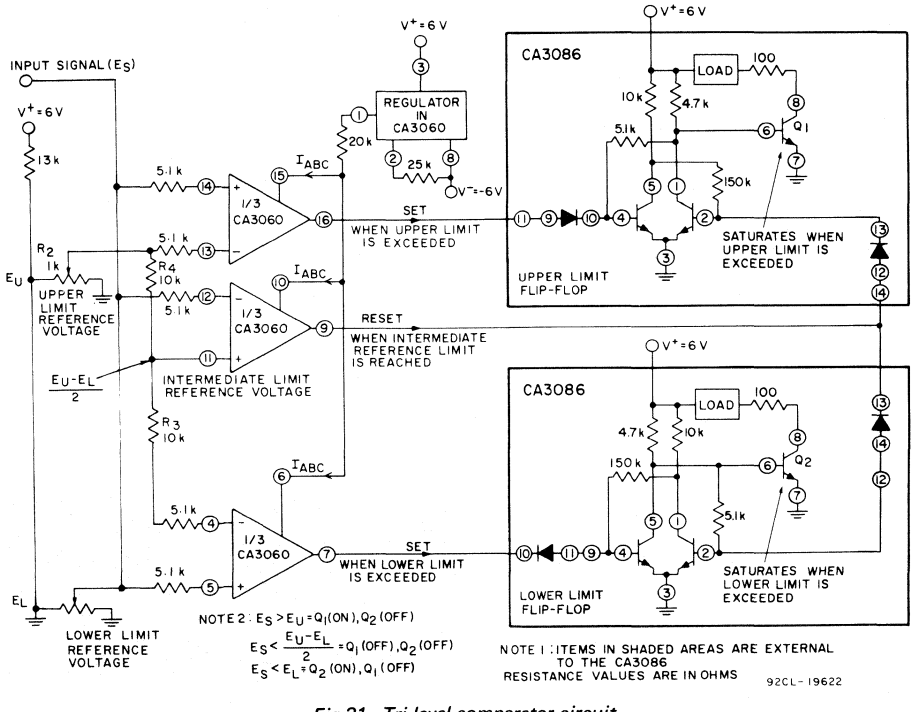


Fig.21—Tri-level comparator circuit.

CA3060

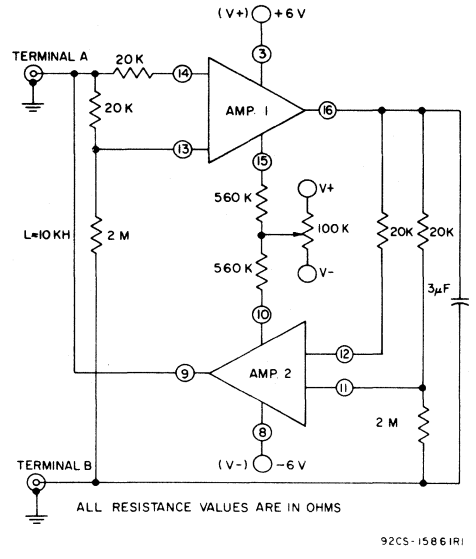


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

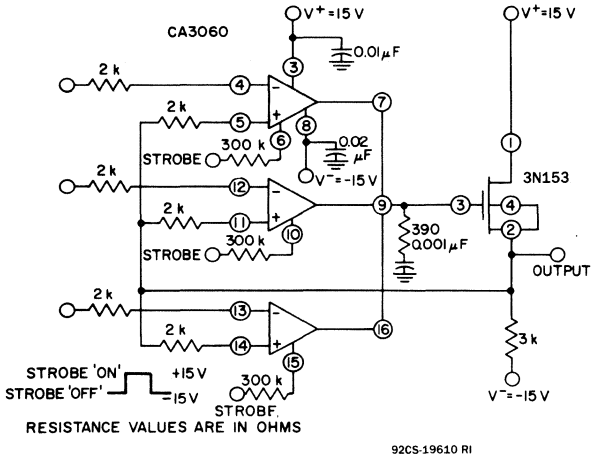


Fig.23—Three-channel multiplexer.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N153 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

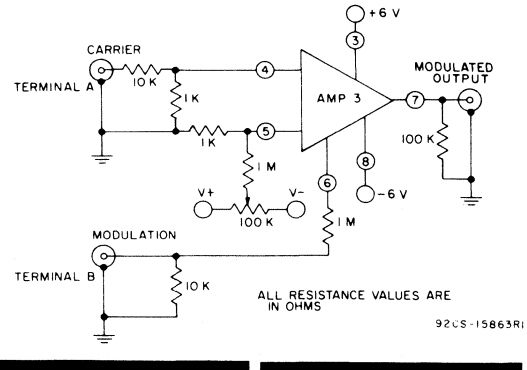
The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V^-.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.



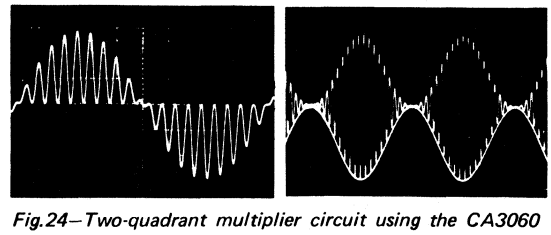


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [(V\text{-}) + V_Y]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left\{[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right\} \text{ or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

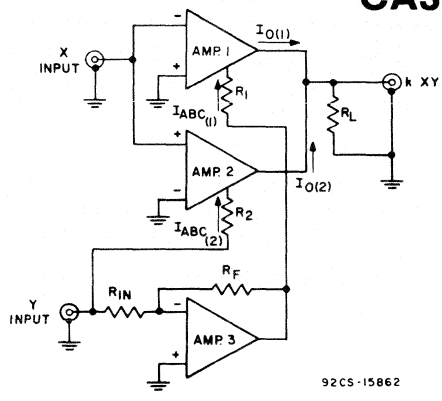


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

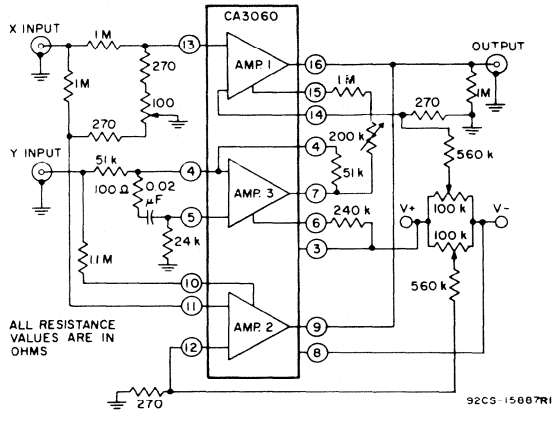


Fig.26—Typical four-quadrant multiplier circuit.

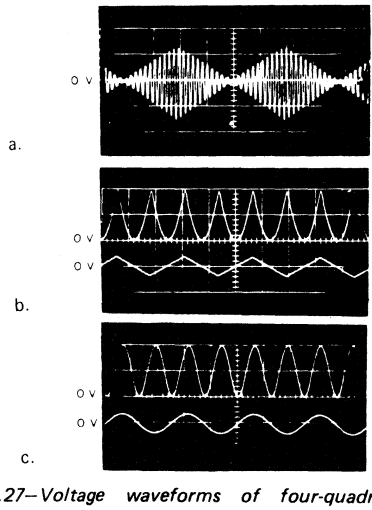


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

CA3078, CA3078A

Micropower Operational Amplifier

Features:

- **Low standby power: as low as 700 nW**
- **Wide supply voltage range: ±0.75 to ±15 V**
- **High peak output current: 6.5 mA min.**
- **Adjustable quiescent current**
- **Output short-circuit protection**

The RCA-CA3078 and CA3078A are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078A is a preminum device having a supply voltage range of $V^{\pm}$ = 0.75 to $V^{\pm}$ = 15 V and an operating temperature range of −25°C to +125°C. The CA3078 has the same lower supply voltage limit but the upper limit is V^{+} = +6 V and V^{-} = −6 V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or the 8-lead dual-in-line plastic "MINI-DIP" package ("E" suffix).

Applications:

- **Portable electronics**
- **Medical electronics**
- **Instrumentation**
- **Telemetry**
- **Intrusion alarms**

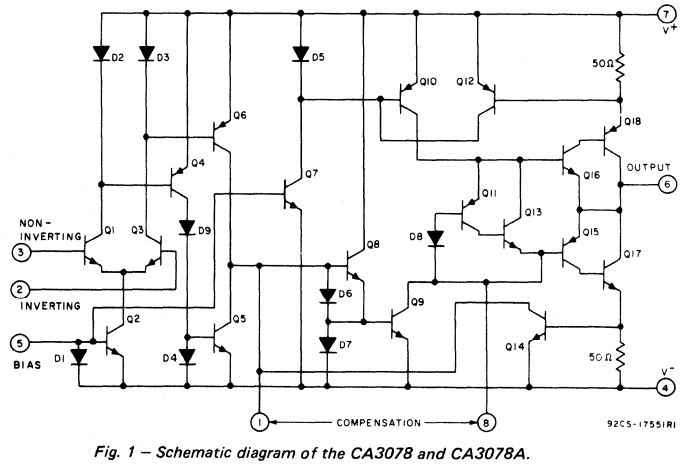


Fig. 1 – Schematic diagram of the CA3078 and CA3078A.

File Number **535**

CA3078, CA3078A

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3078A	CA3078
DC Supply Voltage (between V^+ and V^- terminal	36 V	14 V
Differential Input Voltage	±6 V	±6 V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	150 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	−55 to +125°C	0 to +70°C
Storage	−65 to +150°C	−65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

* Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS For Equipment Design

CHARACTERISTICS SYMBOLS	TEST CONDITIONS			CA3078A LIMITS R_{SET} = 5.1 MΩ					CA3078 LIMITS R_{SET} = 1 MΩ					UNITS
				$T_A = 25°C$			$T_A = -55$ to 125°C		$T_A = 25°C$			$T_A = 0$ to 70°C		
	V^+ & V	R_S kΩ	R_L kΩ	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{IO}	6	≤10	–	–	0.70	3.5	–	4.5	–	1.3	4.5	–	5	mV
V_{IO}		–	–	–	0.50	2.5	–	5.0	–	6	32	–	40	nA
I_{IB}		–	–	–	7	12	–	50	–	60	170	–	200	nA
A_{OL}		–	≥10	92	100	–	90	–	88	92	–	86	–	dB
I_Q		–	–	–	20	25	–	45	–	100	130	–	150	μA
P_D		–	–	–	240	300	–	540	–	1200	1560	–	1800	μW
V_{OM}		–	≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
V_{ICR}		≤10	–	–	−5.5 to +5.8	–	−5 to +5	–	–	−5.5 to +5.8	–	−5 to +5	–	V
CMRR		≤10	–	80	115	–	–	–	80	110	–	–	–	dB
I_{OM}^+ or I_{OM}		–	–	–	12	–	6.5	30	–	12	–	6.5	30	mA
$\Delta V_{IO}/\Delta V^+$		≤10		76	105	–	–	–	76	93	–	–	–	μV/V
$\Delta V_{IO}/\Delta V$			–	76	105	–	–	–	76	93	–	–	–	
				R_{SET} = 13 MΩ,										
V_{IO}	15	≤10	–	–	1.4	3.5	–	4.5	–	–	–	–	–	mV
A_{OL}		–	≥10	92	100	–	88	–	–	–	–	–	–	dB
I_Q		–	–	–	20	30	–	50	–	–	–	–	–	μA
P_D		–	–	–	600	750	–	1350	–	–	–	–	–	μW
V_{OM}		–	≥10	±13.7	±14.1	–	±13.5	–	–	–	–	–	–	V
CMRR		≤10	–	80	106	–	–	–	–	–	–	–	–	dB
I_{IB}		–	–	–	7	14	–	55	–	–	–	–	–	nA
I_{IO}		–	–	–	0.50	2.7	–	5.5	–	–	–	–	–	nA

CA3078, CA3078A

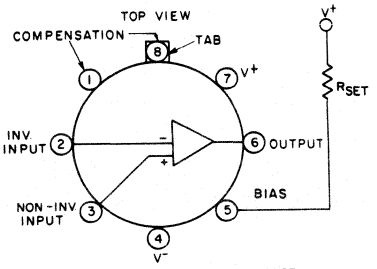
ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$*

Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078A		CA3078		
	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

Typical Values Intended Only for Design Guidance *at $T_A = 25°C$ and $V^+ = +6$ V, $V^- = -6$ V*

CHARACTERISTICS SYMBOLS	TEST CONDITIONS	CA3078A		CA3078	UNITS
		$R_{SET} = 5.1$ MΩ	$R_{SET} = 1$ MΩ	$R_{SET} = 1$ MΩ	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	5	6	6	μV/°C
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	6.3	70	70	pA/°C
BW_{OL}	3dB pt.	0.3	2	2	kHz
SR	See Figs. 20, 21	0.027	0.04	0.04	V/μs
		0.5	1.5	1.5	
⌐¬	10% to 90% Rise Time	3	2.5	2.5	μs
R_I		7.4	1.7	0.87	MΩ
R_O		1	0.8	0.8	kΩ
e_N(10 Hz)	$R_S = 0$	40	–	25	nV/√Hz
i_N(10 Hz)	$R_S = 1$ MΩ	0.25	–	1	pA/√Hz



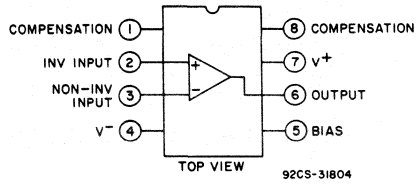


Fig. 2 – Functional diagrams.

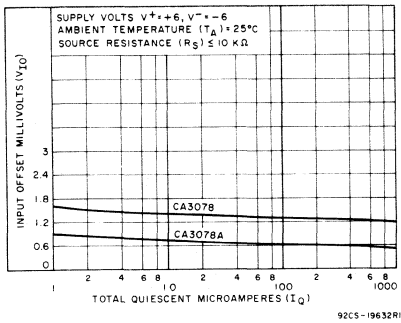


Fig. 3 – Input offset voltage vs. total quiescent current.

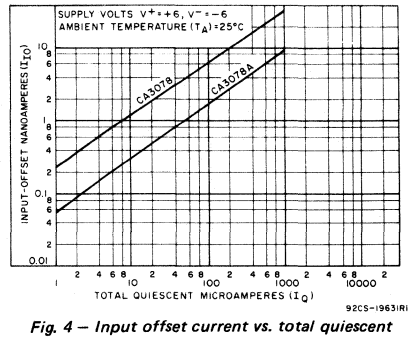


Fig. 4 – Input offset current vs. total quiescent current.

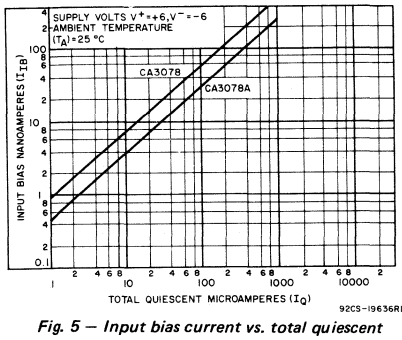


Fig. 5 – Input bias current vs. total quiescent current.

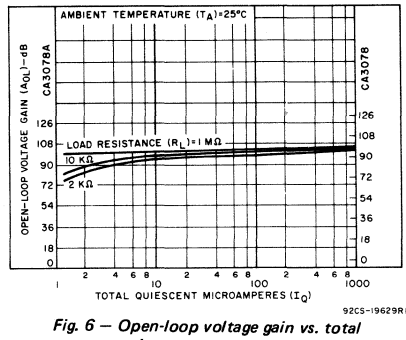


Fig. 6 – Open-loop voltage gain vs. total quiescent current.

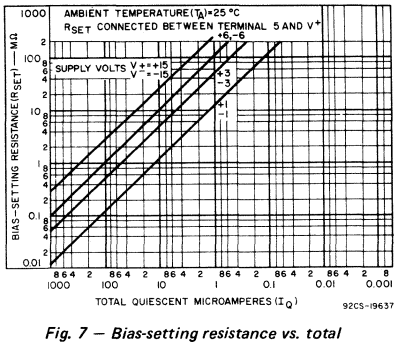


Fig. 7 – Bias-setting resistance vs. total quiescent current.

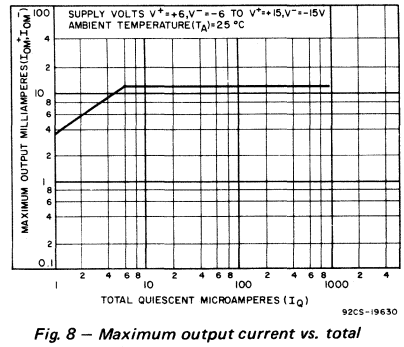


Fig. 8 – Maximum output current vs. total quiescent current.

CA3078, CA3078A

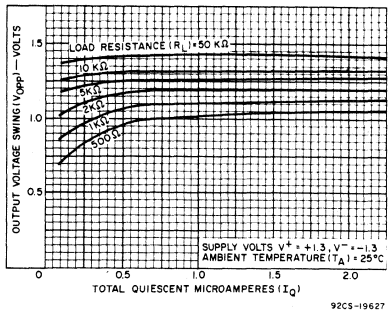


Fig. 9 — Output voltage swing vs. total quiescent current.

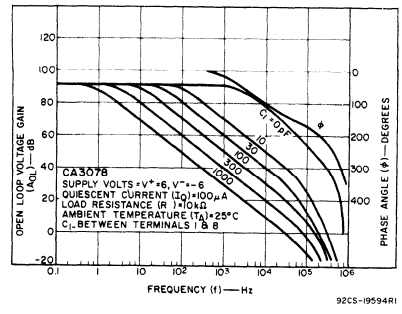


Fig. 10 — Open-loop voltage gain vs. frequency for I_Q = 100 μA — CA3078.

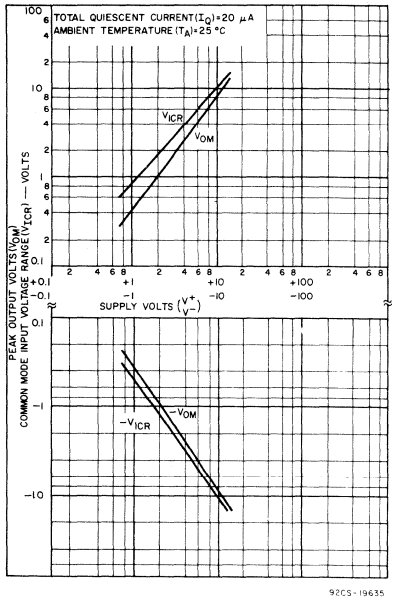


Fig. 11 — Output and common-mode voltage vs. supply voltage.

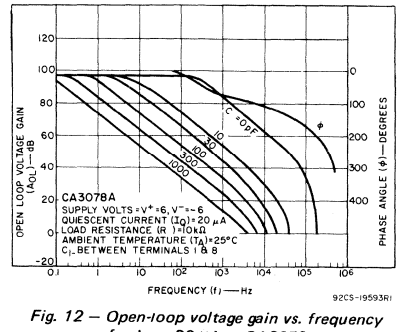


Fig. 12 — Open-loop voltage gain vs. frequency for I_Q = 20 μA — CA3078.

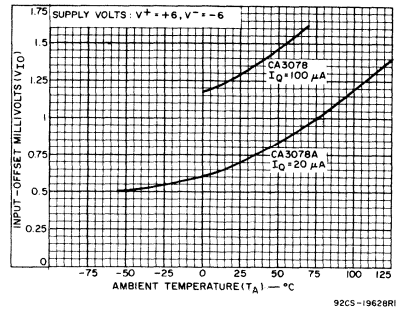


Fig. 13 — Input offset voltage vs. temperature.

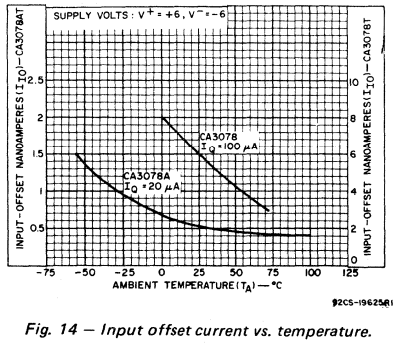


Fig. 14 — Input offset current vs. temperature.

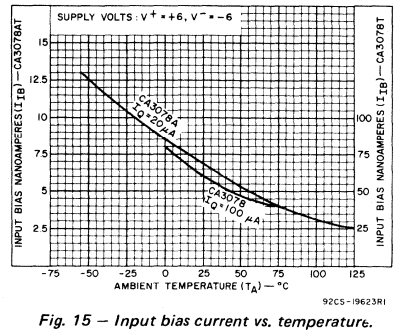


Fig. 15 — Input bias current vs. temperature.

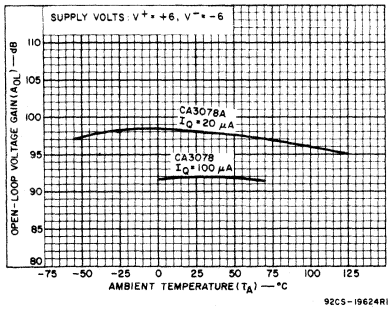


Fig. 16 — Open-loop voltage gain vs. temperature.

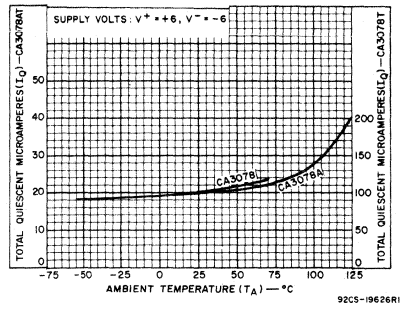


Fig. 17 — Total quiescent current vs. temperature.

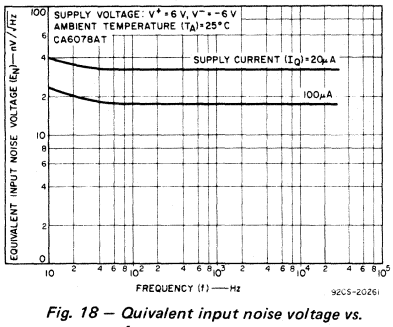


Fig. 18 — Quivalent input noise voltage vs. frequency.

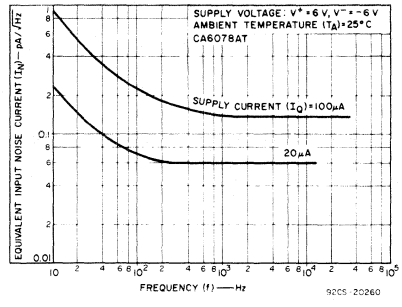


Fig. 19 — Equivalent input noise current vs. frequency.

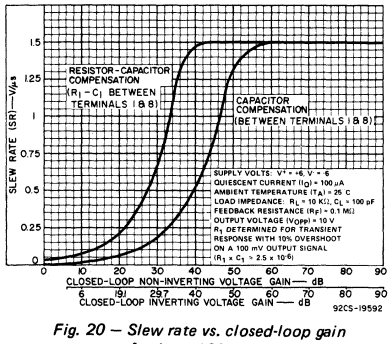


Fig. 20 — Slew rate vs. closed-loop gain for I_Q = 100 μA — CA3078.

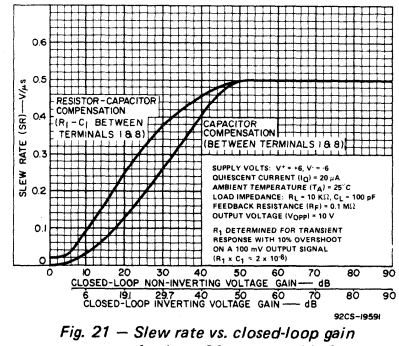


Fig. 21 — Slew rate vs. closed-loop gain for I_Q = 20 μA — CA3078.

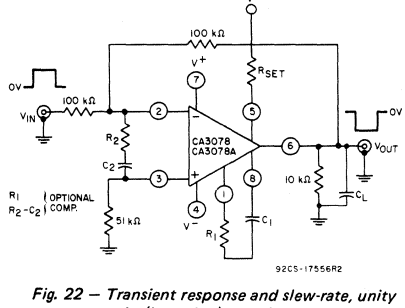


Fig. 22 — Transient response and slew-rate, unity gain (inverting) test circuit.

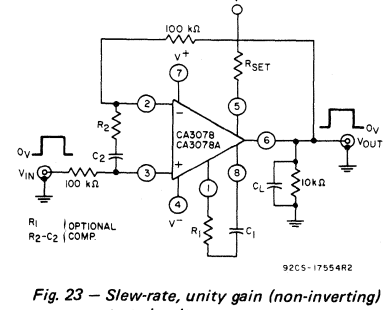


Fig. 23 — Slew-rate, unity gain (non-inverting) test circuit.

CA3078, CA3078A

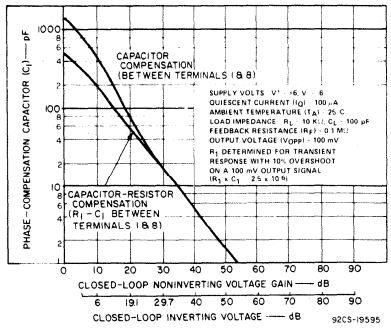


Fig. 24 — Phase compensation capacitance vs. closed-loop gain — CA3078.

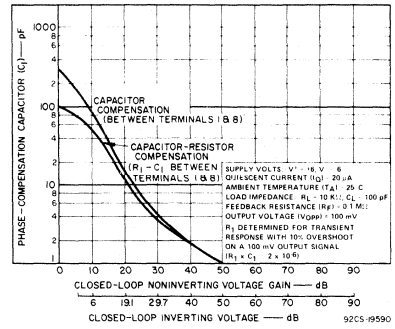


Fig. 25 — Phase compensation capacitance vs. closed-loop gain — CA3078A.

Table I — Unity-gain slew rate vs. compensation — CA3078 and CA3078A

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$	TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV
OUTPUT VOLTAGE (V_O) = ±5 V	AMBIENT TEMPERATURE (T_A) = 25°C
LOAD RESISTANCE (R_L) = 10 kΩ	

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078 — I_Q = 100 µA	kΩ	pF	kΩ	µF	V/µs	kΩ	pF	kΩ	µF	V/µs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A — I_Q = 20 µA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078A and CA3078 can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 100 µA and 20 µA, respectively, for a transient response with 10% overshoot. Figs. 20 and 21 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table I gives an indication of slew rates that can be obtained with various compensation techques at quiescent currents of 100 µA and 20 µA.

Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078A or CA3078 in inverting the non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for

either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

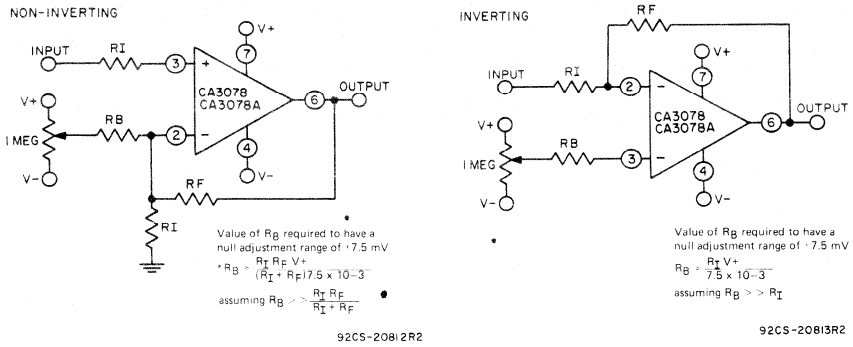


Fig. 26 – Offset voltage null circuits.

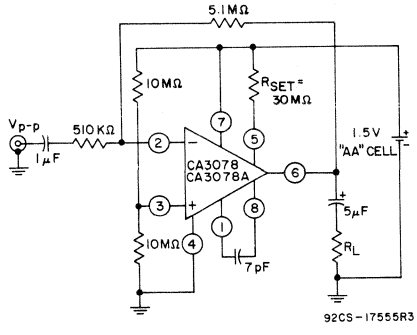


Fig. 27 – Inverting 20-dB amplifier circuit.

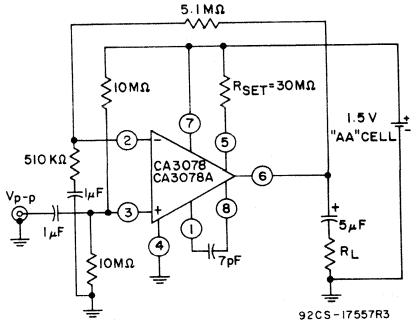


Fig. 28 – Non inverting 20-dB amplifier circuit.

CA3080, CA3080A

Operational Transconductance Amplifiers (OTA's)

Gatable-Gain Blocks

Features:

- **Slew rate (unity gain, compensated): 50 V/μs**
- **Adjustable power consumption: 10μW to 30 mW**
- **Flexible supply voltage range: ±2 V to ±15 V**
- **Fully adjustable gain: 0 to $g_m R_L$ limit**
- **Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)**
- **Extended g_m linearity: 3 decades**

The RCA-CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead TO-5-style package (CA3080, CA3080A), and in the 8-lead TO-5-style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E, CA3080AE), and in chip form (CA3080H).

Applications:

- **Sample and hold**
- **Multiplex**
- **Voltage follower**
- **Multiplier**
- **Comparator**

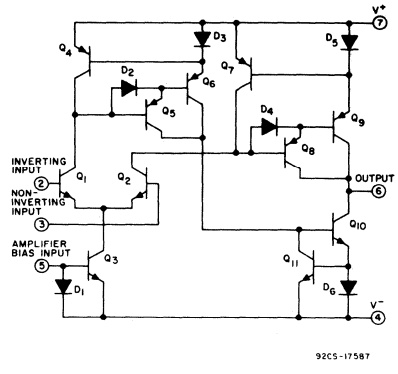


Fig.1 – Schematic diagram for CA3080 and CA3080A.

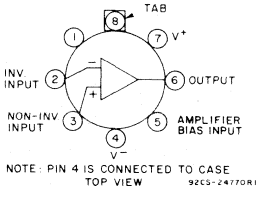
File Number **475**

CA3080, CA3080A

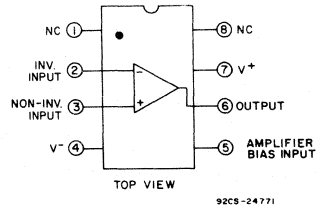
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080, CA3080E, CA3080S	0 to + 70 °C
CA3080A, CA3080AE, CA3080AS	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265 °C

* Short circuit may be applied to ground or to either supply.



TO-5 Style Package



Plastic Package (E Suffix)

Fig.2 – Functional diagrams.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

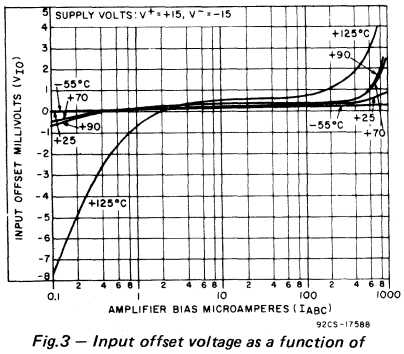


Fig.3 – Input offset voltage as a function of amplifier bias current.

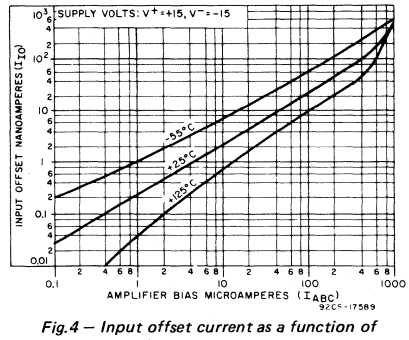


Fig.4 – Input offset current as a function of amplifier bias current.

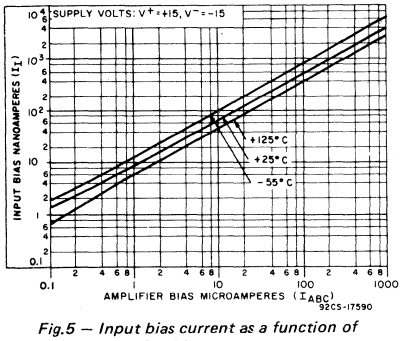


Fig.5 – Input bias current as a function of amplifier bias current.

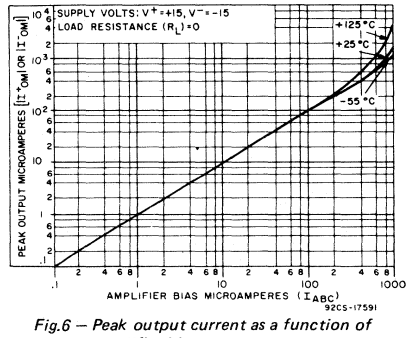


Fig.6 – Peak output current as a function of amplifier bias current.

CA3080, CA3080A

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080, CA3080E, CA3080S LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		T_A = 0 to 70°C	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		T_A = 0 to 70°C	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		T_A = 0 to 70°C	5400	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	$R_L = 0$	350	500	650	μA
		$R_L = 0$, T_A = 0 to 70°C	300	–	–	
Peak Output Voltage:						
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	V
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080, CA3080E, CA3080S	
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	0.3	mV
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\ \mu A$	5	μA
Peak Output Voltage:				
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$	13.8	V
Negative	V^-_{OM}		−14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				
Maximum (uncompensated)	SR		75	V/μs
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Propagation Delay	t_{PHL}, t_{PLH}	I_{ABC}=500 μA	45	ns

CA3080, CA3080A

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS: $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080A, CA3080AE, CA3080AS LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	–	0.3	2	mV
			–	0.4	2	
		$T_A = -55$ to $+125^oC$	–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	–	0.1	3	mV
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = -55$ to $+125^oC$	–	–	8	
Forward Transconductance (large signal)	g_m		7700	9600	12000	μmho
		$T_A = -55$ to $+125^oC$	4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	$I_{ABC} = 5\ \mu A$, $R_L = 0$	3	5	7	μA
		$R_L = 0$	350	500	650	
		$R_L = 0, T_A = -55$ to $+125^oC$	300	–	–	
Peak Output Voltage:						V
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$, $R_L = \infty$	12	13.8	–	
Negative	V^-_{OM}		−12	−14.5	–	
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						$\mu V/V$
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	–	0.08	5	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	–	0.3	5	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080A, CA3080AE, CA3080AS	
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				V/μs
Maximum (uncompensated)	SR		75	
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		.15	MΩ
Input-to-Output Capacitance	C_{I-O}	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	$I_{ABC} = 100\ \mu A$, $T_A = -55$ to $+125^oC$	3	$\mu V/^oC$
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

CA3080, CA3080A

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

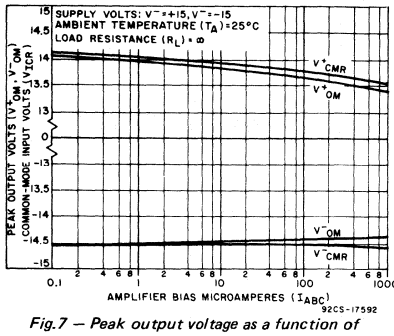


Fig.7 – Peak output voltage as a function of amplifier bias current.

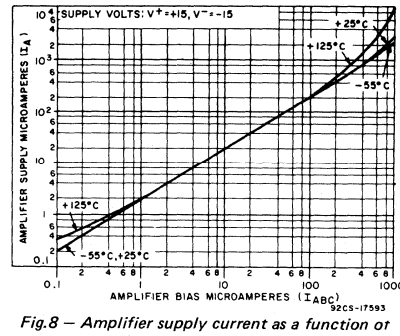


Fig.8 – Amplifier supply current as a function or amplifier bias current.

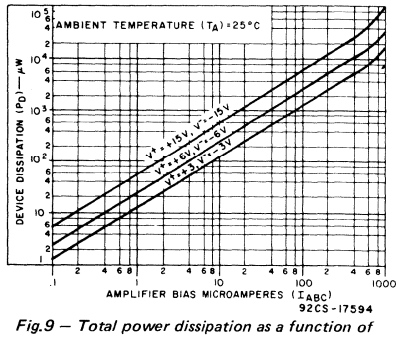


Fig.9 – Total power dissipation as a function of amplifier bias current.

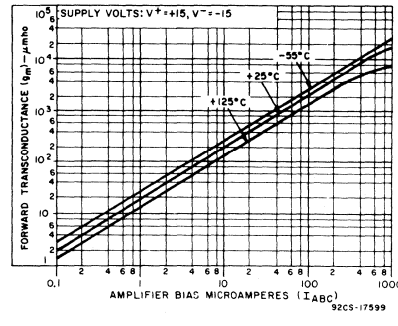


Fig.10 – Transconductance as a function of amplifier bias current.

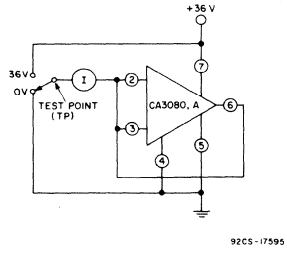


Fig.11 – Leakage current test circuit.

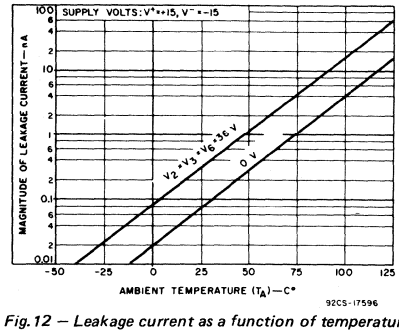


Fig.12 – Leakage current as a function of temperature.

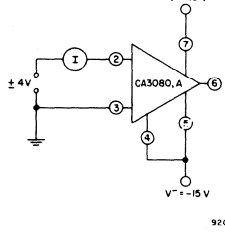


Fig.13 – Differential input current test circuit.

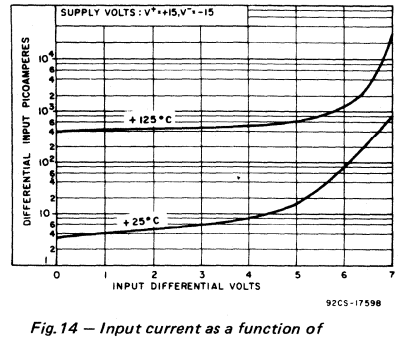


Fig.14 – Input current as a function of input differential voltage.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

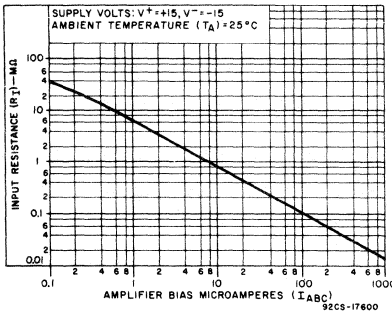


Fig. 15 – Input resistance as a function of amplifier bias current.

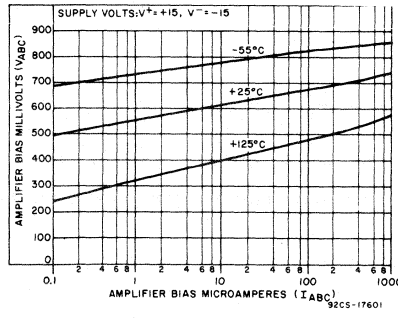


Fig. 16 – Amplifier bias voltage as a function of amplifier bias current.

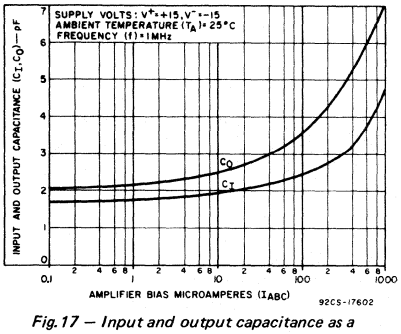


Fig. 17 – Input and output capacitance as a function of amplifier bias current.

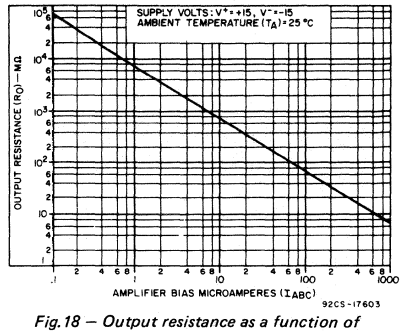


Fig. 18 – Output resistance as a function of amplifier bias current.

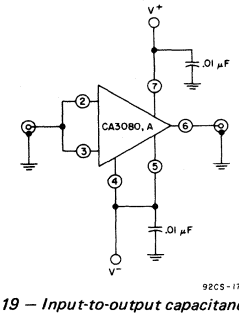


Fig. 19 – Input-to-output capacitance test circuit.

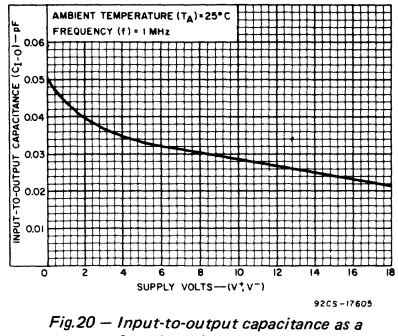
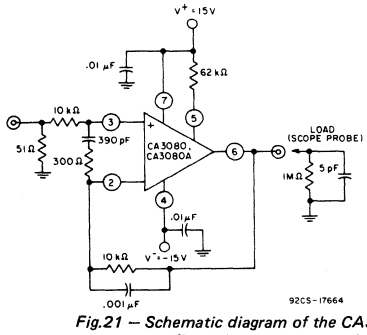


Fig. 20 – Input-to-output capacitance as a function of supply voltage.

APPLICATIONS



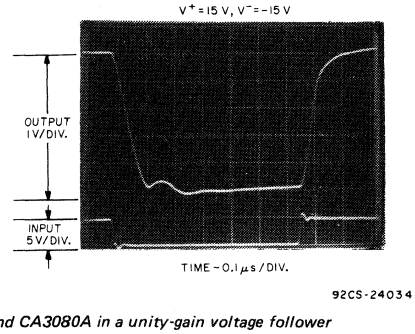


Fig. 21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.

CA3080, CA3080A

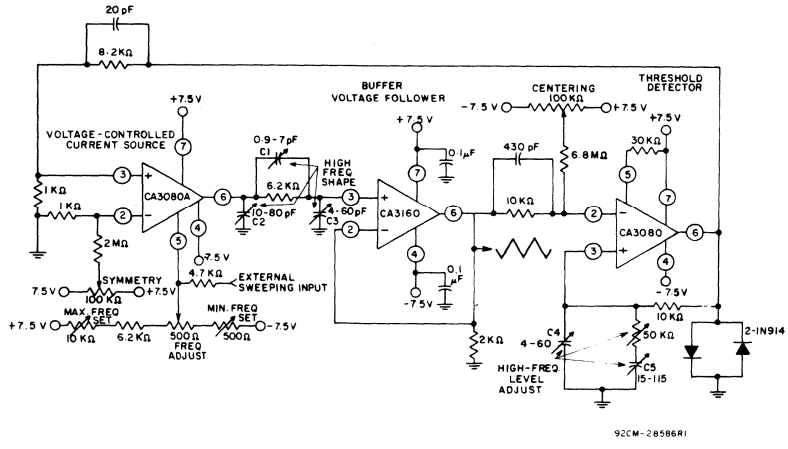
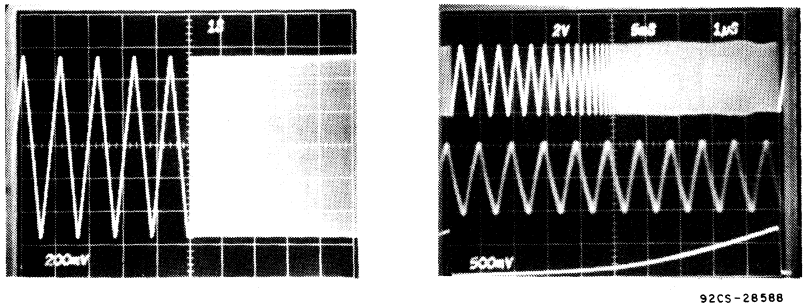


Fig.22 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.23 – Function generator dynamic characteristics waveforms.

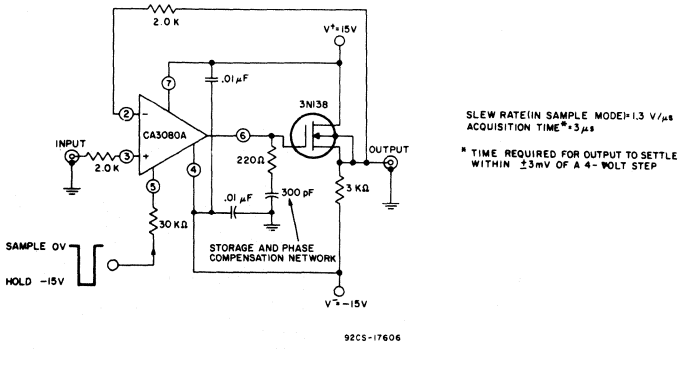


Fig.24 – Schematic diagram of the CA3080A in a sample-hold configuration.

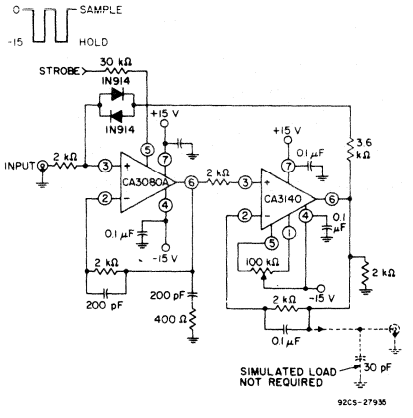
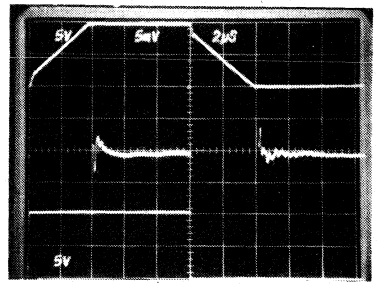


Fig.25 – Sample- and hold circuit.



LARGE-SIGNAL RESPONSE AND SETTLING TIME

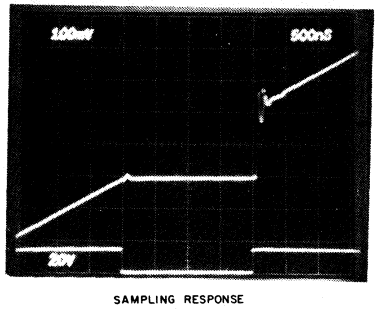
TOP TRACE : OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)

BOTTOM TRACE : INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)

CENTER TRACE : DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.)

92CS-27884

Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



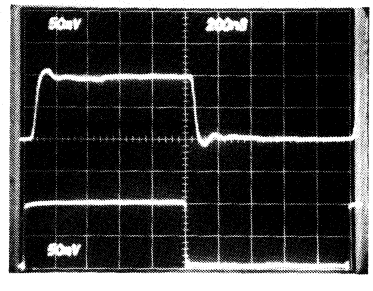
SAMPLING RESPONSE

TOP TRACE : SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)

BOTTOM TRACE : SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)

92CS-27885

Fig.27 – Sampling response for circuit shown in Fig. 25.

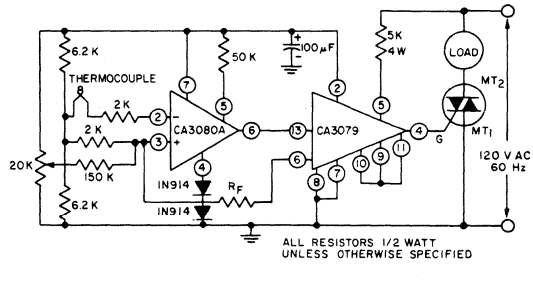


TOP TRACE : OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)

BOTTOM TRACE : INPUT
(50 mV/DIV. AND 200 ns/DIV.)

92CS-27883

Fig.28 – Input and output response for circuit shown in Fig. 25.



92CS-22619RI

Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.

CA3080, CA3080A

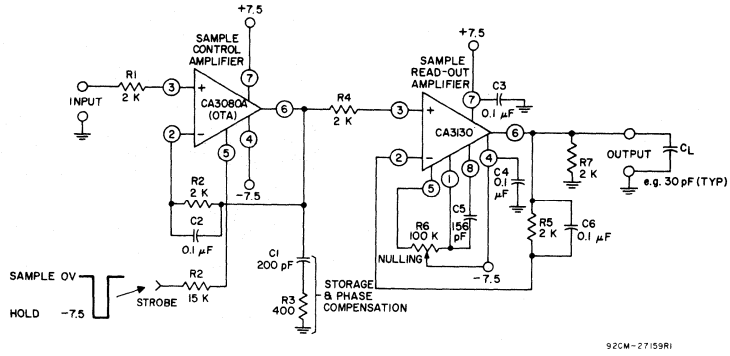
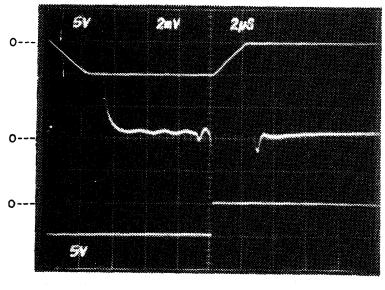
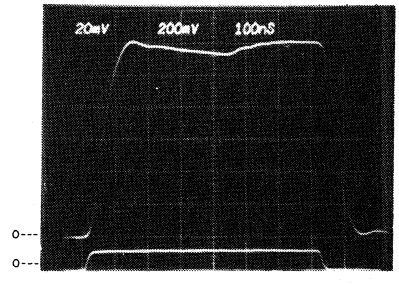


Fig.30 – Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 μs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT—2 mV/DIV. & 2 μs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 μs/DIV.
92CS-27161

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT — 20 mV/DIV. & 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.
92CS-27160

Fig.32 – Small-signal response for circuit shown in Fig. 30.

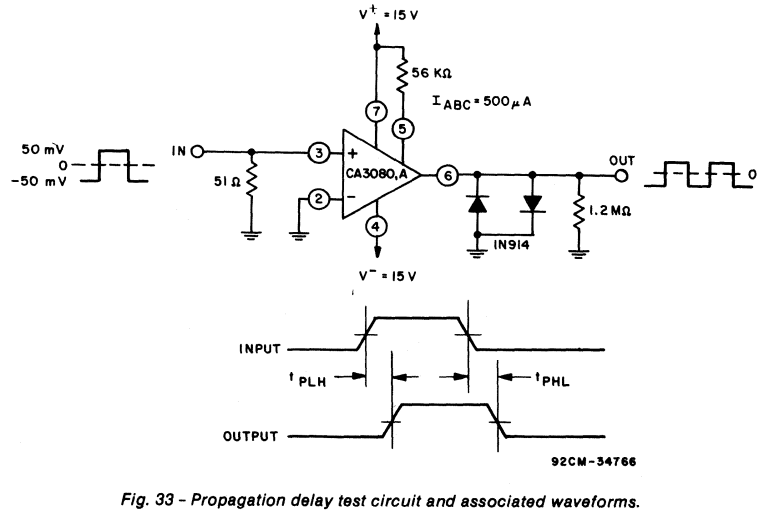


Fig. 33 - Propagation delay test circuit and associated waveforms.

CA3094, CA3094A, CA3094B

Programmable Power Switch/Amplifier

For Control & General-Purpose Applications

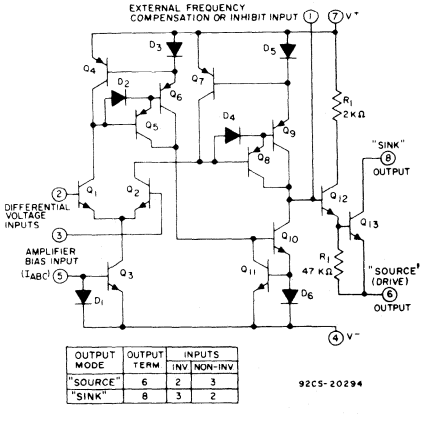
CA3094T,S,E:	For Operation Up to 24 Volts
CA3094AT,S,E:	For Operation Up to 36 Volts
CA3094BT,S:	For Operation Up to 44 Volts

Features:

- *Designed for single or dual power supply*
- *Programmable: strobing, gating, squelching, AGC capabilities*
- *Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)*
- *High-power, single-ended class A amplifier will deliver power output of 0.6 watt [1.6 W device dissipation]*
- *Total harmonic distortion [THD] @ 0.6 W in class A operation - 1.4% typ.*

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transitors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).



OUTPUT MODE	OUTPUT TERM	INPUTS INV	INPUTS NON-INV
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1 — Schematic diagram of CA3094.

Applications:

- *Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor*
- *Over-current, over-voltage, over-temperature protectors*
- *Dual-tracking power supply with RCA-CA3085*
- *Wide-frequency-range oscillator*
- *Analog timer*
- *Level detector*
- *Alarm systems*
- *Voltage follower*
- *Ramp-voltage generator*
- *High-power comparator*
- *Ground-fault interrupter [GFI] circuits*

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs. 28, 29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).

File Number **598**

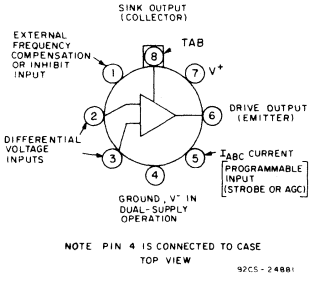
CA3094, CA3094A, CA3094B

MAXIMUM RATINGS, *Absolute-Maximum Values:*

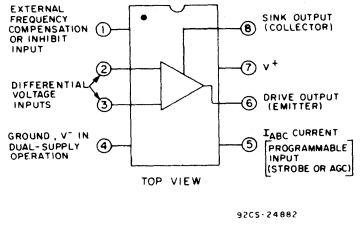
	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ⩽ Term. 2 & 3 ⩽ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

FUNCTIONAL DIAGRAMS



TO-5 Style Package



Plastic Package

TYPICAL CHARACTERISTICS CURVES

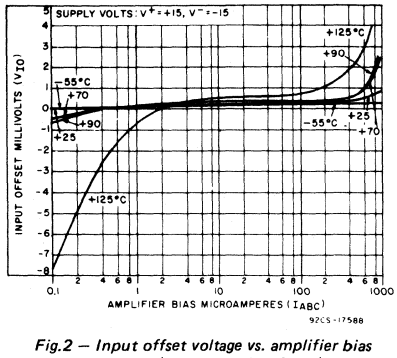


Fig.2 — Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

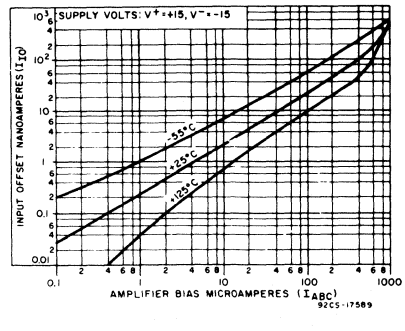


Fig.3 — Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

CA3094, CA3094A, CA3094B

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
INPUT PARAMETERS					
Input Offset Voltage V_{IO}	T_A = 25°C	–	0.4	5	mV
	T_A = 0 to 70°C	–	–	7	mV
Input-Offset-Voltage Change $\lvert\Delta V_{IO}\rvert$	Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA	–	1	8	mV
Input Offset Current I_{IO}	T_A = 25°C	–	0.02	0.2	μA
	T_A = 0 to 70°C	–	–	0.3	μA
Input Bias Current I_I	T_A = 25°C	–	0.2	0.50	μA
	T_A = 0 to 70°C	–	–	0.70	μA
Device Dissipation P_D	I_{out} = 0	8	10	12	mW
Common-Mode Rejection Ratio CMRR		70	110	–	dB
Common-Mode Input–Voltage Range V_{ICR}	V^+ = 30 V High	27	28.8	–	V
	V^+ = 30 V Low	1.0	0.5	–	V
	V^+ = 15 V	+12	+13.8	–	V
	V^- = 15 V	−14	−14.5	–	V
Unity Gain-Bandwidth	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	30	–	MHz
Open-Loop Bandwidth At −3 dB Point BW_{OL}	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	4	–	kHz
Total Harmonic Distortion (Class A Operation) THD	P_D = 220 mW	–	0.4	–	%
	P_D = 600 mW	–	1.4	–	%
Amplifier Bias Voltage (Terminal No.5 to Terminal No.4) V_{ABC}		–	0.68	–	V
Input Offset Voltage Temperature Coefficient $\Delta V_{IO}/\Delta T$		–	4	–	μV/°C
Power-Supply Rejection $\Delta V_{IO}/\Delta V$		–	15	150	μV/V
1/F Noise Voltage E_N	f = 10 Hz, I_{ABC} = 50 μA	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current I_N	f = 10 Hz, I_{ABC} = 50 μA	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance R_I	I_{ABC} = 20 μA	0.50	1	–	MΩ
Differential Input Capacitance C_I	f = 1 MHz, V^+ = 30 V	–	2.6	–	pF

CA3094, CA3094A, CA3094B

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1 V)					
Peak Output Voltage: (Terminal No. 6) With Q13 "ON" V^+_{OM} With Q13 "OFF" V^-_{OM}	V^+ = 30 V R_L = 2 kΩ to ground	26 –	27 0.01	– 0.05	V V
Peak Output Voltage: (Terminal No. 6) Positive V^+_{OM} Negative V^-_{OM}	V^+ = +15 V, V^- = -15 V R_L = 2 kΩ to −15 V	+11 –	+12 −14.99	0.5 – −14.95	V V
Peak Output Voltage: (Terminal No. 8) With Q13 "ON" V^+_{OM} With Q13 "OFF" V^-_{OM}	V^+ = 30 V R_L = 2 kΩ to 30 V	29.95 –	29.99 0.040	– –	V V
Peak Output Voltage: (Terminal No. 8) Positive V^+_{OM} Negative V^-_{OM}	V^+ = 15 V, V^- = − 15 V R_L = 2 kΩ to + 15 V	+14.95 –	+14.99 14.96	– –	V V
Collector-to-Emitter Saturation Voltage (Terminal No. 8) $V_{CE(sat)}$	V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)	V^+ = 30 V	–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13}) h_{fe}	V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	16,000	100,000	–	
Output Capacitance: Terminal No. 6 Terminal No. 8 C_O	f = 1 MHz All Remaining Terminals Tied to Terminal No. 4	– –	5.5 17	– –	pF pF
TRANSFER PARAMETERS					
Voltage Gain A	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	20,000 86	100,000 100	– –	V/V dB
Forward Transconductance To Terminal No. 1 g_m		1650	2200	2750	μmhos
Slew Rate: Open Loop: Positive Slope Negative Slope	I_{ABC} = 500 μA R_L = 2 kΩ	– –	500 50	– –	V/μs V/μs
Unity Gain (Non-Inverting, Compensated)	I_{ABC} = 500 μA R_L = 2 kΩ	–	0.7	–	V/μs

TYPICAL CHARACTERISTICS CURVES (Cont'd)

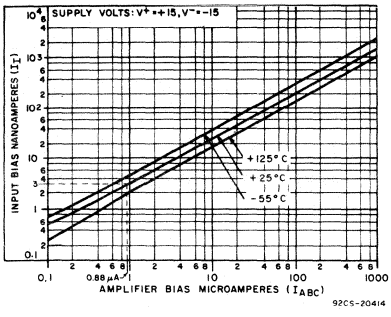


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

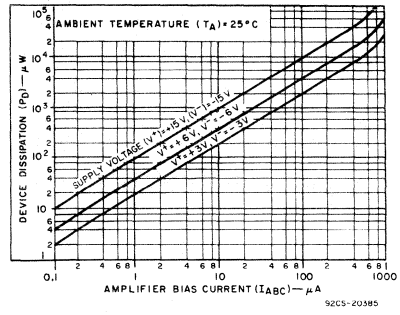


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

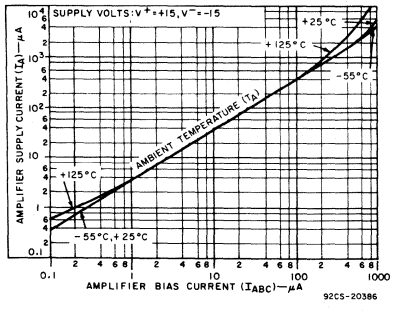


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

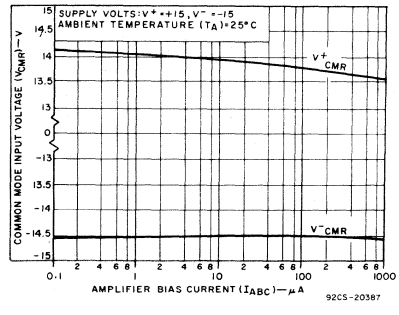


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

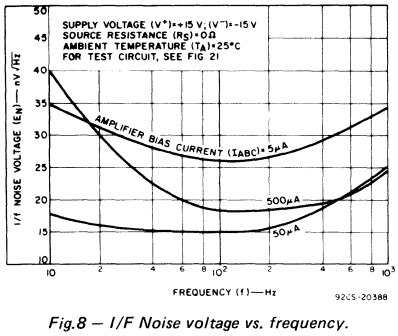


Fig.8 – I/F Noise voltage vs. frequency.

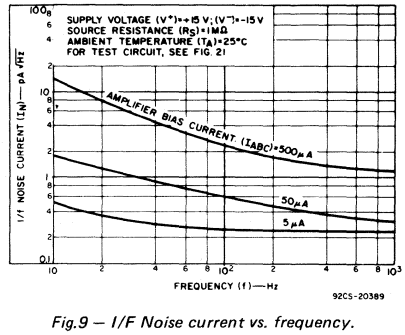


Fig.9 – I/F Noise current vs. frequency.

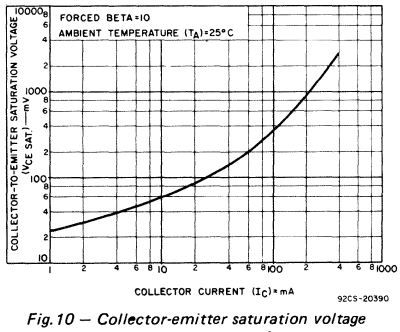


Fig.10 – Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

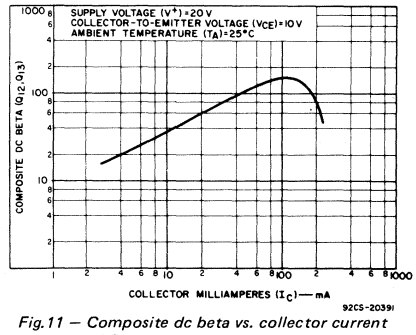


Fig.11 – Composite dc beta vs. collector current of Darlington-connected output transistors (Q_{12}, Q_{13}).

CA3094, CA3094A, CA3094B

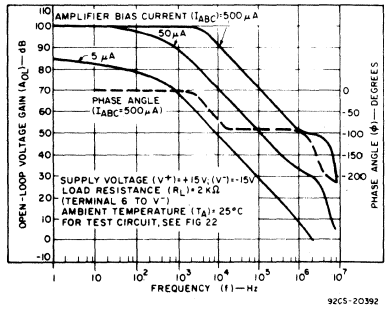


Fig.12 — Open-loop voltage gain vs. frequency.

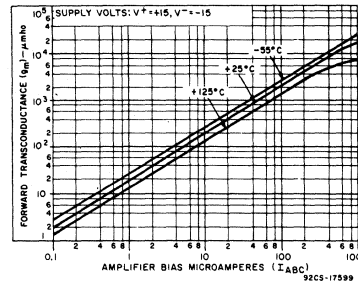


Fig.13 — Forward transconductance vs amplifier bias current.

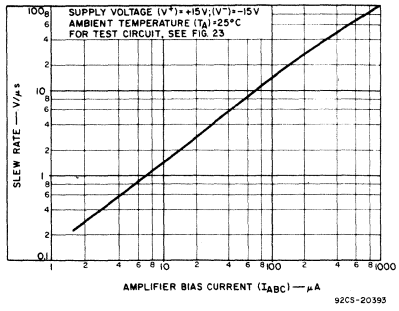


Fig.14 — Slew rate vs amplifier bias current.

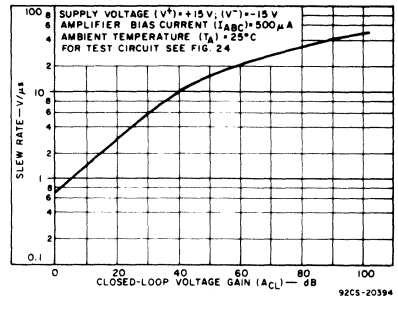


Fig.15 — Slew rate vs closed-loop voltage gain.

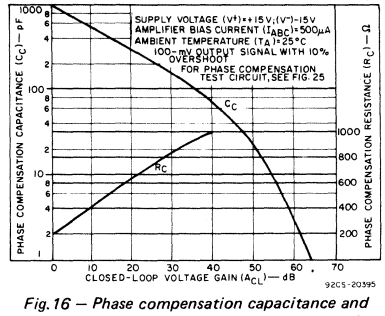


Fig.16 — Phase compensation capacitance and resistance vs closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No.8) and the "Drive" Output (terminal No.6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No.6 and terminal No.4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No.7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No.8 and terminal No.7, the current-limiting resistor should be connected between terminal No.6 and terminal No.4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No.7 and the V^+ supply.

TEST CIRCUITS

I/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig.21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No.2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10, Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are E_n = 18 nV/$\sqrt{Hz}$ and I_N = 1.8 pA/$\sqrt{Hz}$.

CA3094, CA3094A, CA3094B

TEST CIRCUITS

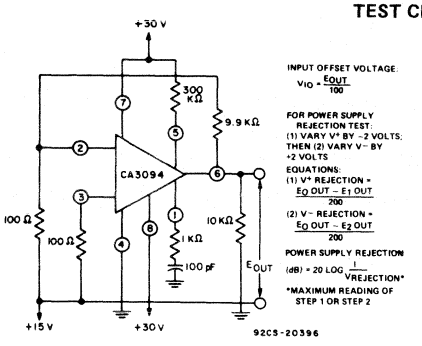


Fig. 17 – Input offset voltage and power-supply rejection test circuit.

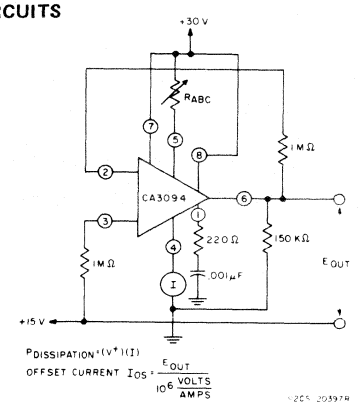


Fig. 18 – Input offset current test circuit.

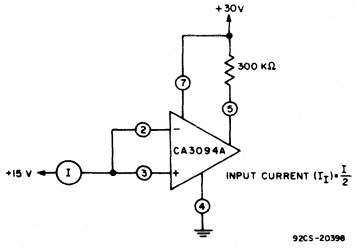


Fig. 19 – Input bias current test circuit.

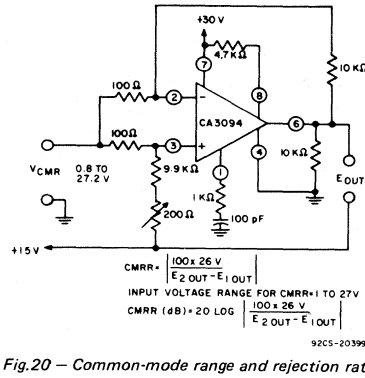


Fig. 20 – Common-mode range and rejection ratio test circuit.

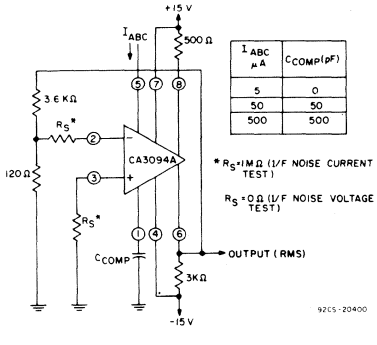


Fig. 21 – 1/F noise test circuit.

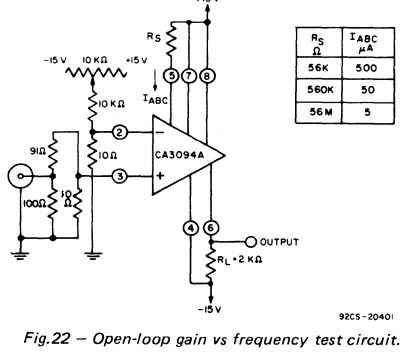


Fig. 22 – Open-loop gain vs frequency test circuit.

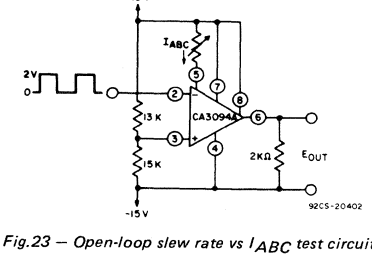


Fig. 23 – Open-loop slew rate vs I_{ABC} test circuit.

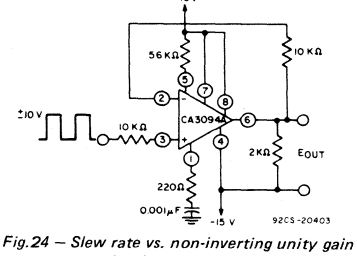
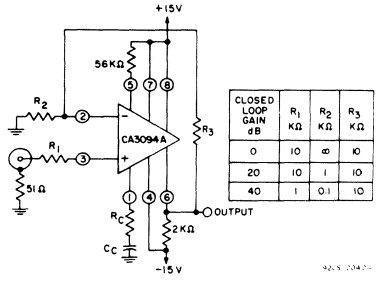


Fig. 24 – Slew rate vs. non-inverting unity gain test circuit.

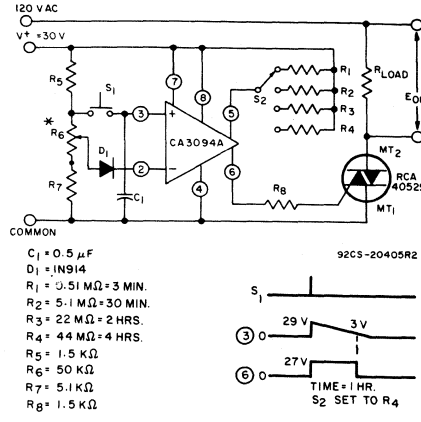
CA3094, CA3094A, CA3094B

TEST CIRCUITS (Cont'd)



CLOSED LOOP GAIN dB	R1 KΩ	R2 KΩ	R3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25 – Phase compensation test circuit.



* POTENTIOMETER REQUIRED FOR INITIAL TIME SET TO PERMIT DEVICE INTERCONNECTING TIME VARIATION WITH TEMPERATURE < 0.3 %/°C.

Fig.26 – Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/ Switch Amplifier IC".

Design Considerations

The selection of the optimum amplifier bias current (I_{ABC}) depends on –

1. The Desired Sensitivity – the higher the I_{ABC}, the higher the sensitivity – i.e., a greater-drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance – the lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and requred input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

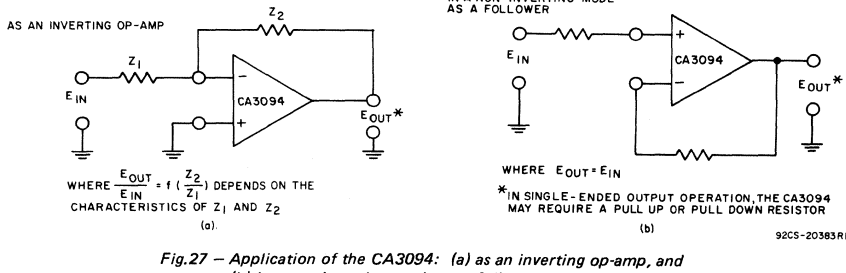
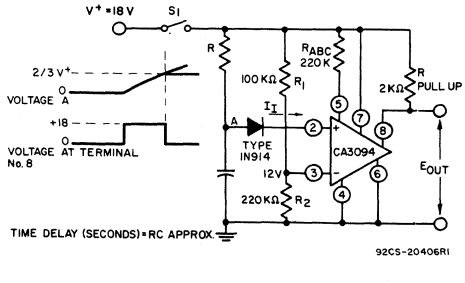


Fig.27 – Application of the CA3094: (a) as an inverting op-amp, and (b) in a non-inverting mode, as a follower.



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given: $I_{ABC} = 5\ \mu A$, $R_{ABC} = 3.6\ M\Omega \approx \frac{18\ V}{5\ \mu A}$

$I_I = 500$ nA @ $I_{ABC} = 100\ \mu A$ (from Fig.4)

$I_I = 5\ \mu A$ can be determined by drawing a line on Fig.4 through $I_{ABC} = 100\ \mu A$ and $I_B = 500$ nA parallel to the typical $T_A = 25^oC$ curve.

Then: $I_I = 33$ nA @ $I_{ABC} = 5\ \mu A$

$$R_{max} = \frac{18 - 12\ volts}{33nA} = 180\ M\Omega\ @\ T_A = 25^oC$$

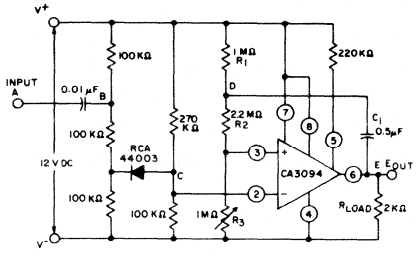
$R_{max} = 180\ M\Omega \times 2/3^* = 120\ M\Omega$ @ $T_A = -55^oC$

* Ratio of I_I at $T_A = +25^oC$ to I_I at $T_A = -55^oC$ for any given value of I_{ABC}.

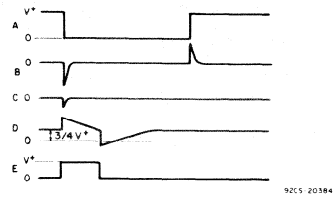
Fig.28 – RC timer.

CA3094, CA3094A, CA3094B

TYPICAL APPLICATIONS (Cont'd)



On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.



At the end of the time constant determined by C_1, R_1, R_2, R_3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input A returns to a high level.

Fig.29 – RC timer triggered by external negative pulse.

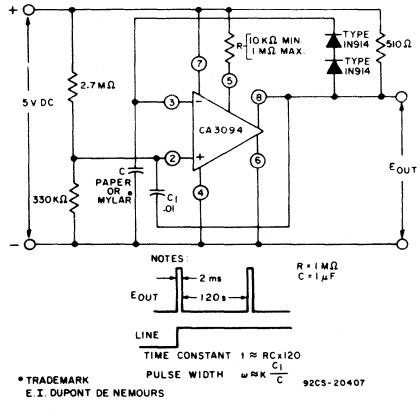


Fig.30 – Free-running pulse generator.

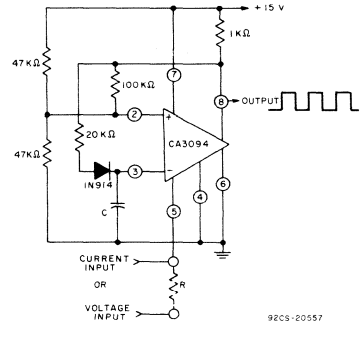


Fig.31 – Current or voltage-controlled oscillator.

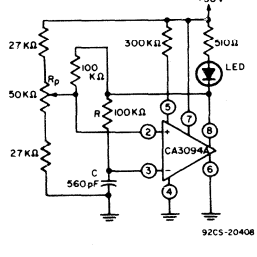


Fig.32 – Single-supply astable multivibrator.

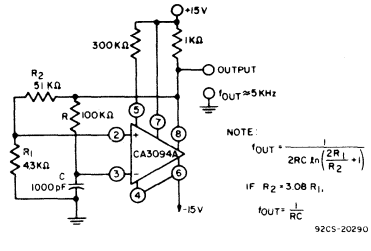
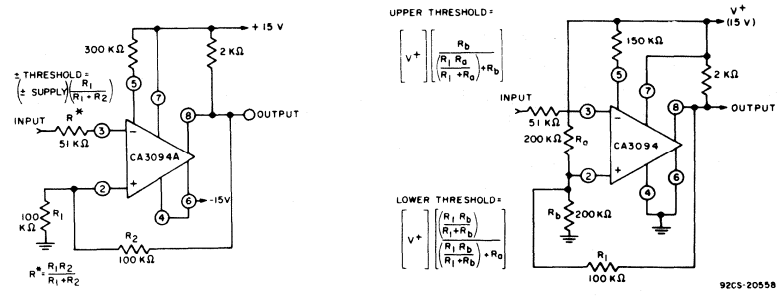


Fig.33 – Dual-supply astable multivibrator.

CA3094, CA3094A, CA3094B

TYPICAL APPLICATIONS (Cont'd)



(a) DUAL SUPPLY (b) SINGLE SUPPLY

Fig.34 — Comparators (threshold detectors) —dual- and single-supply types.

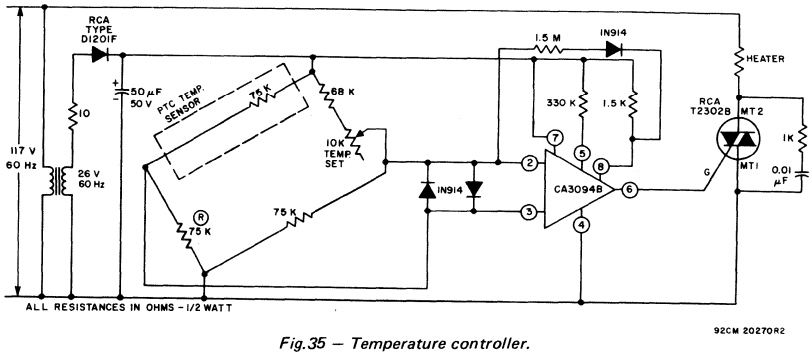


Fig.35 — Temperature controller.

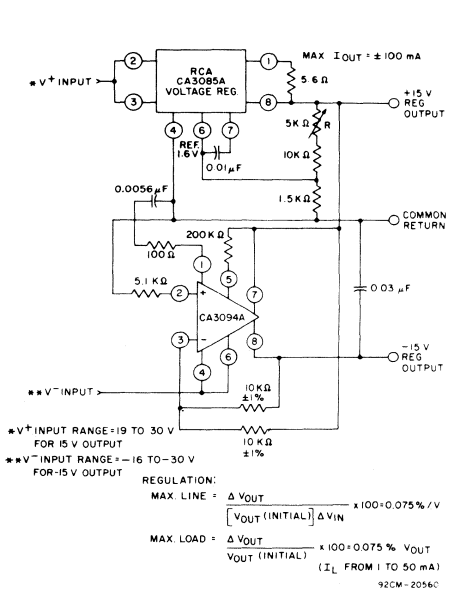


Fig.36 — Dual-voltage tracking regulator.

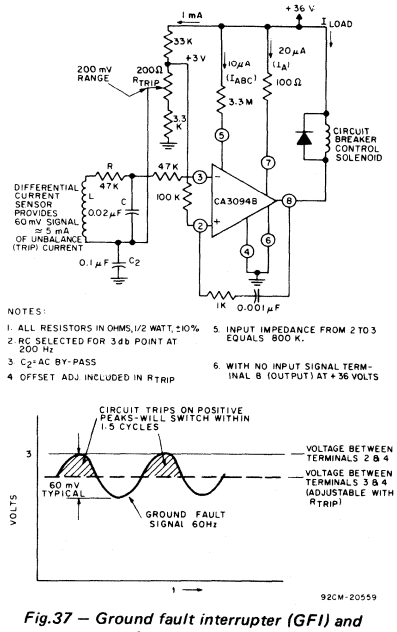
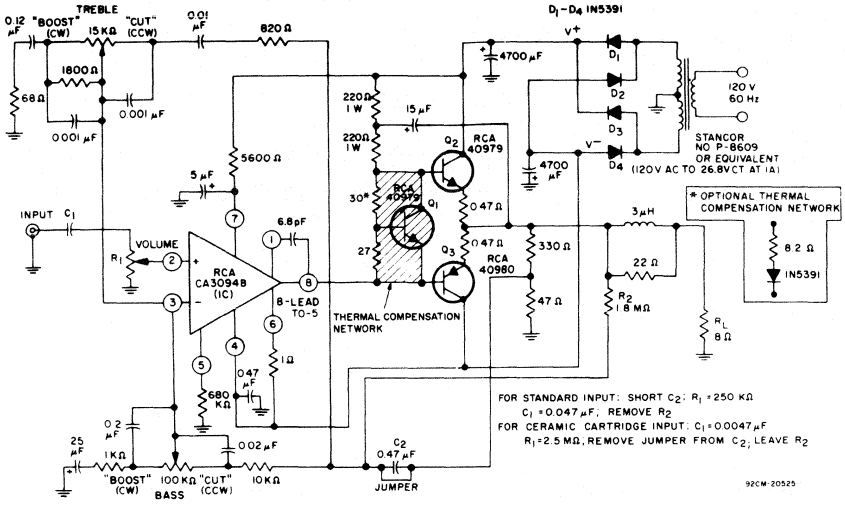


Fig.37 — Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

CA3094, CA3094A, CA3094B



TYPICAL PERFORMANCE DATA
For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 In ICAN-6048	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9 In ICAN-6048	

Fig.38 — 12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

CA3100

Wideband Operational Amplifier

Features:

- *High open-loop gain at video frequencies - 42 dB typ. at 1 MHz*
- *High unity-gain crossover frequency (f_T) - 38 MHz typ.*
- *Wide power bandwidth - V_O = 18 Vp-p typ. at 1.2 MHz*
- *High slew rate - 70 V/μs [typ.] in 20 dB amplifier*
  25 V/μs [typ.] in unity-gain amplifier
- *Fast settling time - 0.6 μs typ.*
- *High output current - ±15 mA min.*
- *LM118, 748/LM101 pin compatibility*
- *Single capacitor compensation*
- *Offset null terminals*

RCA-CA3100S, CA3100T is a large-signal wideband, high-speed operational amplifier which has a unity gain crossover frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 Vp-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and P-MOS transistors on a single monolithic chip.

The CA3100 is supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead TO-5 dual-in-line formed-lead "DIL'CAN" package ("S" suffix).

Applications:

- *Video amplifiers*
- *Fast peak detectors*
- *Meter-driver amplifiers*
- *High-frequency feedback amplifiers*
- *Video pre-drivers*
- *Oscillators*
- *Multivibrators*
- *Voltage-controlled oscillator*
- *Fast comparators*

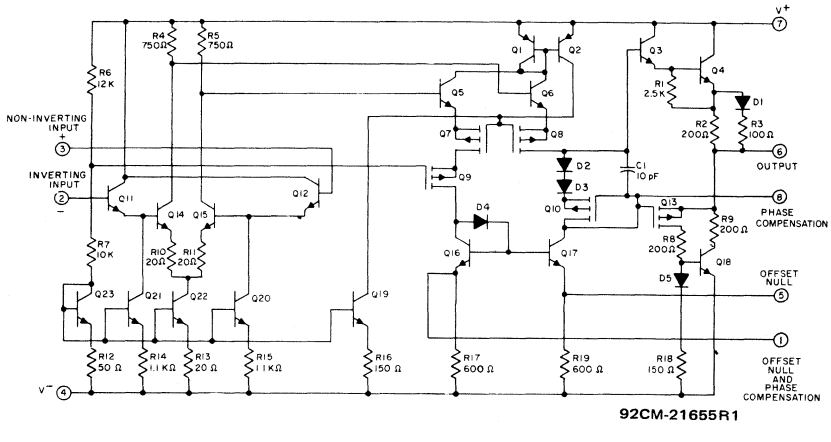
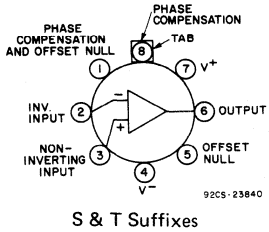


Fig. 1 — Schematic diagram for CA3100.

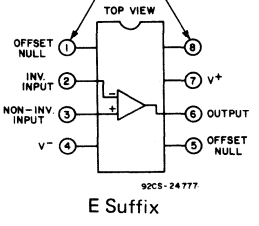
ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS			UNITS
		MIN.	TYP.	MAX.	
STATIC					
Input Offset Voltage, V_{IO}	V_O = 0 ± 0.1 V	–	±1	±5	mV
Input Bias Current, I_{IB}	V_O = 0 ± 1 V	–	0.7	2	μA
Input Offset Current, I_{IO}	V_O = 0 ± 1 V	–	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL}•	V_O = ± 1 V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR ≥ 76 dB	±12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ± 12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	+9	+11	–	V
Maximum Output Voltage: Negative, V_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 2 KΩ	−9	−11	–	V
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	+15	+30	–	mA
Maximum Output Current: Negative, I_{OM}^-	Differential Input Voltage = 0 ± 0.1 V, R_L = 250 Ω	−15	−30	–	mA
Supply Current, I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	C_C = 0, V_O = 0.3 V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	–	V/μs
Slew Rate, SR: Follower Mode	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	–	25	–	V/μs
Power Bandwidth, PBW▲: 20-dB Amplifier	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	–	MHz
Power Bandwidth, PBW▲: Follower Mode	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	–	0.4	–	MHz
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s To Within ± 50 mV of 9 V Output Swing	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ • Low-frequency dynamic characteristic



S & T Suffixes



E Suffix

TERMINAL ASSIGNMENTS

CA3100

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Supply Voltage (between V+ and V− terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V− Terminal Voltage	±0.5	V
Output Current	50	mA•
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C	6.67	mW/°C
Ambient Temperature Range:		
Operating:		
E Type	−40 to +85	°C
S and T Types	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

* If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

• CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

TYPICAL CHARACTERISTIC CURVES

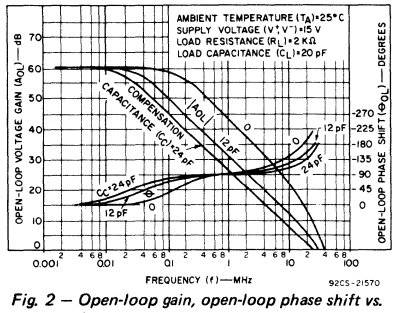


Fig. 2 – Open-loop gain, open-loop phase shift vs. frequency.

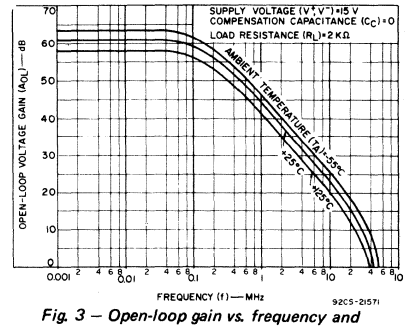


Fig. 3 – Open-loop gain vs. frequency and temperature.

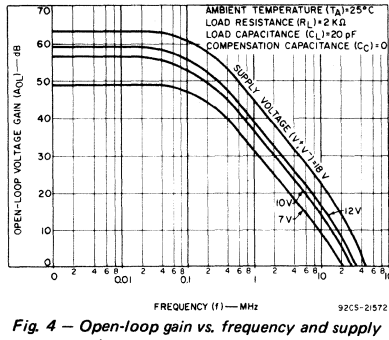


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

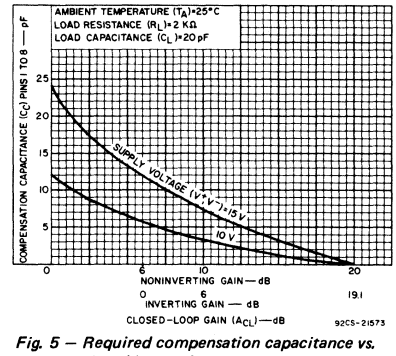


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

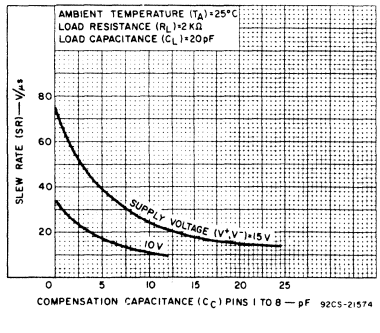


Fig. 6 – Slew rate vs. compensation capacitance.

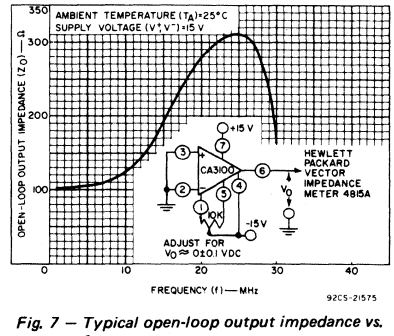


Fig. 7 – Typical open-loop output impedance vs. frequency.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

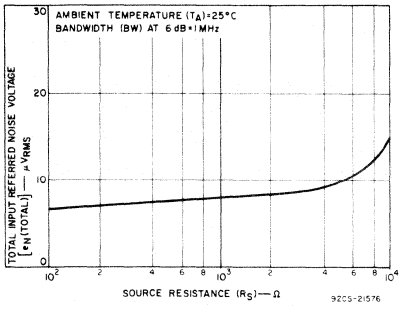


Fig. 8 – Wideband input noise voltage vs. source resistance.

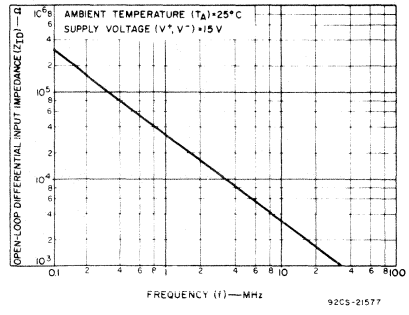


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

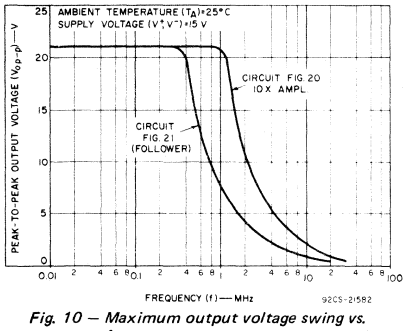


Fig. 10 – Maximum output voltage swing vs. frequency.

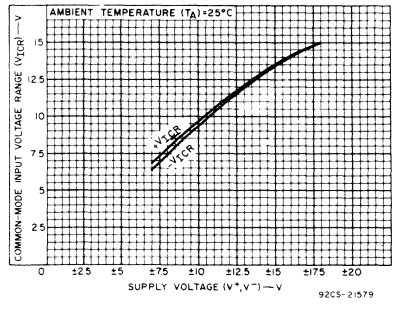


Fig. 11 – Common-mode input voltage range vs. supply voltage.

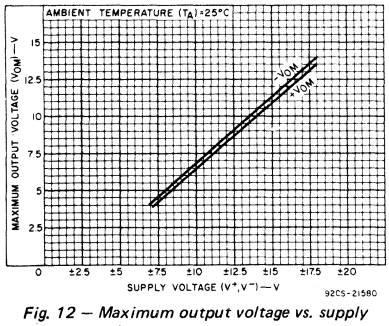


Fig. 12 – Maximum output voltage vs. supply voltage.

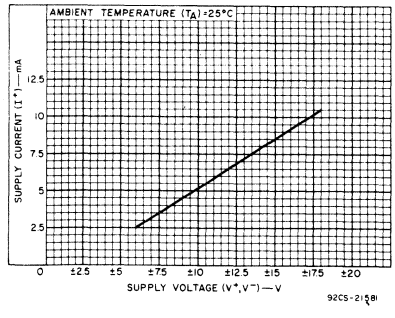


Fig. 13 – Supply current vs. supply voltage.

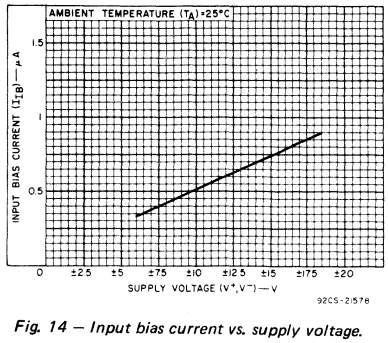


Fig. 14 – Input bias current vs. supply voltage.

CA3100

TEST CIRCUITS

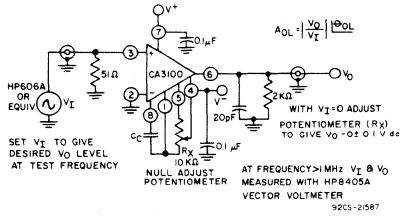


Fig. 15 – Open-loop voltage gain test circuit.

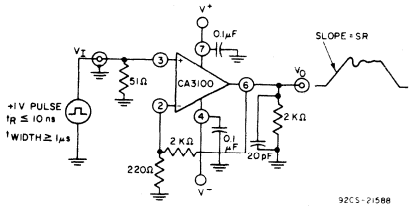


Fig. 16 – Slew rate in 10X amplifier test circuit.

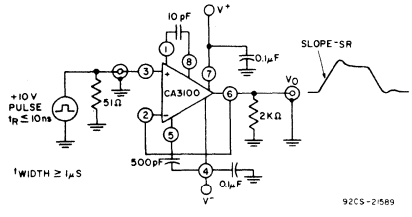


Fig. 17 – Follower slew rate test circuit.

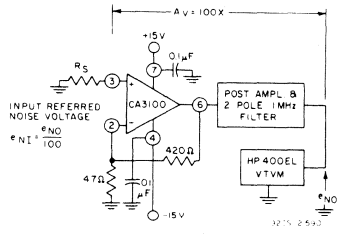


Fig. 18 – Wideband input noise voltage test circuit.

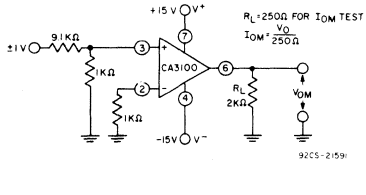


Fig. 19 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

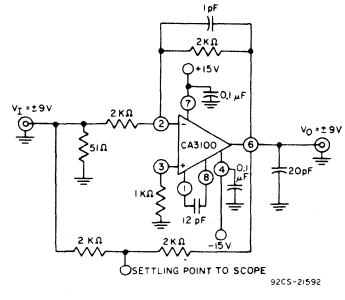


Fig. 20 – Settling time test circuit.

TYPICAL APPLICATIONS

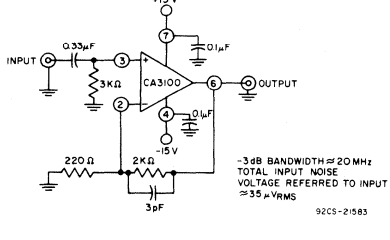


Fig. 21 – 20 dB video amplifier.

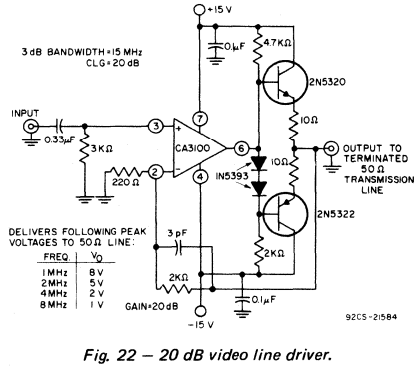


Fig. 22 – 20 dB video line driver.

TYPICAL APPLICATIONS (Cont'd)

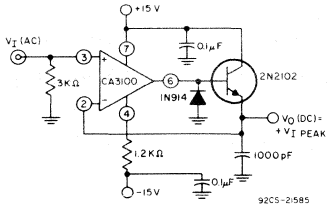


Fig. 23 – Fast positive peak detector.

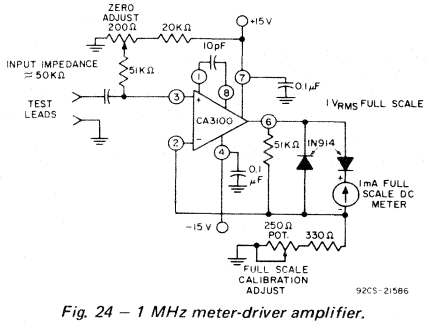
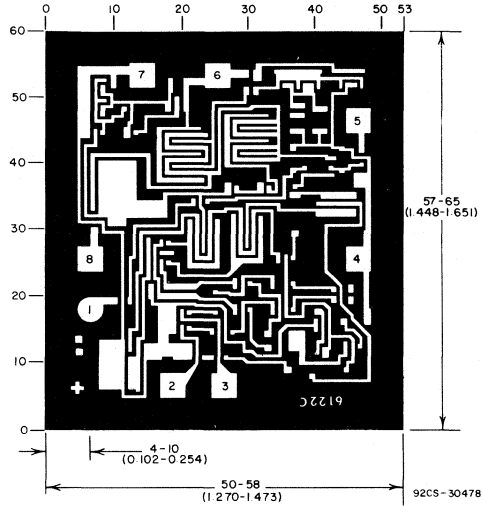


Fig. 24 – 1 MHz meter-driver amplifier.

Chip Dimensions and Pad Layout



CA3100H Chip

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3130A, CA3130
BiMOS Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I=1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I=5 pA typ. at 15-V operation
  =2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

RCA-CA3130A and CA3130 are integrated-circuit operational amplifiers that combine the advantages of both CMOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOS/FET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix). All types operate over the full military-temperature range of -55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

Applications:

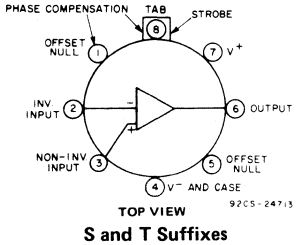
- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (ideal interface with digital CMOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*

File Number **817**

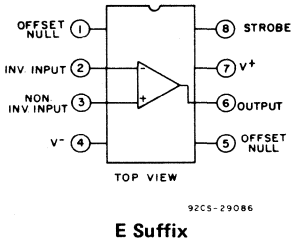
CA3130A, CA3130

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS						Units
	CA3130A (T,S,E)			CA3130 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	2	5	–	8	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	150	–	32	320	μV/V
Maximum Output Voltage:							
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	V
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	V
At R_L=∞ V_{OM}^-	–	0	0.01	–	0	0.01	V
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	mA
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	mA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	10	–	–	10	–	μV/°C



S and T Suffixes



E Suffix

Fig. 1 – Functional diagrams for the CA3130 series.

CA3130A, CA3130

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS: $V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified)	CA3130A CA3130 (T,S,E)	UNITS
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1	±22	mV
Input Resistance, R_I		1.5	TΩ
Input Capacitance, C_I	f = 1 MHz	4.3	pF
Equivalent Input Noise Voltage, e_n	BW = 0.2 MHz, R_S = 1 MΩ*	23	μV
Unity Gain Crossover Frequency, f_T	$C_C = 0$	15	MHz
	C_C = 47 pF	4	
Slew Rate, SR: Open Loop	$C_C = 0$	30	V/μs
Closed Loop	C_C = 56 pF	10	
Transient Response: Rise Time, t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	μs
Overshoot		10	%
Settling Time (4 V_{p-p} Input to <0.1%)		1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.

CHARACTERISTIC	TEST CONDITIONS: $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage, V_{IO}		2	8	mV
Input Offset Current, I_{IO}		0.1	0.1	pA
Input Current, I_I		2	2	pA
Common-Mode Rejection Ratio, CMRR		90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 V_{p-p}, R_L = 5 kΩ	100 k	100 k	V/V
		100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, $R_L = \infty$	300	300	μA
	V_O = 2.5 V, $R_L = \infty$	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	μV/V

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C ..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (all types) ..... −55 to + 125°C
STORAGE (all types) ..... −65 to + 150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 mm) FROM CASE
FOR 10 SECONDS MAX. .... +265°C

*Short circuit may be applied to ground or to either supply.

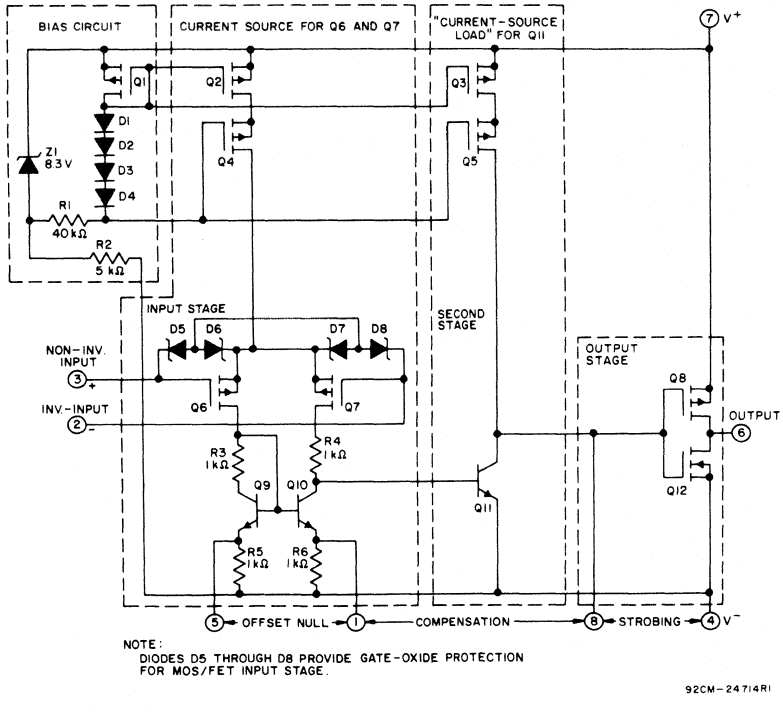


Fig. 2 — Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

CA3130A, CA3130

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

†For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".

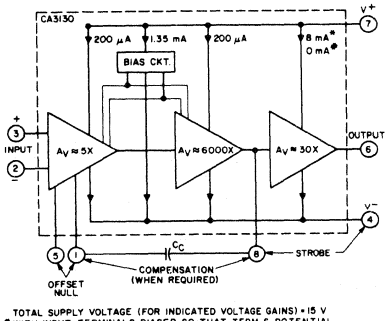


Fig. 3 – Block diagram of the CA3130 Series.

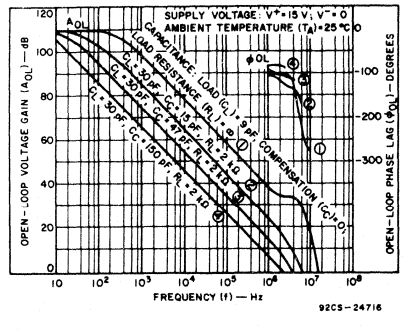


Fig. 4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

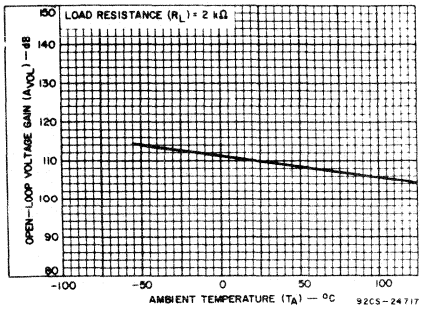


Fig. 5 – Open-loop gain vs. temperature.

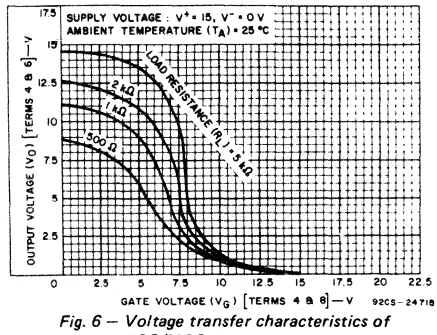


Fig. 6 – Voltage transfer characteristics of COS/MOS output stage.

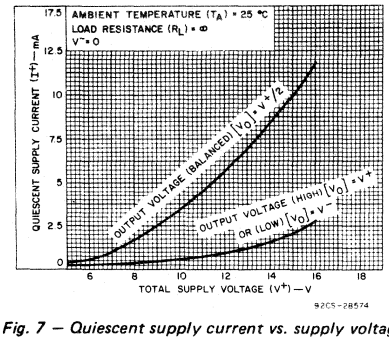


Fig. 7 – Quiescent supply current vs. supply voltage.

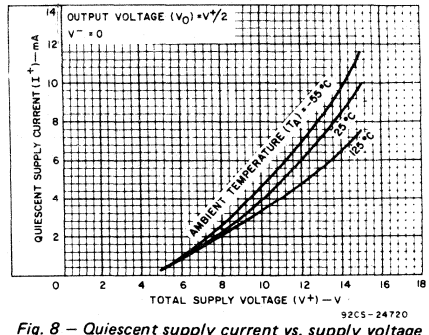


Fig. 8 – Quiescent supply current vs. supply voltage at several temperatures.

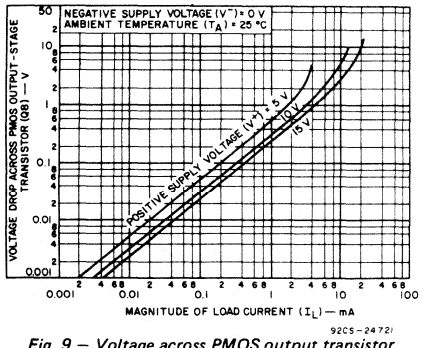


Fig. 9 – Voltage across PMOS output transistor (Q8) vs. load current.

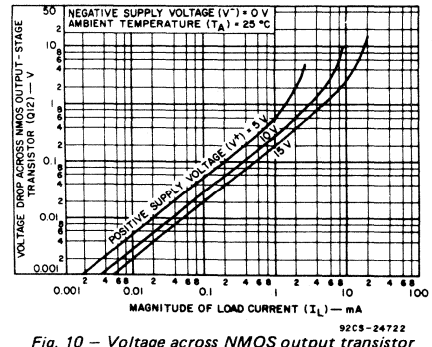


Fig. 10 – Voltage across NMOS output transistor (Q12) vs. load current.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at T_A=25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied

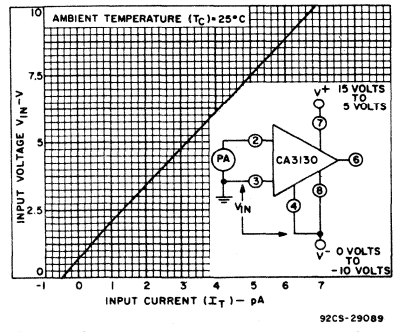


Fig.11 – Input current vs. common-mode voltage.

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

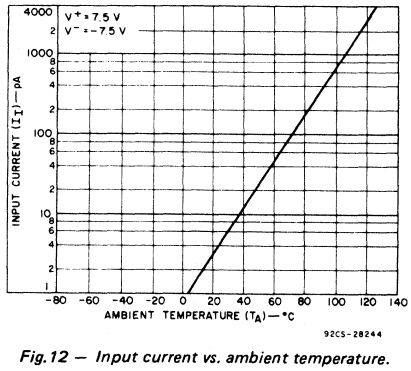


Fig.12 — Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig.13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

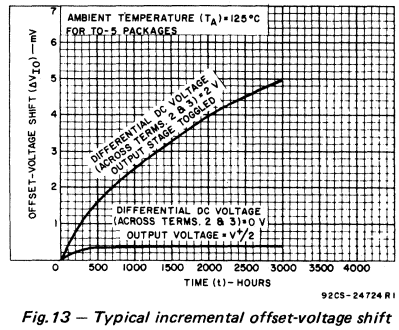


Fig.13 — Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e.,

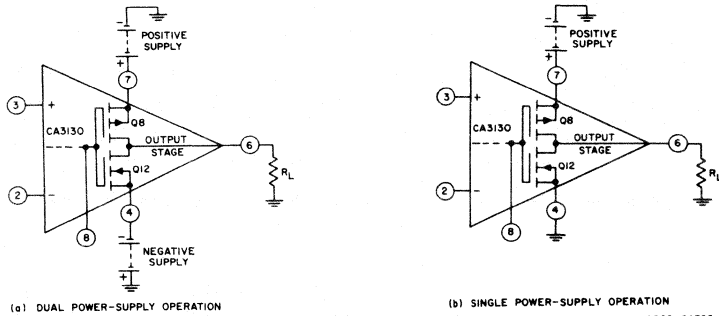


Fig.14 – CA3130 output stage in dual and single power-supply operation.

the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig.14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is

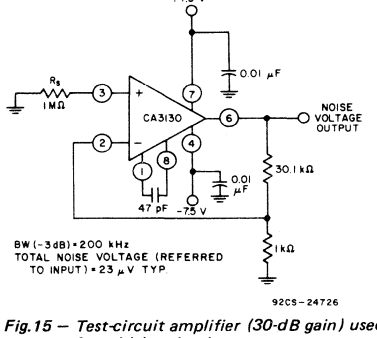
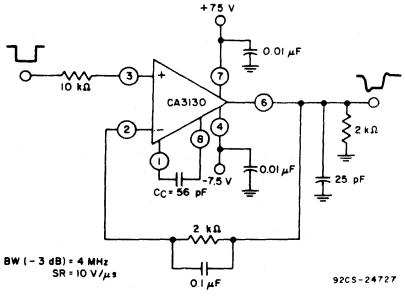
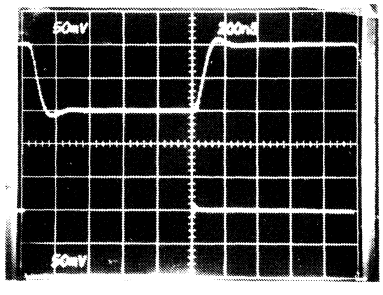


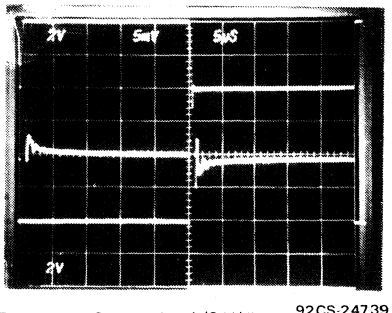
Fig.15 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

CA3130A, CA3130





Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



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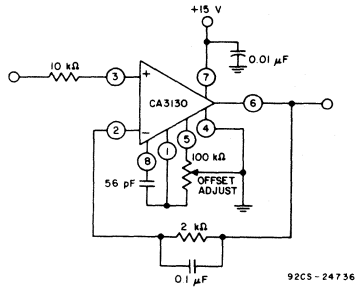
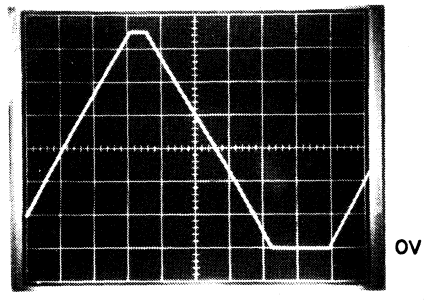
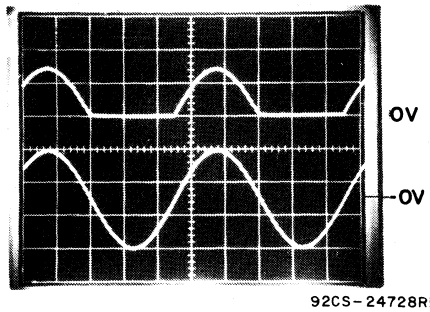
Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

Fig. 16 – Split-supply voltage follower with associated waveforms.





(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



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Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)
(b) Output-waveform with ground-reference sine-wave input

Fig. 17 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

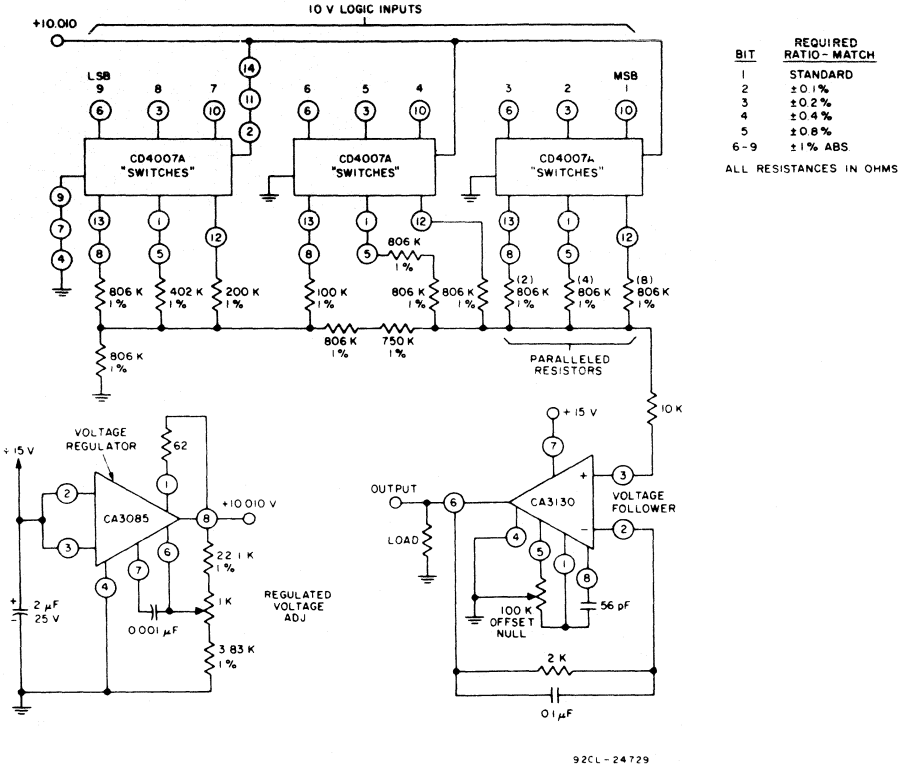
linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.18 This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 18.

of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with varia-



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS

ALL RESISTANCES IN OHMS

Fig. 18–9-bit DAC using CMOS digital switches and CA3130.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly

tions of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

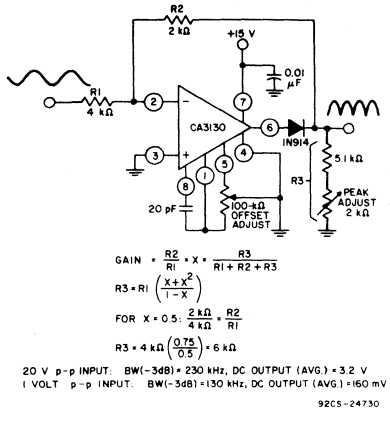
Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

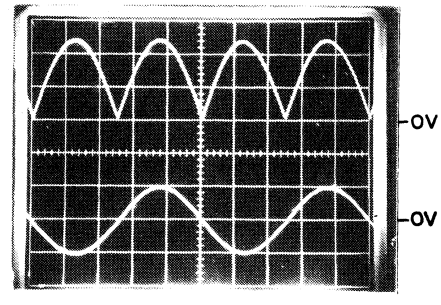
The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

CA3130A, CA3130

negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.





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Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig. 19 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

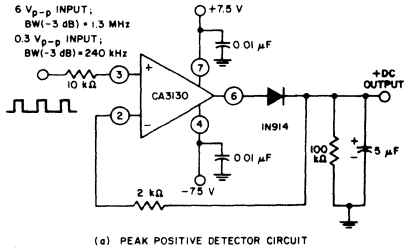
Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 21 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 22 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous ad-



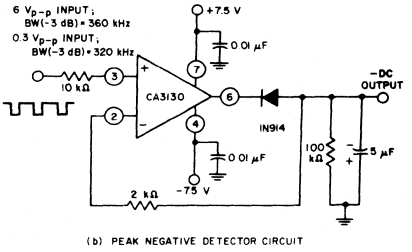


Fig. 20 — Peak-detector circuits.

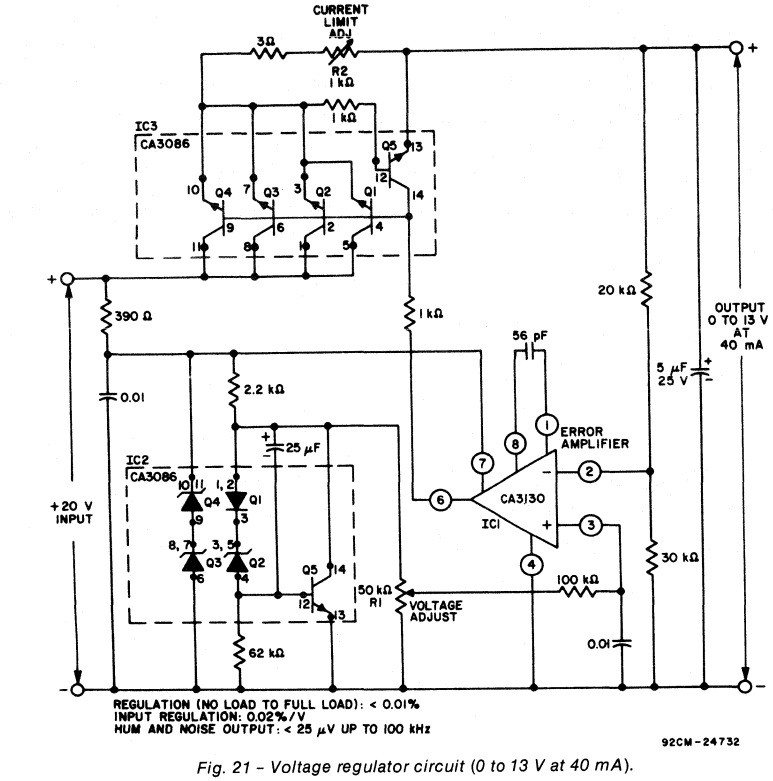


Fig. 21 - Voltage regulator circuit (0 to 13 V at 40 mA).

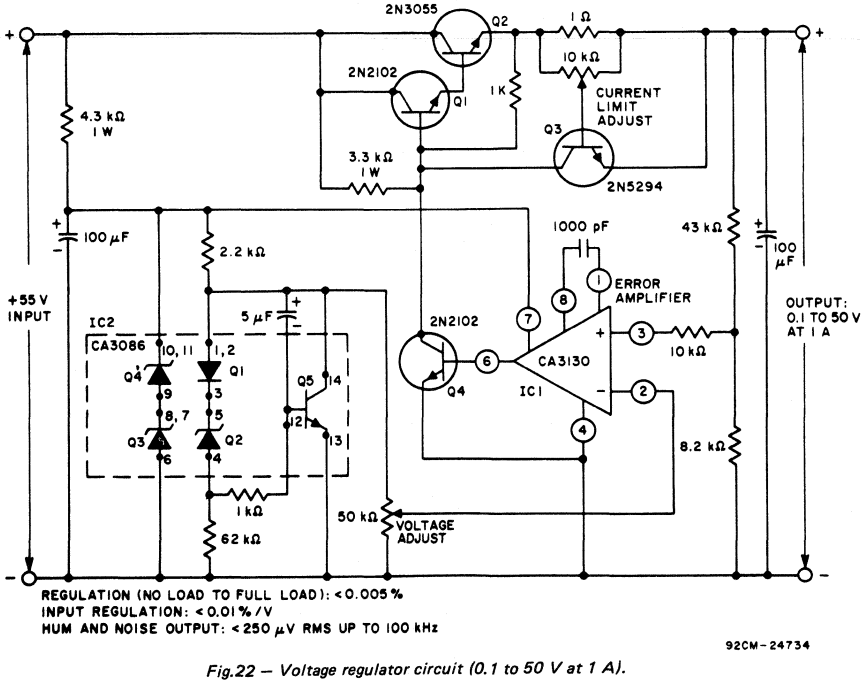


Fig.22 – Voltage regulator circuit (0.1 to 50 V at 1 A).

CA3130A, CA3130

justment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

*See File No. 475 and ICAN-6668.

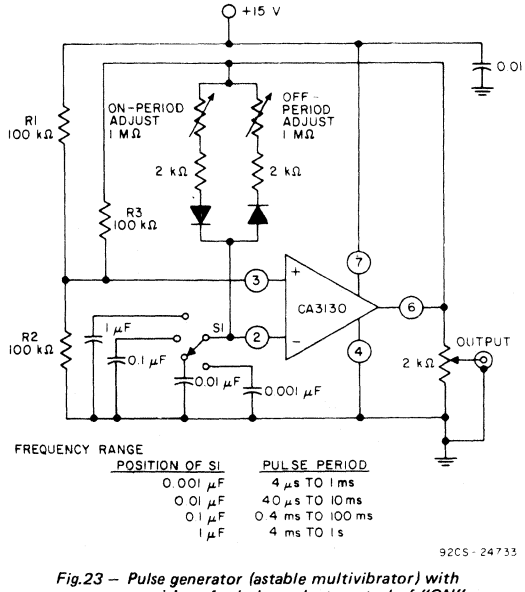


Fig.23 – Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

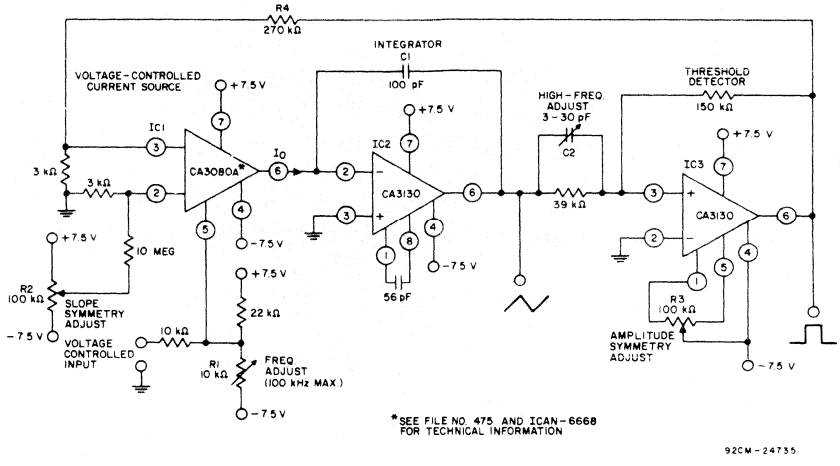


Fig. 24 — Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 25, three CMOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Fig. 25 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (−3 dB) is 50 kHz.

*See File No. 619 for technical information.

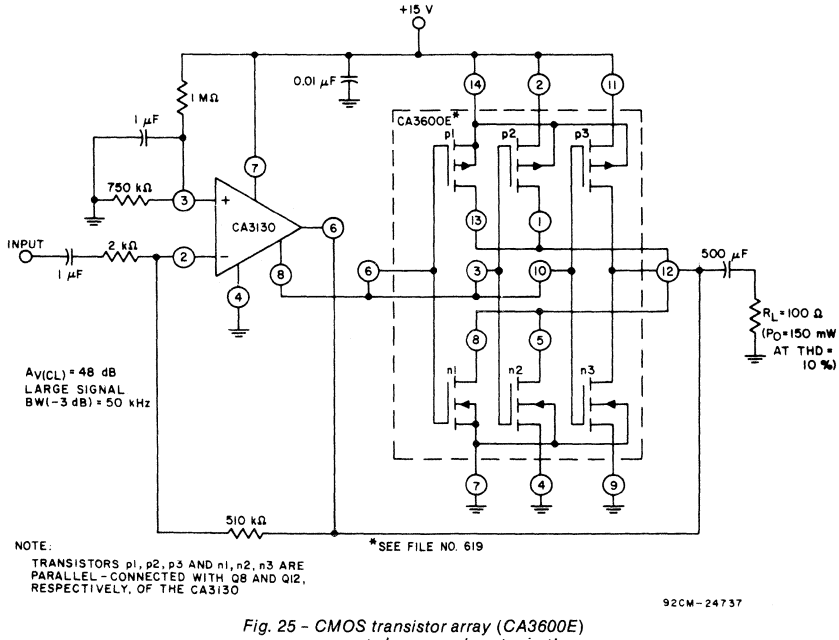
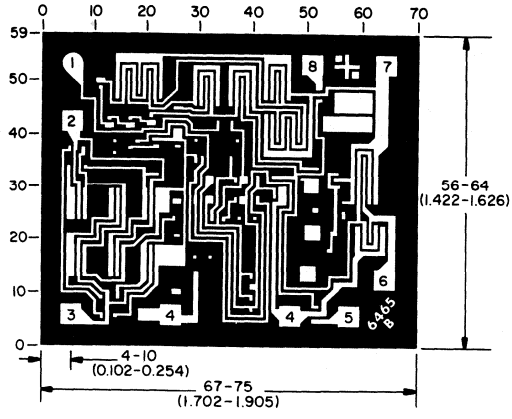


Fig. 25 - CMOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.

CA3130A, CA3130



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and Pad Layout for CA3130H.

CA3140A, CA3140

BiMOS Operational Amplifiers

With MOSFET Input/Bipolar Output

Features:

- *MOSFET Input Stage*
  - *(a) Very high input impedance (Z_{IN})-1.5 TΩ typ.*
  - *(b) Very low input current (I_I)-10 pA typ. at ±15 V*
  - *(c) Wide common-mode input-voltage range (V_{ICR})- can be swung 0.5 volt below negative supply-voltage rail*
  - *(d) Output swing complements input common-mode range*
- *Directly replaces industry type 741 in most applications*

The CA3140A and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 CMOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate-protected MOSFET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140A and CA3140 operate at supply voltages from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line plastic package (Mini-DIP - E Suffix). The CA3140A and CA3140 are intended for operation at supply voltages up to 36 volts (±18 volts). All types can be operated safely over the temperature range from -55° C to +125° C.

Applications:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds-minutes-hours)*
- *Photocurrent instrumentation*
- *Peak detectors*
- *Active filters*
- *Comparators*
- *Interface in 5 V TTL systems and other low-supply voltage systems*
- *All standard operational amplifier applications*
- *Function generators*
- *Tone controls*
- *Power supplies*
- *Portable instruments*
- *Intrusion alarm systems*

File Number **957**

CA3140A, CA3140

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz, R_S = 100 Ω	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz, R_S = 100 Ω	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply: Source	I_{OM^+}		40	40	mA
Sink	I_{OM^-}		18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T		4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR		9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low			220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF	0.08	0.08	μs
Overshoot (See Fig. 37)	t_r	R_L = 2 kΩ, C_L = 100 pF	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17) 1 mV	t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	4.5	4.5	μs
Settling Time at 10 V_{p-p}, (See Fig.17) 10 mV	t_s	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower	1.4	1.4	μs

CA3140A, CA3140

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

CHARACTERISTIC	LIMITS						UNITS
	CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	20 k	100 k	–	20 k	100 k	–	V/V
	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	32	320	–	32	320	μV/V
	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR (See Fig.11) $\Delta V_{IO}/\Delta V$	–	100	150	–	100	150	μV/V
	76	80	–	76	80	–	dB
Max. Output Voltage■ (See Figs.13,20) V_{OM}^+	+12	13	–	+12	13	–	V
V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	mW
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	6	–	–	8	–	μV/°C
Max. Output Voltage,★ V_{OM}^+	–	–	–	–	–	–	V
V_{OM}^-	–	–	–	–	–	–	

● At $V_O = 26V_{p\text{-}p}$, +12V, −14V and $R_L = 2\,k\Omega$.

■ At $R_L = 2\,k\Omega$.

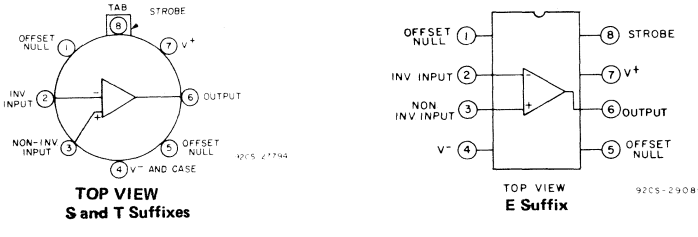


Fig. 1 – Functional diagrams of the CA3140 series.

CA3140A, CA3140

MAXIMUM RATINGS, *Absolute-Maximum Values:*

CA3140, CA3140A

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 36 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ± 8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK -
UP TO 55°C ..... 1 W
ABOVE 55°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING (ALL TYPES) ..... -55 to +125°C
STORAGE (ALL TYPES) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. ..... +265°C

* Short circuit may be applied to ground or to either supply.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25°C$

CHARACTERISTIC		CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\lvert V_{IO} \rvert$	2	5	mV
Input Offset Current	$\lvert I_{IO} \rvert$	0.1	0.1	pA
Input Current	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain	A_{OL}	100 k	100 k	V/V
(See Figs.4,18)		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	−0.5	−0.5	V
(See Fig.20)		2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	100	100	μV/V
		80	80	dB
Maximum Output Voltage	V_{OM}^+	3	3	V
(See Figs.13,20)	V_{OM}^-	0.13	0.13	
Maximum Output Current:				
Source	I_{OM}^+	10	10	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig.6)		7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	mA
Device Dissipation	P_D	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	μA

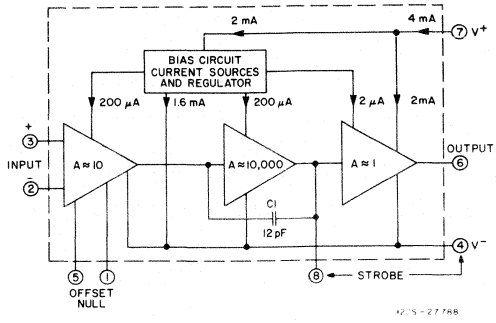


Fig.2 – Block diagram of CA3140 series.

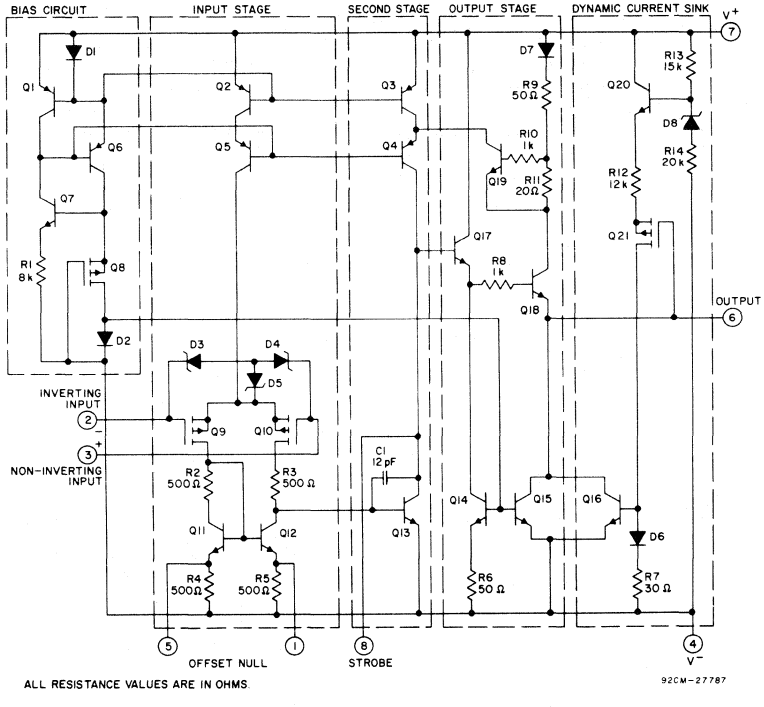


Fig.3 – Schematic diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differen-

tial-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage — Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage — The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V− bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V− supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V− bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit — Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

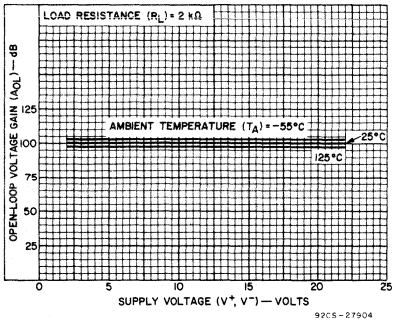


Fig.4 — Open-loop voltage gain vs supply voltage and temperature.

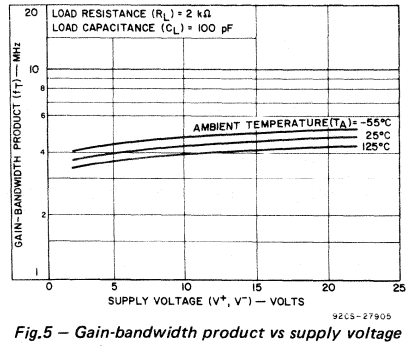


Fig.5 — Gain-bandwidth product vs supply voltage and temperature.

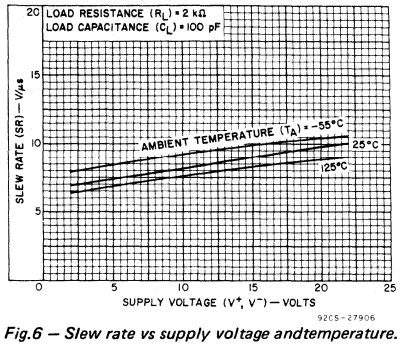


Fig.6 — Slew rate vs supply voltage andtemperature.

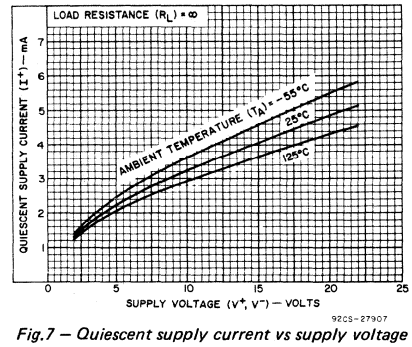


Fig.7 — Quiescent supply current vs supply voltage and temperature.

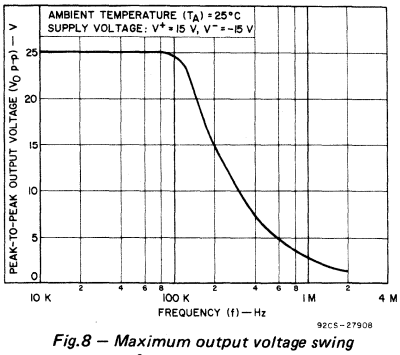


Fig.8 — Maximum output voltage swing vs frequency.

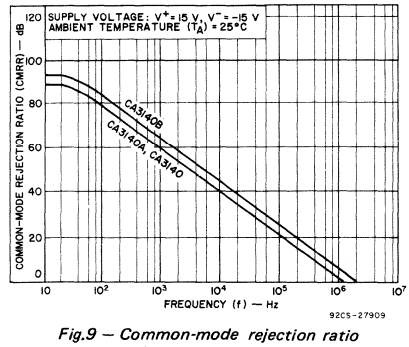


Fig.9 — Common-mode rejection ratio vs frequency.

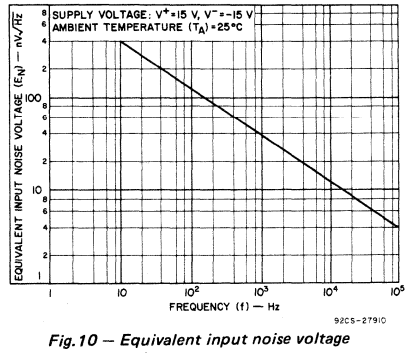


Fig.10 — Equivalent input noise voltage vs frequency.

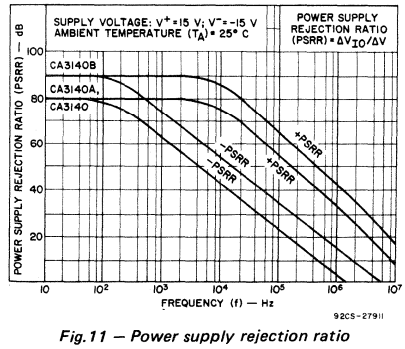


Fig.11 — Power supply rejection ratio vs frequency.

CA3140A, CA3140

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained — a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

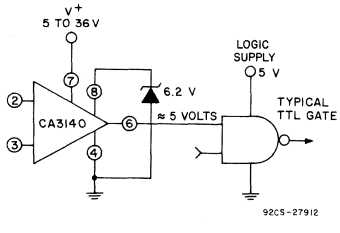


Fig.12 — Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

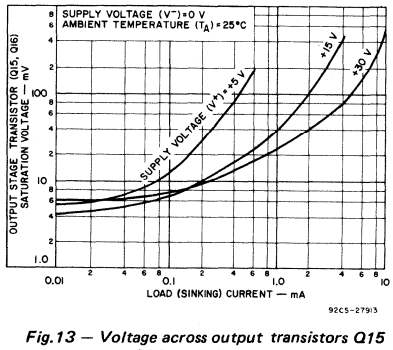


Fig.13 — Voltage across output transistors Q15 and Q16 vs load current.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

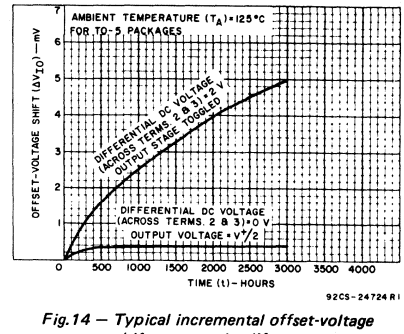


Fig.14 — Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total

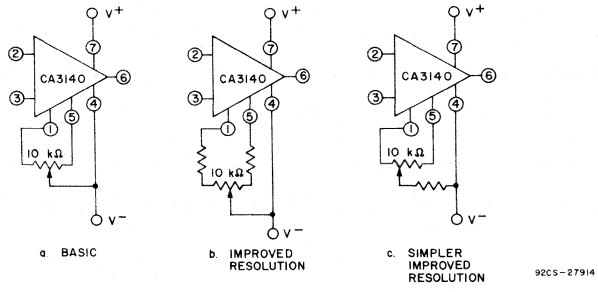


Fig.15 – Three offset-voltage nulling methods.

supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.

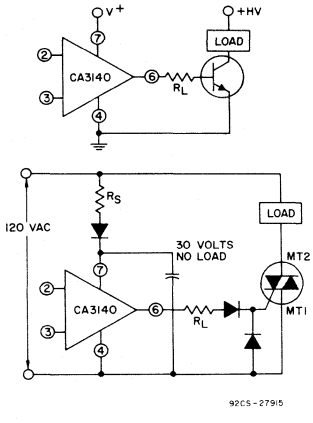


Fig.16 – Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3140 series.

BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast setting time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Fig. 18.

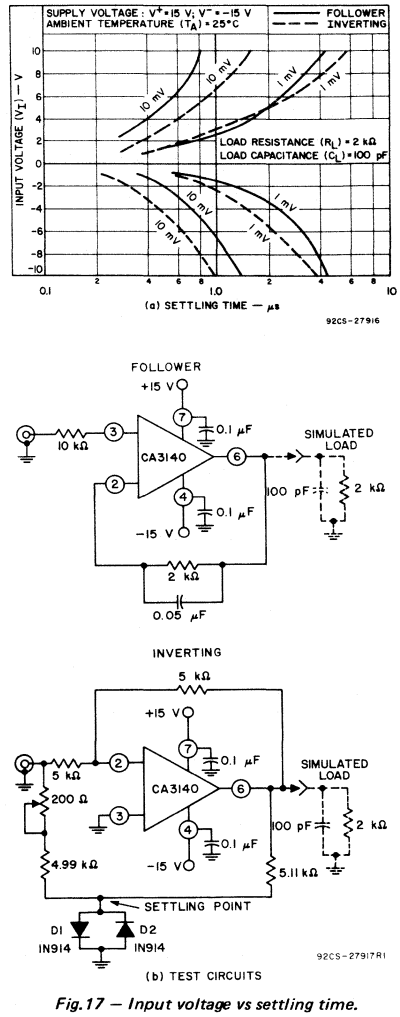


Fig.17 – Input voltage vs settling time.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting re-

CA3140A, CA3140

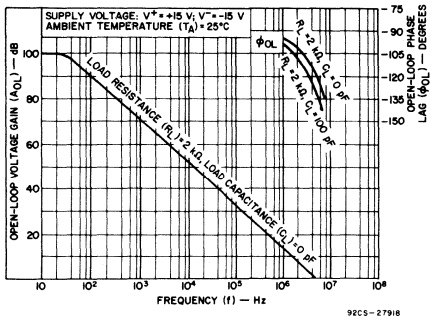


Fig. 18 — Open-loop voltage gain and phase lag vs frequency.

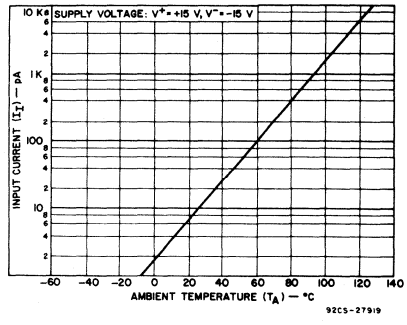


Fig. 19 — Input current vs ambient temperature.

sistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1

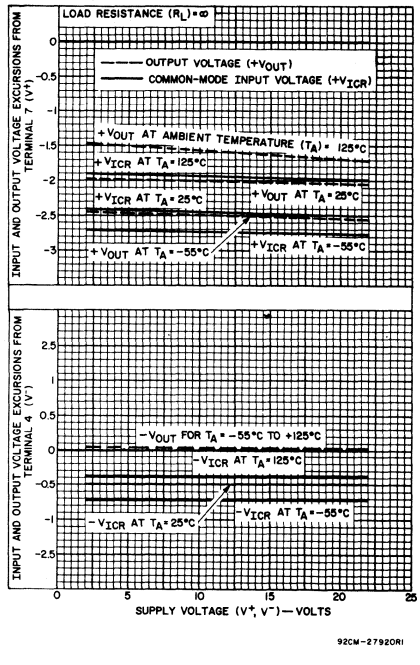


Fig. 20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

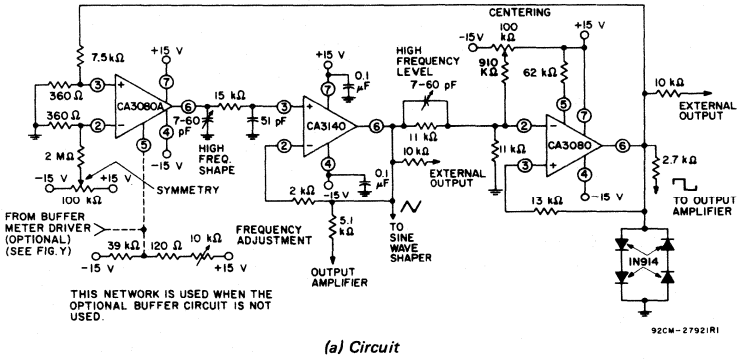
Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

input of the CA3080A current source, thereby, completing the positive feedback loop.

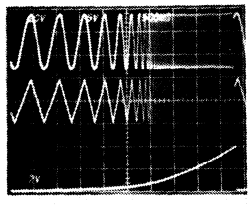
The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.



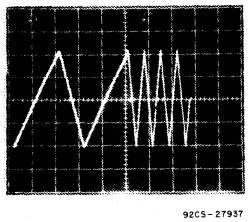
(a) Circuit



TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS 5 V/DIV AND 500 ms/DIV
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR 2 V/DIV AND 500 ms/DIV
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR 10 V/DIV AND 500 ms/DIV

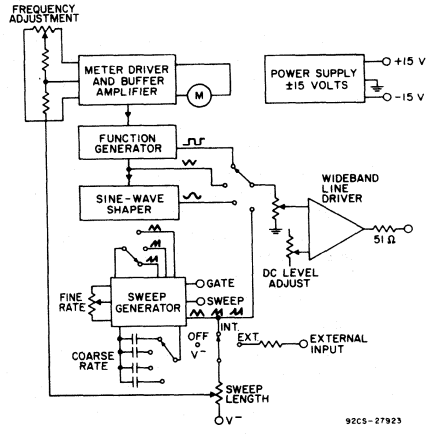
92CS-27922

(b1) Function generator sweeping



92CS-27937

(b2) Function generator with fixed frequencies



(c) Interconnections

1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency ⩾ 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

Fig.21 – Function generator.

CA3140A, CA3140

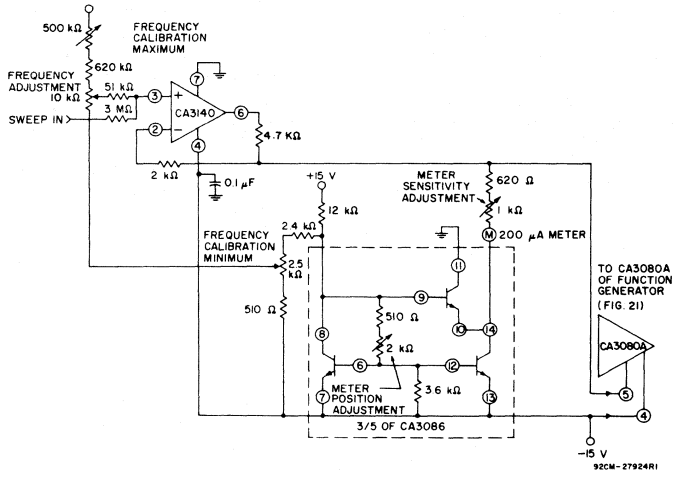


Fig. 22 – Meter driver and buffer amplifier.

METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessarv

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

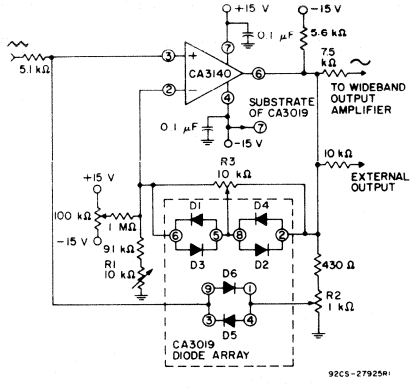


Fig. 23 — Sine-wave shaper.

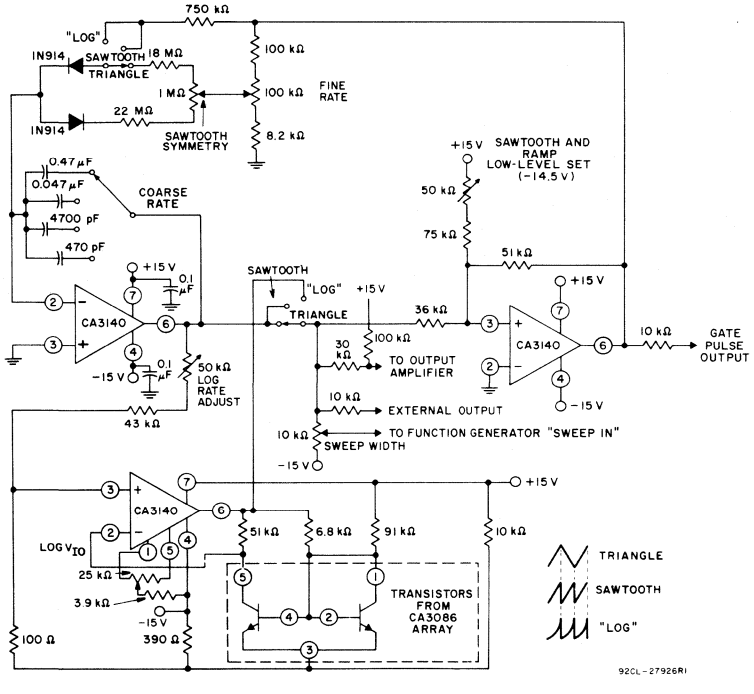


Fig. 24 — Sweeping generator.

CA3140A, CA3140

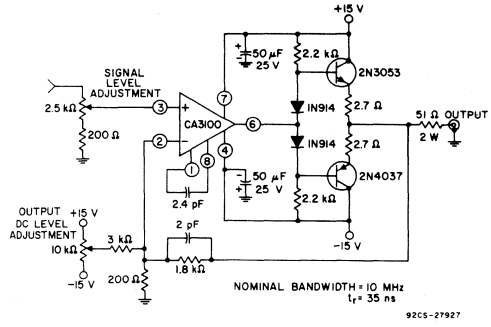


Fig. 25 – Wideband output amplifier.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts.

Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

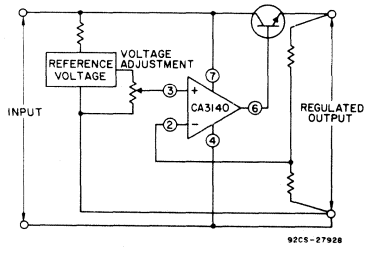


Fig. 26 – Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

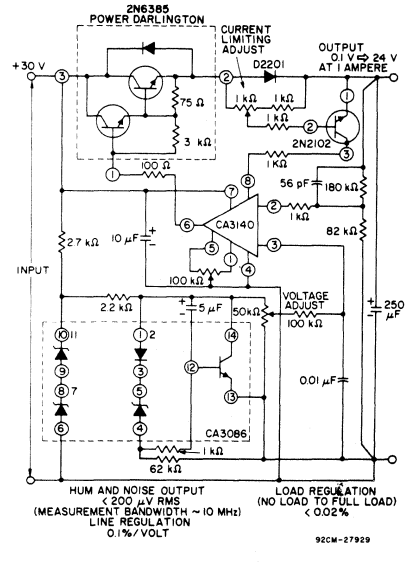


Fig. 27 – Regulated power supply.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

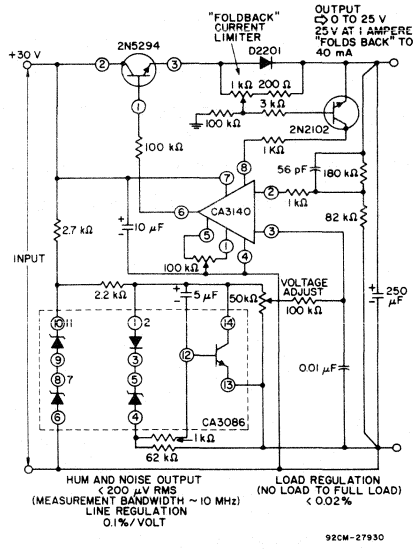
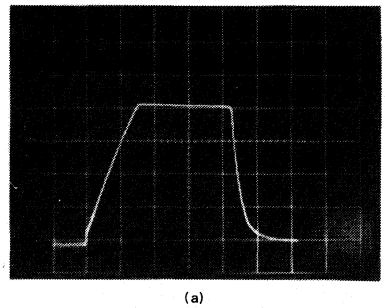
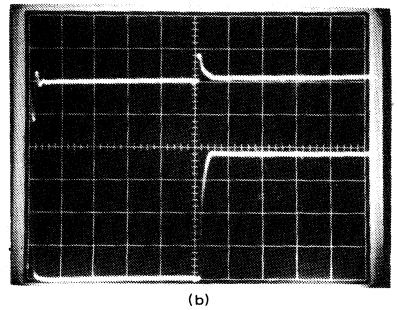


Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS / DIV AND ~1 s/DIV.)
92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE : OUTPUT VOLTAGE
(200 mV/DIV AND 5 μs/DIV)
BOTTOM TRACE : COLLECTOR OF LOAD SWITCHING TRANSISTOR, LOAD = 1 AMPERE
(5 VOLTS/DIV AND 5μs/DIV)
92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

CA3140A, CA3140

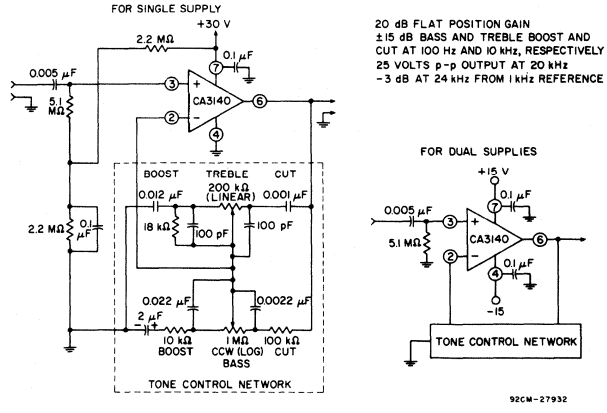


Fig. 30 — Tone control circuit using CA3130 series (20-dB midband gain).

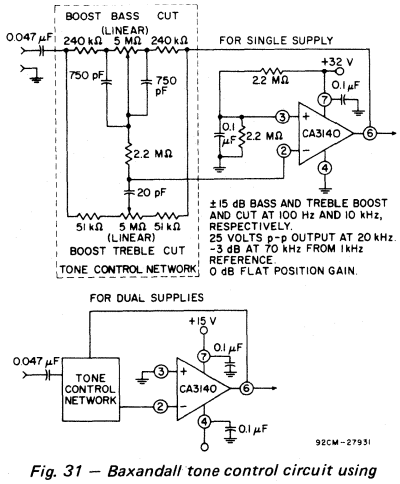


Fig. 31 — Baxandall tone control circuit using CA3140 series.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is −3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L, Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus per-

mitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

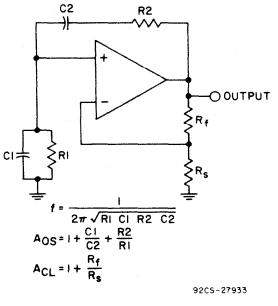


Fig. 32 – Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

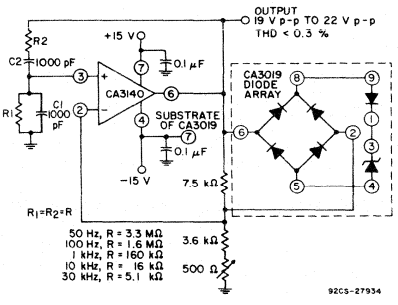


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

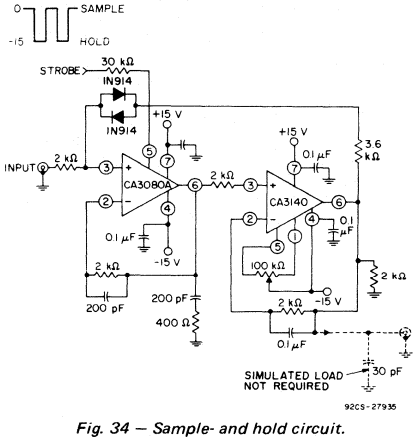


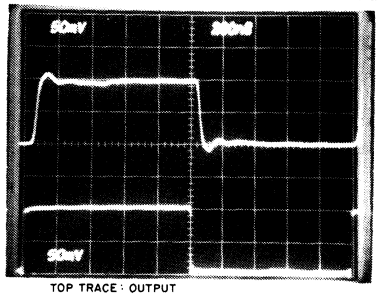
Fig. 34 – Sample- and hold circuit.

In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate

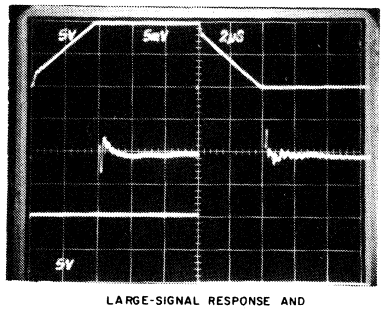
$$\frac{dv}{dt} = \frac{i}{c} = 0.5\ \text{mA}/200\ \text{pF} = 2.5\ \text{V}/\mu\text{s}.$$

* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

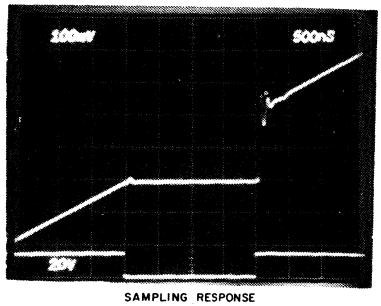
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 μV/μs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 μV/μs, but the slew rate would decrease to 0.25 V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5V/DIV. AND 2μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5mV/DIV. AND 2μs/DIV.) 92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample- and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.● In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

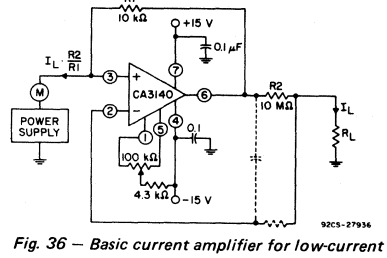


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

● "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".

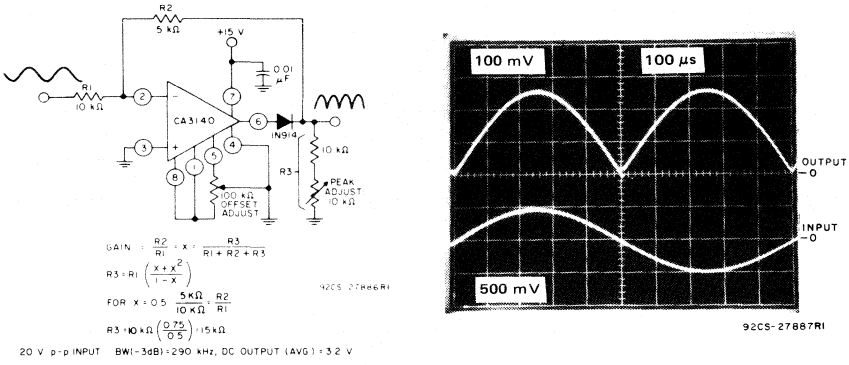
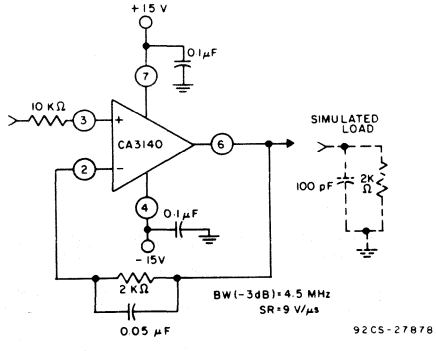
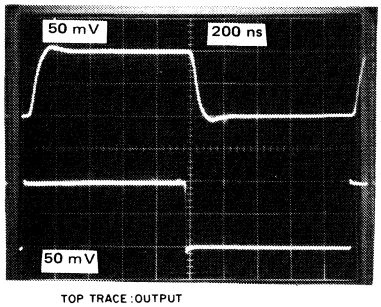
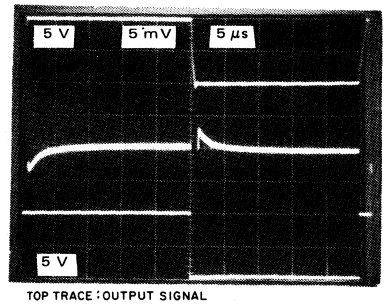


Fig. 37 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.





TOP TRACE : OUTPUT
(50 mV/DIV AND 200 ns/DIV)
BOTTOM TRACE : INPUT
(50 mV/DIV AND 200 ns/DIV)
(a) SMALL-SIGNAL RESPONSE
(50 mV/DIV. AND 200 ns/DIV)
92CS-27879



TOP TRACE : OUTPUT SIGNAL
(5 V/DIV. AND 5 μs/DIV.)
CENTER TRACE : DIFFERENCE SIGNAL
(5m V/DIV. AND 5 μs/DIV.)
BOTTOM TRACE : INPUT SIGNAL
(5V/DIV. AND 5 μs/DIV)
(b) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)
92CS-27880

Fig. 38 — Split-supply voltage-follower test circuit and associated waveforms.

CA3140A, CA3140

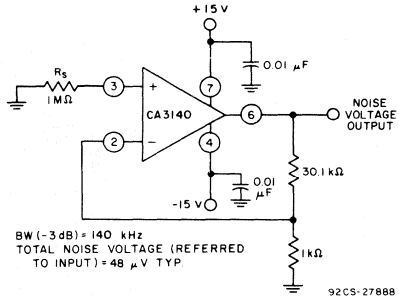
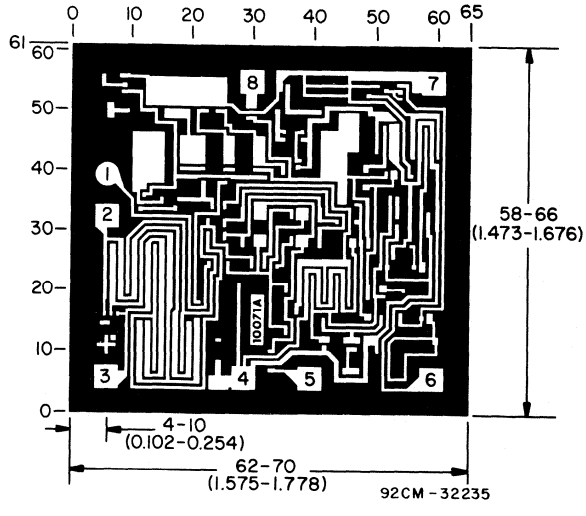


Fig. 39 – Test circuit amplifier (30-dB gain) used for wideband noise measurement.



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3160A, CA3160

BiMOS Operational Amplifiers

With MOSFET Input, CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15-V operation
  2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

The RCA-CA3160A and CA3160 are integrated-circuit operational amplifiers that combine the advantages of both CMOS and bipolar transistors on a monolithic chip. The CA3160 series circuits are frequency-compensated versions of the popular CA3130 series.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5 to 16 volts, or +2.5 to +8 volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3160 series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3160 is available in chip form (H suffix).

Applications:

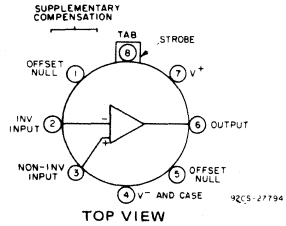
- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital CMOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers*
  (e.g., follower for single-supply D/A converter)
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

The CA3160A and CA3160 are also available in the 8-lead dual-in-line plastic package (Mini-DIP-E suffix). All types operate over the full military-temperature range of −55° C to +125° C. The CA3160A offers superior input characteristics over those of the CA3160.

CA3160A, CA3160

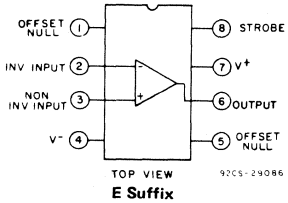
ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS						Units
	CA3160A (T, S, E)			CA3160 (T, S, E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	2	5	–	6	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL} V_O=10 V_{p-p}, R_L=2 kΩ	50 k	320 k	–	50 k	320 k	–	V/V
	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	80	95	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	150	–	32	320	μV/V
Maximum Output Voltage: At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	V
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	V
At R_L=∞ V_{OM}^-	–	0	0.01	–	0	0.01	V
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	mA
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	mA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	6	–	–	8	–	μV/°C



TOP VIEW

S and T Suffixes



E Suffix

CA3160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

Fig. 1 – Functional diagrams of the CA3160 Series.

CA3160A, CA3160

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS	CA3160/ CA3160A (T, S, E)	UNITS
	$V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified)		
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1	±22	mV
Input Resistance, R_I		1.5	TΩ
Input Capacitance, C_I	f = 1 MHz	4.3	pF
Equivalent Input Noise Voltage, e_n	BW= 0.2 MHz; R_S=1 MΩ	40	μV
	BW= 0.2 MHz; R_S=10MΩ	50	μV
Equivalent Input Noise Voltage, e_n	R_S= 100 Ω; 1 kHz	72	$nV\sqrt{Hz}$
	R_S= 100 Ω; 10 kHz	30	$nV\sqrt{Hz}$
Unity Gain Crossover Frequency, f_T		4	MHz
Slew Rate, SR:		10	V/μs
Transient Response: Rise Time, t_r	C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	μs
Overshoot		10	%
Settling Time (4 V_{p-p} Input to <0.1%)		1.8	μs

CHARACTERISTIC	TEST CONDITIONS	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
	$V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified)			
Input Offset Voltage, V_{IO}		2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	pA
Input Current, I_I		2	2	pA
Common-Mode Rejection Ratio, CMRR		90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 V_{p-p}	100 k	100 k	V/V
	R_L = 5 kΩ	100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, R_L = ∞	300	300	μA
	V_O = 2.5 V, R_L = ∞	500	500	μA
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	μV/V

CA3160A, CA3160

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C ..... 630 mW
ABOVE 55°C .... Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C ..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types).... −55 to +125°C
STORAGE (All Types) ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 MM) FROM CASE
FOR 10 SECONDS MAX. ..... +265°C

*Short circuit may be applied to ground or to either supply.

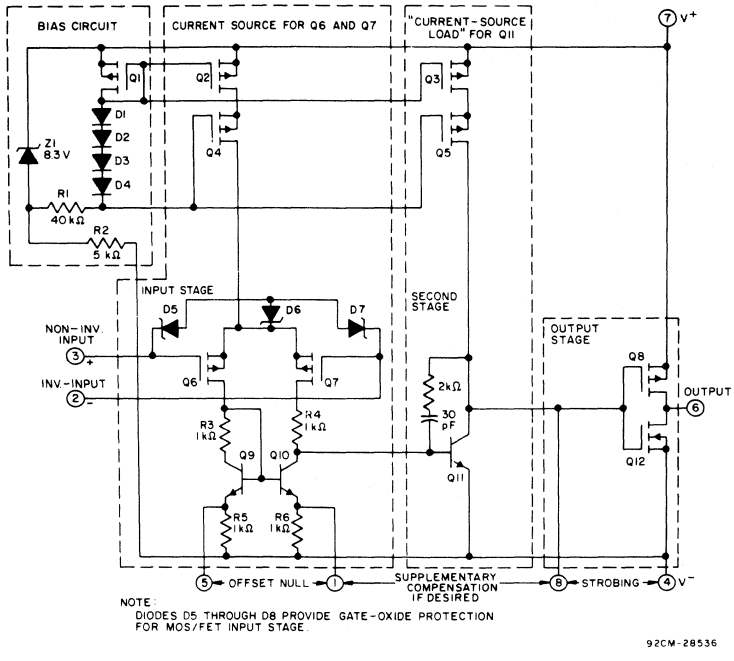


Fig.2 – Schematic diagram of the CA3160 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig.3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages — The circuit of the CA3160 is shown in Fig.2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

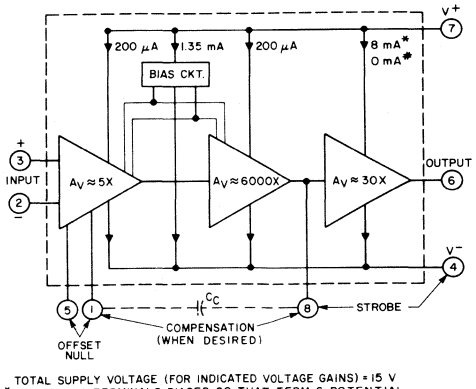
Second-Stage — Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit — At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage — The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig.6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

† For general information on the characteristics CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V
*WITH INPUT TERMINALS BIASED SO THAT TERM. 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
*WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.
92CS-28573

Fig. 3 — Block diagram of the CA3160 Series.

CA3160A, CA3160

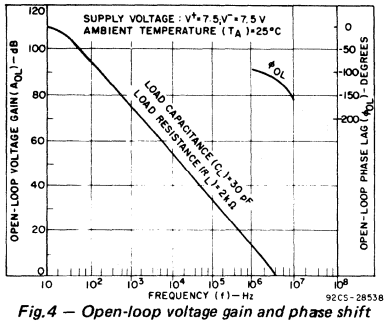


Fig.4 — Open-loop voltage gain and phase shift vs. frequency.

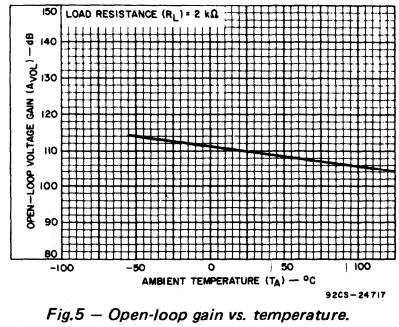


Fig.5 — Open-loop gain vs. temperature.

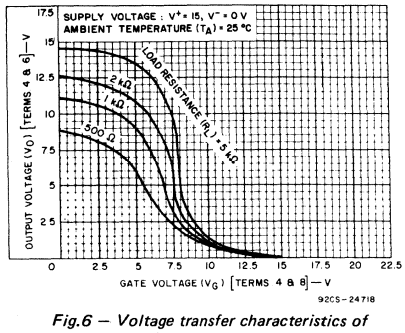


Fig.6 — Voltage transfer characteristics of COS/MOS output stage.

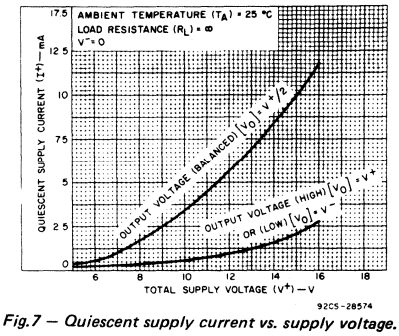


Fig.7 — Quiescent supply current vs. supply voltage.

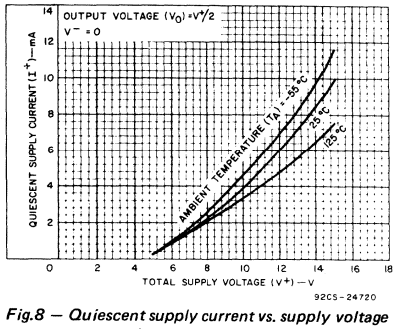


Fig.8 — Quiescent supply current vs. supply voltage at several temperatures.

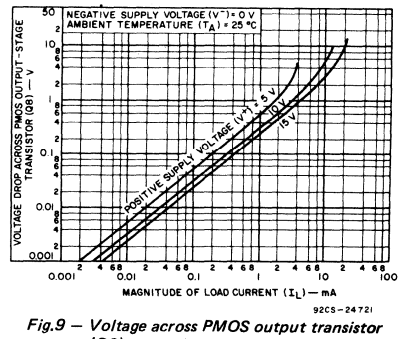


Fig.9 — Voltage across PMOS output transistor (Q8) vs. load current.

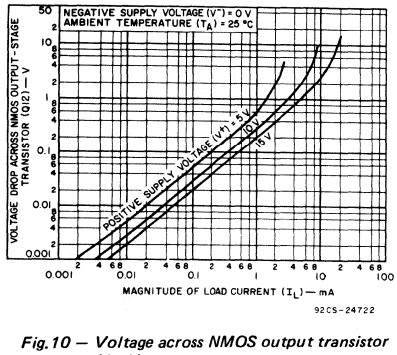


Fig.10 — Voltage across NMOS output transistor (Q12) vs. load current.

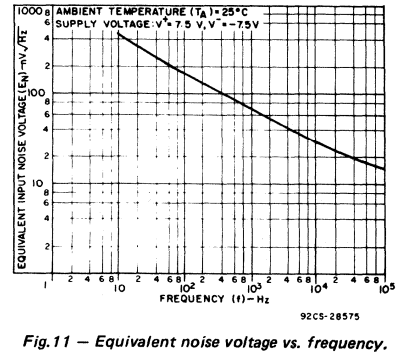


Fig.11 — Equivalent noise voltage vs. frequency.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5 pA at T_A=25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 12 contains

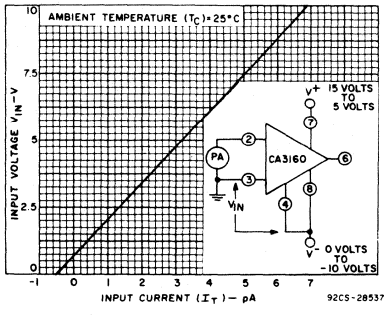


Fig. 12 – Input current vs. common-mode voltage.

data showing the variation of input current as a function of common-mode input voltage at T_A=25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 13 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

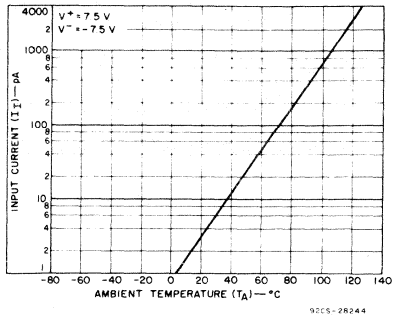


Fig. 13 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 14 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those en-

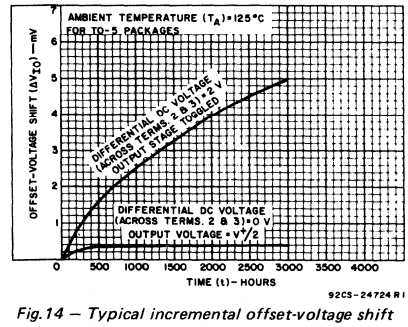


Fig. 14 – Typical incremental offset-voltage shift vs. operating life.

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countered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA3160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 15(a) and 15(b) show the CA3160 connected for both dual- and single-supply operation.

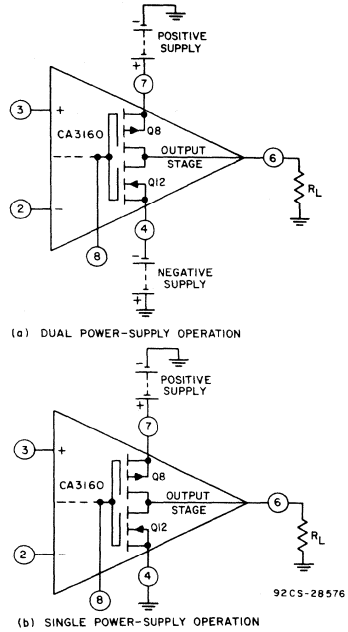


Fig. 15 – CA3160 output stage in dual and single power-supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 15(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40 μV when the test-circuit amplifier of Fig.16 is operated at a total supply voltage of 15 volts. This value of

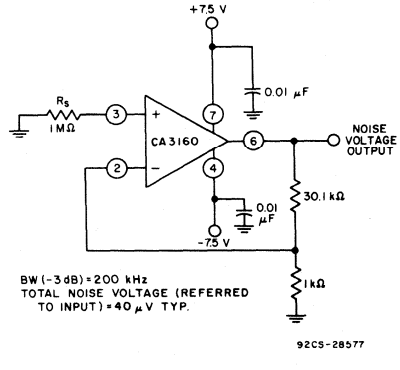
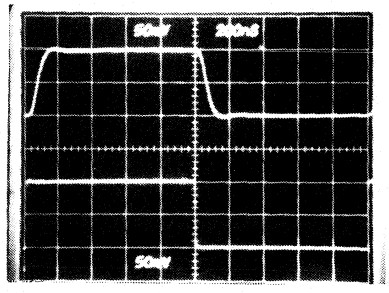
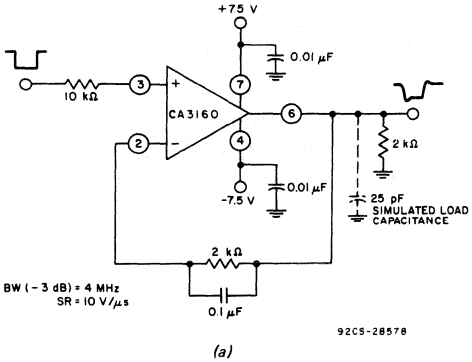


Fig. 16 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

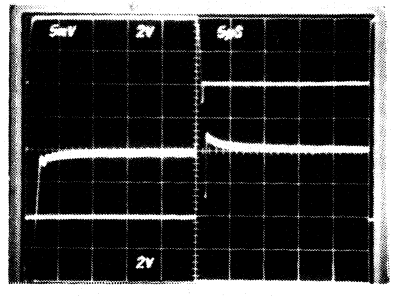
total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



(b) Small Signal Response
Top Trace: Output
Bottom Trace: Input



(a)



(c) Input-Output Difference Signal Showing Settling Time
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

Fig. 17 – Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig.17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig.18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig.18b with input-signal ramping. The waveforms in Fig.18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig.18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.19. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 19.

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* "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

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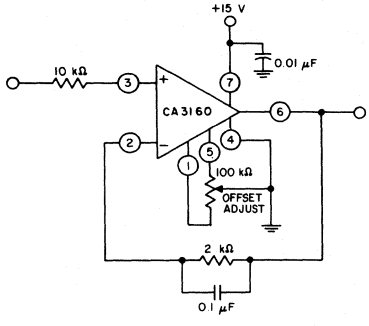
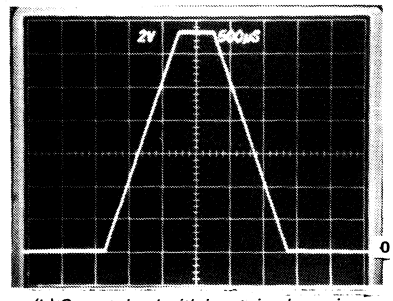
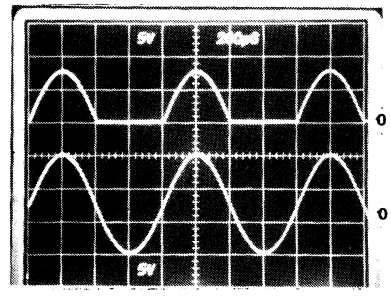


(a)



(b) Output signal with input-signal ramping.



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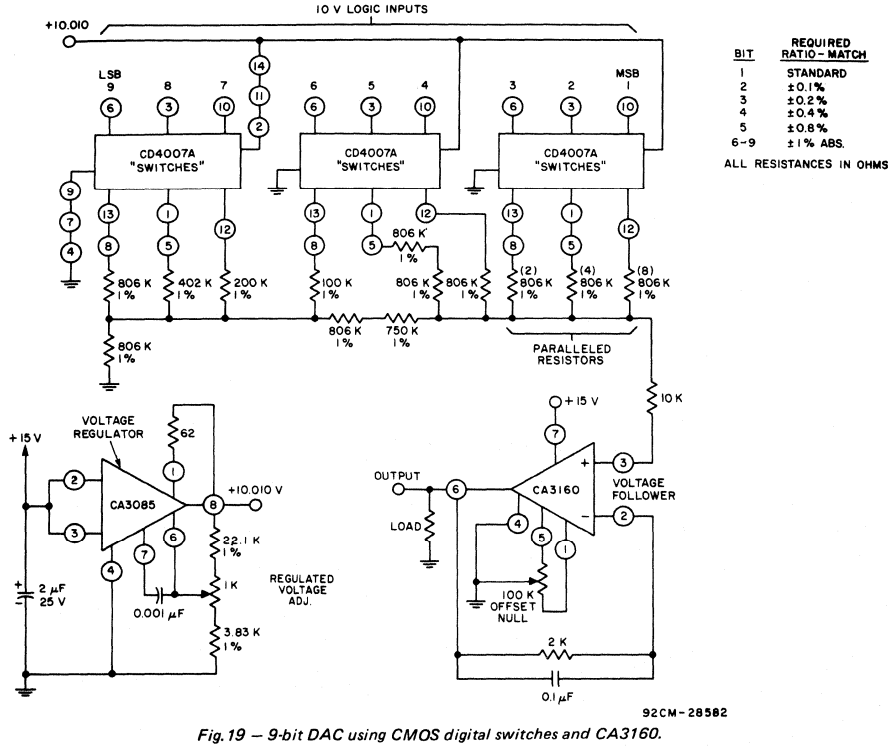
(c) Output-Waveform with Ground-Reference Sine-Wave Input
Top Trace: Output
Bottom Trace: Input

Fig. 18 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080.)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig. 19 – 9-bit DAC using CMOS digital switches and CA3160.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

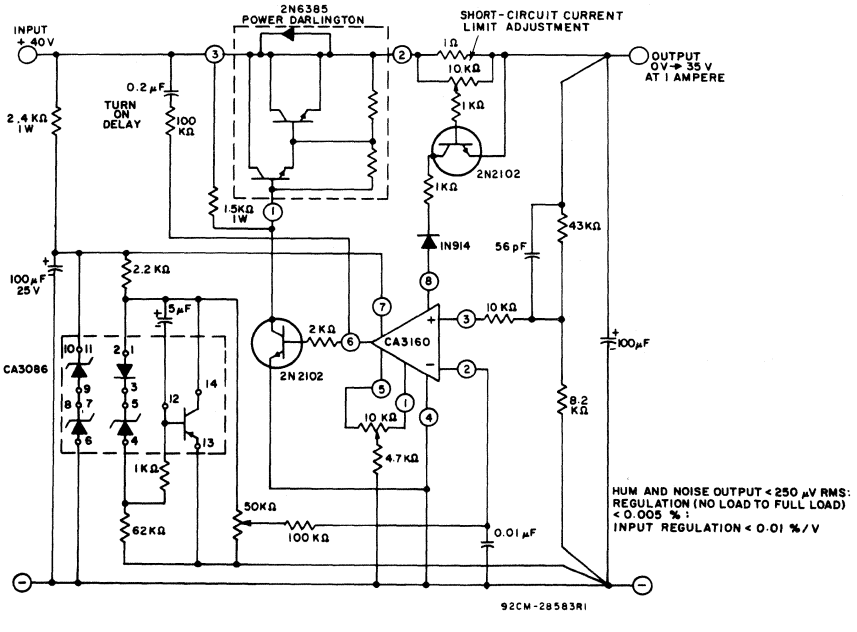


Fig.20 – Voltage regulator circuit (0.1 to 35 V at 1 A).

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Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

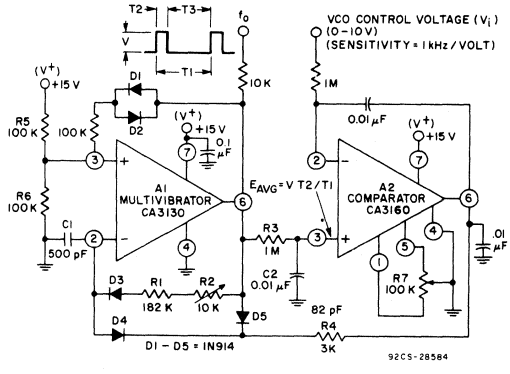


Fig.21 – Voltage-controlled oscillator.

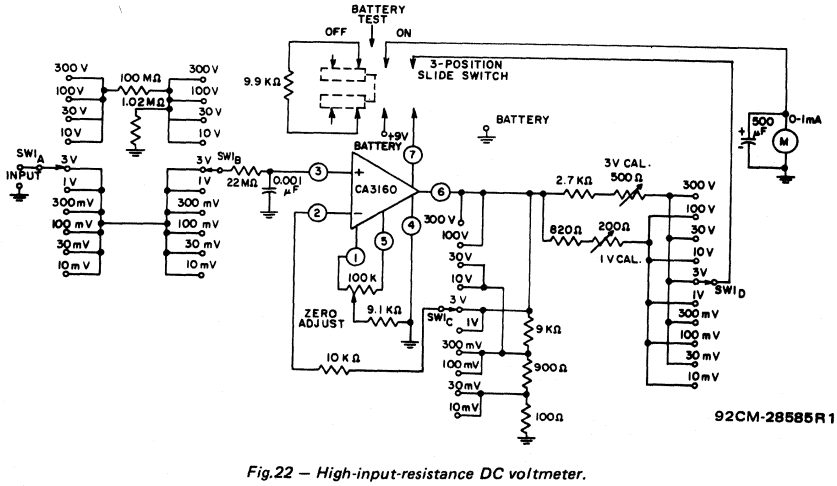


Fig.22 – High-input-resistance DC voltmeter.

Function Generator

A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

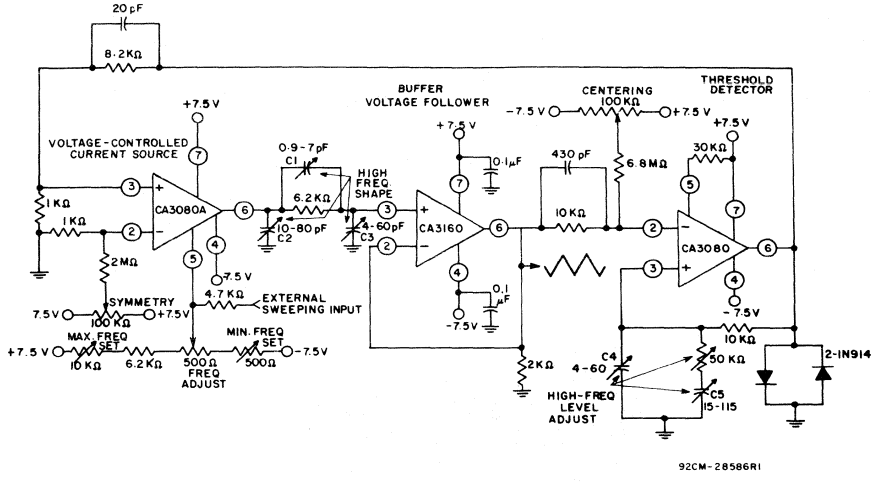
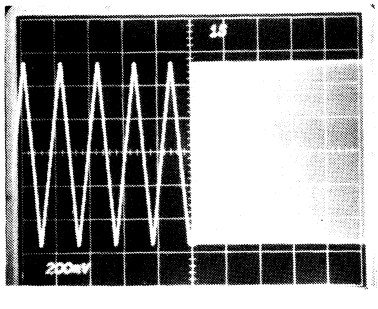
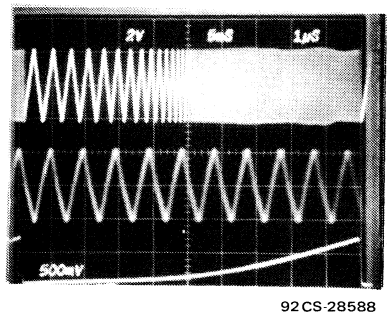


Fig.23(a) – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(b) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



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(c) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

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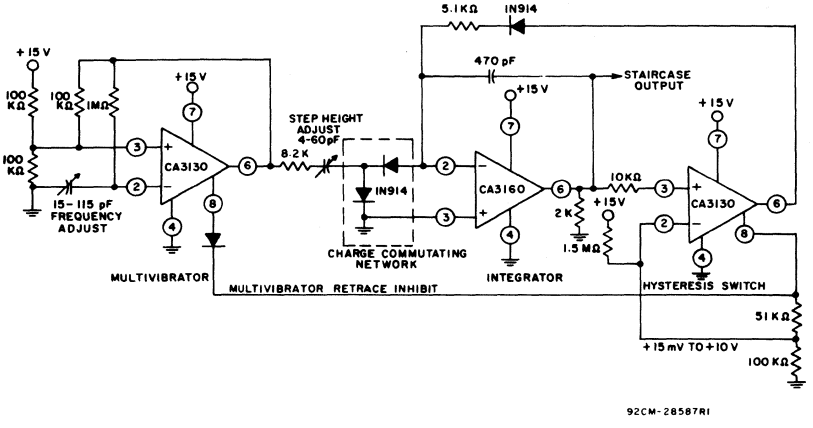
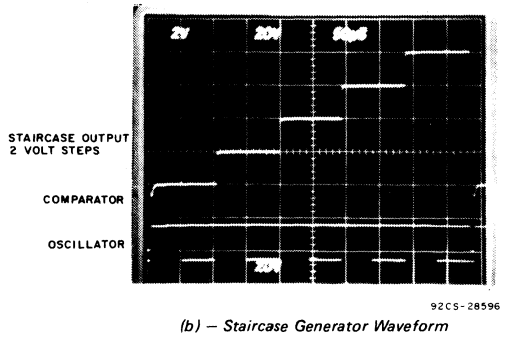
Staircase Generator

Fig. 24 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.





(b) – Staircase Generator Waveform
Top Trace: Staircase Output 2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 12.

To further enhance the stability of this circuit, the CA3160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

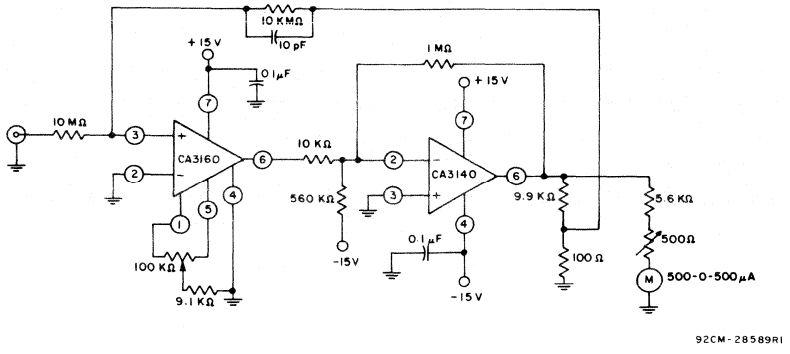


Fig.25 — Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

Single-Supply Sample-and-Hold System

Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

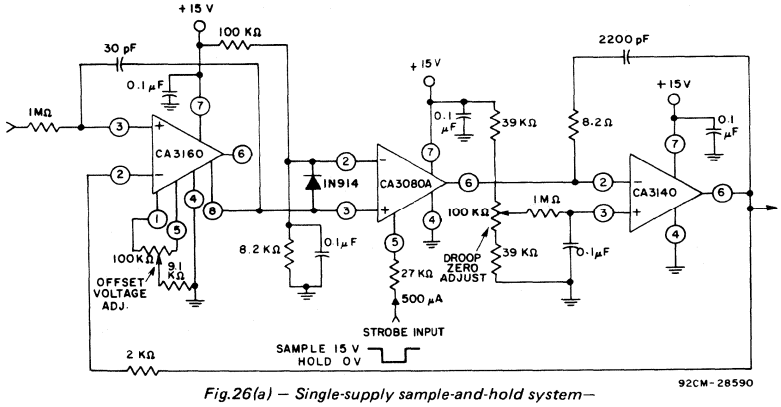
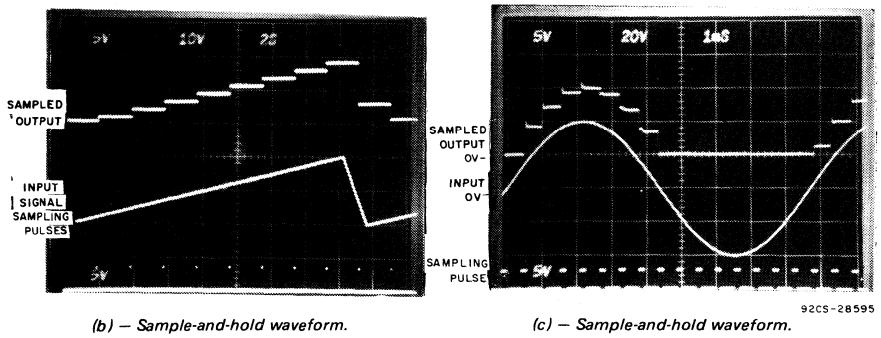


Fig.26(a) — Single-supply sample-and-hold system— input 0-to-10 volts.



(b) — Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses

(c) — Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulse

CA3160A, CA3160

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

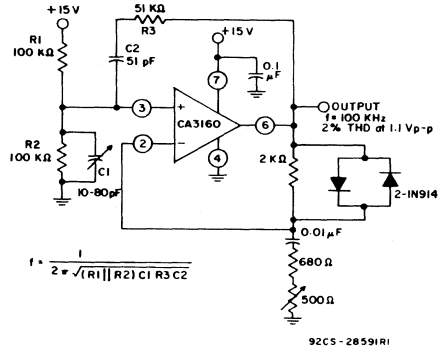


Fig.27 – Single-supply Wien Bridge oscillator.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 28, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Fig. 28 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (–3 dB) is 190 kHz.

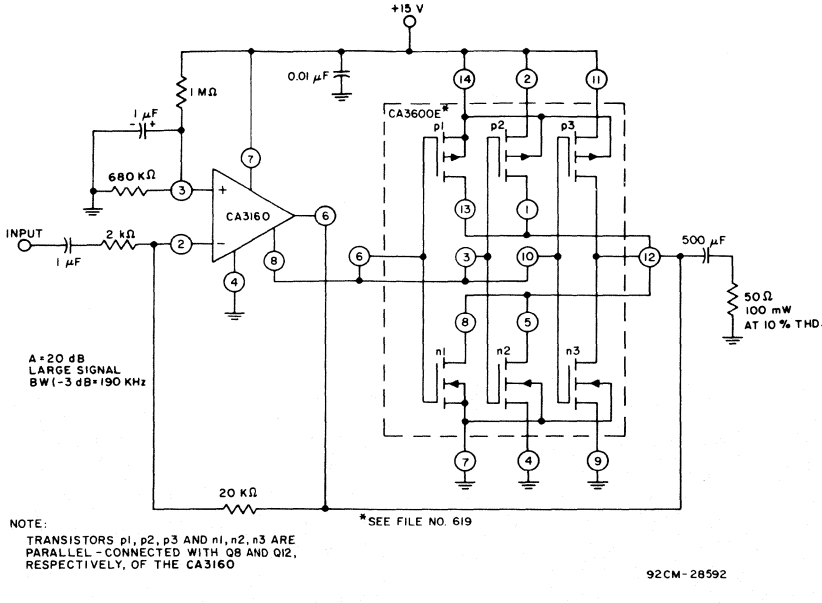
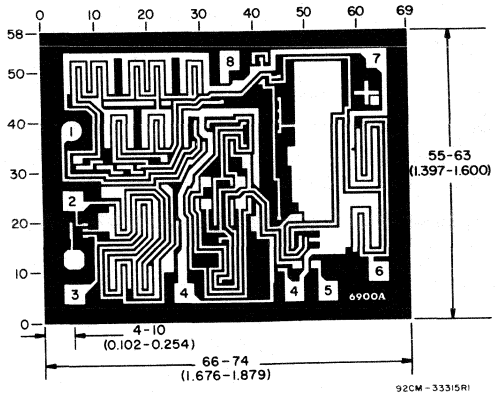


Fig.28 – CMOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.

CA3160A, CA3160



Dimensions and pad layout for CA3160H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photograph and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3193A, CA3193

BiMOS Precision Operational Amplifier

Features:

- *Low V_{IO}: 200 μV max. (CA3193A)*
  500 μV max. (CA3193A)
- *Low $\Delta V_{IO}/\Delta T$: 3 μV/° C max. (CA3193A)*
  5 μV/° C max. (CA3193)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 150 pA/° C max. (CA3193)*
- *Low $\Delta I_I/\Delta T$: 3.7 nA/° C max. (CA3193)*

The CA3193A and CA3193 are ultra-stable, precision-instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193A and CA3193 amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin-compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741-series types in most applications.

The CA3193A and CA3193 can also be used as functional replacements for op-amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage-versus-temperature coefficient the CA3193A and CA3193 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high-gain filters, buffers, strain-gauge bridge amplifiers and precision voltage references.

The three types in the CA3193 series are functionally identical. The CA3193 and CA3193A operate from supply voltages of ± 3.5 V to ± 18 V and have operating temperature ranges of -25° C to +85° C and 0° C to +70° C, respectively.

Applications:

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

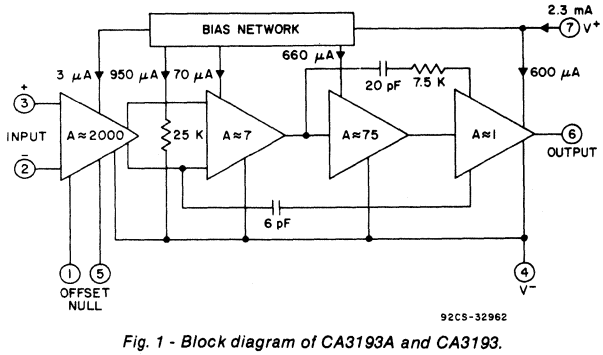


Fig. 1 - Block diagram of CA3193A and CA3193.

File Number **1249**

Absolute-Maximum Ratings, *Absolute-Maximum Values at T_A =25° C*

	CA3193	CA3193A
DC Supply Voltage	± 18	± 18
Differential-Mode Input Voltage	± 5	± 5
Common-Mode DC Input Voltage	(V^+ -4), V^-	(V^+ -4), V^-
Input Terminal Current	1	1
Device Dissipation		
Without Heat Sink		
Up to 55° C	630	630
Above 55° C	Derate Linearly 6.67	
Temperature Range	0 to 70	-25 to 85
Output Short-Circuit Duration*	Indefinite	Indefinite
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265

* Short circuit may be applied to ground or to either supply.

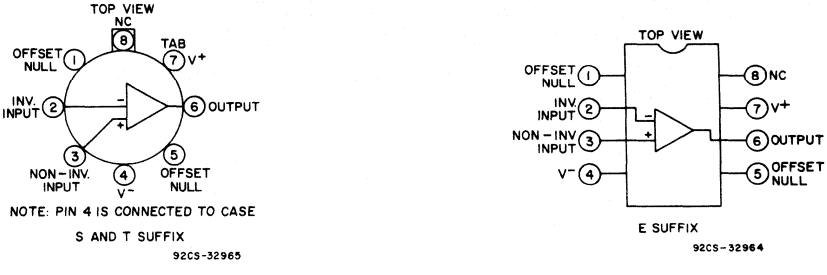


Fig. 2 - Functional diagram of CA3193A and CA3193.

The CA3193A and CA3193 types are supplied in standard 8-lead TO-5 style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN-S suffix) and 8-lead dual-in-line plastic (Mini-DIP-E suffix) packages.

Circuit Description

The block diagram of the CA3193 amplifier, Fig. 1 shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figs. 3 and 4, respectively.

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1, Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1, Q2) are provided by the cascode-connected p-n-p transistors Q3, Q5 and Q4, Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7, Q8 in Figs. 3 and 4) with appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9, Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17, Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15, Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{BE}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15, Q16).

Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5 kΩ resistor connected between the input and output nodes of the third stage.

CA3193A, CA3193

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, e_n p-p (0.1 to 10 Hz)	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n							
$f_O = 10$ Hz	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	—	—	24	—	nV/
$f_O = 10$ kHz	—	24	—	—	24	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	22	—	—	22	—	
Input Noise Current, i_n p-p (0.1 to 10 Hz)	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n							
$f_O = 10$ Hz	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	—	—	0.75	—	pA/
$f_O = 10$ kHz	—	0.72	—	—	0.72	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	110	115	—	100	110	—	dB
		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$	100	130	—	100	130	—	dB
		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)							
$R_L \geq 1$ KΩ	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ $f = 1$ kHz	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} =$ 20 mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−25	—	85	0	—	70	°C

CA3193A, CA3193

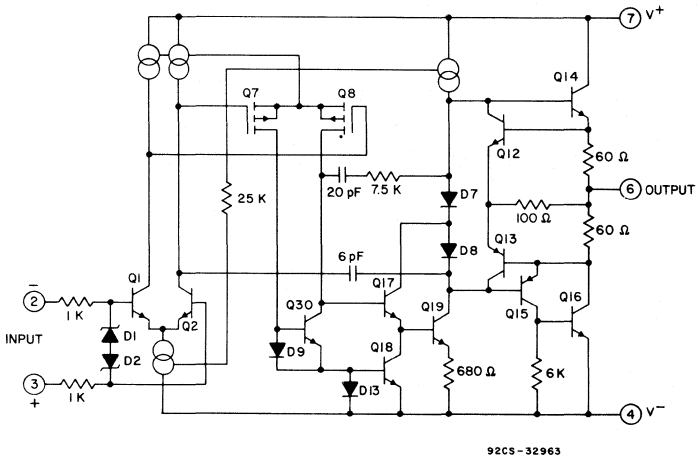


Fig. 3 - CA3193 simplified schematic diagram.

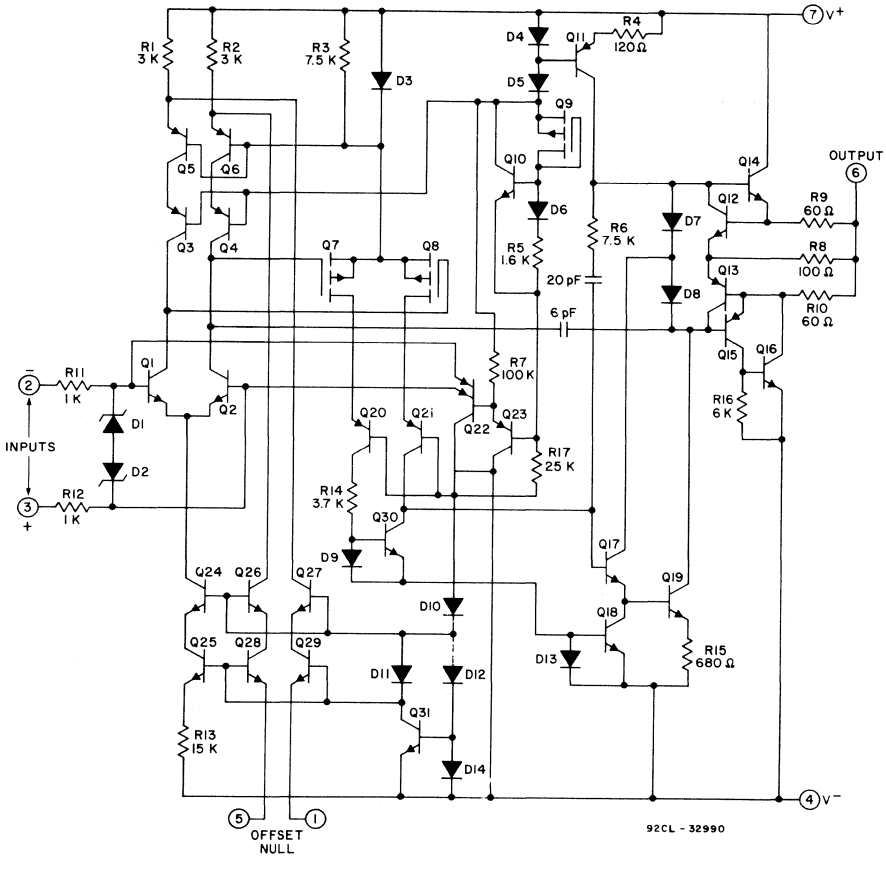


Fig. 4 - Schematic diagram of CA3193A and CA3193.

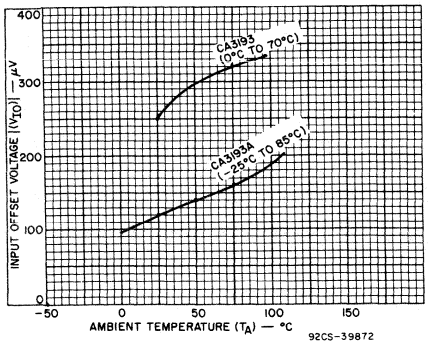


Fig. 5 - Typical input offset-voltage temperature characteristic for CA3193 series.

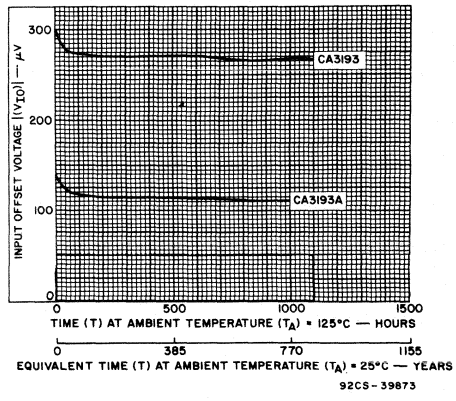


Fig. 6 - Input offset voltage vs. time.

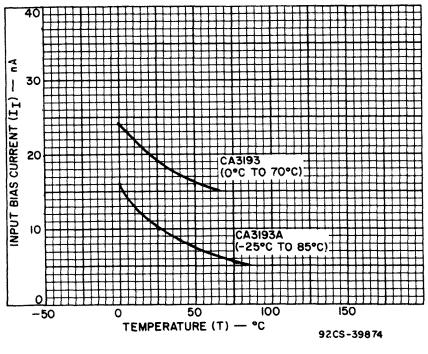


Fig. 7 - Typical input bias current vs. temperature.

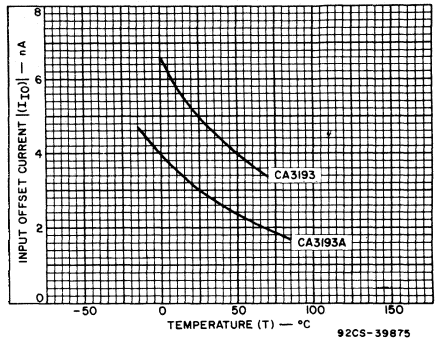


Fig. 8 - Typical input offset current vs. temperature.

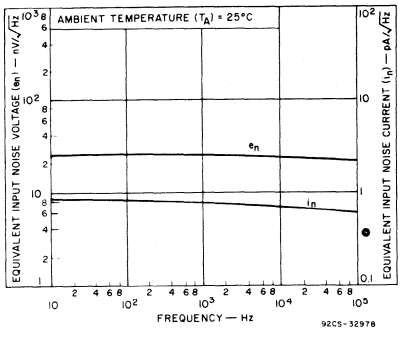


Fig. 9 - Input noise voltage and current density vs. frequency.

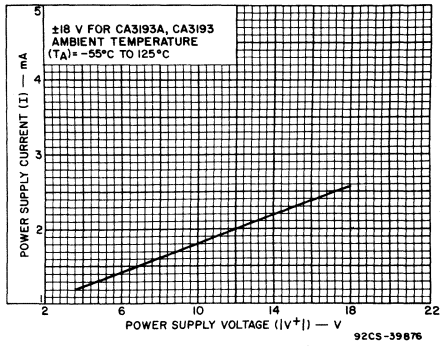


Fig. 10 - Power supply voltage (V^+, V^-) vs. supply current.

CA3193A, CA3193

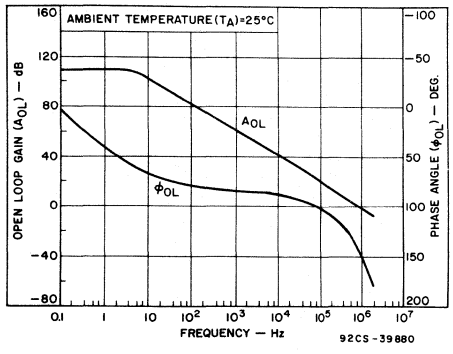


Fig. 11 - Open-loop gain and phase-shift response for CA3193B.

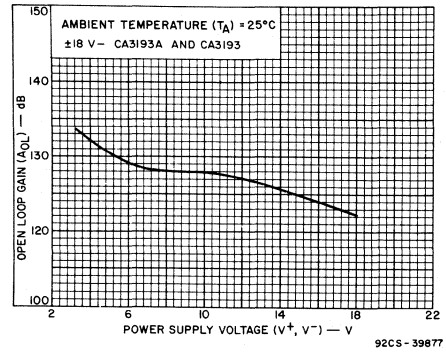


Fig. 12 - Open-loop gain vs. power-supply voltage.

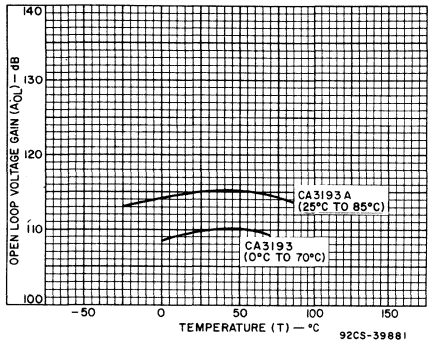


Fig. 13 - Open-loop gain vs. temperature for CA3193 series.

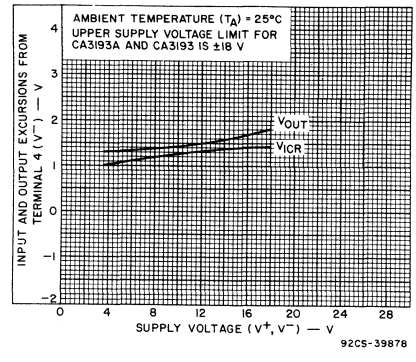


Fig. 14 - Maximum undistorted output voltage vs. frequency.

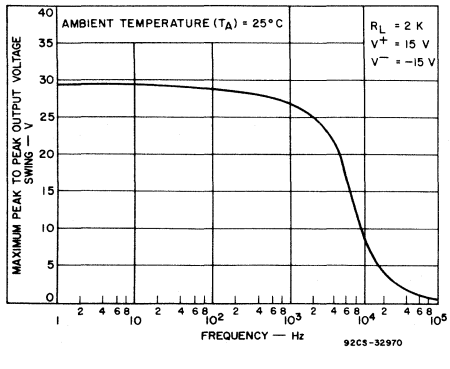
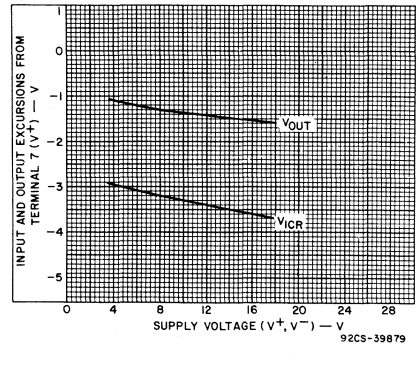


Fig. 15 - Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

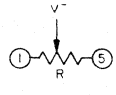
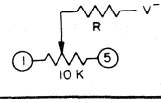
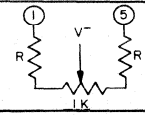


Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to V^-, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3193 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V^+ supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3193A CA3193	10K 10K	50K 20K	10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

TEST CIRCUITS

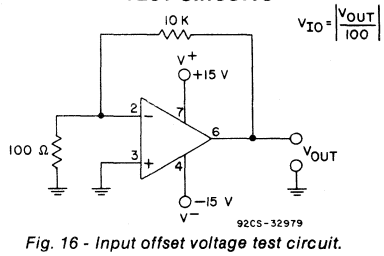
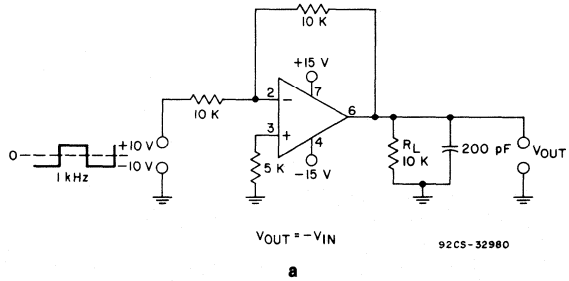
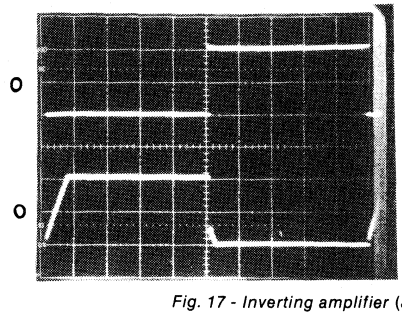


Fig. 16 - Input offset voltage test circuit.



a



TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT. : $\frac{10\,V}{DIV}$

HOR. : $\frac{.1\,ms}{DIV}$

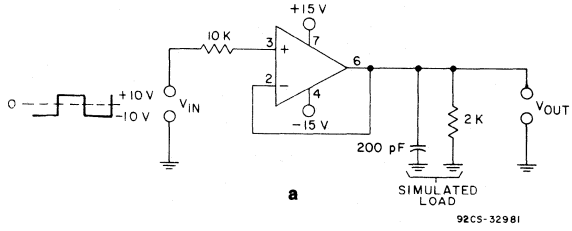
$V^+ = 15\,V$
$V^- = -15\,V$
$R_L = 10\,K$

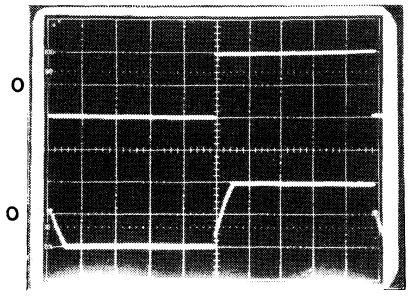
92CS-32989

b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.

CA3193A, CA3193





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\ V}{DIV}$

HOR : $\frac{.1\ ms}{DIV}$

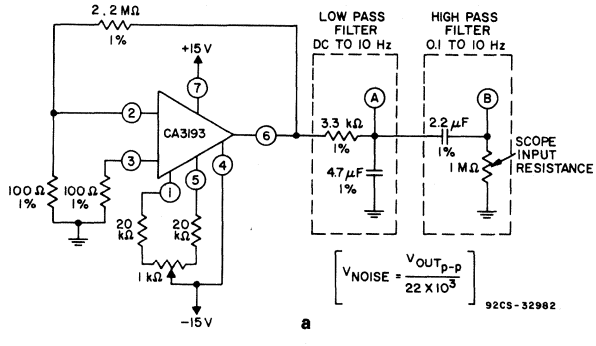
$V+ = 15\ V$

$V^- = 15\ V$

$R_L = 2K$

92CS-32988

Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.



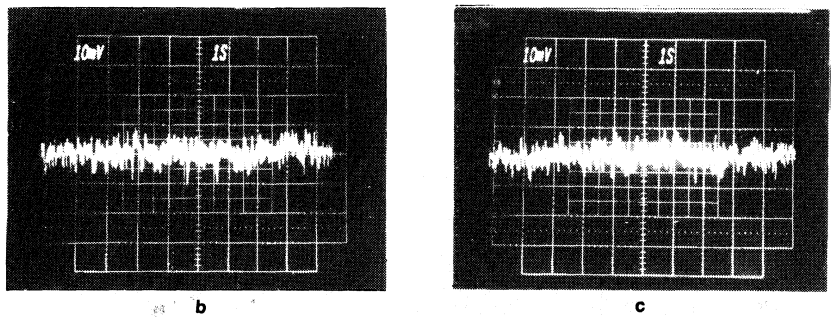
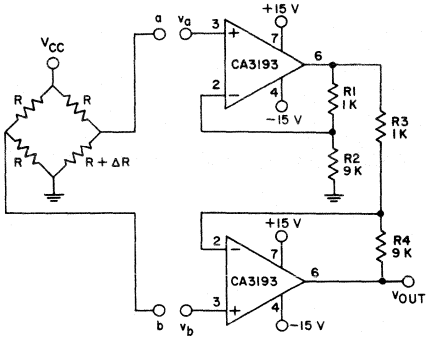


Fig. 19 - Low frequency noise (a) test circuit - 0.1 to 10 Hz (b) output A waveform - 0 to 10 Hz noise (c) output B waveform - 0 to 10 Hz noise.

APPLICATION CIRCUITS



$$V_{OUT} = -V_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + V_b\left(\frac{R4}{R3}+1\right)$$

FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

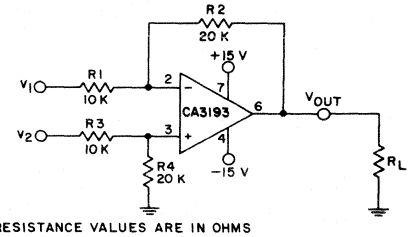
$$V_{OUT} = V_b - V_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (V_b - V_a)(10)$

92CS-32984

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = V_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - V_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

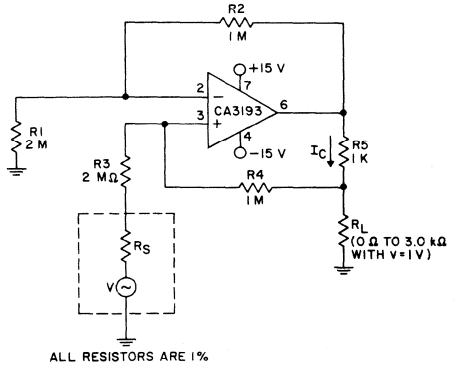
FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R
WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN V_{OCM} = 0.0005 V_{IN} OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

92CS-32983R1

Fig. 21 - Differential amplifier (simple subtractor) using CA3193.



ALL RESISTORS ARE 1%

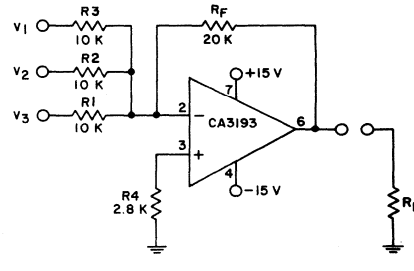
IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L
FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH v = 1 V

$$I_L = \frac{V}{R3\,R5} = \frac{V}{(2\,M)(1K)} = \frac{V}{2\,K} = 500\,\mu A$$

92CS-32985

Fig. 22 - Using CA3193 as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}V_1 + \frac{R_F}{R2}V_2 + \frac{R_F}{R3}V_3\right)$$

$$V_{OUT} = -(2V_1 + 2V_2 + 2V_3)$$

92CS-32973R1

ALL RESISTANCE VALUES ARE IN OHMS

Fig. 23 - Typical summing amplifier application.

CA3193A, CA3193

The CA3193 is an excellent choice for use with thermocouples. In Fig. 24, the CA3193 amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

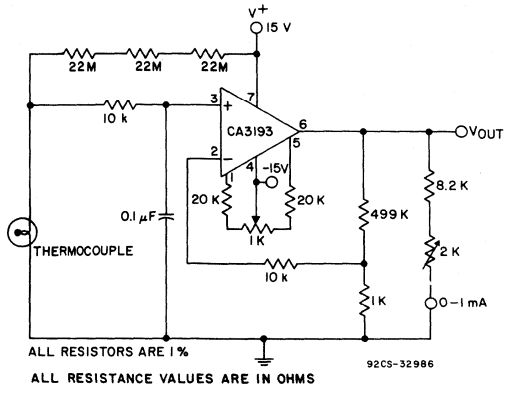


Fig. 24 - The CA3193 used in a thermocouple circuit.

CA3240A, CA3240

Dual BiMOS Operational Amplifiers

With MOSFET Input, Bipolar Output

Features:
- *Dual version of CA3140*
- *Internally compensated*
- *MOSFET input stage*
  - *(a) Very high input impedance (Z_{IN}) - 1.5 TΩ typ.*
  - *(b) Very low input current (I_I) - 10 pA typ. at ±15 V*
  - *(c) Wide common-mode input-voltage range (V_{ICR}) - can be swung 0.5 volt below negative supply-voltage rail*
- *Directly replaces industry types 747 and 1458 in most applications*

The RCA-CA3240A and CA3240 are dual versions of the popular CA3140-series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating-temperature range of −40 to +85° C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix). The CA3240 is also available in chip form (H suffix).

Applications:
- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds - minutes - hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Intrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

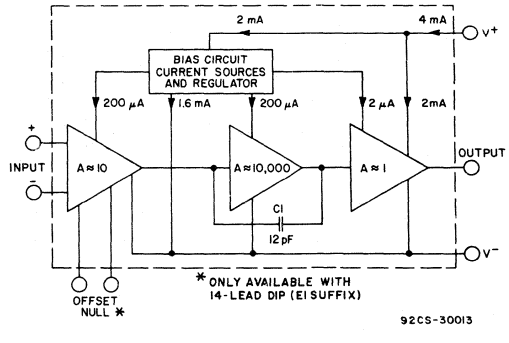


Fig. 1 — Block diagram of one-half CA3240 series.

File Number **1050**

CA3240A, CA3240

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	4 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	−40 to +85°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION●	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ±1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

● Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

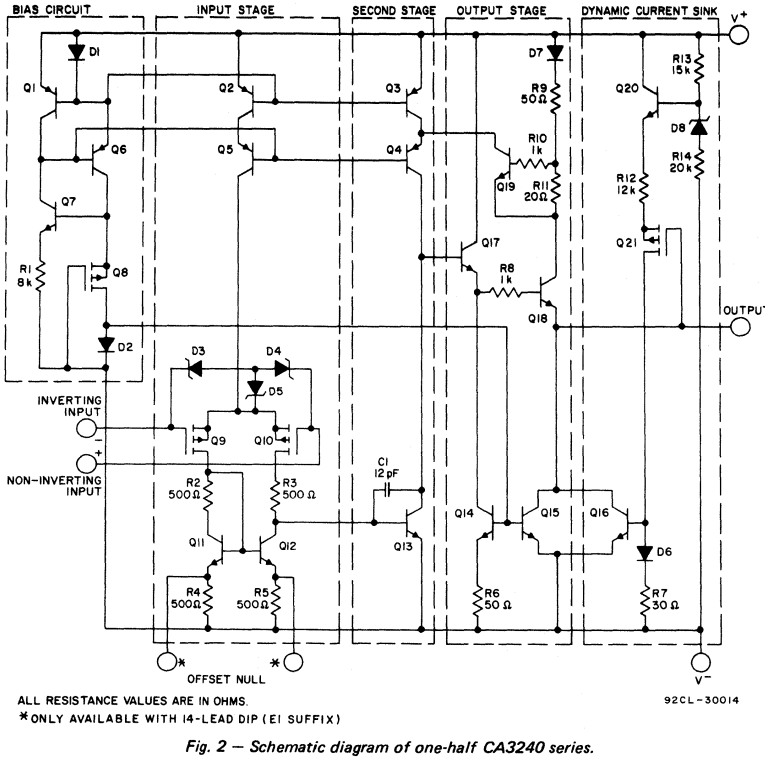


Fig. 2 — Schematic diagram of one-half CA3240 series.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and V^+.* The dynamic current sink becomes active whenever the output terminal is more negative than V^+ by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V^-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V (V_{CE}(sat)) of V^- with a 2-kΩ load to ground. *When the load is returned to V^+, it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (approx. 2 kΩ) between the output and V^-.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	LIMITS						UNITS
	CA3240A			CA3240			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}●	20 k	100 k	–	20 k	100 k	–	V/V
(See Figs. 4, 19)	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR	–	32	320	–	32	320	μV/V
(See Fig. 9)	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig. 16)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$ PSRR	–	100	150	–	100	150	μV/V
(See Fig. 11)	76	80	–	76	80	–	dB
Maximum Output Voltage,■ V_{OM}^+	+12	13	–	+12	13	–	V
(See Figs. 22, 16) V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Maximum Output Voltage,† V_{OM}^-	0.4	0.13	–	0.4	0.13	–	V
Supply Current, (See Fig. 7) For Both Amps. I^+	–	8	12	–	8	12	mA
Total Device Dissipation, P_D	–	240	360	–	240	360	mW

● At V_O = 26 V_{p-p}, +12 V, −14 V and R_L = 2 kΩ.

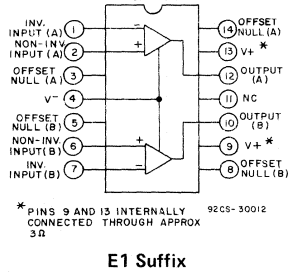
■ At R_L = 2 kΩ.

† At V^+ = 5 V, V^- = GND, I_{Sink} = 200 μA.

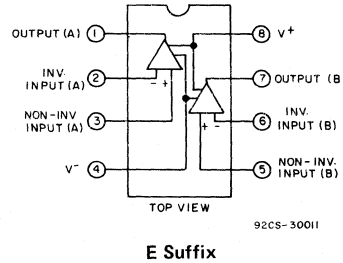
CA3240A, CA3240

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25°C$	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz, R_S = 1 MΩ	48	48	μV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz, R_S= 100 Ω	40	40	$nV/\sqrt{Hz}$
		f=10 kHz, R_S= 100 Ω	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply Source	I_{OM}^+		40	40	mA
Sink	I_{OM}^-		11	11	mA
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T		4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR		9	9	V/μs
Transient Response: Rise Time	t_r	R_L=2 kΩ, C_L=100 pF	0.08	0.08	μs
Overshoot (See Fig. 20)	t_r	R_L=2 kΩ, C_L=100 pF	10	10	%
Settling Time at 10 V_{p-p}, (See Fig. 17)	1 mV, t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower	4.5	4.5	μs
	10 mV, t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower	1.4	1.4	μs
Crosstalk		f = 1 kHz	120	120	dB



E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 3 – Functional diagrams.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At $V^+ = 15$ V, $V^- = 15$ V, $T_A = -40$ to $+85^oC$ Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\|V_{IO}\|$	3	10	mV
Input Offset Current,♦	$\|I_{IO}\|$	32	32	pA
Input Current,♦	I_I	640	640	pA
Large-Signal Voltage Gain,	A_{OL}●	63 k	63 k	V/V
(See Figs. 4, 19)		96	96	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
(See Fig. 9)		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 16)	V_{ICR}	−15 to +12.3	−15 to +12.3	V
Power-Supply Rejection Ratio,	$\frac{\Delta V_{IO}/\Delta V}{PSRR}$	150	150	μV/V
(See Fig. 11)		76	76	dB
Maximum Output Voltage,■	V_{OM}^+	12.4	12.4	V
(See Figs. 16, 22)	V_{OM}^-	−14.2	−14.2	
Supply Current, (See Fig. 7) For Both Amps.	I^+	8.4	8.4	mA
Total Device Dissipation,	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage,	$\Delta V_{IO}/\Delta T$	15	15	μV/°C

● At $V_O = 26\ V_{p\text{-}p}$, +12 V, −14 V and $R_L = 2\ k\Omega$.
■ At $R_L = 2\ k\Omega$.
♦ At $T_A = 85^oC$

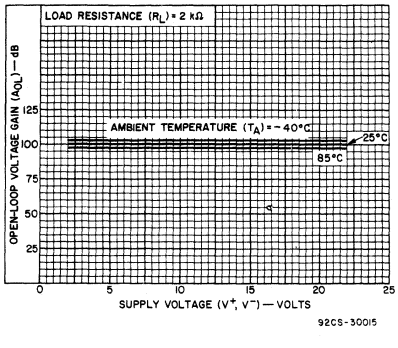


Fig. 4 — Open-loop voltage gain as a function of supply voltage and temperature.

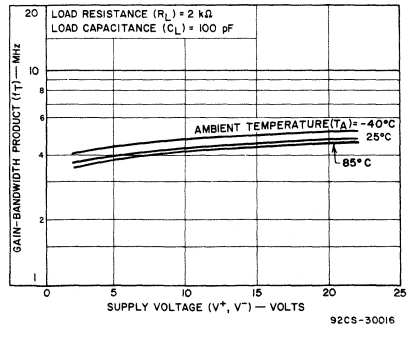


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

CA3240A, CA3240

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\|V_{IO}\|$	2	5	mV
Input Offset Current,	$\|I_{IO}\|$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	−0.5	−0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio,	PSRR	31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage,	V_{OM}^+	3	3	V
(See Figs. 16,22)	V_{OM}^-	0.3	0.3	
Maximum Output Current: Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW

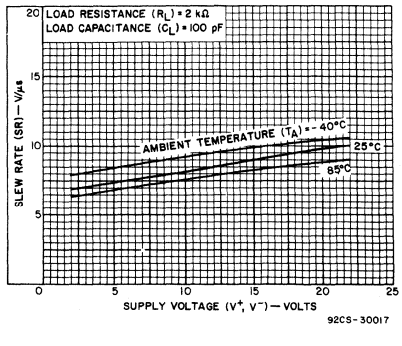


Fig. 6 — Slew rate as a function of supply voltage and temperature.

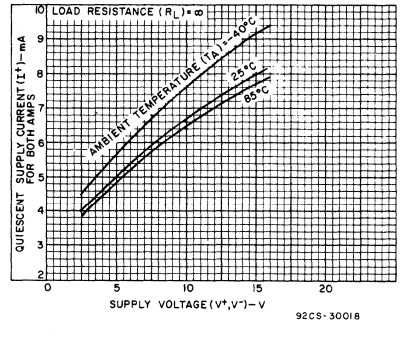


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

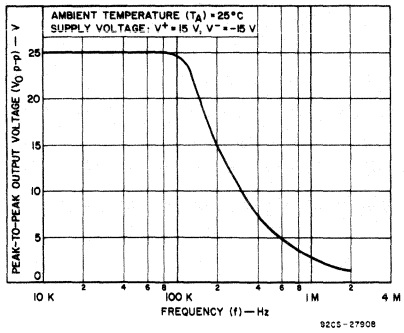


Fig. 8 — Maximum output voltage swing as a function of frequency.

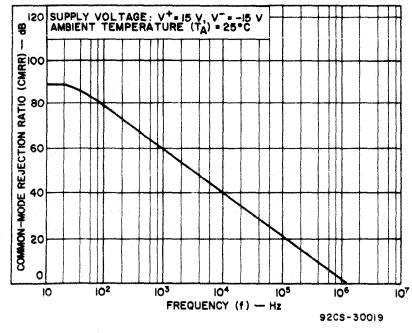


Fig. 9 — Common-mode rejection ratio as a function of frequency.

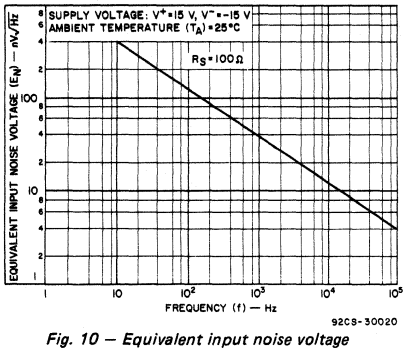


Fig. 10 — Equivalent input noise voltage as a function of frequency.

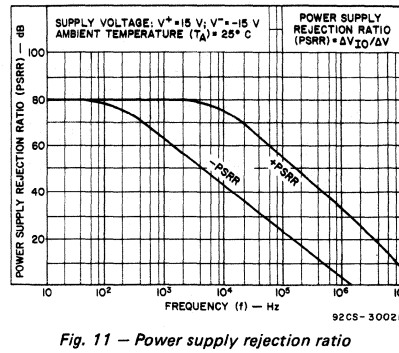


Fig. 11 — Power supply rejection ratio as a function of frequency.

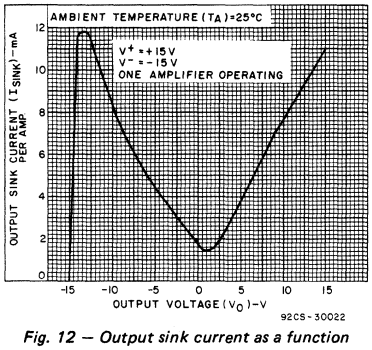


Fig. 12 — Output sink current as a function of output voltage.

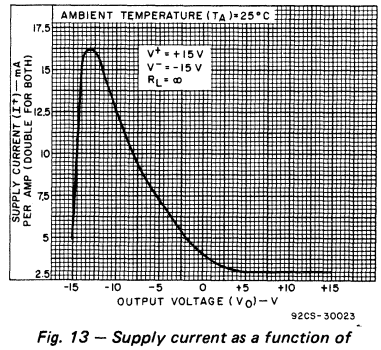


Fig. 13 — Supply current as a function of output voltage.

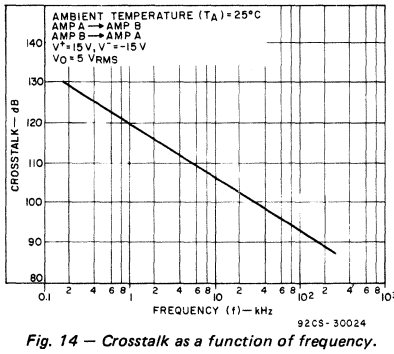


Fig. 14 — Crosstalk as a function of frequency.

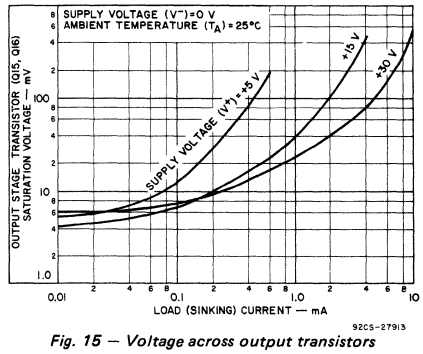


Fig. 15 — Voltage across output transistors Q15 and Q16 as a function of load current.

CA3240A, CA3240

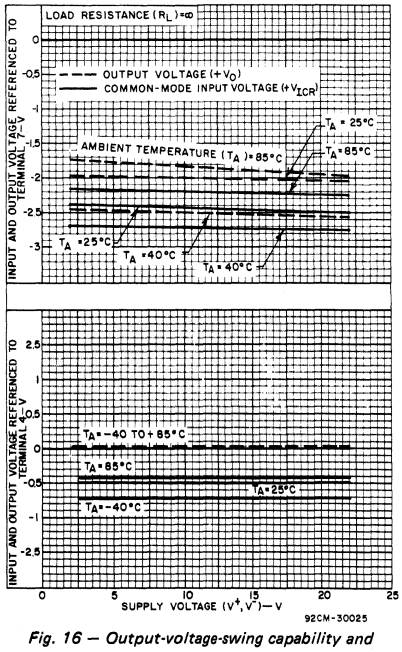


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

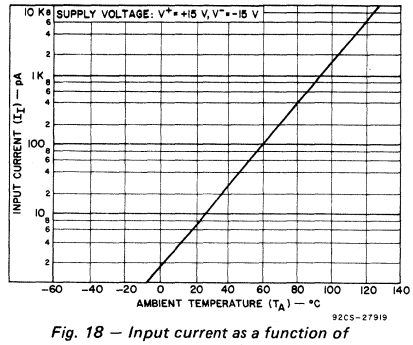


Fig. 18 — Input current as a function of ambient temperature.

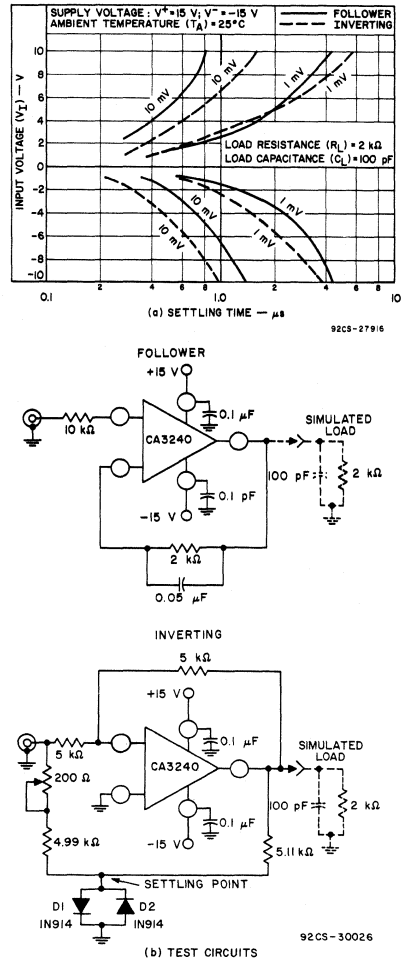


Fig. 17 — Input voltage as a function of settling time.

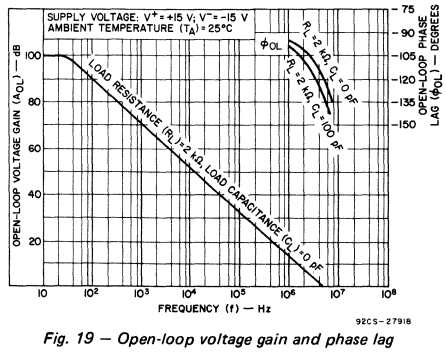
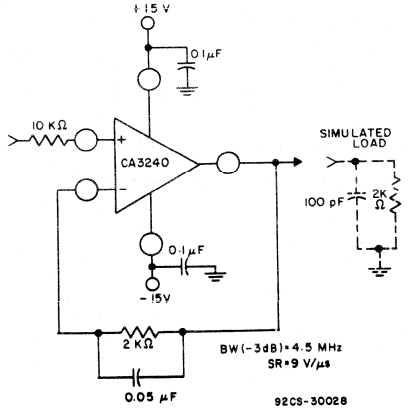


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.



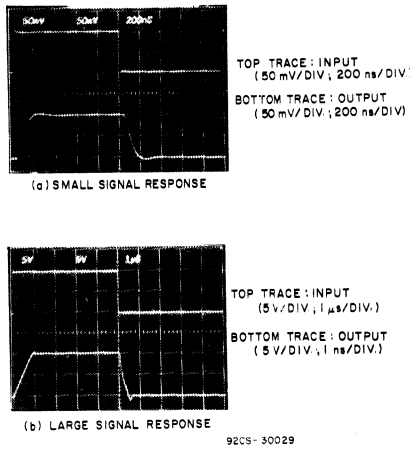


Fig. 20 — Split-supply voltage-follower test circuit and associated waveforms.

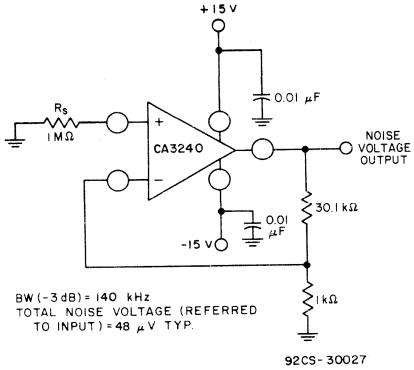


Fig. 21 — Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

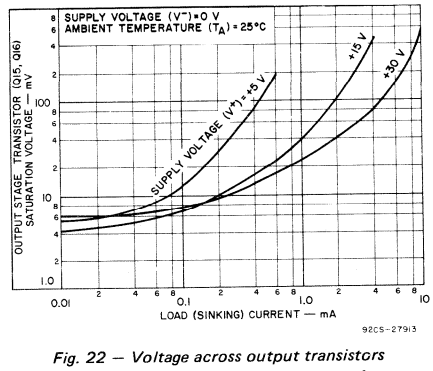


Fig. 22 — Voltage across output transistors Q15 and Q16 as a function of load current.

CA3240A, CA3240

APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

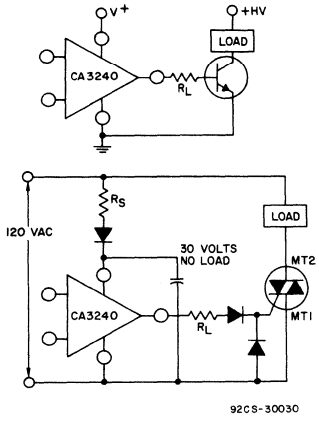


Fig. 23 — Methods of utilizing the V_{CE}(sat) sinking-current capability of the CA3240 series.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

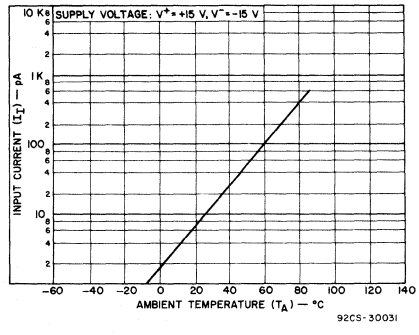


Fig. 24 — Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

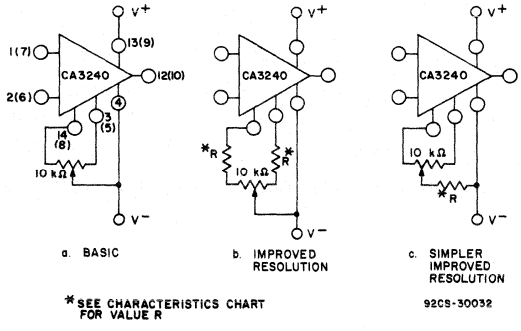


Fig. 25 – Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

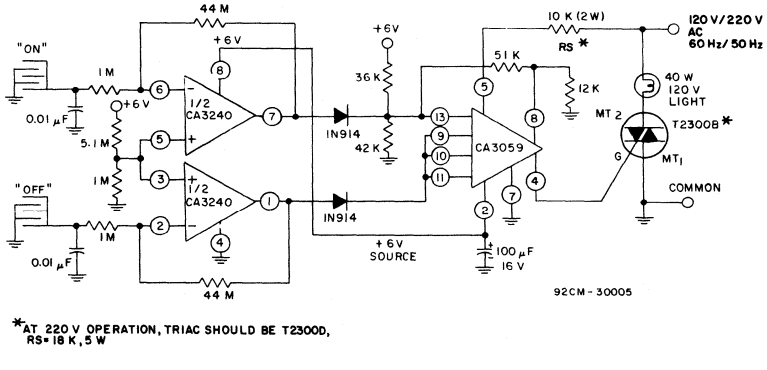


Fig. 26 – On/off touch switch.

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5 V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

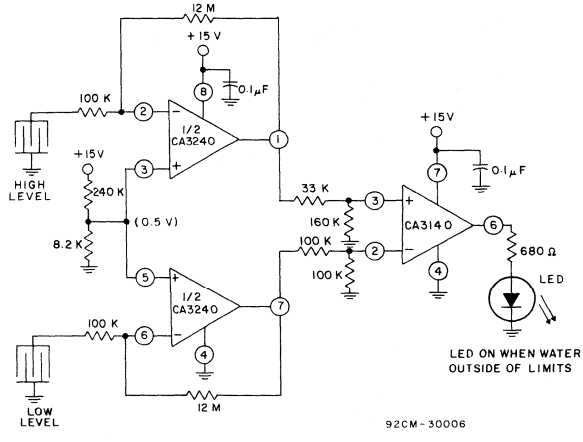


Fig. 27 – Dual level detector.

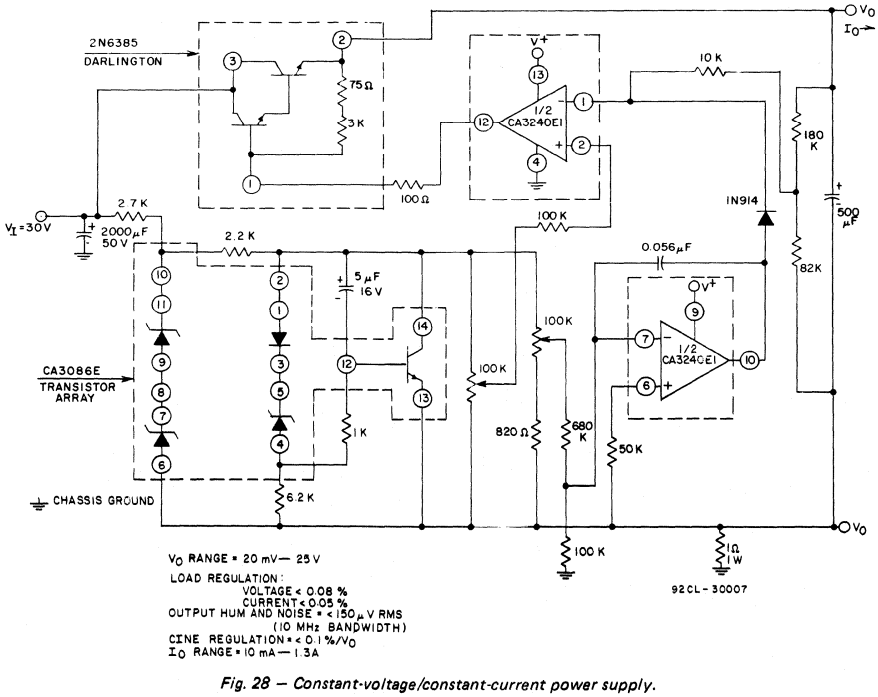


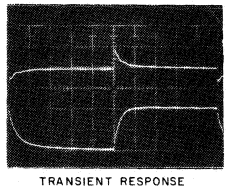
Fig. 28 – Constant-voltage/constant-current power supply.

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.

Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.



TRANSIENT RESPONSE

TOP TRACE: OUTPUT VOLTAGE
(500 mV/cm AND 5 μs/cm)
BOTTOM TRACE: COLLECTOR OF LOAD
SWITCHING TRANSISTOR
LOAD = 100 mA TO 1A
(5 V/cm AND 5 μs/cm)

92CS-30034

Fig. 29 – Transient response.

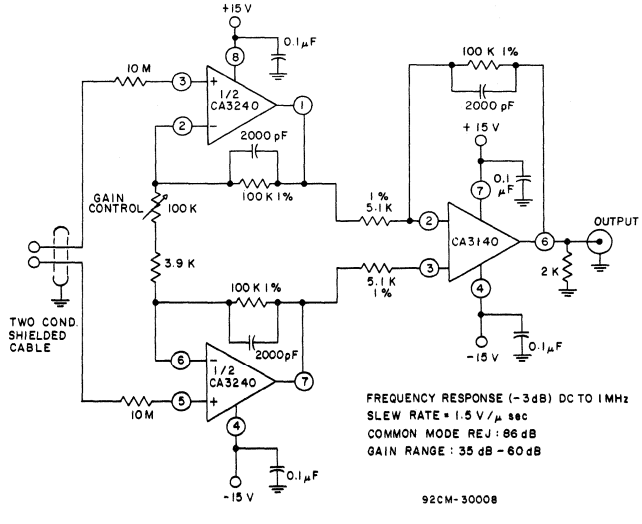
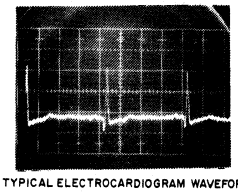


Fig. 30 – Precision differential amplifier.



TYPICAL ELECTROCARDIOGRAM WAVEFORM

Fig. 31 – Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

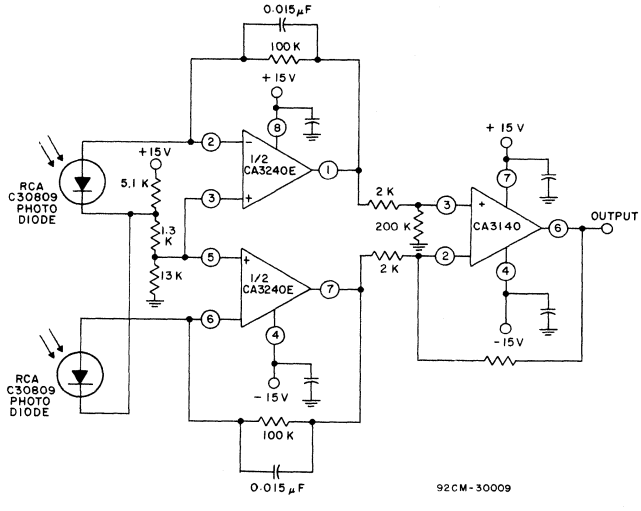
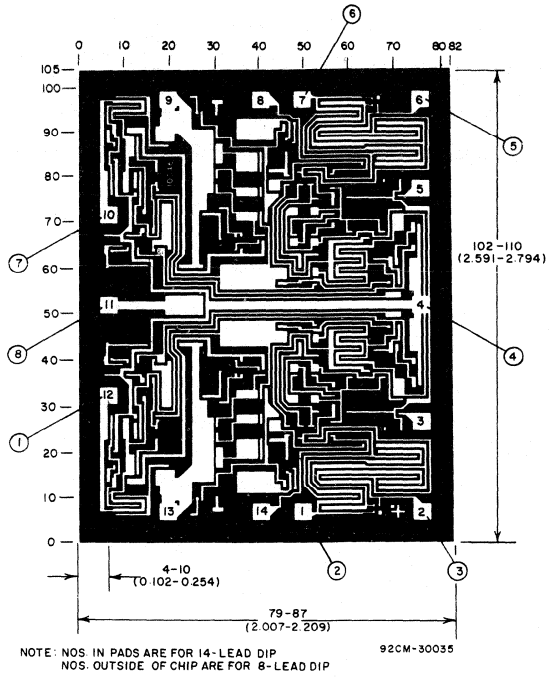


Fig. 32 – Differential light detector.

CA3240H Dimensions and Pad Layout



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^{o} instead of 90^{o} with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Advance Information/
Preliminary Data

CA3260A, CA3260

BiMOS Operational Amplifiers

With MOSFET Input, CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I=1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I=5 pA typ. at 15-V operation
  =2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

The RCA-CA3260A and CA3260 are integrated-circuit operational amplifiers that combine the advantages of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260-series circuits operate at supply voltages ranging from 4 to 16 volts, or ±2 to ±8 volts when using split supplies.

The CA3260 series is supplied in standard 8-lead TO-5-style packages (T suffix) and 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" packages (S suffix). The CA3260 is available in chip form (H suffix).

The CA3260A and CA3260 are also available in the 8-lead dual-in-line plastic package (Mini-DIP E suffix). All types operate over the full military-temperature range of -55° C to +125° C. The CA3260A offers superior input characteristics over those of the CA3260.

Applications:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital CMOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers*
  (e.g., follower for single-supply D/A converter)
- *Voltage regulators*
  (permits control of output voltage down to zero volts)
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*

File Number **1266**

CA3260A, CA3260

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals)..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C..... 630 mW
ABOVE 55°C ... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
UP TO 90°C..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING (All Types) ..... -55 to +125°C
STORAGE (All Types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION*..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
At distance 1/16 ± 1/32 in.
(1.59 ± 0.79 mm) from case
for 10 s max. ..... +265°C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS	CA3260A (T, S, E)	CA3260 (T, S, E)	UNITS
V^+=+7.5 V, V^-=-7.5 V, T_A=25°C (Unless Otherwise Specified)				
Input Resistance, R_I		1.5	1.5	TΩ
Input Capacitance, C_I	f=1 MHz	4.3	4.3	pF
Unity Gain Crossover Frequency, f_T		4	4	MHz
Slew Rate, SR		10	10	V/μs
Transient Response: Rise Time, t_r	C_L=25 pF, R_L=2 kΩ (Voltage Follower)	0.09	0.09	μs
Overshoot		10	10	%
Settling Time (4 V_{p-p} Input to < 0.1%)		1.8	1.8	μs
V^+=5 V, V^-=0 V, T_A=25°C (Unless Otherwise Specified)				
Input Offset Voltage, V_{IO}		2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	pA
Input Current, I_I		2	2	pA
Common-Mode Rejection Ratio, CMRR		70	60	dB
Large-Signal Voltage Gain, A_{OL}	V_O=4 V_{p-p}, R_L=20 kΩ	100 k 100	100 k 100	V/V dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.5	0 to 2.5	V
Supply Current, I^+	V_O=5 V, R_L=∞	1	1	mA
	V_O=2.5 V, R_L=∞	1.2	1.2	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	μV/V

CA3260A, CA3260

ELECTRICAL CHARACTERISTICS for Each Amplifier at T_A=25°C, V^+=15 V, V^-=0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS						UNITS
	CA3260A (T,S,E)			CA3260 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	—	2	5	—	6	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	—	0.5	20	—	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	—	5	30	—	5	50	pA
Large-Signal Voltage Gain, A_{OL}	50 k	320 k	—	50 k	320 k	—	V/V
V_O=10 V_{p-p}, R_L=10 kΩ	94	110	—	94	110	—	dB
Common-Mode Rejection Ratio, CMRR	80	95	—	70	90	—	dB
Common-Mode Input Voltage Range, V_{ICR}	0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	—	32	150	—	32	320	μV/V
Maximum Output Voltage:							V
At R_L=10 kΩ V_{OM}^+	11	13.3	—	11	13.3	—	
At R_L=10 kΩ V_{OM}^-	—	0.002	0.01	—	0.002	0.01	
At R_L=∞ V_{OM}^+	14.99	15	—	14.99	15	—	
At R_L=∞ V_{OM}^-	—	0	0.01	—	0	0.01	
Maximum Output Current, I_{OM}^+ (Source) @ V_O=7.5 V	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O=7.5 V	12	20	45	12	20	45	
Total Supply Current, I^+ R_L=∞ V_O(Ampli.A)=V_O (Ampli.B)=7.5 V	—	9	15.5	—	9	15.5	mA
V_O (Ampli.A)=V_O (Ampli.B)=0 V	—	1.2	3	—	1.2	3	
V_O (Ampli.A)=0 V V_O(Ampli.B)=7.5 V	—	5	8.5	—	5	8.5	
Input Offset Voltage Temp.Drift, $\Delta V_{IO}/\Delta T$	—	6	—	—	8	—	μV/°C
Crosstalk f=1 kHz	—	120	—	—	120	—	dB

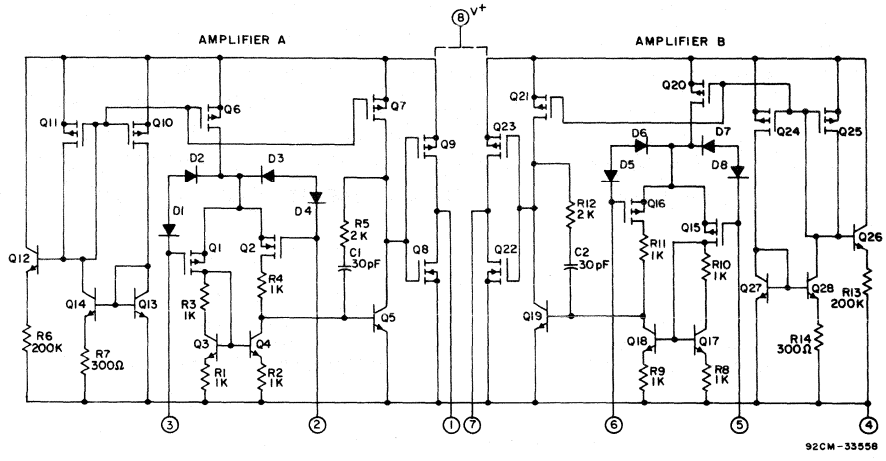
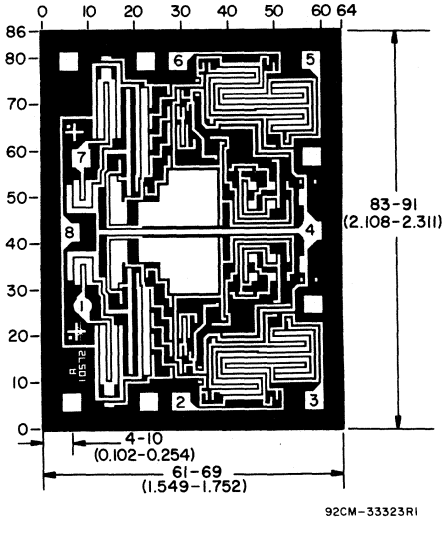


Fig. 1 - Schematic diagram of CA3260 series.

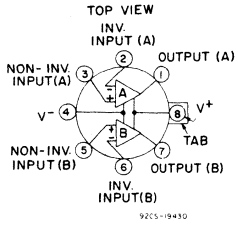


Dimensions and pad layout for CA3260H.

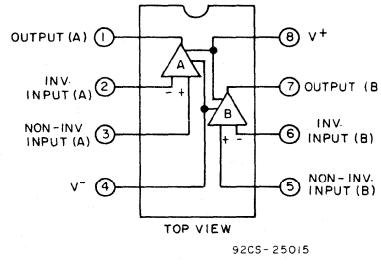
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3260A, CA3260



S and T Suffixes
Pin compatible with the industry-standard 1458



E Suffix
Pin compatible with the industry-standard 1458

Fig. 2 - Functional diagrams for the CA3260 Series.

CA3280A, CA3280

Dual Variable Operational Amplifiers

Features:

- *Low initial input-offset voltage: 500 μV max. (CA3280A)*
- *Low offset-voltage change versus I_{ABC}: <500 μV typ. for all types*
- *Low offset-voltage drift: 5 μV/C max. (CA3280A)*
- *Excellent matching of the two amplifiers for all characteristics*
- *Internal current-driven linearizing diodes reduce the external input current to an offset component*

The RCA-CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Interdigitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer

Applications:

- *Voltage-controlled amplifiers*
- *Voltage-controlled oscillators*
- *Multipliers*
- *Demodulators*
- *Sample and hold*
- *Instrumentation amplifiers*
- *Function generators*
- *Triangle wave-to-sine wave converters*
- *Comparators*
- *Audio preamplifiers*

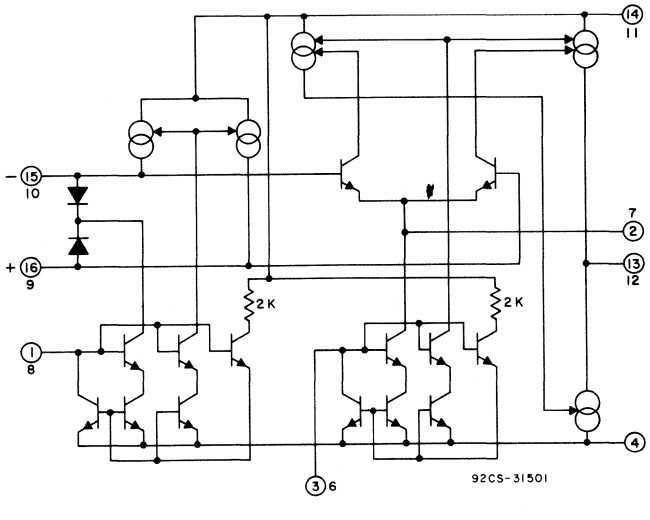


Fig. 1 – Functional diagram of 1/2 CA3280.

File Number **1174**

CA3280A, CA3280

characteristic is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced by RCA in 1969*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and highspeed comparators.

The operating-temperature ranges are -55 to +125° C for the CA3280A, and 0 to +70° C for the CA3280.

The CA3280 and CA3280A are supplied in the 16-lead dual-in-line plastic package (E suffix), in the 16-lead dual-in-line frit-seal ceramic package (F suffix, and are also supplied in chip form (H suffix).

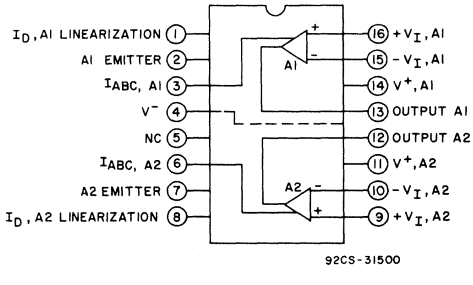
*"OTA Obsoletes Op Amp," by C.F. Wheatley and H.A. Wittlinger, NEC Proceedings, December, 1969.

For additional application information on this device and on OTA's in general, please refer to Application Notes: ICAN-6818, ICAN-6668, and ICAN-6077.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V+ AND V- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE RANGE	V+ to V-
INPUT SIGNAL CURRENT AT $I_D = 0$	100 μA
AMPLIFIER BIAS CURRENT	10 mA
OUTPUT SHORT CIRCUIT DURATION*	Indefinite
LINEARIZING DIODE BIAS CURRENT, I_D	5 mA
PEAK INPUT CURRENT WITH LINEARIZING DIODE	$\pm I_D$
POWER DISSIPATION, P_D:	
Either Amplifier	600 mW
Total Package	750 mW
Above 55° C	Derate linearly at 6.67 mW/° C
AMBIENT TEMPERATURE RANGE, T_A:	
Operating:	
CA3280	0 to +70° C
CA3280A	-55 to +125° C
Storage, All Types	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 sec. max	+265° C

*Short circuit may be applied to ground or to either supply.



Terminal Assignment

CA3280A, CA3280

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $V^{\pm}$ = 15 V (Unless Otherwise Stated)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	I_{ABC}=1 mA	–	–	3	–	–	0.5	mV
	I_{ABC}=100μA	–	0.7	3	–	0.25	0.5	
	I_{ABC}=10μA	–	–	3	–	–	0.5	
	I_{ABC}=1mA to 10μA T_A=full temp. range	–	0.8	4	–	0.8	1.5	
Input Offset Voltage Change, $\lvert\Delta V_{IO}\rvert$	I_{ABC}=1μA to 1mA	–	0.5	1	–	0.5	1	mV
	I_{ABC}=100μA T_A=full temp. range	–	5	–	–	3	5	μV/°C
Amplifier Bias Voltage, V_{ABC}	I_{ABC}=100μA	–	1.2	–	–	1.2	–	V
Peak Output Voltage: Positive VOM^+	I_{ABC}=500μA	12	13.7	–	12.5	13.7	–	V
Negative VOM^-		12	–14.3	–	–13.3	–14.3	–	
Positive VOM^+	I_{ABC}=5μA	12	13.9	–	12.5	13.9	–	
Negative VOM^-		12	–14.5	–	–13.5	–14.5	–	
Common-Mode Input Voltage Range, V_{ICR}	I_{ABC}=100μA	–13	–	13	–13	–	13	V
Noise Voltage, e_N: 10 Hz	I_{ABC}=500μA	–	20	–	–	20	–	$\frac{nV}{\sqrt{Hz}}$
1 kHz		–	8	–	–	8	–	$\frac{\mu V}{\sqrt{Hz}}$
10 kHz		–	7	–	–	7	–	$\frac{nV}{\sqrt{Hz}}$
Input Offset Current, I_{IO}	I_{ABC}=500μA	–	0.3	0.7	–	0.3	0.7	μA
Input Bias Current, I_{IB}	I_{ABC}=500μA	–	1.8	5	–	1.8	5	μA
	I_{ABC}=500μA T_A=full temp. range	–	3	8	–	3	8	
Peak Output Current: Source IOM^+	I_{ABC}=500μA	350	410	650	350	410	650	μA
Sink IOM^-		–350	–410	–650	–350	–410	–650	
Source IOM^+	I_{ABC}=5μA	3	4.1	7	3	4.1	7	
Sink IOM^-		–3	–4.1	–7	–3	–4.1	–7	
Sink and Source, IOM^-, IOM^+	I_{ABC}=500μA T_A=full temp. range	350	450	550	350	450	550	
Linearization Diodes: Dynamic Impedance	I_D = 100μA	–	700	–	–	700	–	Ω
Offset Current	I_D =100μA	–	10	–	–	10	–	μA
	I_D=10μA	–	0.5	1	–	0.5	1	

CA3280A, CA3280

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Diode Network Supply Current	I_{ABC}=100μA	250	400	800	250	400	800	μA
Amplifier Supply Current (Per amplifier)	I_{ABC}=500μA	–	2	2.4	–	2	2.4	mA
Amplifier Output Leakage Current, I_{OL}	I_{ABC}=0, V_O=0V	–	0.015	0.1	–	0.015	0.1	nA
	I_{ABC}=0, V_O=30V	–	0.15	1	–	0.15	1	
Common-Mode Rejection Ratio, CMRR	I_{ABC}=100μA	80	100	–	94	100	–	dB
Power-Supply Rejection Ratio, PSRR	I_{ABC}=100μA	86	105	–	94	105	–	dB
Open-Loop Voltage Gain, A_{OL}	I_{ABC}=100μA, R_L=∞, V_O=20 Vp-p	94	100	–	94	100	–	dB
		50K	100K	–	50K	100K	–	V/V
Forward Transconductance: Large Signal, Gm	I_{ABC}=50μA	–	0.8	1.2	–	0.8	1.2	mmho
Small Signal, gm	I_{ABC}=1mA	–	16	22	–	16	22	
Input Resistance, R_I	I_{ABC}=10μA	0.5	–	–	0.5	–	–	MΩ
Channel Separation	f=1 kHz	–	94	–	–	94	–	dB
Open-Loop Total Harmonic Distortion	f=1 kHz, I_{ABC}= 1.5 mA, R_L=15kΩ, V_O= 20 Vp-p	–	0.4	–	–	0.4	–	%
Bandwidth	I_{ABC}=1mA, R_L=100Ω	–	9	–	–	9	–	MHz
Slew Rate, SR: Open Loop	I_{ABC}=1mA	–	125	–	–	125	–	V/μs
Capacitance: Input, C_I	I_{ABC}=100μA	–	4.5	–	–	4.5	–	pF
Output, C_O		–	7.5	–	–	7.5	–	
Output Resistance, R_O	I_{ABC}=100μA	–	63	–	–	63	–	MΩ

Figs. 2 and 3 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common-mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single-ended converters, as shown in Fig. 4. A matched resistor network requires ratio matching of 0.01% or trimming for 80 dB of common-mode rejection. The CA3280, with its excellent common-mode rejection ratio, is capable of converting a small (±25 mV) differential input signal to a single-ended output without the need for a matched resistor network.

Fig. 5 shows the CA3280 in a typical gain-control application. The input-signal range as a function of distortion at various levels of linearization diode current is shown in Fig. 6 This curve shows only the AGC capability of the diode network, but gain control can also be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely gmR_L. For example, with an I_{ABC} of 1 mA, the gm is approximately 16 mmhos. With the CA3280 operating into a 5 kΩ resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low-value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

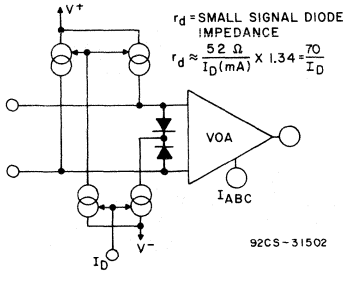


Fig. 2 – VOA showing linearization diodes and current drive.

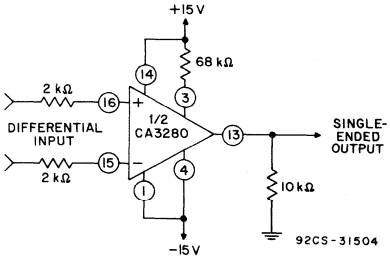


Fig. 4 – Differential to single-ended converter.

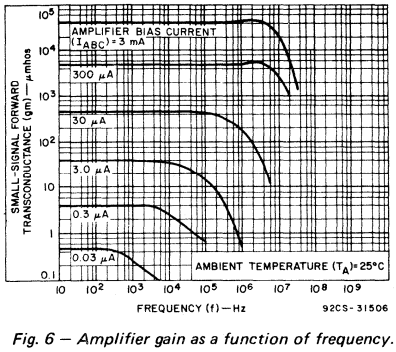


Fig. 6 – Amplifier gain as a function of frequency.

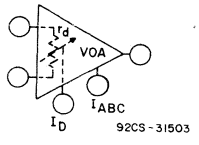


Fig. 3 – Block diagram of linearized VOA.

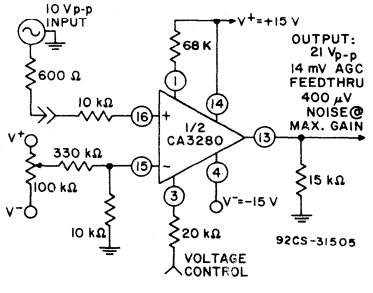


Fig. 5 – Typical gain control circuit.

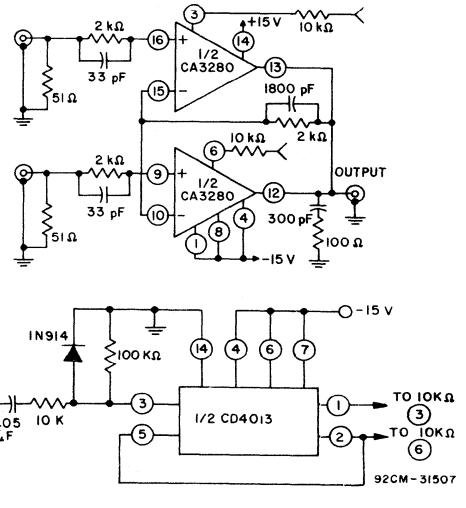


Fig. 7 – Two-channel linear multiplexer.

CA3280A, CA3280

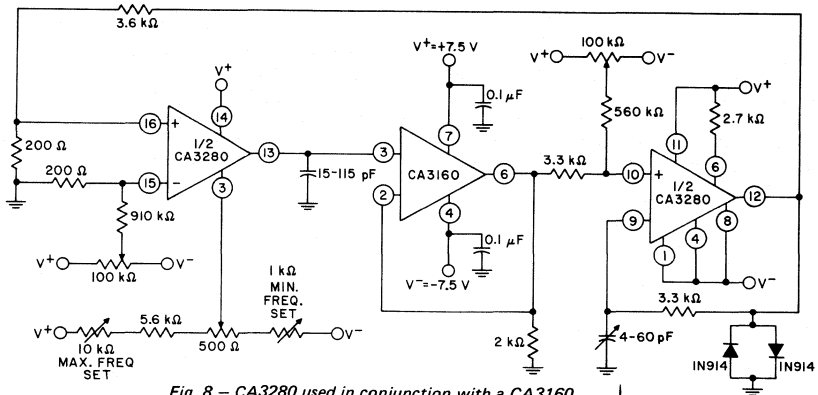


Fig. 8 — CA3280 used in conjunction with a CA3160 to provide a function generator with a tunable range of from 2 Hz to 1 MHz.

Fig. 9 shows a triangle wave-to-sine wave converter using the CA3280. Two 100KΩ resistors are connected between the differential amplifier emitters and V+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is approximately 0.37% for this circuit.

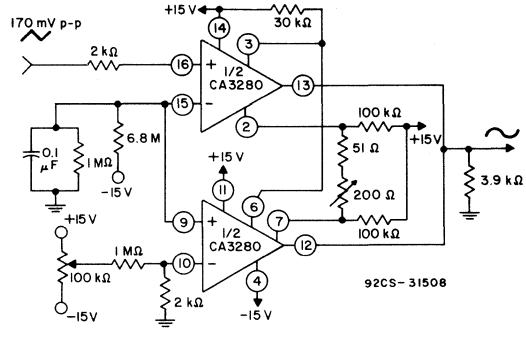


Fig. 9 — Triangle wave-to-sine wave converter.

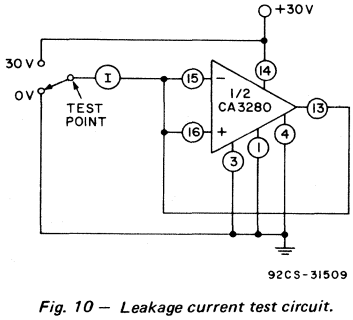


Fig. 10 — Leakage current test circuit.

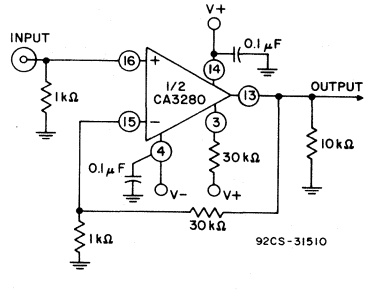
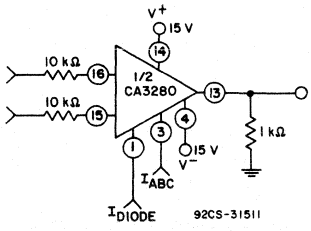
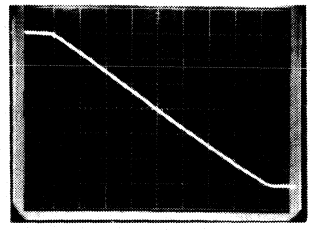


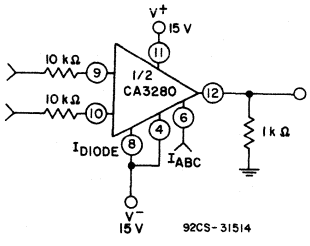
Fig. 11 — Channel separation test circuit.

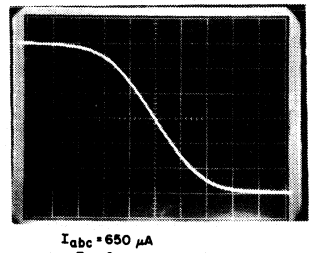




I_{abc} = 650 μA
I_D = 200 μA
VERT = 200 μA/DIV
HOR = 1 V/DIV
92CS-31512

a) With diode programming terminal active





I_{abc} = 650 μA
I_D = 0
VERT = 200 μA/DIV
HOR = 25 mV/DIV
92CS-31513

b) With diode programming terminal cut-off

Fig. 12 – CA3280 transfer characteristics.

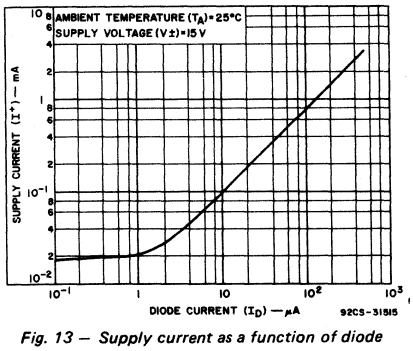


Fig. 13 – Supply current as a function of diode current.

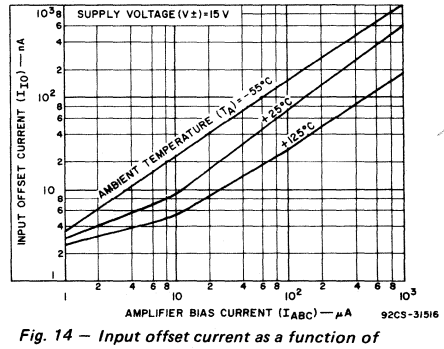


Fig. 14 – Input offset current as a function of amplifier bias current.

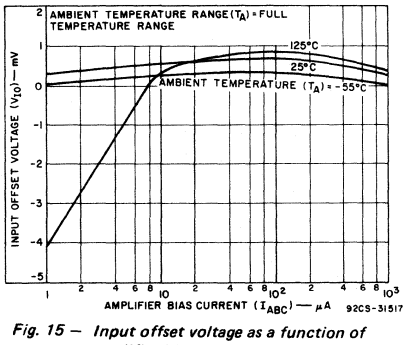


Fig. 15 – Input offset voltage as a function of amplifier bias current.

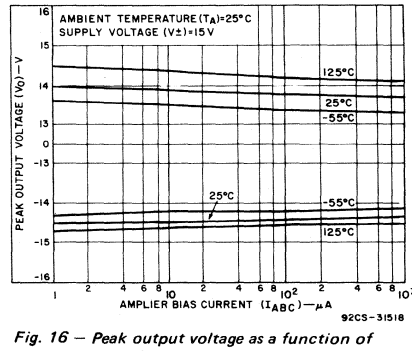


Fig. 16 – Peak output voltage as a function of amplifier bias current.

CA3280A, CA3280

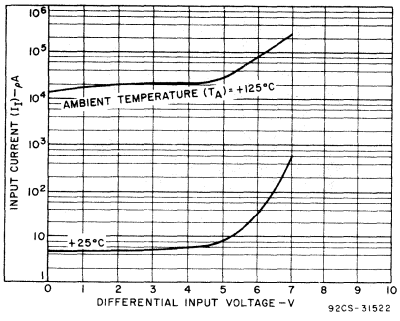


Fig. 17 – Input current as a function of input differential voltage.

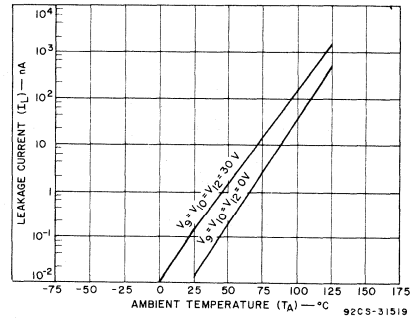


Fig. 18 – Leakage current as a function of temperature.

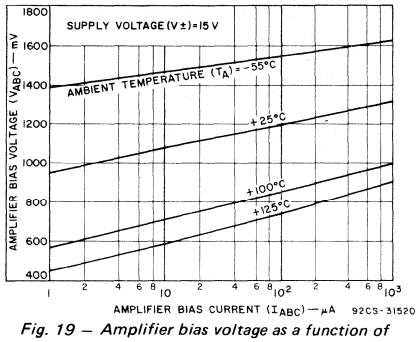


Fig. 19 – Amplifier bias voltage as a function of amplifier bias current.

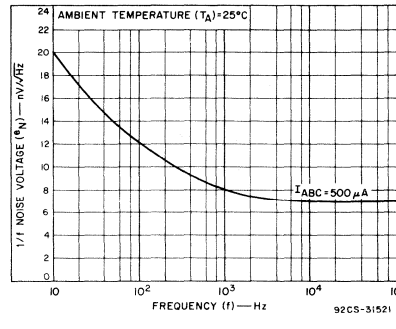


Fig. 20 – 1/F noise as a function of frequency.

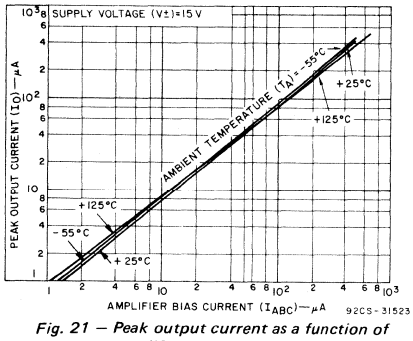


Fig. 21 – Peak output current as a function of amplifier bias current.

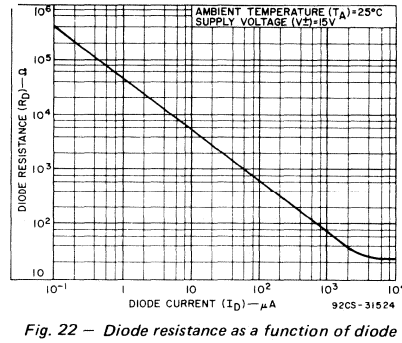


Fig. 22 – Diode resistance as a function of diode current.

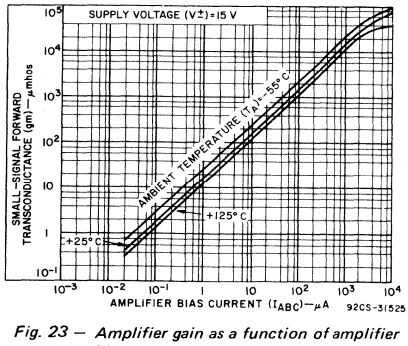


Fig. 23 – Amplifier gain as a function of amplifier bias current.

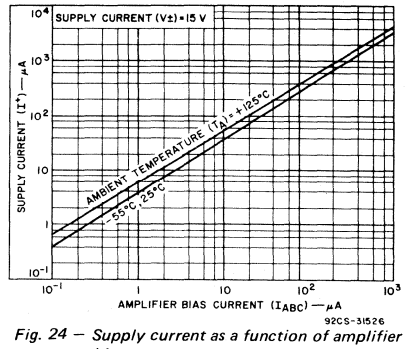


Fig. 24 – Supply current as a function of amplifier bias current.

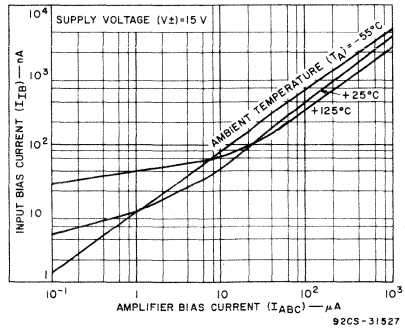
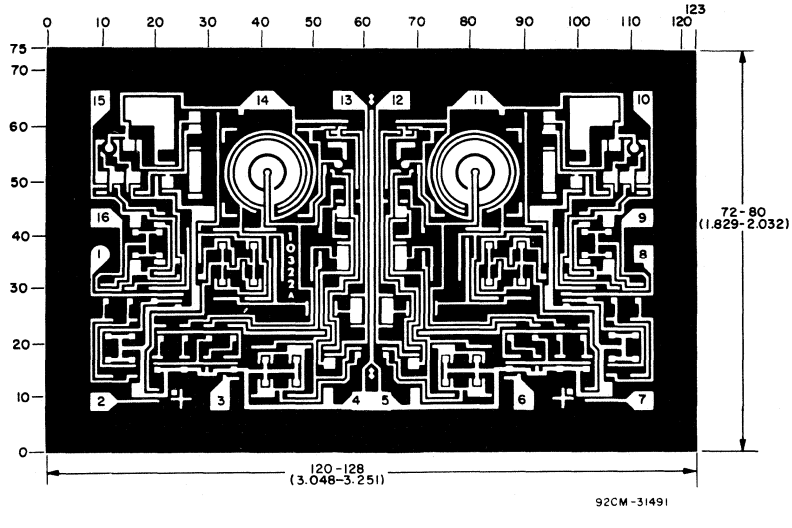


Fig. 25 – Input bias current as a function of amplifier bias current.



Dimensions and pad layout for CA3280H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3401

Quad Single-Supply Operational Amplifier

For Automotive Electronics and Industrial Control Systems

Features:

- *Single-supply operation – +5 V to +18 Vdc*
- *Internally compensated*
- *Wide unity-gain bandwidth – 5 MHz typ.*
- *Low input bias current – 50 nA typ.*
- *High open-loop gain – 2000 V/V typ.*

The RCA-3401 is a high-gain monolithic quad operational amplifier designed specifically for applications using a single positive power supply. No external compensation is necessary. Closed-loop stability in each of the four independent amplifiers is maintained by a 3-pF on-chip capacitor. The CA3401 is idealiy suited for applications in industrial control systems, automotive electronics, and general purpose amplifiers, e.g. oscillators, tachometers, active filters, and multichannel amplifiers.

The CA3401 is supplied in a 14-lead dual-in-line plastic package (E suffix), and is also available in chip form (H suffix). It is a direct replacement for the Motorola MC3401P, and is pin-compatible with the Motorola MC3301P and the National Semi-conductor LM3900N. The CA3401 can be operated over the temperature range of -55 to +125° C, although the limit values of certain specified electrical characteristics apply only over the range of 0 to +75° C.

Applications:

- *Automotive*
- *Constant-Current Sources*
- *Multivibrators*
- *Sample and Hold*
- *Square-Wave Generator*
- *Oscillators*
- *Tachometers*
- *Active Filters*
- *Multi-Channel Amplifiers*
- *Summing Amplifiers*

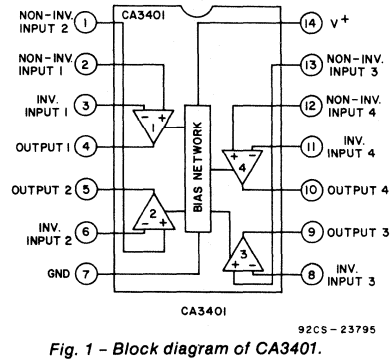


Fig. 1 – Block diagram of CA3401.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

DC SUPPLY VOLTAGE	+18 V
INPUT SIGNAL CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25° C	625 mW
Above T_A = 25° C	Derate lineary 5 mW/° C
AMBIENT TEMPERATURE RANGE:	
Operating	-55 to + 125° C
Storage	-65 to + 150° C
LEAD TEMPERATURE (During soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	300° C

File Number **630**

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $V^+ = 15$ V (Unless Indicated Otherwise)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
STATIC					
Output Voltage:					
High, V_{OH}		13.5	14.2	–	V
Low, V_{OL}		–	0.03	0.1	
Max. Undistorted Output Swing, V_{OP-P}	$0^oC<T_A<75^oC$	10	13.5	–	
Output Current:					
Source, I_{SOURCE}		5	10	–	mA
Sink, I_{SINK}		0.5	1	–	
Total Quiescent Current: I_Q					
Noninverting inputs open		–	6.9	10	mA
Noninverting inputs grounded		–	7.8	14	
Input Bias Current, I_{IB}	$R_L = \infty$ $T_A = 25^oC$	–	50	300	nA
	$R_L = \infty$ $0^oC \leq T_A \leq 75^oC$	–	–	500	
DYNAMIC					
Open-Loop Voltage Gain, A_{OL}	$T_A = 25^oC$	1000	2000	–	V/V
	$0^oC \leq T_A \leq 75^oC$	800	–	–	
Input Resistance, R_I		0.1	1	–	MΩ
Slew Rate, SR	$C_L = 100$ pF, $R_L = 5$ kΩ	–	0.6	–	V/μs
Unity Gain Gandwidth, BW		–	5	–	MHz
Phase Margin, ϕ		–	70	–	Degrees
Power Supply Rejection	f = 100 Hz	–	55	–	dB
Channel Separation, e_{01}/e_{02}	f = 1 kHz	–	65	–	dB

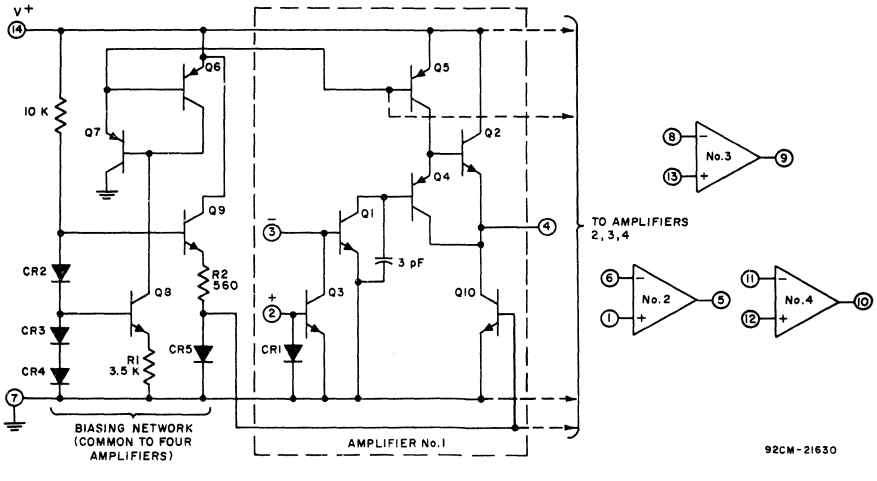


Fig.2 – Schematic diagram of CA3401.

CA3401

TEST CIRCUITS

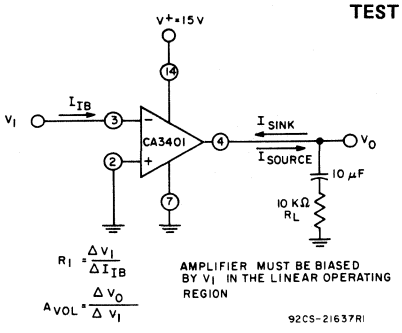


Fig.3 – Open-loop gain and input resistance, input bias current and output current test circuit.

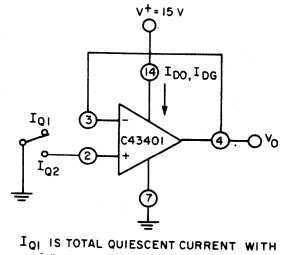


Fig.4 – Quiescent power supply current test circuit.

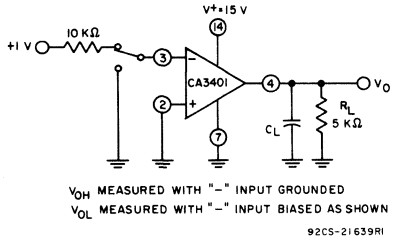


Fig.5 – Output voltage swing test circuit.

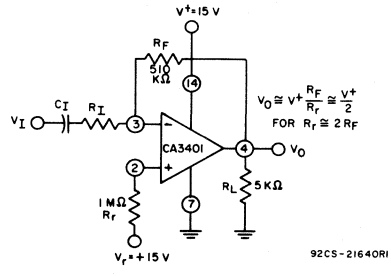


Fig.6 – Peak-to-peak output voltage test circuit.

TYPICAL CHARACTERISTIC CURVES

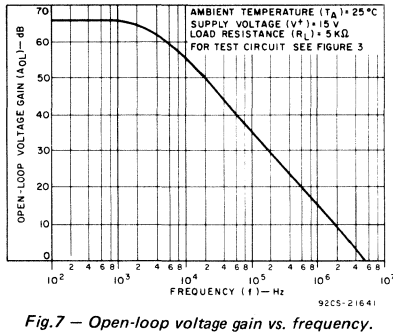


Fig.7 – Open-loop voltage gain vs. frequency.

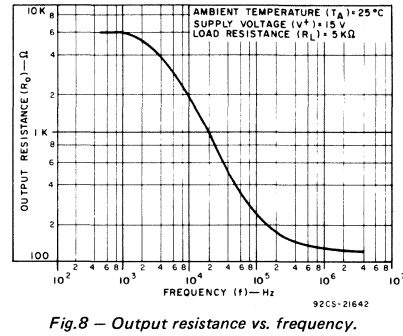


Fig.8 – Output resistance vs. frequency.

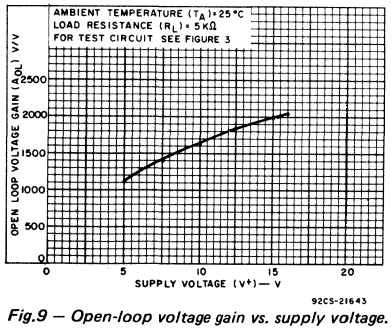


Fig.9 – Open-loop voltage gain vs. supply voltage.

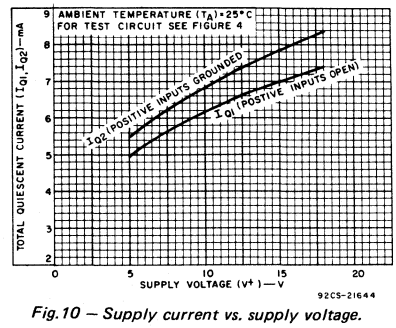


Fig.10 – Supply current vs. supply voltage.

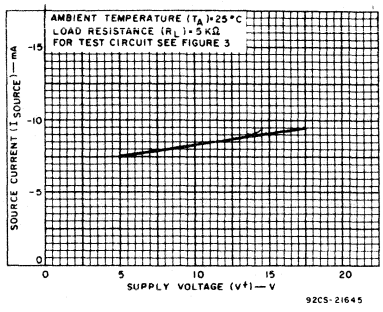


Fig.11 – Source current vs. supply voltage.

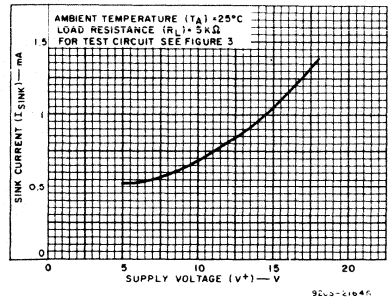
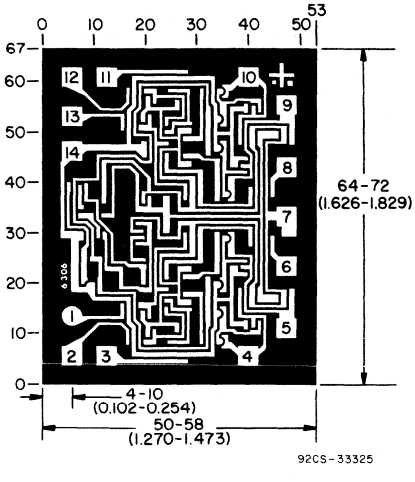


Fig.12 – Sink current vs. supply voltage.



Dimensions and pad layout for CA3401H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3410A, CA3410

Product Preview

Quad BiMOS Operational Amplifiers

With MOSFET Input, Bipolar Outputs

Features:

- *Internally compensated*
- *MOSFET input stage*
  - (a) *Very high input impedance (Z_{IN}) -1.5 TΩ typ.*
  - (b) *Very low input current (I_I) -10 pA typ. at ± 15 V*
  - (c) *Wide common-mode input-voltage range (V_{ICR}) - can be swung to the negative supply-voltage rail*
  - (d) *Rugged input stage - bipolar diode protected*
- *Directly replaces industry type 324 in many applications*
- *Operation from 6-to-36 volts single or dual supplies*
- *Characterized for ± 15-volt operation and for TTL supply systems with operation down to 6 volts*
- *Wide bandwidth - 5 MHz unity gain at ± 15 V or a single 30 V supply*
- *High voltage-follower slew rate - 10 V/μs*

The RCA-CA3410A and CA3410 are BiMOS integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

The CA3410A and CA3410 are supplied in the 14-lead dual-in-line plastic package (E suffix). They are pin-compatible with the industry standard 324 and 084 operational amplifiers in similar packages. The CA3410A and CA3410 have an operating-temperature range of -40 to +85°C.

Applications:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds - minutes - hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Instrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

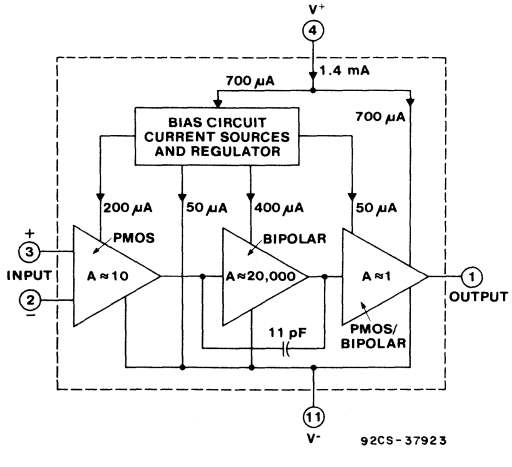


Fig. 1 - Block diagram of 1/4 of the CA3410E.

File Number **1546**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	6 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±16 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	625 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	-40 to +85°C
STORAGE	-65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION*	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)	
FROM CASE FOR 10 SECONDS MAX.	+265°C

*Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

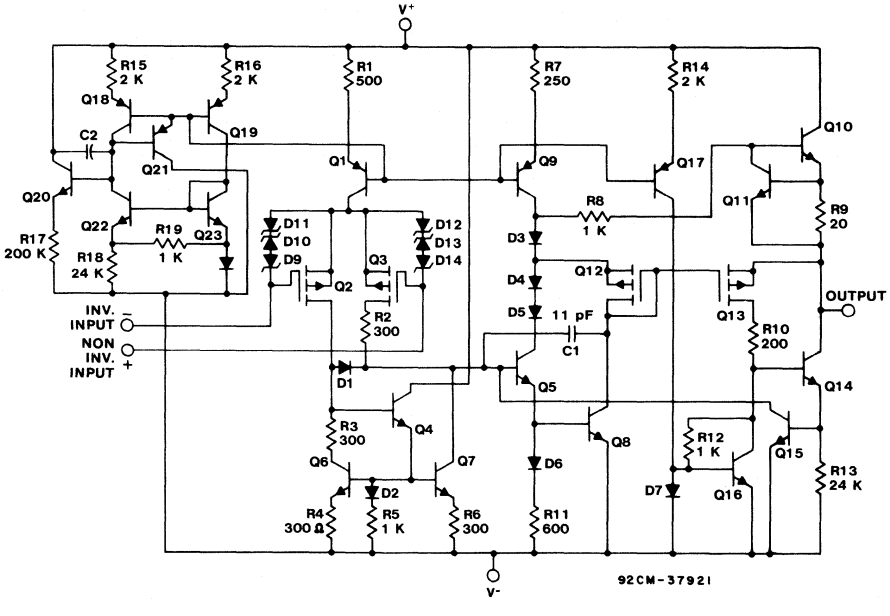


Fig. 2 - Schematic diagram for 1/4 of the CA3410.

Circuit Description

The schematic diagram of one amplifier section of the CA3410 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q2 and Q3 with gate-to-source protection against static discharge damage provided by zener diodes D9, D10, D11, and D12, D13, D14. Constant current bias is applied to the differential amplifier from transistors Q1 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistors Q5 and Q8 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion.

CA3410A, CA3410

ELECTRICAL CHARACTERISTICS for Equipment Design at V^+ = 15 V, V^- = 15 V, T_A = 25° C Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		CA3410A			CA3410			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	—	3	8	—	8	15	mV
Input Offset Current	I_{IO}	—	0.5	10	—	0.5	30	pA
Input Current	I_I	—	10	30	—	10	40	pA
Large-Signal Voltage Gain	A_{OL}	20 k	100 k	—	20 k	100 k	—	V/V
R_L = 2 kΩ	V_O = ± 10 V	86	100	—	86	100	—	dB
Common-Mode Rejection Ratio	CMRR	—	32	100	—	32	320	μV/V
		80	90	—	70	90	—	dB
Common-Mode Input-Voltage Range	V_{ICR}	-15	-15.5 to 13	12.5	-15	-15.5 to 13	12.5	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V$	—	50	100	—	50	316	μV/V
	PSRR	80	86	—	70	86	—	dB
Maximum Output Voltage Swing	V_{OM}^+	13	13.9	—	13	13.9	—	V
R_L = 2 kΩ	V_{OM}^-	-10.5	-11.2	—	-10.5	-11.2	—	
Maximum Output Voltage Swing	V_{OM}^+	13.5	14.2	—	13.5	14.2	—	V
R_L = 10 kΩ	V_{OM}^-	-11	-12.2	—	-11	-12.2	—	
Total Supply Current	I^+	—	8	10	—	8	12	mA
Total Device Dissipation	P_D	—	240	300	—	240	360	mW

Circuit Description (Cont'd)

Output Stage

The output stage is a physo-complementary amplifier with n-p-n output transistors. Diode D3 complements Q10, while diode connected PMOS transistor Q12 complements PMOS transistor Q13. N-P-N transistor Q14 provides the sinking current while n-p-n transistor Q10 provides the sourcing current.

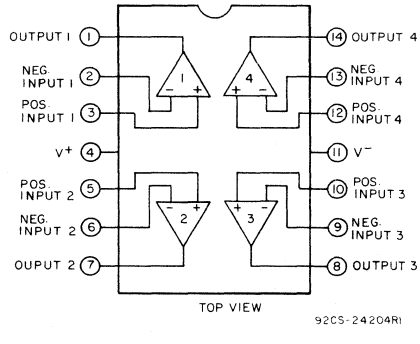


Fig. 3 - Functional diagram.

CA3410A, CA3410

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = 15$ V, $V^- = -15$ V, $T_A = 25°C$		TYPICAL VALUES CA3410A	TYPICAL VALUES CA3410	UNITS
Input Resistance	R_i			1.5	1.5	TΩ
Input Capacitance	C_i			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage	e_n	BW = 140 kHz, R_S = 1 MΩ		48	48	μV
Equivalent Input Noise Voltage	e_n	f = 1 kHz	R_S =	40	40	nV/√Hz
		f = 10 kHz	100 Ω	30	30	
Short-Circuit Current to Opposite Supply						
Source	I_{OM}^+			35	35	mA
Sink	I_{OM}^-			17	17	
Gain-Bandwidth Product	f_T			5.4	5.4	MHz
Slew Rate	SR			10	10	V/μs
Transient Response:						
Rise Time:	t_r	R_L = 2 kΩ		0.08	0.08	μs
Overshoot		C_L = 100 pF		10	10	%
Crosstalk		f = 1 kHz		120	120	dB

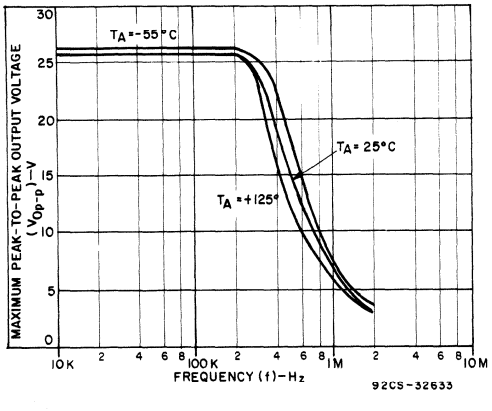


Fig. 4 - Output voltage as a function of frequency and temperature.

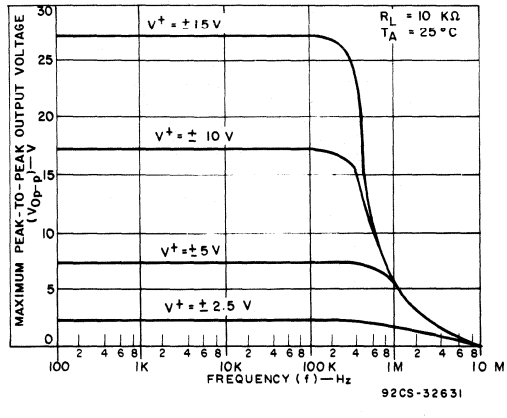


Fig. 5 - Output voltage as a function of frequency and supply voltage.

CA3410A, CA3410

ELECTRICAL CHARACTERISTICS for Equipment Design at V^+ = 15 V, V^- = 15 V, T_A = -40 to 100°C Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3410A	CA3410	
Input Offset Voltage	V_{IO}	4	10	mV
Input Offset Current	I_{IO}	8	10	mA
Input Current	I_I	10	20	mA
Large-Signal Voltage Gain	A_{OL}	50 k	50 k	V/V
R_L = 2 kΩ	V_O = ± 10 V	94	94	dB
Common-Mode Rejection Ratio	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	-15 to +12.50	-15 to +12.50	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V$	150	150	μV/V
	PSRR	76	76	dB
Maximum Output Voltage	V_{OM}^+	13.50	13.50	V
R_L = 2 kΩ	V_{OM}^-	-10.50	-10.50	
Supply Current	I^+	9	10	mA
Total Device Dissipation	P_D	270	300	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	10	12	μV/°C

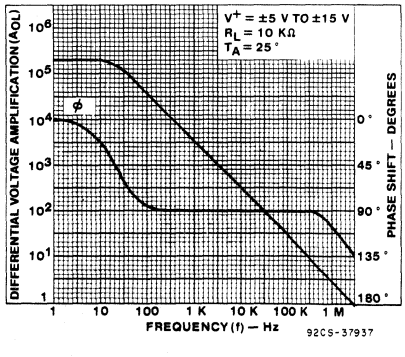


Fig. 6 - Differential voltage amplification as a function of frequency.

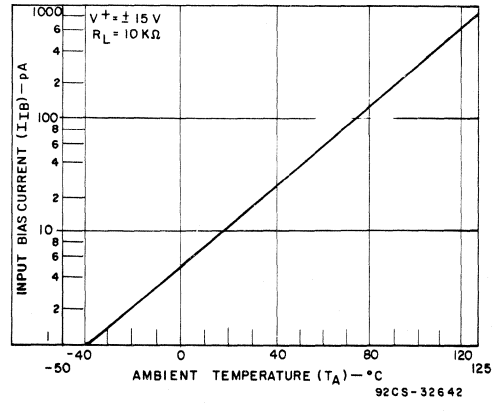


Fig. 7 - Input bias current as a function of ambient temperature.

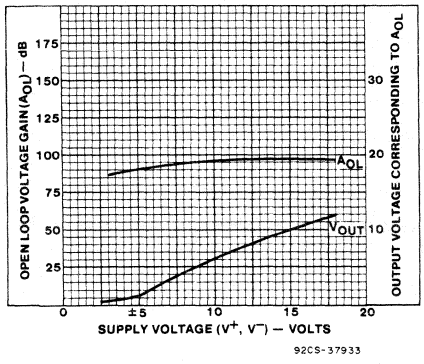


Fig. 8 - Open-loop voltage gain as a function of supply voltage and output voltage.

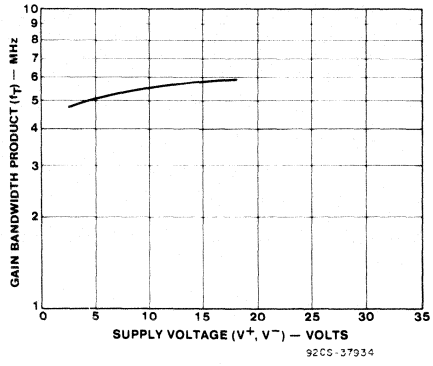


Fig. 9 - Gain-bandwidth product as a function of supply voltage.

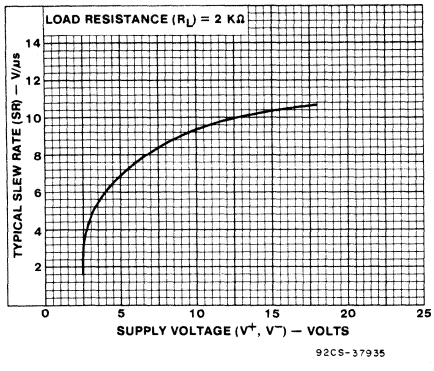


Fig. 10 - Slew rate as a function of supply voltage.

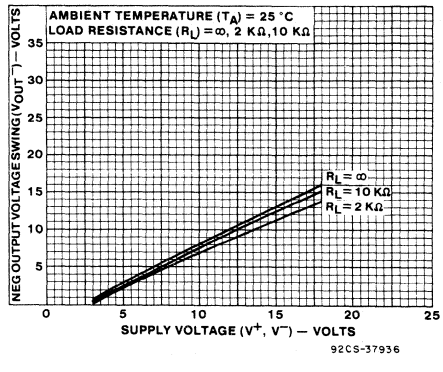


Fig. 11 - Negative output voltage swing as a function of supply voltage.

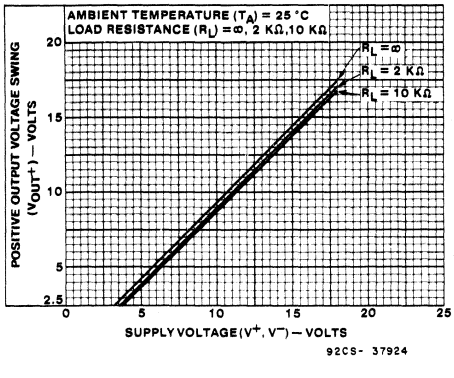


Fig. 12 - Positive output voltage swing as a function of supply voltage.

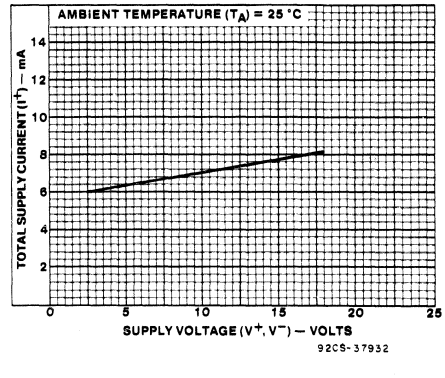


Fig. 13 - Total supply current as a function of supply voltage.

CA3410A, CA3410

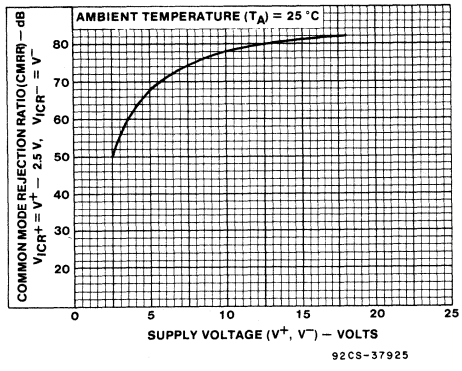


Fig. 14 - Typical common-mode rejection ratio as a function of supply voltage.

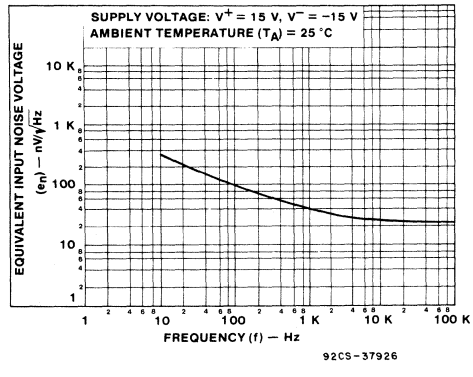


Fig. 15 - Equivalent input noise voltage as a function of frequency.

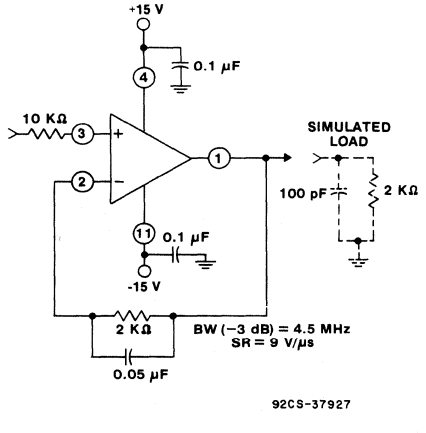


Fig. 16 - Split-supply voltage-follower test circuit.

APPLICATIONS CONSIDERATIONS

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3410 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 18 uses the CA3410E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3410E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3410E, triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3410E), the triac is turned off and held off in a similar manner. Note that power for the CA3410E is supplied by the CA3059 internal power supply.

The advantage of using the CA3410E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

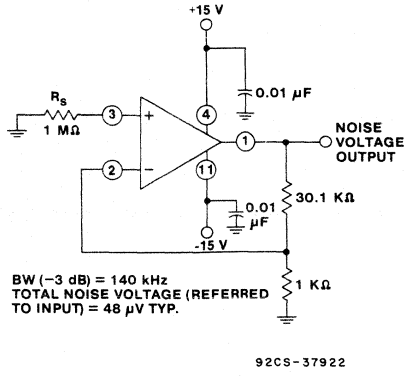


Fig. 17 - Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

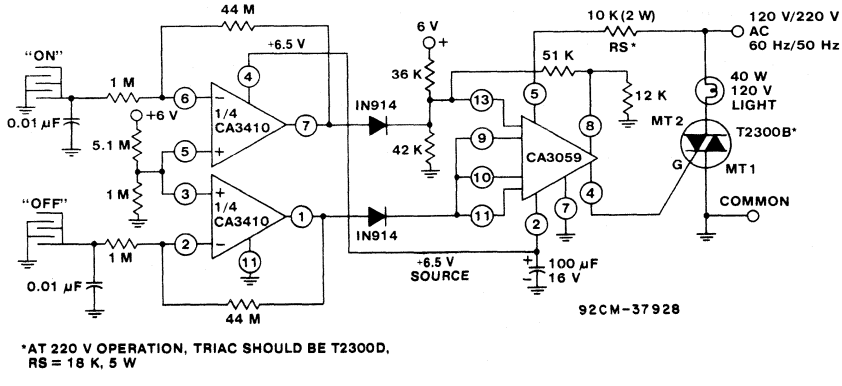


Fig. 18 - On/off touch switch.

Dual Level Detector (window comparator)

Fig. 19 illustrates a simple dual liquid level detector using the CA3410E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3410E in a circuit similar to that of the on/off touch switch shown in Fig. 18. The changes in voltage for both the upper and lower level sensors are processed by the amp 3 of their CA3410 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

CA3410A, CA3410

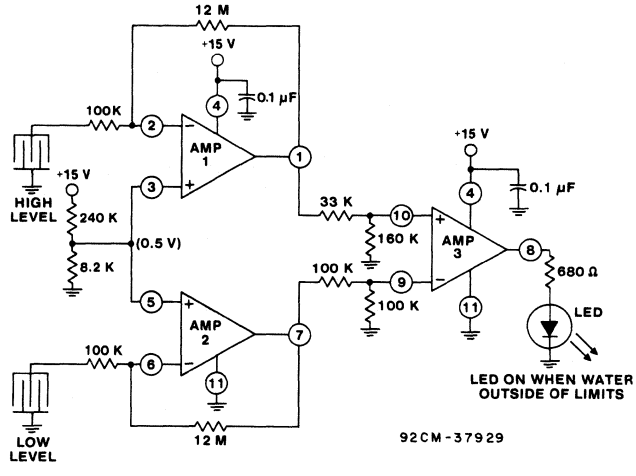


Fig. 19 - Dual level detector.

Precision Differential Amplifier

Fig. 20 shows the CA3410 in the classical precision differential amplifier circuit. The CA3410 is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 21 shows a typical electrocardiogram waveform obtained with this circuit.

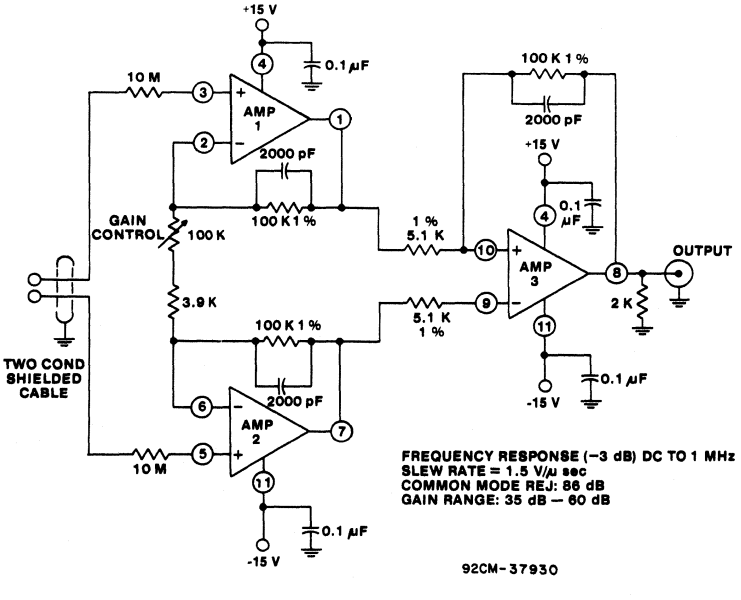
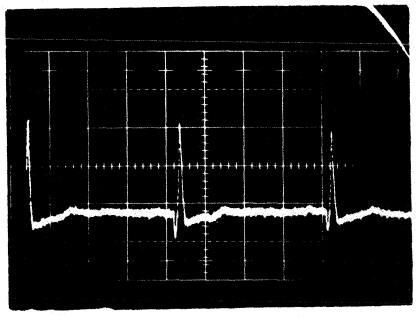


Fig. 20 - Precision differential amplifier.



VERTICAL : 1.0 mV/ DIV.
(AMPLIFIER GAIN = 100 X)
(SCOPE SENSITIVITY = 0.1V/DIV.

HORIZONTAL : > 0.2 SEC/DIV (UNCAL)

92CS-30033

TYPICAL ELECTROCARDIOGRAM WAVEFORM

Fig. 21 - Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 22, the CA3410E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3410 outputs are subtracted in the second stage (Amp 3) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

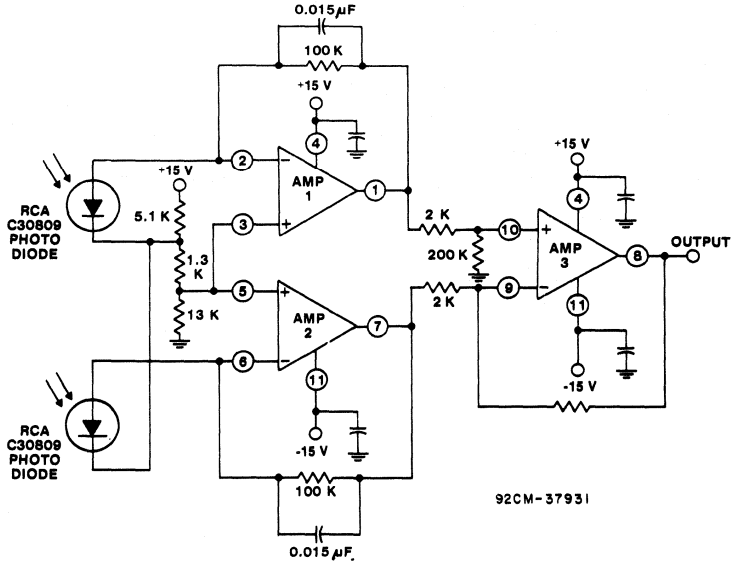


Fig. 22 - Differential light detector.

CA3420A, CA3420

Advance Information/
Preliminary Data

Low-Supply Voltage, Low-Input Current BiMOS Op Amps

Features:
- *2-V supply at 300-μA supply current*
- *1-pA (typ.) input current (essentially constant to 85° C)*
- *Rail-to-rail output swing (Drive ±2 mA into 1-kΩ load)*
- *Pin compatible with 741 op amp*

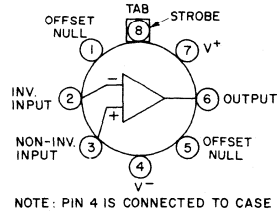
Applications:
- *pH probe amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable equipment*
- *Inaccessible field equipment*
- *Battery-dependent equipment (Medical and military)*

The RCA-CA3420A and CA3420• are integrated-circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. The CA3420A and CA3420 BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very-high-input impedance, very-low-input currents (less than 1 pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10° C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase-compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single-supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5 mA min. is provided by using non-linear current mirrors.

The CA3420-series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

• Formerly Dev. Type No. TA10841

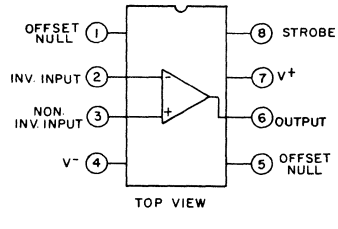
TERMINAL ASSIGNMENTS



NOTE: PIN 4 IS CONNECTED TO CASE

TOP VIEW 92CS-33997

S AND T SUFFIXES



TOP VIEW

92CS-29086

E SUFFIX

File Number **1320**

CA3420A, CA3420

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25° C):

DC Supply Voltage
(Between V^+ and V^- Terminals) ..... 22 V
Differntial-Mode
Input Voltage ..... ±15 V
Common-Mode DC
Input Voltage ..... (V^+ + 8 V) to (V^- -0.5 V)
Input-Terminal Current ..... 1 mA
Device Dissipation:
Without Heat Sink —
Up to 55° C ..... 630 mW
Above 55° C ..... Derate linearly 6.67 mW/° C
With Heat Sink -
Up to 110° C ..... 630 mW
Above 110° C ..... Derate linearly 16.7 mW° C

Temperature Range:
Operating (All Types) ..... -55 to +125° C
Storage (All Types) ..... -65 to +150° C
Output Short-Circuit
Duration* ..... Indefinite
Lead Temperature
(During Soldering):
At Distance 1/16 ± 1/32 Inch
(1.59 ± 0.79 mm) from case
For 10 seconds max. ..... +265° C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

Characteristic		Test Conditions V+ = +10V; V- = -10V TA = 25° C		CA3420A (T,S,E)	CA3420 (T,S,E)	Units
Input Resistance	R_I			150	150	TΩ
Input Capacitance	C_I			4.9	4.9	pF
Output Resistance	R_O			300	300	Ω
Equivalent Input Noise Voltage	e_n	f = 1 KHz	R_S 100 Ω	62	62	nV/ Hz
		f = 10 KHz	R_S 100 Ω	38	38	nV/ Hz
Short-Circuit Current Source To Opposite Supply Source IOM+				2.6	2.6	mA
Sink IOM-				2.4	2.4	mA
Gain-Bandwidth Product	f_T			0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	V/μs
Transient Response Rise Time tr		R_L = 2 K Ω, C_L = 100 pF		0.7	0.7	μs
Overshoot		R_L = 2 K Ω, C_L = 100 pF		15	15	%
Current from Terminal 8 To V-	I_{8^+}			20	20	μA
Current from Terminal 8 To V+	I_{8^-}			2	2	mA

CA3420A, CA3420

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 1V, V- = -1V, TA = 25°C unless otherwise specified

Characteristic	Limits						Units
	CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.01	4	—	0.01	4	pA
Input Current $\|I_I\|$ *	—	0.02	5	—	1	5	pA
Large-Signal Voltage Gain	20K	100K	—	10K	100K	—	V/V
AQL (R_L = 10 KΩ)	86	100	—	80	100	—	dB
Common-Mode	—	560	1000		560	1800	μV/V
Rejection Ratio CMRR	60	65	—	55	65	—	dB
Common-Mode Input VICR +	+0.2	+0.5	—	+0.2	+0.5	—	V
Voltage Range VICR -	-1	-1.3	—		-1.3	—	V
Power Supply Rejection	—	32	320	—	100	1000	μV/V
Ratio PSRR ΔVIO/ΔV	70	90	—	60	80	—	dB
Max Output Voltage VOM +	+0.90	+0.95	—	+0.90	+0.95	—	V
RL = 00 VOM -	-0.85	-0.91	—	-0.85	-0.91	—	V
Supply Current I+	—	350	650	—	350	650	μA
Device Dissipation P_D	—	0.7	1.1	—	0.7	1.1	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	μV/°C

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 10V, V- = -10V, TA = 25°C unless otherwise specified

Characteristic	Limits						Units
	CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.03	4	—	0.03	4	pA
Input Current $\|I_I\|$ *	—	0.05	5	—	0.05	5	pA
Large-Signal Voltage Gain	20K	100K	—	10K	100K	—	V/V
AQL (R_L = 10K Ω)	86	100	—	80	100	—	dB
Common-Mode	—	100	320	—	100	320	μV/V
Rejection Ratio CMRR	70	80	—	70	80	—	dB
Common-Mode Input VICR +	+9.0	+9.3	—	+8.5	+9.3	—	V
Voltage Range VICR -	-10	-10.3	—	-10	-10.3	—	V
Power Supply Rejection	—	32	320	—	32	320	μV/V
Ratio PSRR ΔVIO/ΔV	70	90	—	70	90	—	dB
Max Output Voltage VOM +	+9.7	+9.9	—	+9.7	+9.9	—	V
RL = 00 VOM -	-9.7	-9.85	—	-9.7	-9.85	—	V
Supply Current I+	—	450	1000	—	450	1000	μA
Device Dissipation P_D	—	9	14	—	9	14	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	μV/°C

* The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

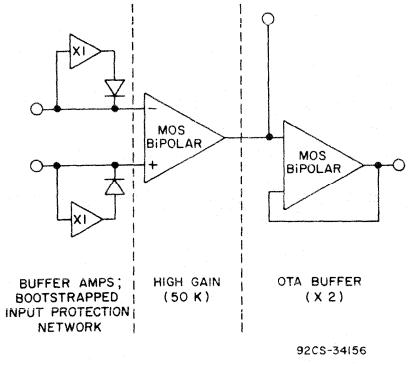


Fig. 1 - Functional diagram for CA3420.

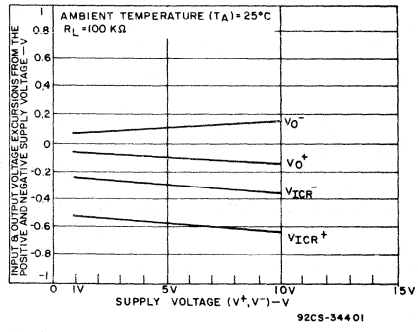


Fig. 2 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

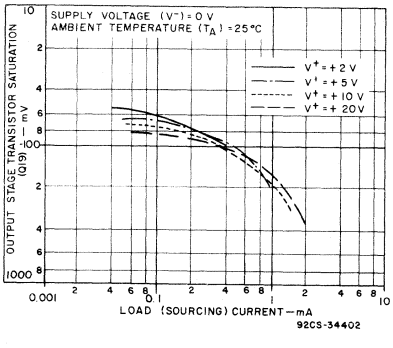


Fig. 3 - Output voltage versus load sourcing current.

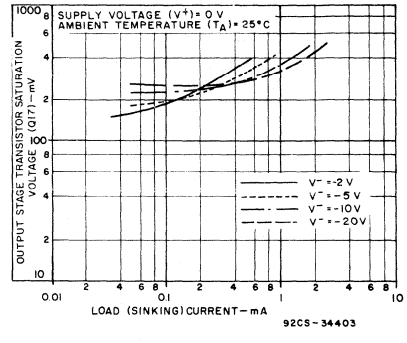


Fig. 4 - Output voltage versus load sinking current.

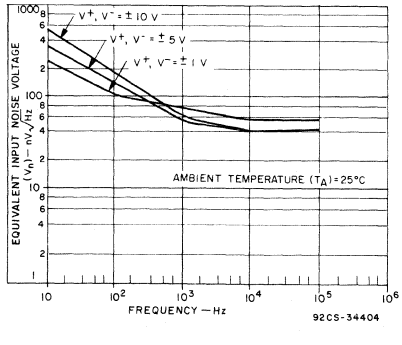


Fig. 5 - Input noise voltage versus frequency.

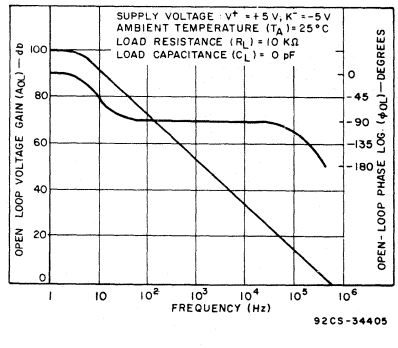


Fig. 6 - Open-loop gain and phase-shift response.

CA3420A, CA3420

Application Circuits

Picoameter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA3420 highly suited for use in a picoameter circuit. With only a single 10K megohm resistor, this circuit covers the range from ±1.5 pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

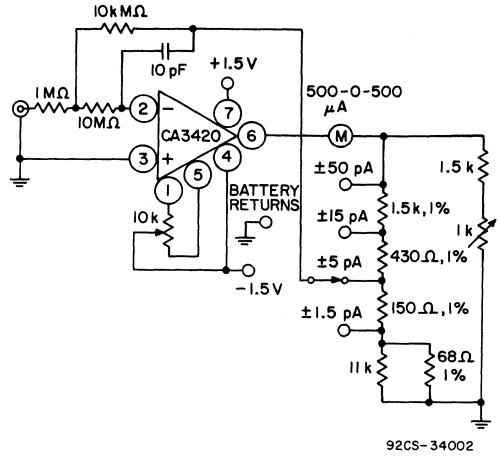


Fig. 7 - Picoameter circuit.

High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high-input-resistance dc voltmeter. Only two 1.5 V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000-megohms) dc voltmeter. Full-scale deflection is ±500 mV, ±150 mV, and ±15 mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300 μA. At full-scale deflection this current rises to 800 μA. Carbon-zinc battery life should be in excess of 1,000 hours.

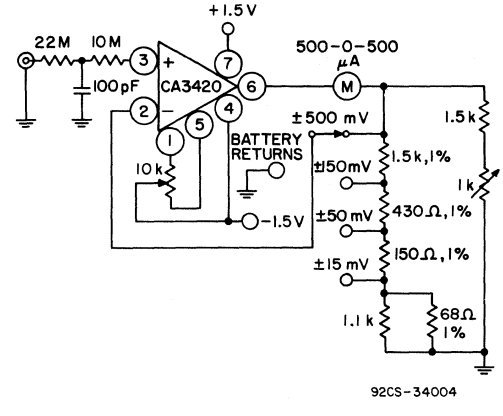
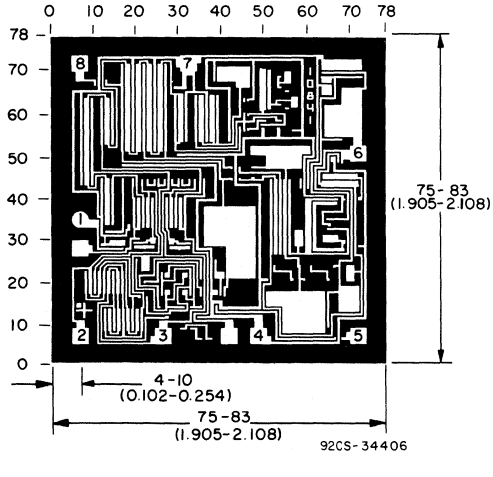


Fig. 8 - High input resistance voltmeter.



The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CA3420H.

Advance Information/
Preliminary Data

CA3440A, CA3440

Nanopower BiMOS Op Amp

Features:
- *300-nW (typ.) standby power at $V^+ = 5$ V*
- *Supply current, BW, slew rate programmable using external resistor*
- *10-pA (typ.) input current*
- *5 to 15-V supply*
- *Output drives typical bipolar-type loads*
- *Low-cost 8-lead Mini-DIP, TO-5*

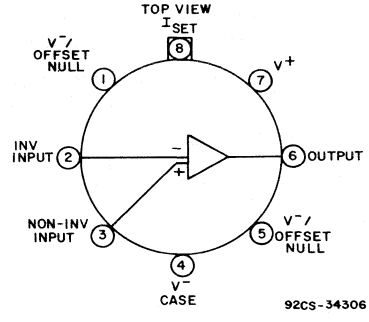
The RCA-CA3440A and CA3440• are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440A and CA3440 BiMOS op amps feature gate-protected PMOS transistors in the input circuit to provide very-high-input impedance and very-low-input current (10 pA). These devices operate at total supply voltages from 5 to 15 volts and can be operated over the temperature range from -55°C to +125°C. Their virtues are programmability and very low standby power consumption (300 nW). These operational amplifiers are internally phase-compensated to achieve stable operation in the unity-gain follower configuration. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative-supply terminals, an important attribute for single-supply applications. The output stage uses MOS complementary source-follower form which permits moderate load driving capability (10 KΩ) at very low total standby currents (50 nA).

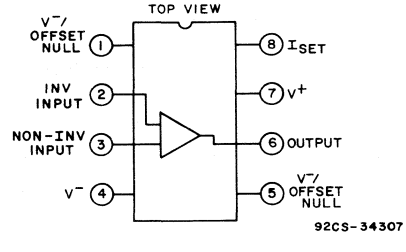
The CA3440A and CA3440 have the same 8-lead terminal pin-out used for "741" and other industry-standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

• Formerly Dev. Type No. TA10590.



S and T Suffixes



E Suffix

Functional diagrams for CA3440A and CA3440.

CA3440A, CA3440

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 25 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±9 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
AT 125°C ..... 418 mW
BELOW 125°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS V^+=+5 V; V^-=-5 V, R_{SET}=10 MΩ; T_A=25°C		CA3440A	CA3440	UNITS
Input Resistance, R_I			2	2	TΩ
Input Capacitance, C_T			3.5	3.5	pF
Ouput Resistance, R_O			450	450	Ω
Equivalent Input Noise Voltage, e_n	f= 1 kHz	R_S=100 Ω	110	110	nV/√Hz
	f=10 kHz		110	110	
Short-Circuit Current Source IOM^+			15	15	mA
To Opposite Supply Sink IOM^-			4.5	4.5	
Gain-Bandwidth Product, f_T			63	63	kHz
Slew Rate, SR			0.03	0.03	V/μs
Transient Response Rise Time, t_r	R_L= 10 kΩ, C_L=100 pF		5.6	5.6	μs
Overshoot			10	10	%

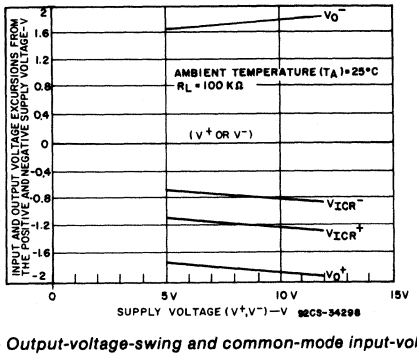


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

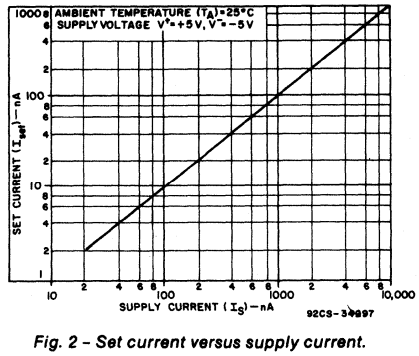


Fig. 2 - Set current versus supply current.

CA3440A, CA3440

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = +5 V, V^- = -5 V, T_A = 25°C Unless Otherwise Specified, R_{SET}=10 MΩ

CHARACTERISTIC	LIMITS						UNITS
	CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current, $\|I_{IO}\|$	—	2.5	20	—	2.5	30	pA
Input Current, $\|I_I\|$	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL	10K	100K	—	10K	100K	—	V/V
(R_L=10 KΩ)	80	100	—	80	100	—	dB
Common-Mode	—	100	320	—	100	320	μV/V
Rejection Ratio, CMRR	70	80	—	70	80	—	dB
Common-Mode Input $VICR^+$	+3.5	+3.7	—	+3.5	+3.7	—	V
Voltage Range, $VICR^-$	−5.0	−5.3	—	−5.0	−5.3	—	V
Power Supply Rejection Ratio, $\Delta VIO/\Delta V$	—	32	320	—	32	320	μV/V
PSRR	70	90	—	70	90	—	dB
Maximum Output Voltage, VOM^+	+3	+3.2	—	+3	+3.2	—	V
VOM^-	−3	−3.2	—	−3	−3.2	—	V
Supply Current, I^+	—	10	17	—	10	17	μA
Device Dissipation, P_D	—	100	170	—	100	170	μW
Input Offset Voltage Temperature Drift, $\Delta VIO/\Delta T$	—	4	—	—	4	—	μV/°C

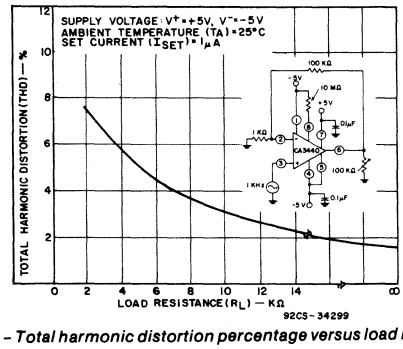


Fig. 3 - Total harmonic distortion percentage versus load resistance.

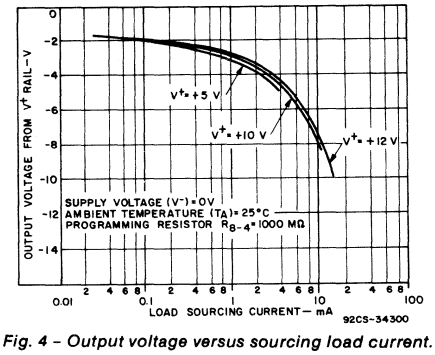


Fig. 4 - Output voltage versus sourcing load current.

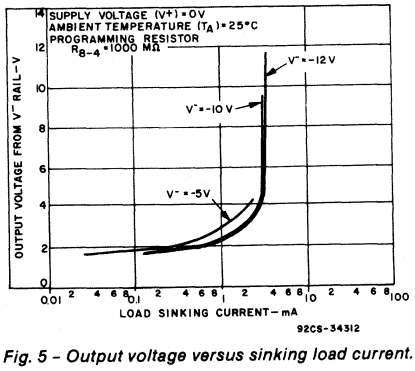


Fig. 5 - Output voltage versus sinking load current.

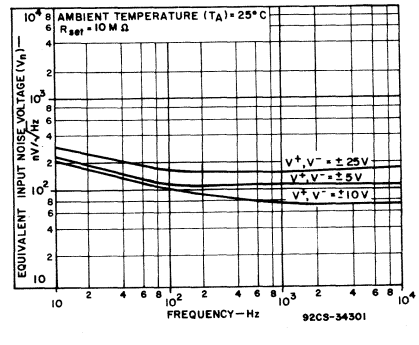


Fig. 6 - Input noise voltage versus frequency.

CA3440A, CA3440

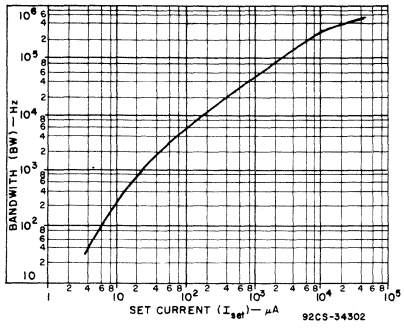


Fig. 7 - Bandwidth versus set current.

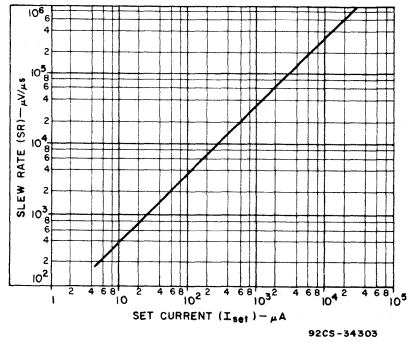


Fig. 8 - Slew rate versus set current.

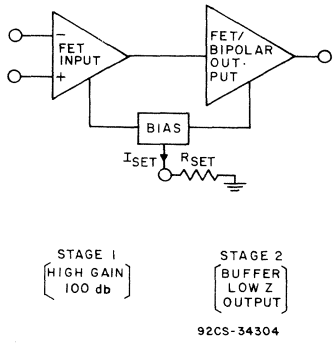


Fig. 9 - Nanopower op amp (supply current programmable using R_{SET}) 1-pA typical input bias current, 4.0 to 15-volt supply.

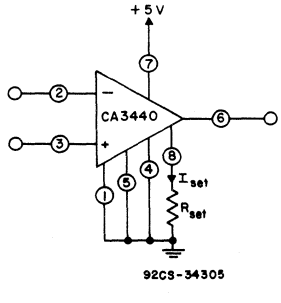


Fig. 10 - Nanopower op amp (usable standby power versus programming resistor R_{SET}).

As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	Standby Power	BW	SR
1 MΩ	250 μW	164 kHz	0.17 V/μs
10 MΩ	25 μW	27 kHz	0.017 V/μs
100 MΩ	2.5 μW	2.6 kHz	.0017 V/μs
1000 MΩ	250 nW	78 Hz	0.00017 V/μs

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or −V via R_{SET}.

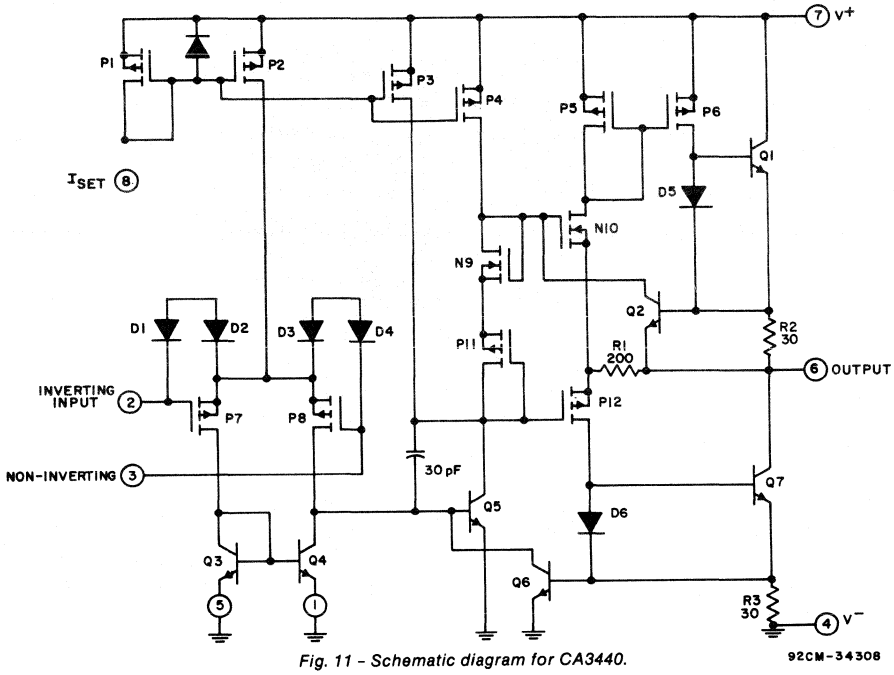


Fig. 11 - Schematic diagram for CA3440.

APPLICATIONS CIRCUITS

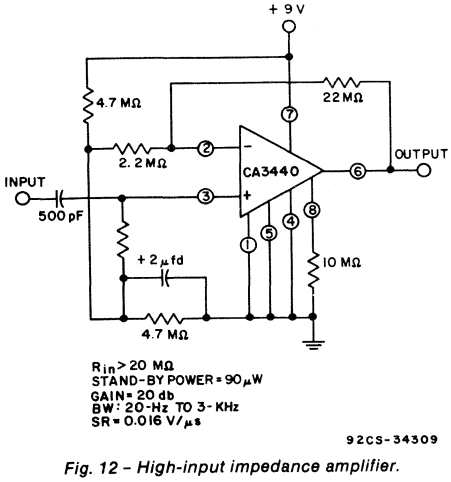


Fig. 12 - High-input impedance amplifier.

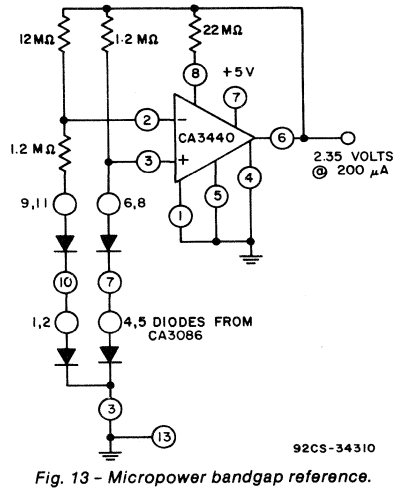
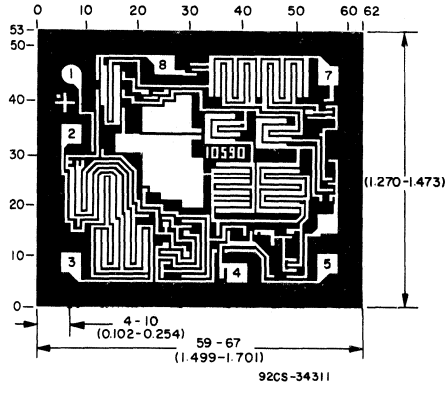


Fig. 13 - Micropower bandgap reference.

CA3440A, CA3440



Dimensions and pad layout for CA3440H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Product Preview

CA3450

Video Line Driver, High-Speed Operational Amplifier

Features:

- *High open loop gain at video frequencies:* A_{OL} = > 40 dB at f = *5 MHz*
- *Power bandwidth of 10 MHz;* $A_{\text{Closed Loop}}$ = *5;* V_O = ± 3.5 V
- *Slew rate of 330 V/μsec* ($A_V \geq 10$) *at full load*
- f_T = *170 MHz;* C_C = *5 pF with a load of 50 ohm || 20 pF || 1 MΩ (scope input)*
- I_{OUT} *into ± 4 V of 75 mA, min.*
- *Offset null terminals*

The RCA CA3450• is a large signal video line driver and high speed operational amplifier capable of driving 50 ohm transmission lines and flash A/Ds. The uncompensated unity gain crossing occurs at 230 MHz without load. It can operate dual or single supplies of ± 8V or 16V, respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75 mA SINK or SOURCE. The CA3450 is capable of driving Flash A/D's in video or high-speed instrumentation (accurate) applications with bandwidth up to 10 MHz with a 20 MHz clocking rate. Offset voltage nulling terminals are also available.

The CA3450 is available in a 16-lead dual-in-line plastic package (E suffix).

Applications:

- *Video line driver*
- *High-frequency unity gain buffer*
- *Pulse amplifier*
- *High-speed comparator*
- *High-frequency oscillator and video amplifiers*
- *Driver for A/Ds in video applications: 10-MHz BW*

•Formerly RCA Developmental Type No. TA11371A.

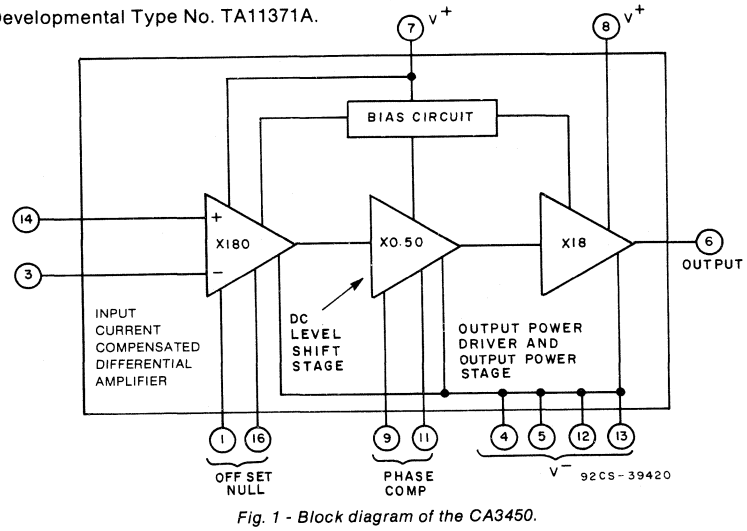


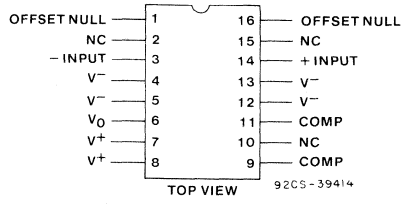
Fig. 1 - Block diagram of the CA3450.

File Number **1732**

CA3450

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTATE (Between V+ and V- Terminal) ..... 14.5 V
DIFFERENTIAL INPUT VOLTAGE ..... ±5 V
DEVICE DISSIPATION:
Up to 55° C ..... 1.5 W
Above 55° C ..... Derate linearly at 16.6 mW/° C
Up to 90° C with heat sink ..... Derate linearly at 25 mW/° C
OUTPUT CURRENT (SINK OR SOURCE) ..... 100 mA
TEMPERATURE RANGE
OPERATING ..... -25° C to 85° C
STORAGE ..... -55° C to 150° C
MAXIMUM JUNCTION TEMPERATURE ..... 150° C
MAXIMUM THERMAL RESISTANCE
Junction to Air (θJ-A) ..... 60° C/W
Junction to Case (θJ-C) ..... 12° C/W
To Pins 4, 5, 12, 13 at seat



TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, C_C = 5 pF, V+, V- = 6 V*

CHARACTERISTIC	CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
STATIC					
Input Offset Voltage, $\|V_{IO}\|$	T_A = 25° C	—	8	15	mV
	T_A = 100° C	—	10	30	
Input Bias Current, $\|I_{IB}\|$	T_A = 25° C	—	100	350	nA
Input Offset Current, $\|I_{IO}\|$	T_A = 25° C	—	50	150	
Open Loop DC Gain, A_{OL}	V_{OUT} = ± 2.5 V; R_L = 50 Ω	60	70	—	dB
Power Supply Rej. Ratio, P_{SRR}	ΔV = ± 1 V	60	70	—	
Common-Mode Rejection Ratio, C_{MRR}	V_{ICR}± = ± 3.5 V	50	60	—	
Common-Mode Input Range, V_{ICR}		±3.5	±3.7	—	V
Supply Current, I		—	30	35	mA

*All tests are performed with ± 6 volts at the terminals of the device.

A 10 ohm, 1/4 watt supply decoupling resistor is shown in all application circuits of this device. The resistor serves two purposes, first it provides a means of decoupling the IC directly at its terminals without introducing additional supply resonance due to parallel connected capacitors. Secondly, it also provides protection for the device in event of a substained short circuit applied directly to the output terminals.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, C_C = 5 pF, V+, V- = 6 V*

CHARACTERISTIC	CONDITION	LIMITS			UNITS
		MIN.	TYP.	MAX.	
DYNAMIC (UNITY GAIN COMPENSATED UNLESS OTHERWISE NOTED), C_C = 5 pF					
Bandwidth (Unity Gain Crossing)	No Load	—	190	—	MHz
A_V = 1	1 MΩ ‖ 20 pF	—	180	—	
(See Fig. 3)	50 Ohms ‖ 20 pF ‖ 1 MΩ	—	170	—	
Bandwidth (Unity Gain Crossing)	No Load	210	230	—	
(Open Loop)	50 Ohms	170	190	—	
A_V = Open Loop	20 pF ‖ 1 MΩ	180	200	—	
C_C = 0	50 Ohms ‖ 20 pF ‖ 1 MΩ	160	180	—	
Bandwidth (Unity Gain Crossing)	No Load	200	210	—	
$A_V \geq 10$ C_C = 0 pF	50 Ω	175	190	—	
$R_{Feedback}$ = 450 Ω	1M ‖ 20 pF	180	195	—	
$R_{Pin\ 3-G}$ = 50 Ω (See Fig. 3)	50 Ω ‖ 1M ‖ 20 pF	170	188	—	
Slew Rate, SR	20 pF ‖ 1 MΩ Load	—	220	—	V/μs
A_V = 1	50 Ω ‖ 20 pF ‖ 1 MΩ Load	—	160	—	
% Over Shoot	20 pF ‖ 1 MΩ ‖ 50 Ω	—	30	—	%
0.1% Setting Time (Inv.)	50 Ω ‖ 20 pF ‖ 1 MΩ	—	35	—	ns
(Non-Inv.)	50 Ω ‖ 20 pF ‖ 1 MΩ	—	50	—	
Power Bandwidth	A_V = 5, V_{op-p} = ± 3.5 V,	—	10	—	MHz
Power Bandwidth = Slew Rate/π ($V_{o(p-p)}$	S_R = 220 V/μs 20 pF ‖ 1 MΩ Load				
	A_V = 5, V_{op-p} = ± 2.5 V, S_R = 160 V/μs	—	10	—	
	50 Ω ‖ 20 pF ‖ 1 MΩ Load				
Slew Rate	20 pF ‖ 1 MΩ	375	420	—	V/μs
A_V = ≥ 10, C_C = 0 pF	50 Ω ‖ 20 pF ‖ 1 MΩ	300	330	—	
% Overshoot	20pF ‖ 1 MΩ	—	20	—	%
	50 Ω ‖ 20 pF ‖ 1 MΩ	—	10	—	
0.1% Setting Time	20 pF ‖ 1 MΩ	—	40	—	ns
Follower Mode	50 Ω ‖ 20 pF ‖ 1 MΩ	—	35	—	
1% Setting Time	20 pF ‖ 1 MΩ	—	35	—	
Follower Mode	50 Ω ‖ 20 pF ‖ 1 MΩ	—	25	—	
$\|I_{OUT}\|$ into +4 V or -4 V		—	75	—	mA
Output Voltage Swing into 75 Ohms	V_{OM}+	+4	+4.1	—	V
DC	V_{OM}-	-4	-4.1	—	

*All tests are performed with ± 6 volts at the terminals of the device.

CA3450

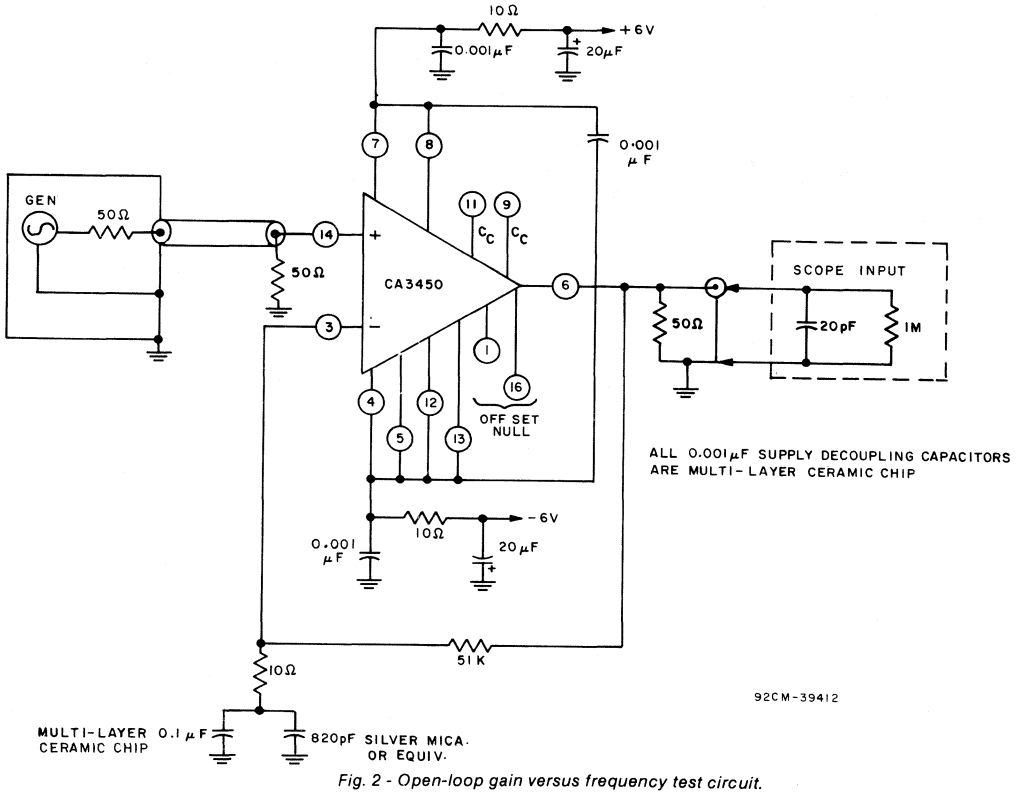


Fig. 2 - Open-loop gain versus frequency test circuit.

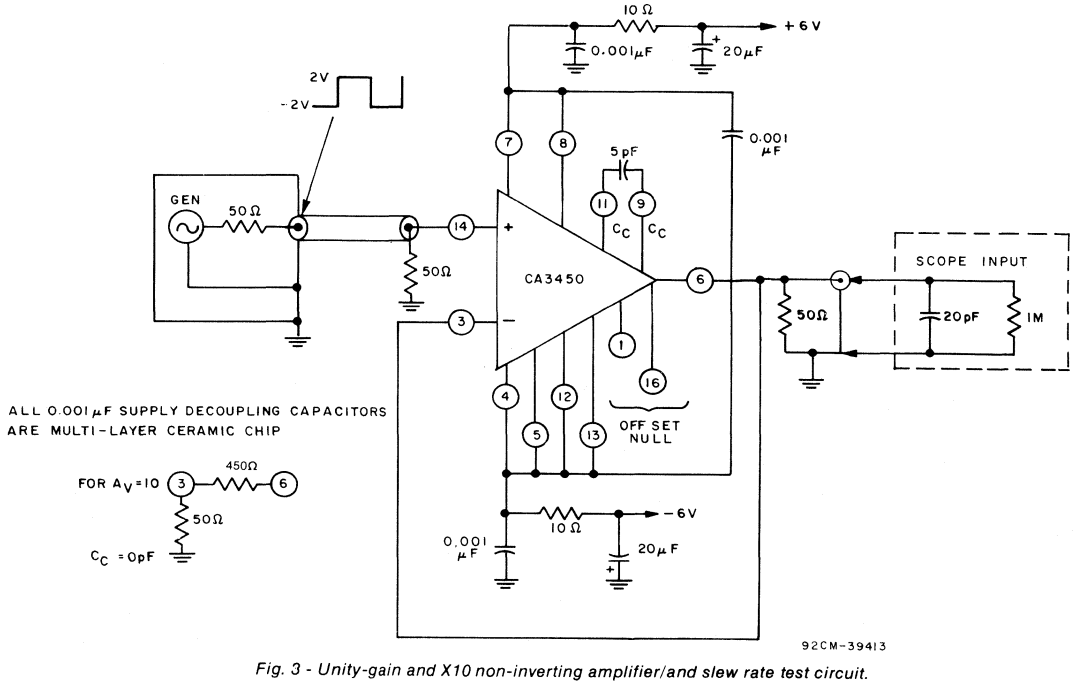


Fig. 3 - Unity-gain and X10 non-inverting amplifier/and slew rate test circuit.

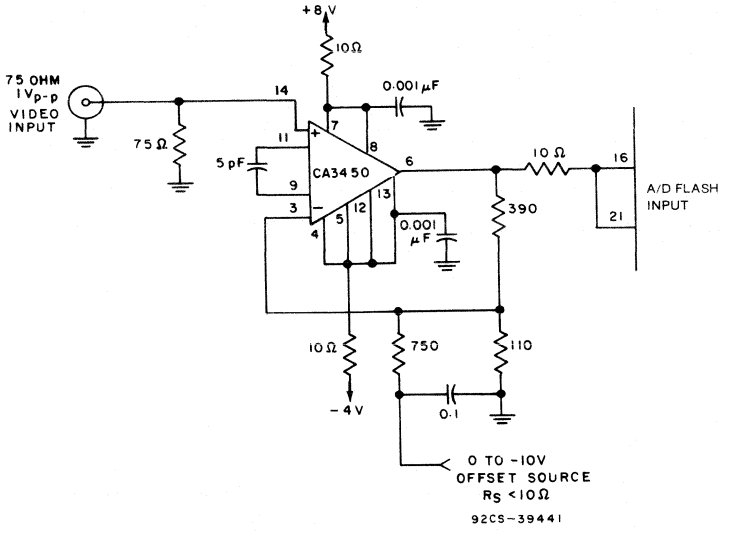
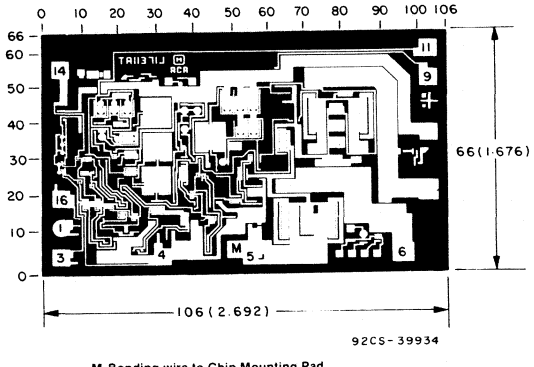


Fig. 4 - Typical high-bandwidth X5 amplifier for driving the CA3318 Flash A/D.



M-Bonding wire to Chip Mounting Pad.
Pins 12 and 13 Connected to Chip Mounting Pad.
No Chip Pads for 2, 10, 12, 13, 15.

Dimensions and pad layout for CA3450H.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Scale graduations are in mils (10^{-3} inch).

CA3493A, CA3493

BiMOS Precision Operational Amplifier

Features:
- *Low V_{IO}: 200 μV max. (CA3493A)*
  500 μV max. (CA3493)
- *Low $\Delta V_{IO}/\Delta T$: 3μV/°C max. (CA3493A)*
  5 μV/°C max. (CA3493)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 150 pA/°C max. (CA3493)*
- *Low $\Delta I_I/\Delta T$: 3.7 nA/°C max. (CA3493)*

The CA3493A and CA3493 are ultra-stable, precision-instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3493A and CA3493 amplifiers are internally phase-compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin-compatible with many industrial types such as 725, 108A, OP-5, OP-7, LM11 and LM714 where positive nulling is employed.

Because of their low offset voltage and low offset voltage-versus-temperature coefficient, the CA3493A and CA3493 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high-gain filters, buffers, strain-gauge bridge amplifiers and precision voltage references.

These op amps are functionally identical. The CA3493A and CA3493 operate from supply voltages of ±3.5 V to ±18 V and have operating temperature ranges of 0°C to +70°C and −25°C to +85°C, respectively.

These types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN S suffix) and 8-lead dual-in-line plastic (Mini-DIP E suffix) packages.

Circuit Description

The block diagram of the CA3493 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3493 amplifier are shown in Figs. 3 and 4, respectively.

Applications:
- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

File Number **1290**

CA3493A, CA3493

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3493A	CA3493	
DC Supply Voltage	±18	±18	V
Differential-Mode Input Voltage	±5	±5	V
Common-Mode DC Input Voltage	(V+ −4), V−	(V+ −4), V−	V
Input Terminal Current	1	1	mA
Device Dissipation			
Without Heat Sink			
Up to 55 °C	630	630	mW
Above 55 °C	Derate Linearly 6.67		mW/°C
Temperature Range	−25 to 85	0 to 70	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	°C

*Short circuit may be applied to ground or to either supply.

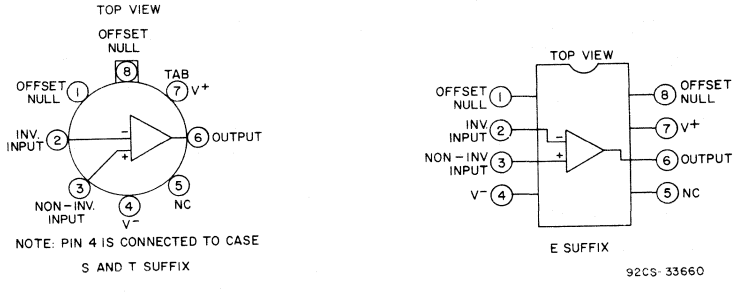


Fig. 1 - Functional diagram of CA3493A and CA3493.

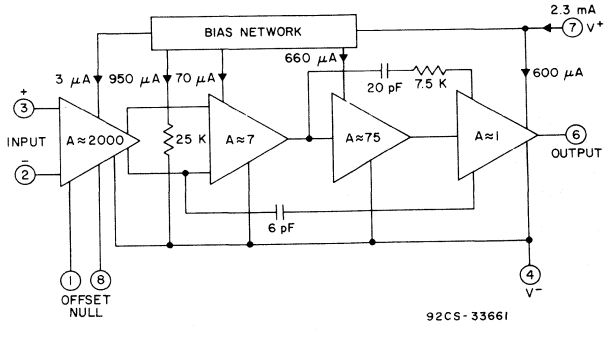


Fig. 2 - Block diagram of CA3493A and CA3493.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

CA3493A, CA3493

ELECTRICAL CHARACTERISTICS at $T_A = 25\,°C$, $V^+ = 15\ V$ and $V^- = 15\ V$ unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, $e_{n\ p\text{-}p}$ (0.1 to 10 Hz)	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n							
$f_O = 10$ Hz	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	—	—	24	—	nV/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	24	—	—	24	—	
$f_O = 100$ kHz	—	22	—	—	22	—	
Input Noise Current, $i_{n\ p\text{-}p}$ (0.1 to 10 Hz)	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n							
$f_O = 10$ Hz	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	—	—	0.75	—	pA/$\sqrt{\text{Hz}}$
$f_O = 10$ kHz	—	0.72	—	—	0.72	—	
$f_O = 100$ kHz	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	110	115	—	100	110	—	dB
		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$	100	130	—	100	130	—	dB
		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)							
$R_L \geq 1$ KΩ	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ f = 1 kHz	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} = 20$ mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−25	—	85	0	—	70	°C

CA3493A, CA3493

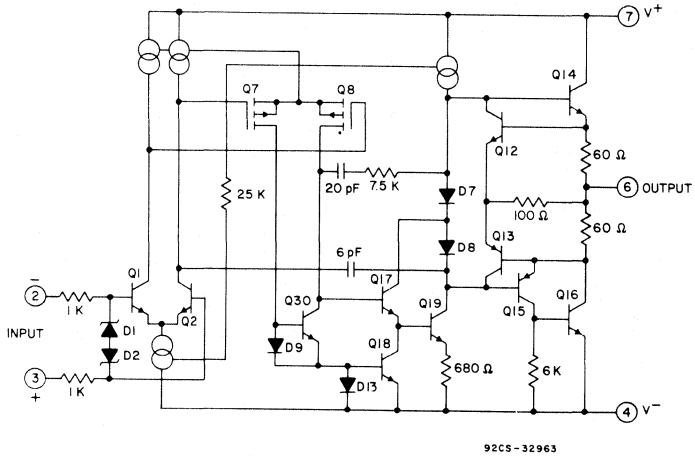


Fig. 3 - CA3493 simplified schematic diagram.

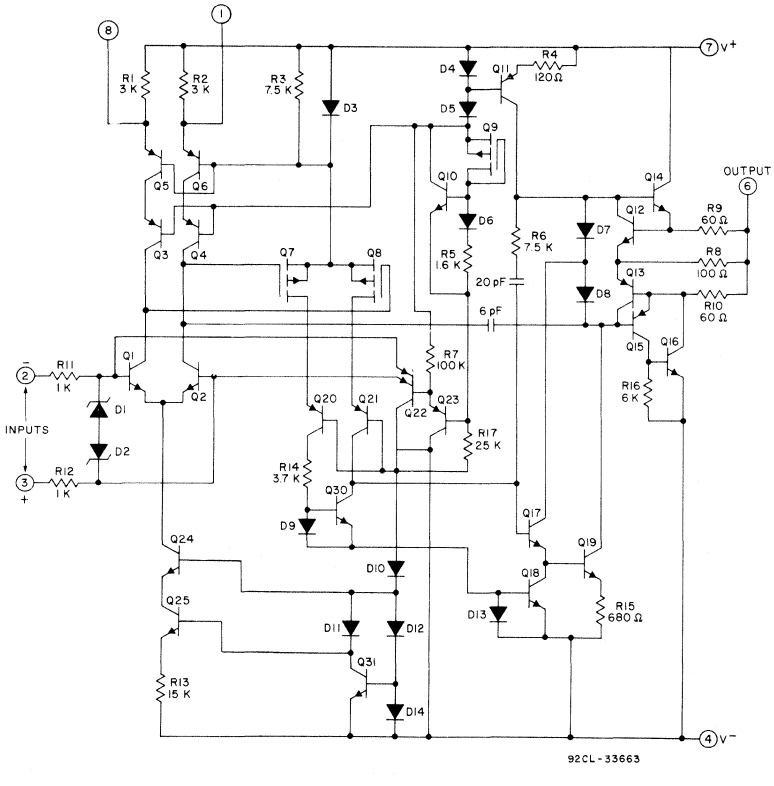


Fig. 4 - Schematic diagram of CA3493A and CA3493.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3493 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

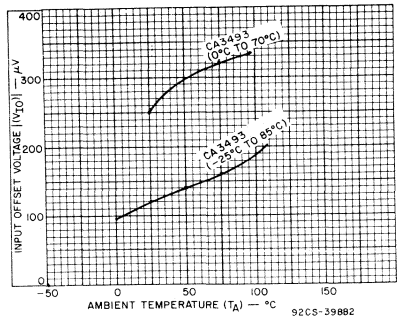


Fig. 5 - Typical input offset-voltage temperature characteristic for CA3493A and CA3493.

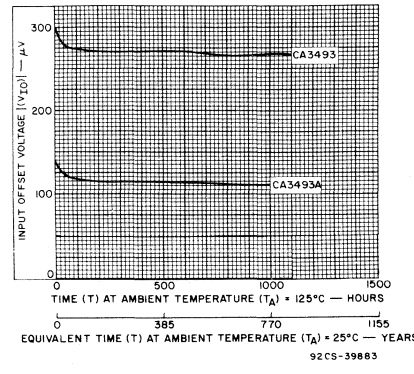


Fig. 6 — Input offset voltage vs. time.

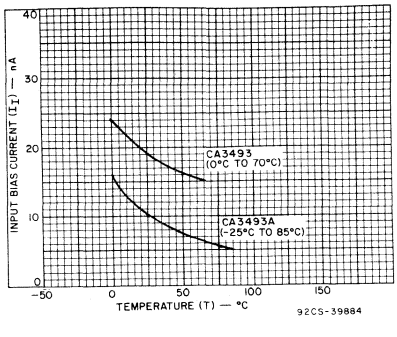


Fig. 7 — Typical input bias current vs. temperature

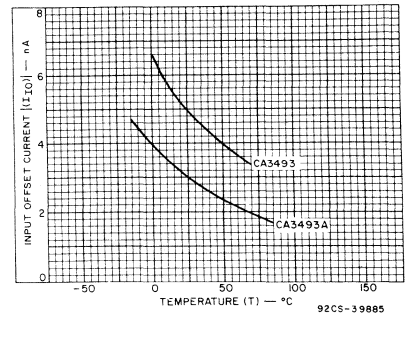


Fig. 8 — Typical input offset current vs. temperature.

CA3493A, CA3493

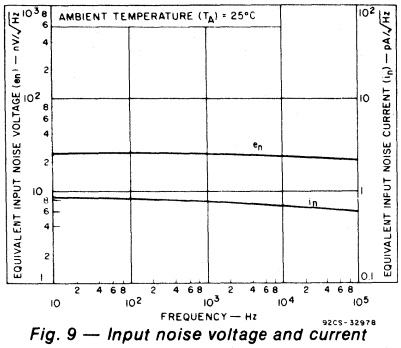


Fig. 9 — Input noise voltage and current density vs. frequency.

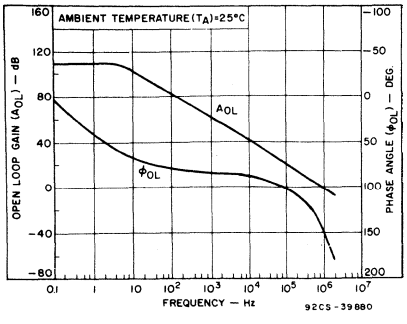


Fig. 11 - Open-loop gain and phase-shift response for CA3493.

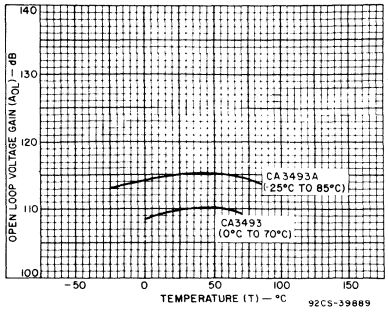


Fig. 13 - Open-loop gain vs. temperature for CA3493A and CA3493.

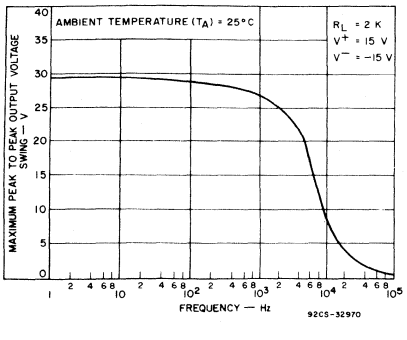


Fig. 14 — Maximum undistorted output voltage vs. frequency.

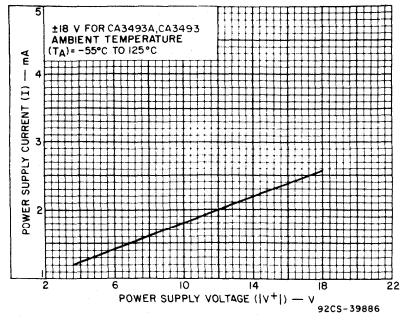


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

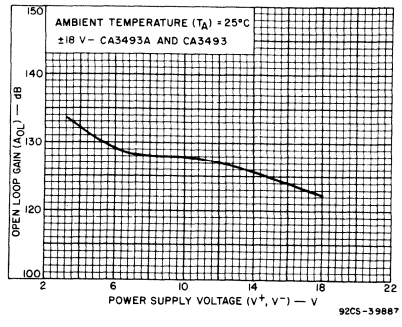


Fig. 12 — Open-loop gain vs. power-supply voltage.

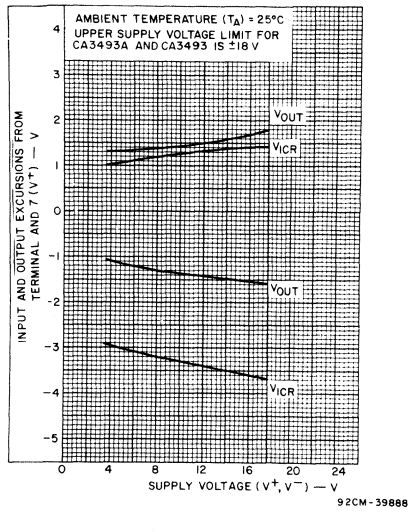


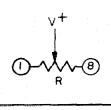
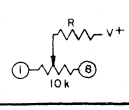
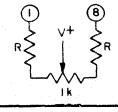
Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 8, with its wiper returned to V^+, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3493 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V^- supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3493A CA3493	10K 10K	50K 20K	10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

92CS-33672

Test Circuits

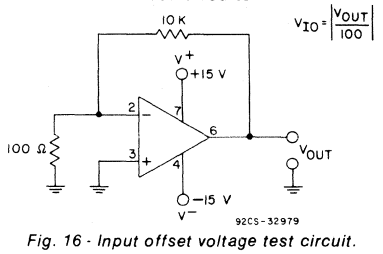
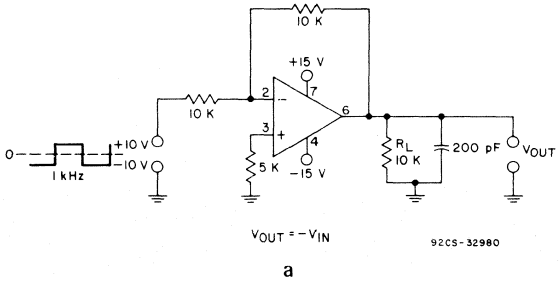
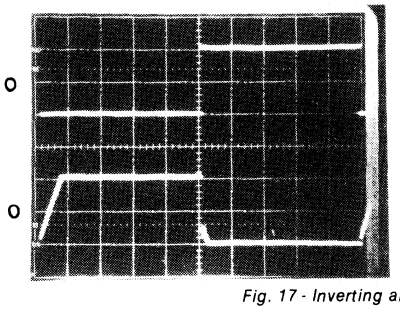


Fig. 16 - Input offset voltage test circuit.



a



b

TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT. : $\frac{10\,V}{DIV}$

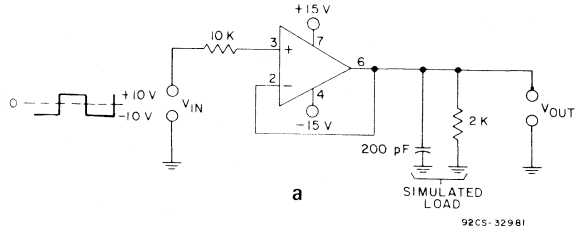
HOR. : $\frac{.1\,ms}{DIV}$

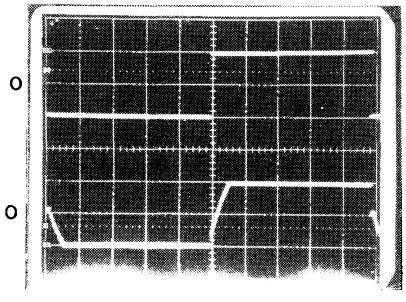
$V^+ = 15\,V$
$V^- = -15\,V$
$R_L = 10\,K$

92CS-32989

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.

CA3493A, CA3493





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\ V}{DIV}$

HOR : $\frac{.1\ ms}{DIV}$

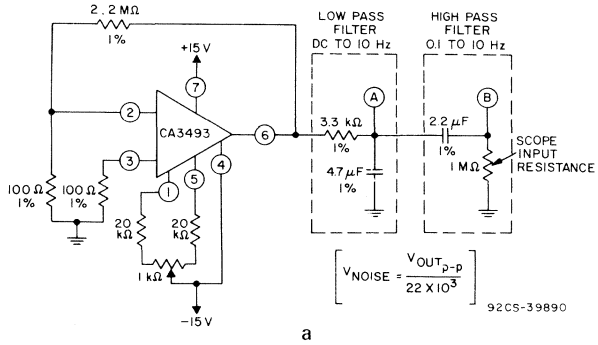
$V+ = 15\ V$

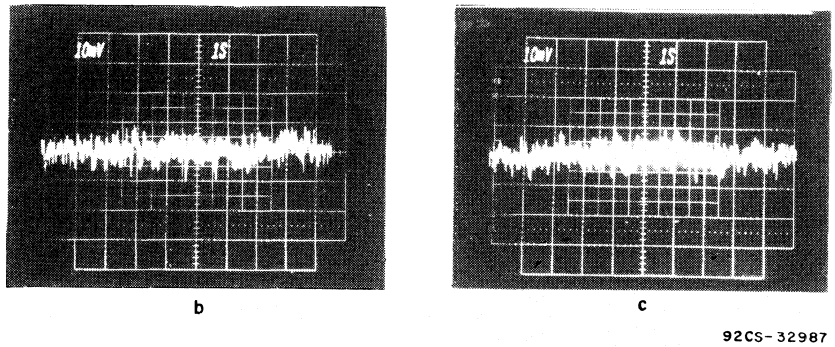
$V^- = 15\ V$

$R_L = 2K$

92CS-32988

Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.

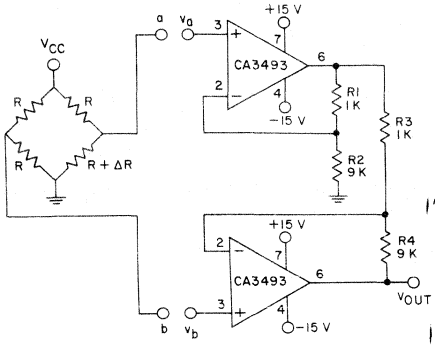




92CS-32987

Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -v_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + v_b\left(\frac{R4}{R3}+1\right)$$

FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

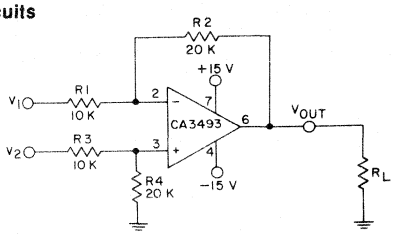
$$V_{OUT} = v_b - v_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{v_b - v_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (v_b - v_a)(10)$

92CS-39891

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = v_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - v_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

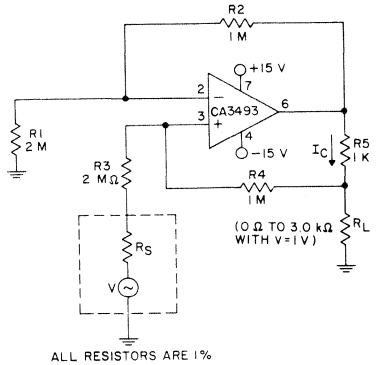
FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

92CS-39894

Fig. 21 - Differential amplifier (simple subtractor) using CA3493.



ALL RESISTORS ARE 1%

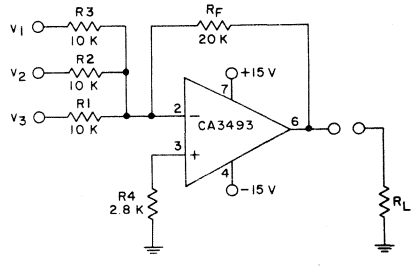
IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH v = 1 V

$$I_L = \frac{v}{R3}\frac{R4}{R5} = \frac{v}{(2\,M)(1K)} = \frac{v}{2\,K} = 500\ \mu A$$

92CS-39892

Fig. 22 - Using CA3493 as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}v_1 + \frac{R_F}{R2}v_2 + \frac{R_F}{R3}v_3\right)$$

$$V_{OUT} = -(2v_1 + 2v_2 + 2v_3)$$

92CS-39893

ALL RESISTANCE VALUES ARE IN OHMS

Fig. 23 - Typical summing amplifier application.

CA3493A, CA3493

The CA3493 is an excellent choice for use with themocouples. In Fig. 24, the CA3493 amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

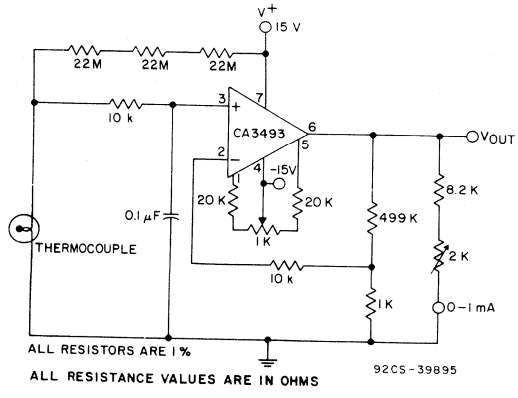


Fig. 24 - The CA3493 used in a thermocouple circuit.

Product Preview

CA5422

Dual BiMOS Operational Amplifier

For Microprocessor Applications and Other
Low-Supply Voltage and Low-Input Current Applications

Features:

- *Below 5-V supply at 400 μA supply current*
- *1-pA (typ.) input current*
- *Rail-to-rail output swing*
- *Easily feasible for use as a (1) dual op amp; (2) dual comparator; and (3) op amp and comparator*
- *Ideally suited for CMOS and QMOS applications*
- *+5-V characteristics for microprocessor applications*
- *±1 V, ±10 V operation feasible*

The RCA CA5422• is an integrated circuit operational amplifier that combines PMOS transistors and bipolar transistors on a single monolithic chip. The CA5422 BiMOS operational amplifier features gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents. The CA5422 is a dual monolithic integrated circuit in which each amplifier has unique characteristics. This device is capable of operating at a total supply voltage from 2 to 20 volts, either single or dual supply. Characteristics are available for +5-V microprocessor applications.

An internal network on Amplifier A features a unique guard-banding technique for reducing the doubling of leakage current for every 10° C increase in temperature up to 85° C.

Bootstrapping terminals provided on Amplifier A null the input currents on either/both input terminal(s). Access terminals are available for connections to an external capacitor for additional frequency compensation. The input offset voltage can also be reduced on Amplifier A through external nulling terminals. The PMOS input stages for the first amplifier result in common-mode input voltage capability from 0.45 volt below the negative supply terminal, to approximately V+ -0.5 V, an important attribute for single-supply applications. The output stage is an OTA-type amplifier that can swing essentially from rail-to-rail with an infinite load resistor.

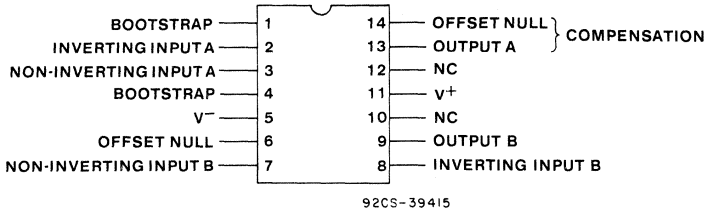
Applications

- *pH probe amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable equipment*
- *Inaccessible field equipment*
- *Battery-dependent equipment (medical and military)*
- *Humidity sensors*
- *Ionization chambers*
- *Piezo-electric pre-amplifiers (charge amplifiers)*
- *Battery monitoring systems*
- *Photodiode amplifiers (IR)*
- *Signal-processing amplifiers for microprocessor applications*

The second amplifier provides an overall gain of 300 with inputs compatible with other BiMOS operational amplifiers. Its output can swing to within 0.3 V (typ.) from the positive rail and down to 3 mV (typ.) from the negative rail with a 2K load resistor. The output driving current of 2 mA (min.) is provided by using non-linear current mirrors.

The CA5422 is available in a 16-lead dual-in-line plastic package (E suffix).

•Formerly RCA Developmental Type No. 11214.



92CS-39415

TERMINAL ASSIGNMENT

File Number **1731**

CA5422

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

DC SUPPLY VOLTAGE (BETWEEN V^+ and V^- TERMINALS) ..... 22 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±15 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
  WITHOUT HEAT SINK -
    Up to 55°C ..... 630 mW
    Above 55°C ..... Derate linearly 6.67 mW/°C
  WITH HEAT SINK -
    Up to 110°C ..... 630 mW
    Above 110°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
  OPERATING (ALL TYPES) ..... -55 to +125°C
  STORAGE (ALL TYPES) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... Indefinite
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

*Short circuit may be applied to ground or to either supply.

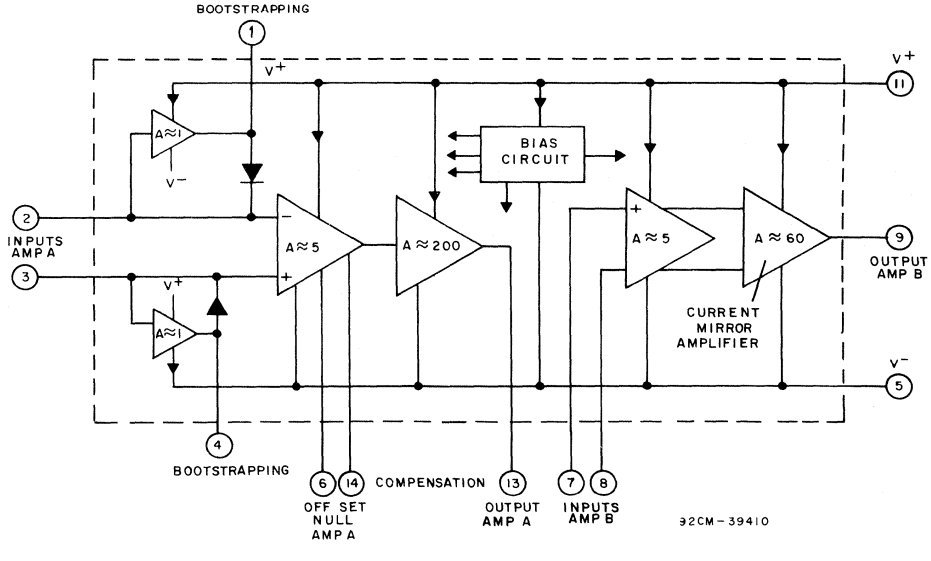


Fig. 1 - Block diagram of the CA5422.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At $V^+ = 5$, $V^- = 0$, $T_A = 25°C$ Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		AMPLIFIER A			AMPLIFIER B			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$\|V_{IO}\|$	—	1.8	10	—	2.8	10	mV
Input Offset Current	$\|I_O\|$	—	0.02	4*	—	0.3	15	pA
Input Bias Current	$\|I_{IB}\|$	—	0.16	5*	—	0.4	25	pA
Large-Signal Voltage Gain $V_O = 0.5$ V to 3.5 V, $R_L = \infty$	A_{OL}	60	75	—	50	58	—	dB
Common-Mode Rejection Ratio $V_{ICR_A} = 0$ to 4 V, $V_{ICR_B} = 0$ to 3 V	CMRR	60	75	—	45	60	—	dB
Common-Mode Input Voltage Range	V_{ICR}^+	4	4.5	—	3	3.5	—	V
	V_{ICR}^-	0	-0.5	—	0	-0.5	—	
Power Supply Rejection Ratio $\Delta V_{IO}/\Delta V$, $\Delta V = 2$	PSRR	70	85	—	50	60	—	dB
Device Dissipation	P_D	—	9	—	—	—	—	mW
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	—	20	—	—	20	—	μV/°C
Bootstrap Current to Null Input Current		—	20	—	—	—	—	μA
I_{OUT}^+ to Gnd		30	50	—	2	3	—	μA
I_{OUT}^- to +5 V		1.5	3.6	—	2	2.5	—	mA
Gain-Bandwidth Product	f_t	—	160	—	—	1	—	kHz
Slew Rate	SR	—	0.25	—	—	1	—	V/μs
Maximum Output Voltage Swing	V_{OUT}							
$R_L = \infty$	V_{OM}^+	4.8	4.9	—	4.8	4.95	—	V
	V_{OM}^-	—	-0.04	-0.1	—	-0.003	-0.01	
$R_L = 10$ kΩ	V_{OM}^+	0.4	0.5	—	4.8	4.9	—	
	V_{OM}^-	—	-0.03	-0.1	—	-0.003	-0.01	
$R_L = 2$ kΩ	V_{OM}^+	0.075	0.1	—	4.45	4.7	—	
	V_{OM}^-	—	-0.035	-0.09	—	-0.003	-0.01	
Supply Current $V_O = 0.2$ V to 4.9 V	I^+	—	400	700	—	400	700	μA

*This specification is limited by high-speed production test equipment rather than the device.

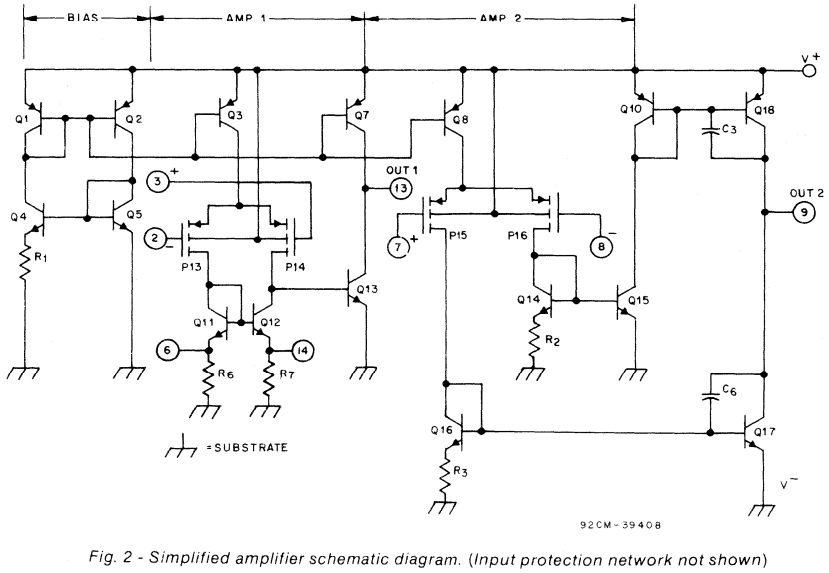


Fig. 2 - Simplified amplifier schematic diagram. (Input protection network not shown)

CA5422

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 1, V^- = 1, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		AMPLIFIER A			AMPLIFIER B			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$\|V_{IO}\|$	—	2	10	—	5	15	mV
Input Offset Current	$\|I_O\|$	—	0.02	4*	—	0.3	10	pA
Input Bias Current	$\|I_{IB}\|$	—	0.2	5*	—	0.5	15	pA
Large-Signal Voltage Gain	A_{OL}		TBE			TBE		
Common-Mode Rejection Ratio V_{CM} = -0.2 to -1 V	CMRR	65	70	—	TBE	TBE	—	dB
Common-Mode Input Voltage Range	V_{ICR}^+	0.2	0.5	—	TBE	TBE	—	V
	V_{ICR}^-	-1	-1.3	—	TBE	TBE	—	
Power Supply Rejection Ratio ΔV^+ = 1 V, ΔV^- = 1 V	PSRR	60	75	—	50	60	—	dB
Output Current								
Source, V_O = -1 V	I_{SOURCE}		TBE			TBE		
Sink, V_O = +1 V	I_{SINK}		TBE			TBE		
Maximum Output Voltage Swing	V_{OUT}							
R_L = ∞	V_{OM}^+		TBE		0.9	0.95	—	V
	V_{OM}^-				-0.85	-0.91	—	
R_L =	V_{OM}^+		TBE			TBE		
	V_{OM}^-							
R_L =	V_{OM}^+		TBE			TBE		
	V_{OM}^-							
Supply Current	I^+	—	300	700	—	300	700	μA

*This specification is limited by high-speed production test equipment rather than the device.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 10, V^- = 10, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		AMPLIFIER A			AMPLIFIER B			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_O = 1 V	$\|V_{IO}\|$	—	3.5	15	—	5	20	mV
Input Offset Current	$\|I_O\|$	—	0.3	4*	—	0.7	10	pA
Input Bias Current	$\|I_{IB}\|$	—	0.5	5*	—	2	15	pA
Large-Signal Voltage Gain	A_{OL}							
V_O = ±7 V, R_L = ∞		70	75	—	60	63	—	dB
R_L = 10 kΩ		60	70	—	35	40	—	
Common-Mode Rejection Ratio	CMRR							
V_{CM} = -10 V to +5 V		75	80	—	60	70	—	dB
V_{CM} = -10 V to +9 V		60	70	—	TBE	TBE	—	
Common-Mode Input Voltage Range	V_{ICR}^+	9	9.3	—	TBE	TBE	—	V
	V_{ICR}^-	-10	-10.3	—	TBE	TBE	—	
Power Supply Rejection Ratio ΔV^+ = 1 V, ΔV^- = 1 V	PSRR	60	75	—	60	70	—	dB
Output Current								
Source, V_O = -10 V	I_{SOURCE}	90	120	—	2000	5000	—	μA
Sink, V_O = +10 V	I_{SINK}	2000	5000	—	2000	4000	—	
Maximum Output Voltage Swing	V_{OUT}							
R_L = ∞	V_{OM}^+	9.7	9.9	—	9.8	9.85	—	
	V_{OM}^-	-9.9	-10	—	-9.9	-9.9	—	
R_L = 10 kΩ	V_{OM}^+	0.5	0.6	—	9.8	9.85	—	V
	V_{OM}^-	-9.5	-9.95	—	-9.9	-9.9	—	
R_L = 2 kΩ	V_{OM}^+	—	—	—	8	8.5	—	
	V_{OM}^-	-9	-9.5	—	-8	-9.5	—	
Supply Current	I^+	—	700	2000	—	700	2000	μA

*This specification is limited by high-speed production test equipment rather than the device.

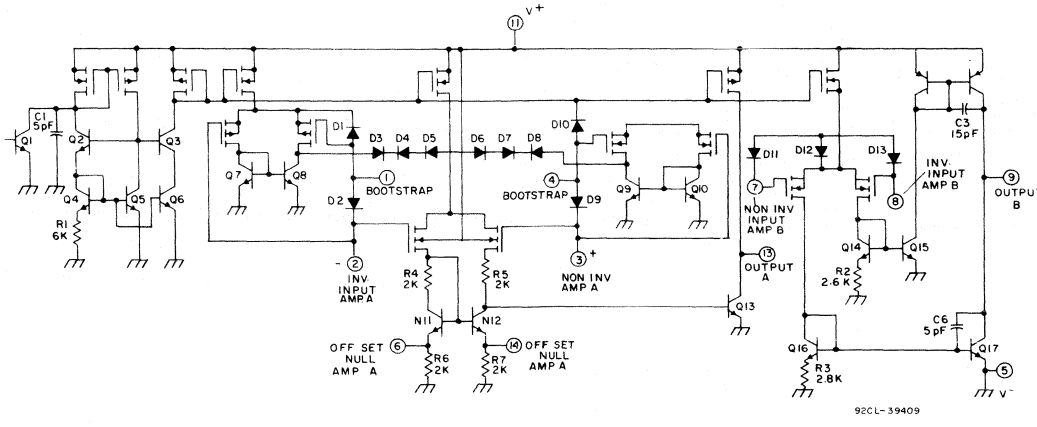


Fig. 3 - Complete schematic diagram of the amplifier.

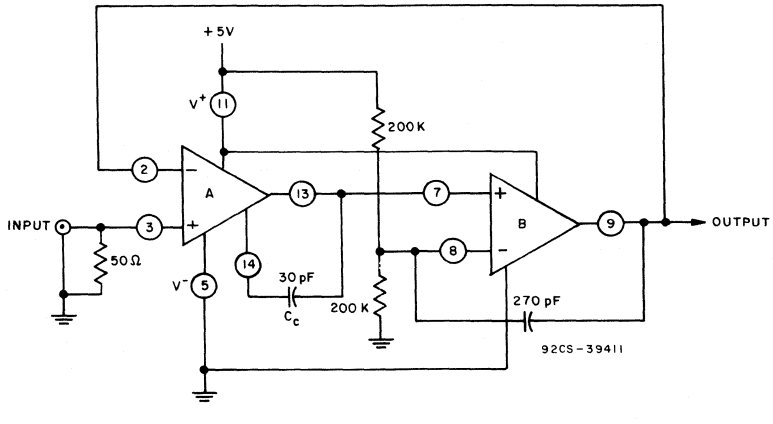


Fig. 4 - The CA5422 large and small-signal response circuit for the combined Amplifiers A and B.

CA6078A, CA6741

Operational Amplifiers

CA6078AT – Micropower Type
CA6741T – General-Purpose Type

For Applications where Low Noise
(Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise:
device rejected if any noise burst exceeds 20 μV (peak),
referred to input over a 30-second time period.

RCA-CA6078AT and CA6741T* are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

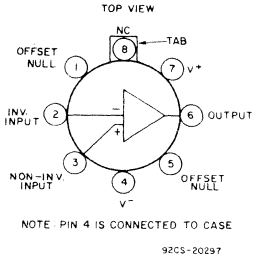
These low-noise versions of the CA3078AT and CA3741T are a result of improved processing developments and rigid burst-noise inspection criteria. A highly selective test circuit (See Fig. 2) assures that each type meets the rigid low-noise standards shown in the data section. This low-burst-noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short-circuit protection, latch-free operation, wide common-mode and differential-mode signal ranges, and low-offset nulling capability.

For detailed data, characteristics curves, schematic diagram dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini–Dip) package. For terminal arrangements, see page 4.

*Formerly Dev. No. TA5807X and TA6029 respectively.



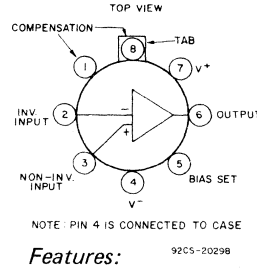
CA6741T

Applications:

- **Low-noise AC amplifier**
- **Narrow-band or band-pass filter**
- **Integrator or differentiator**
- **DC amplifier**
- **Summing amplifier**

Features:

- **Internal phase compensation**
- **Input bias current: 500 nA max.**
- **Input offset current: 200 nA max.**
- **Open-loop voltage gain: 50,000 (94 dB) min.**
- **Input offset voltage: 5 mV max.**



CA6078AT

Applications:

- **Portable electronics**
- **Medical electronics**
- **DC amplifier**
- **Narrow-band or band-pass filter**
- **Integrator or differentiator**
- **Instrumentation**
- **Telemetry**
- **Summing amplifier**

Features:

- **Open-loop voltage gain: 40,000 (92 dB) min.**
- **Input offset voltage:3.5 mV max.**
- **Operates with low total supply voltage: 1.5 V min. (± 0.75 V)**
- **Low quiescent operating current: adjustable for application optimization**
- **Input bias current: adjustable to below 1 nA**

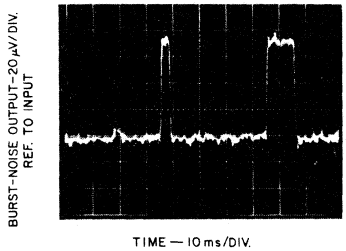
File Number **630**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

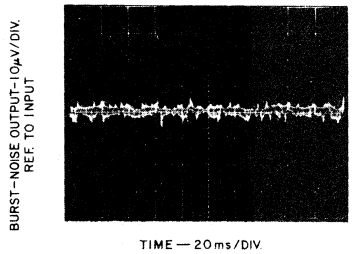
	CA6741T	CA6078AT
DC Supply Voltage (between V^+ and V^- terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V^+ to V^-
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	—
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.

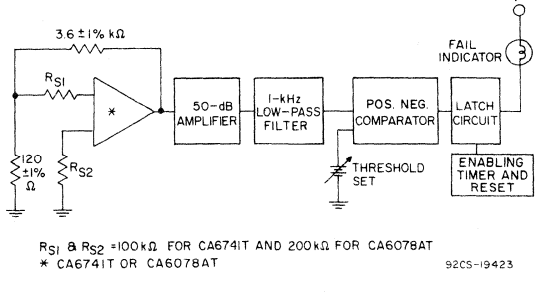


Fig.2—Block diagram of burst-noise "popcorn" test equipment.

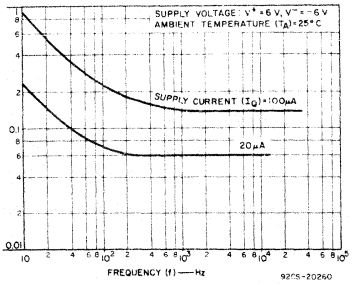
CA6078A, CA6741

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz; $R_{S1} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15$ V	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz; $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10$ V	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\ \Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\ \Omega$	±12	±14	–	V
		$R_L \geq 2\ k\ \Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA



g.3—I_N vs. Frequency for CA6078AT.

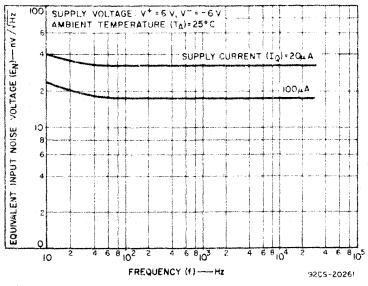


Fig.4—E_N vs. Frequency for CA6078AT.

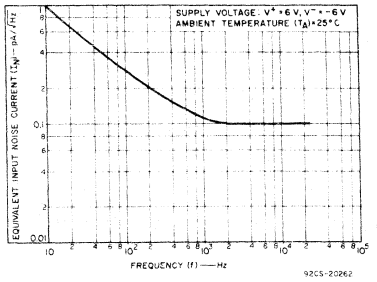
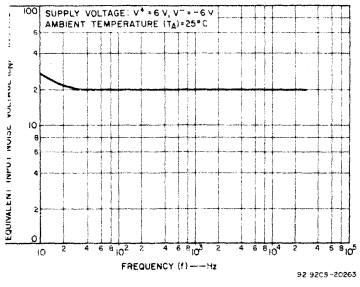


Fig.5—I_N vs. Frequency for CA6741T.



ig.6—E_N vs. Frequency for CA6741T.

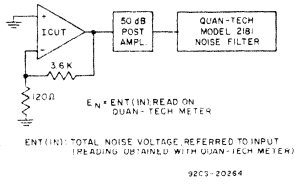


Fig.7—Test block diagram for E_N.

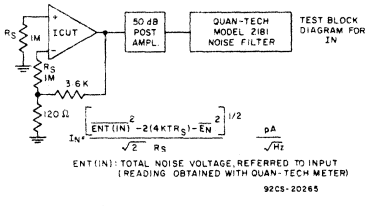


Fig.8—Test block diagram for I_N.

Voltage Comparators

Voltage Comparator Circuits — Technical Data

CA139, CA139A, CA239, CA239A
CA339, CA339A, LM339*, LM339A*

Quad Voltage Comparators

For Industrial, Commerical, and Military Applications

Features:

- *Operation from single or dual supplies*
- *Common-mode input-voltage range to ground*
- *Output voltage compatible with TTL, DTL, ECL, MOS and CMOS*
- *Differential input-voltage range equal to the supply voltage*
- *Maximum input-offset voltage (V_{IO}):*
  CA139A, CA239A, CA339A - 2 mV
  CA139, CA239, CA339 - 5 mV
- *Replacement for industry types 139, 239, 339, 139A, 239A, and 339A*

The RCA-CA139, CA239, CA339, CA139A, CA239A, and CA339A types consist of four independent single- or dual-supply voltage comparators on a single monolithic substrate. The common-mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counter parts CA139, CA239, and CA339 plus an even lower input-offset-voltage characteristic. These devices are supplied in a 14-lead dual-in-line plastic package (E suffix) and in a 14-lead dual-in-line hermetic (frit-seal) ceramic package (F suffix). The CA339 is also available in chip form (H suffix).

Applications:

- *Square-wave generators*
- *Time-delay generators*
- *Pulse generators*
- *Multivibrators*
- *High-voltage digital logic gates*
- *A/D converters*
- *MOS clock timers*

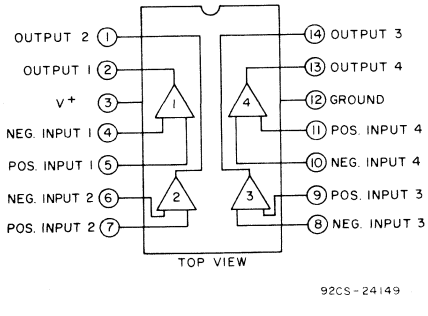


Fig. 1 - Functional diagram.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **795**

CA139, CA139A, CA239, CA239A
CA339, CA339A, LM339, LM339A

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$:*

DC SUPPLY VOLTAGE	36 V or ±18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	−0.3 V to +36 V
INPUT CURRENT ($V_I < -0.3$ V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲	
(Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/^{o}C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125^{o}C
Storage	−65 to +150^{o}C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265^{o}C

* Inputs must not go more negative than −0.3 V.

▲ Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximately 20 mA.

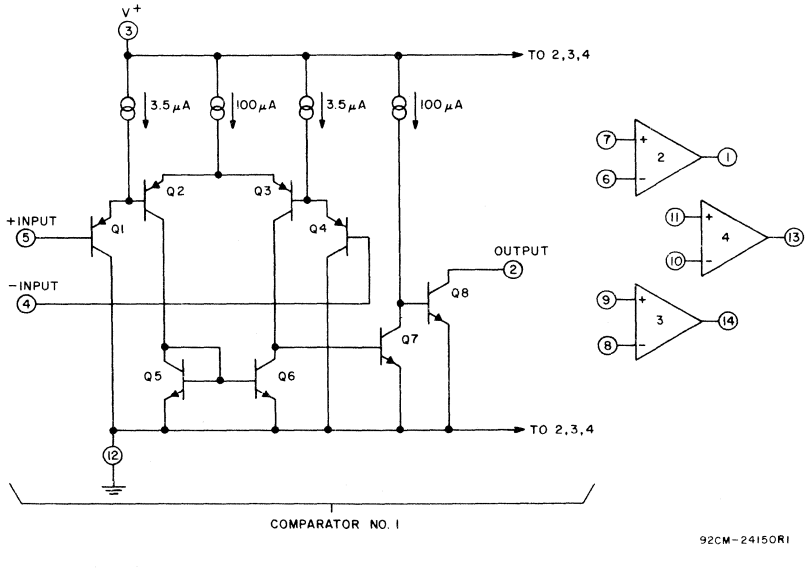


Fig. 2—Schematic diagram.

CA139, CA139A, CA239, CA239A CA339, CA339A, LM339, LM339A

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	$V^+ = 5$ V, Unless otherwise indicated		CA139			CA139A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point $V \cong 1.4$ V	V_{REF} = 1.4 V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ⩾0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leqslant$ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
		Note 1	–	–	100	–	–	100	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
		Note 1	–	–	300	–	–	300	
Total Supply Current (I^+)	$R_L = \infty$ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geqslant 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geqslant 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geqslant 1$ V, $V_I^+ = 0$, $V_O \leqslant +1.5$ V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geqslant 15$ kΩ, $V^+ = 15$ V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 50 V, R_L = 5.1 kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	V_{RL} = 5 V, R_L = 5.1 kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.

CA139 / CA139A (−55 to +125°C) | CA239 / CA239A (−25 to +85°C) | CA339 / CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) − 1.5 V, but either or both inputs can go to +30 V without damage.

CA139, CA139A, CA239, CA239A
CA339, CA339A, LM339, LM339A

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V^+ = 5$ V Unless otherwise indicated		LIMITS CA239, CA339 Min.	CA239, CA339 Typ.	CA239, CA339 Max.	CA239A, CA339A Min.	CA239A, CA339A Typ.	CA239A, CA339A Max.	UNITS
Input Offset Voltage (V_{IO}) At Output Switch Point $V \cong 1.4$ V	V_{REF} = 1.4 V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ≥0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leq$ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	5	50	–	5	50	nA
		Note 1	–	–	150	–	–	150	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	250	–	25	250	nA
		Note 1	–	–	400	–	–	400	
Total Supply Current (I^+)	$R_L = \infty$ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geq 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geq 1$ V, $V_I^+ = 0$, $V_O \leq +1.5$ V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geq 15$ kΩ, $V^+ = 15$ V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139 / CA139A (−55 to +125°C) CA239 / CA239A (−25 to +85°C) CA339 / CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) − 1.5 V, but either or both inputs can go to +30 V without damage.

CA139, CA139A, CA239, CA239A
CA339, CA339A, LM339, LM339A

TYPICAL CHARACTERISTICS

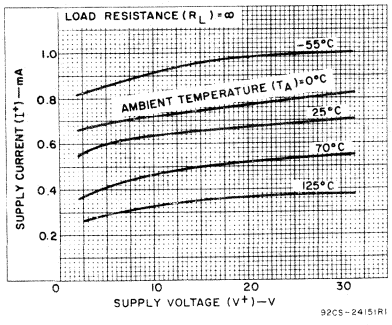


Fig. 3—Supply current vs. supply voltage.

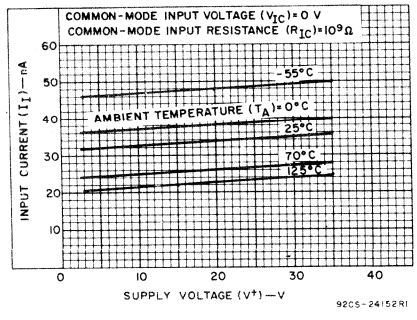


Fig. 4—Input current vs. supply voltage.

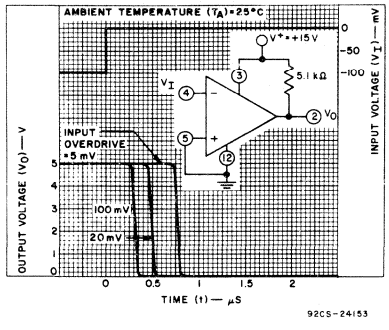


Fig. 5—Response time for various input overdrives—negative transition.

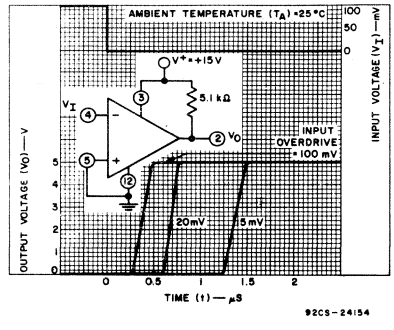


Fig. 6—Response time for various input overdrives—positive transition.

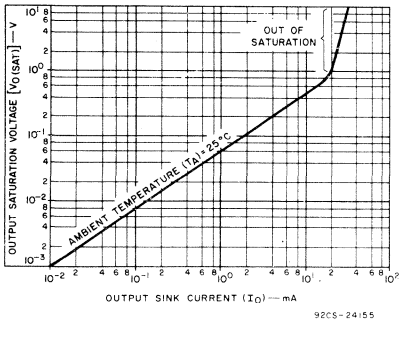
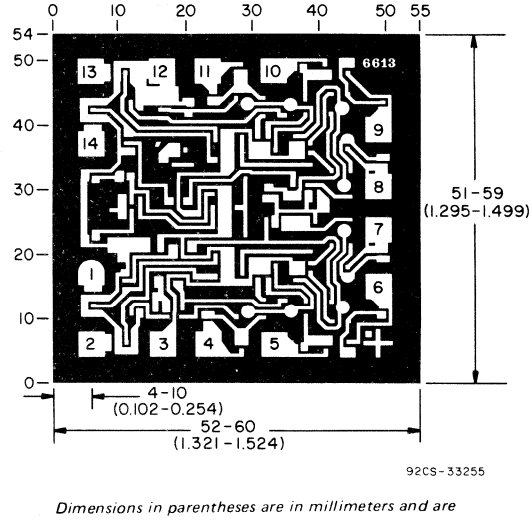


Fig. 7—Output saturation voltage vs. output sink current.

Chip Version (CA339H)



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA311, LM311*

Voltage Comparator

For Commercial and Industrial Applications

Features:

- *Single- or dual-supply operation*
- *Power consumption - 135 mW at ±15 V*
- *Strobe capability*
- *Low input-offset current - 6 nA(typ.)*
- *Differential input-voltage range - ±30 V*
- *Directly interchangeable with National Semiconductor LM311 Series*

The RCA CA311 is a monolithic voltage comparator that operates from dual supplies up to ±15 V, or from single supplies down to 5 V. This single supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition they can drive lamps or relays, and switch voltages up to 40 V at currents as high as 50 mA.

The inputs and outputs of the CA311 can be isolated from system ground, allowing the output to drive loads referred to ground V^+, or V^-.

Applications:

- *Multivibrators*
- *Positive and negative peak detectors*
- *Crystal oscillators*
- *Zero-crossing detectors*
- *Solenoid, relay, and lamp drivers*

The CA311 is available in 8-lead TO-5 style packages with standard leads (T suffix), dual-in-line formed leads ("DIL-CAN", S suffix), 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

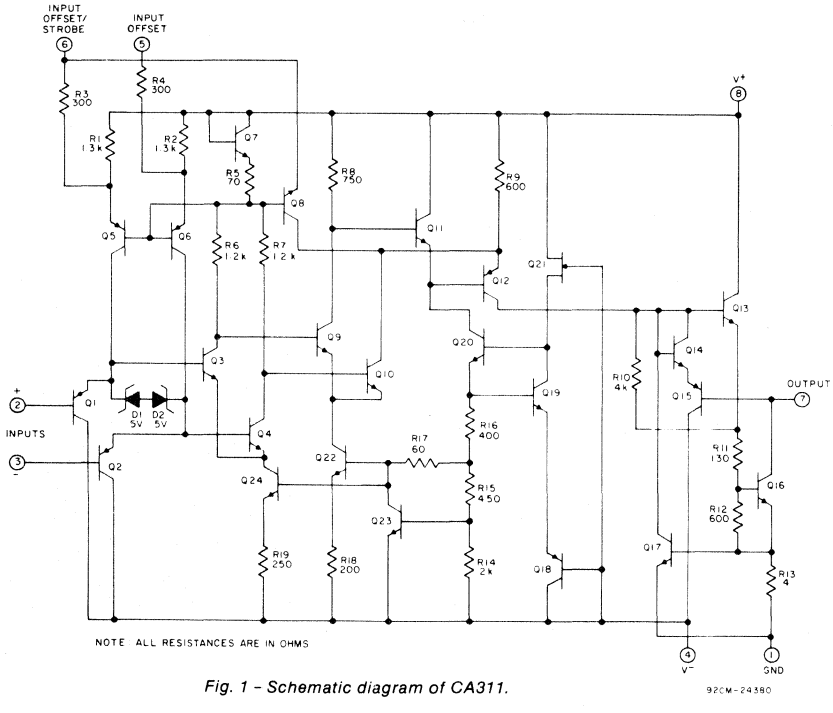


Fig. 1 - Schematic diagram of CA311.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **797**

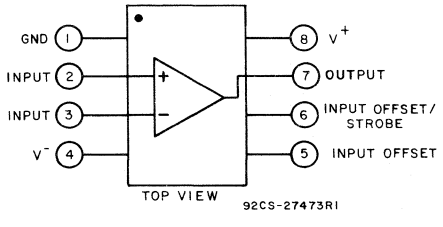
CA311, LM311

Maximum Ratings, *Absolute Maximum Values at T_A = 25°C:*

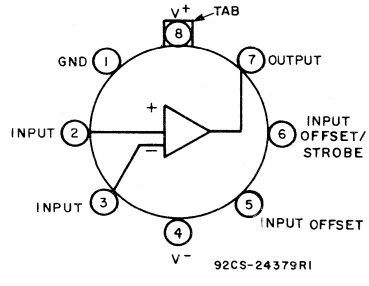
DC SUPPLY VOLTAGE (between V+ and V⁻ terminals) ..... 36 V
DC INPUT VOLTAGE* ..... ±15 V
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}) ..... 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) ..... 30 V
OUTPUT SHORT-CIRCUIT DURATION ..... 10 s
DEVICE DISSIPATION:
UP TO T_A = 25°C ..... 500 mW
Above T_A = 25°C ..... derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +70°C†
Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

†Types CA311 E, S, and T can be operated over the temperature range of -55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE.



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGE.

TYPICAL CHARACTERISTICS

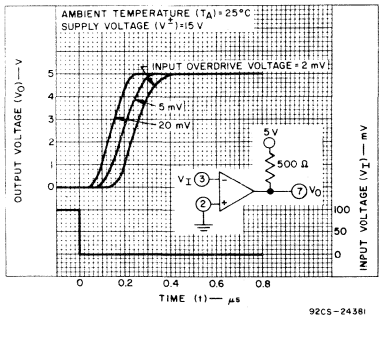


Fig. 2 - Response time for various input overdrive voltages - positive input.

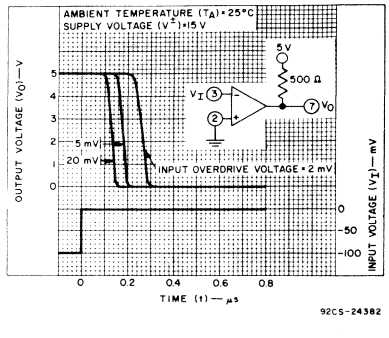


Fig. 3 - Response time for various input overdrive voltages - negative input.

CA311, LM311

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		TEST CONDITIONS: SUPPLY VOLTAGE (V±) = 15V UNLESS OTHERWISE SPECIFIED		LIMITS: CA311 MIN.	LIMITS: CA311 TYP.	LIMITS: CA311 MAX.	UNITS
Input Offset Voltage	V_{IO}	$R_S \leq 5$ kΩ, Note 2	T_A = 25°C	—	2	7.5	mV
			Note 1	—	—	10	
Saturation Voltage		$V_I \leq$ -10 mV, I_O = 50 mA	T_A = 25°C	—	0.75	1.5	V
		V+ ≥ 4.5 V, V⁻ -0, $V_I \leq$ -10 mV, $I_{SINK} \leq$ 8 mA	Note 1	—	0.23	0.4	
Input Voltage Range	V_{IPP}		Note 1	—	±14	—	V
Input Offset Current	I_{IO}	Note 2	T_A = 25°C	—	6	50	nA
			Note 1	—	—	70	
Input Bias Current	I_{IB}	Note 2	T_A = 25°C	—	100	250	nA
			Note 1	—	—	300	
Postive Supply Current	I^+		T_A = 25°C	—	5.1	7.5	mA
Negative Supply Current	I^-		T_A = 25°C	—	4.1	5	mA
Output Leakage Current		$V_I \geq$ 10 mV, V_O = 35 V	T_A = 25°C	—	—	50	nA
Strobe on Current			T_A = 25°C	—	3	—	mA
Voltage Gain, A			T_A = 25°C	40	200	—	V/mV
Response Time		100 mV Input Step with 5 mV Overdrive Voltage	T_A = 25°C	—	200	—	ns
Input Voltage Range			T_A = 25°C	-14.5	13.8 -14.7	13	V

Note 1: Ambient temperature (T_A) over applicable operating temperature of 0 to + 70° C.

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1 mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ± 15 V dual supply.

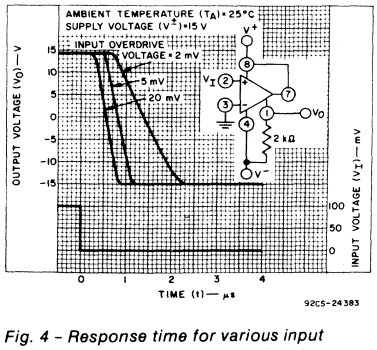


Fig. 4 - Response time for various input overdrive voltages - positive input.

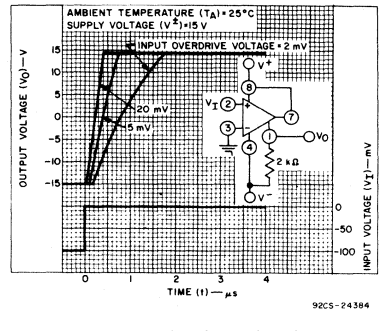


Fig. 5 - Response time for various input overdrive voltages - negative input.

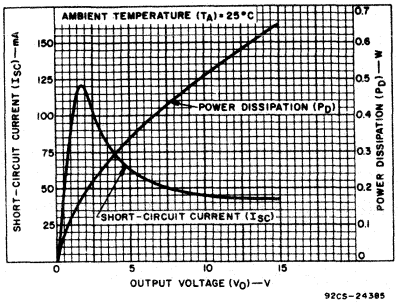


Fig. 6 - Output limiting characteristics.

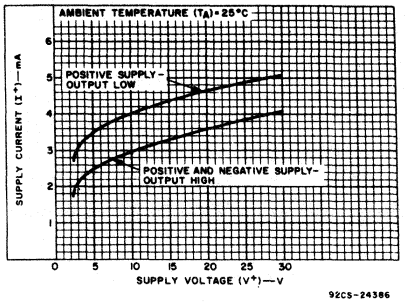


Fig. 7 - Supply current vs. supply voltage.

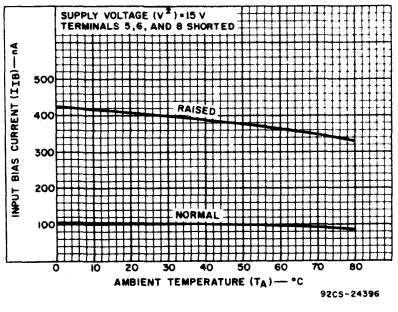


Fig. 8 - Input bias current vs. ambient temperature.

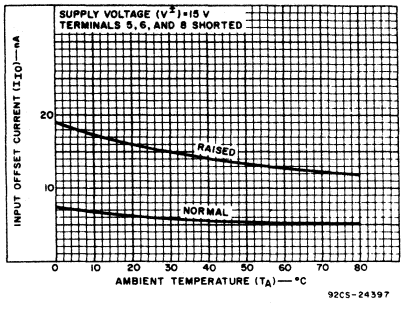


Fig. 9 - Input offset current vs. ambient temperature.

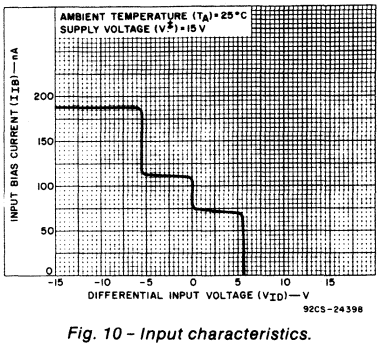


Fig. 10 - Input characteristics.

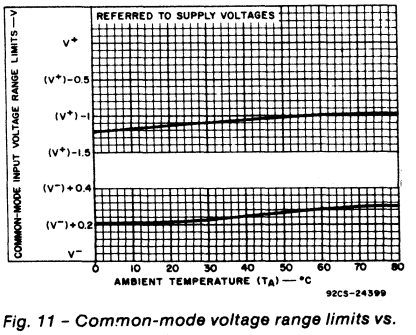


Fig. 11 - Common-mode voltage range limits vs. ambient temperature.

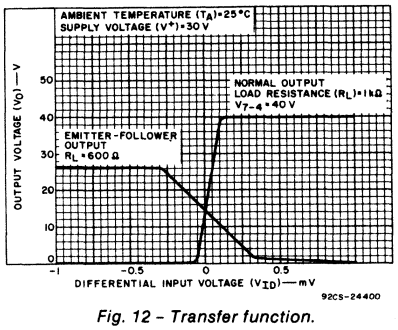


Fig. 12 - Transfer function.

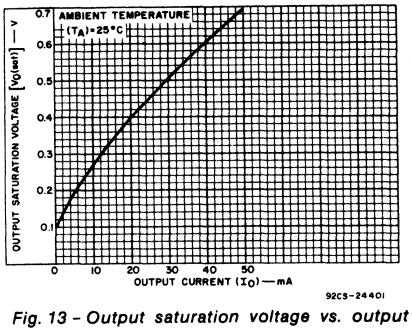


Fig. 13 - Output saturation voltage vs. output current.

CA311, LM311

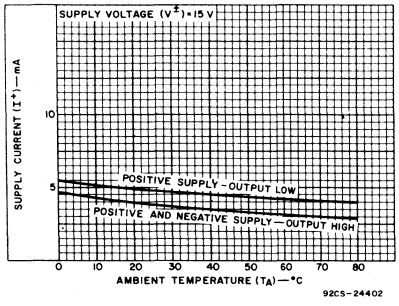


Fig. 14 - Supply current vs. ambient temperature.

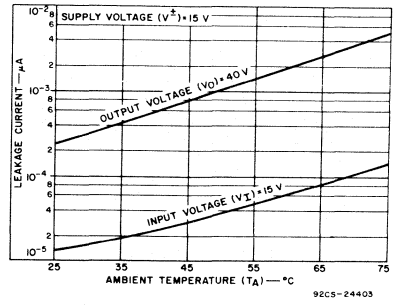


Fig. 15 - Input and output leakage current vs. ambient temperature.

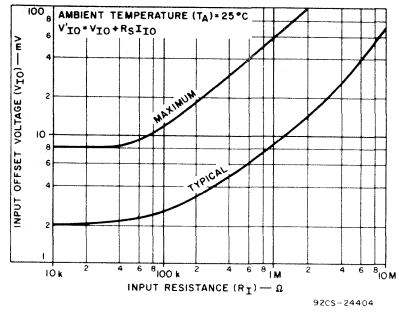


Fig. 16 - Offset error.

TYPICAL APPLICATIONS

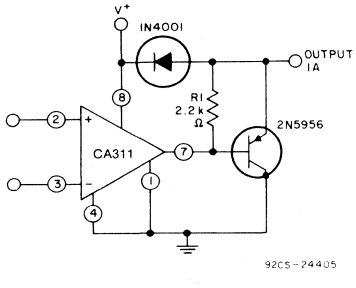


Fig. 17 - Comparator and solenoid driver.

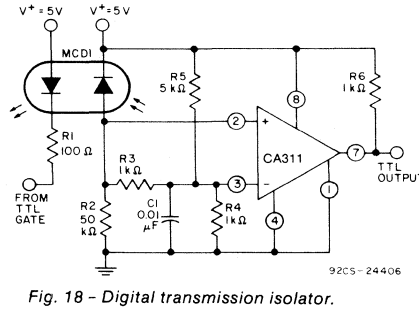


Fig. 18 - Digital transmission isolator.

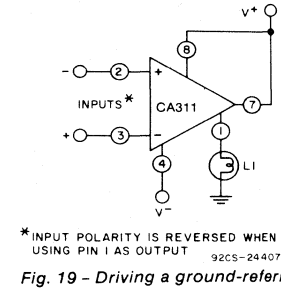


Fig. 19 - Driving a ground-referred load.

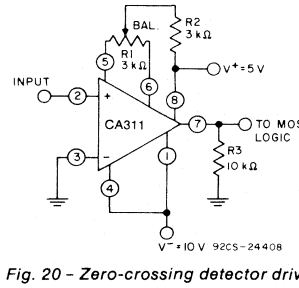


Fig. 20 - Zero-crossing detector driving MOS logic.

TYPICAL APPLICATIONS (cont'd)

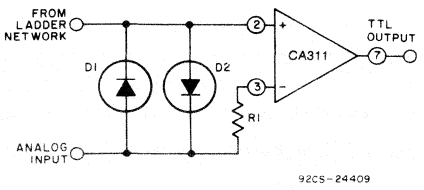


Fig. 21 - Using clamp diodes to improve response.

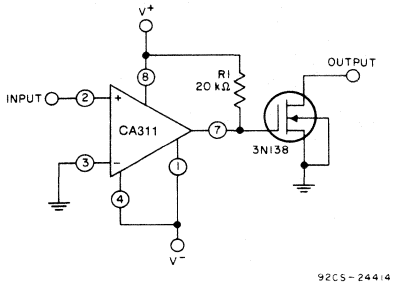


Fig. 23 - Zero-crossing detector driving and MOS switch.

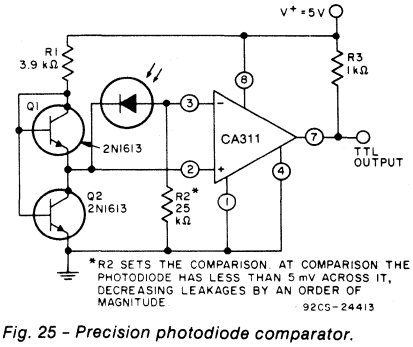


Fig. 25 - Precision photodiode comparator.

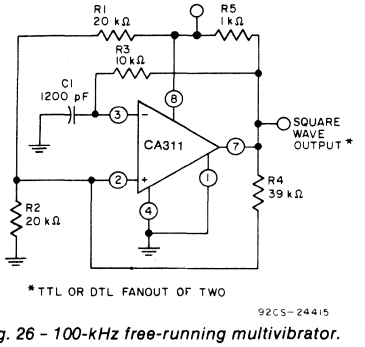


Fig. 26 - 100-kHz free-running multivibrator.

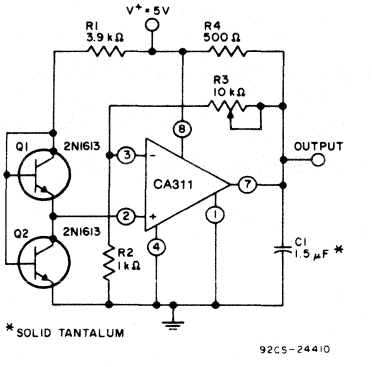


Fig. 22 - Low-voltage adjustable-reference supply.

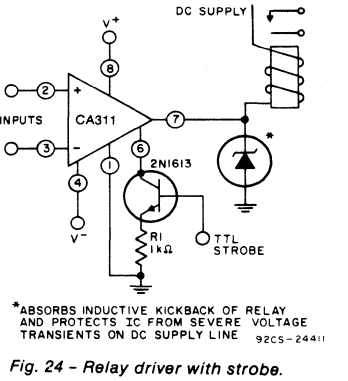


Fig. 24 - Relay driver with strobe.

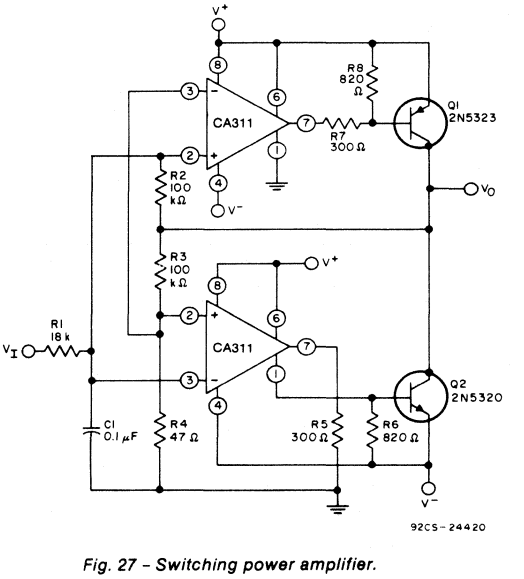


Fig. 27 - Switching power amplifier.

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TYPICAL APPLICATIONS (cont'd)

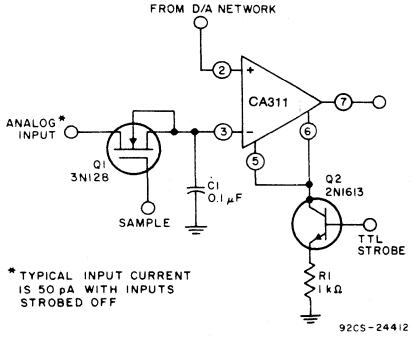


Fig. 28 – Strobing off both input and output stages.

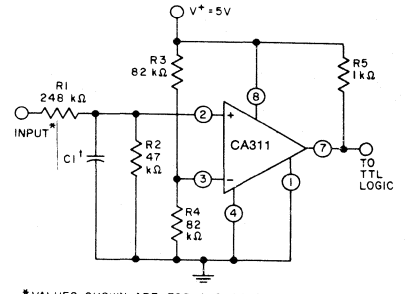


Fig. 29 – TTL interface with high-level logic.

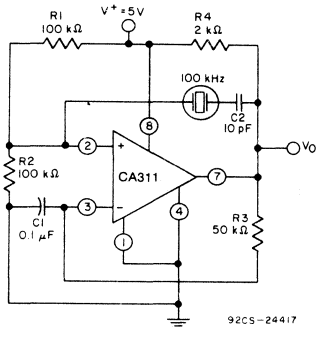


Fig. 30 – Crystal oscillator.

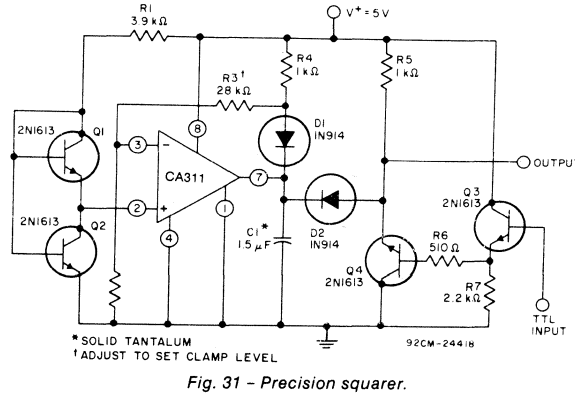


Fig. 31 – Precision squarer.

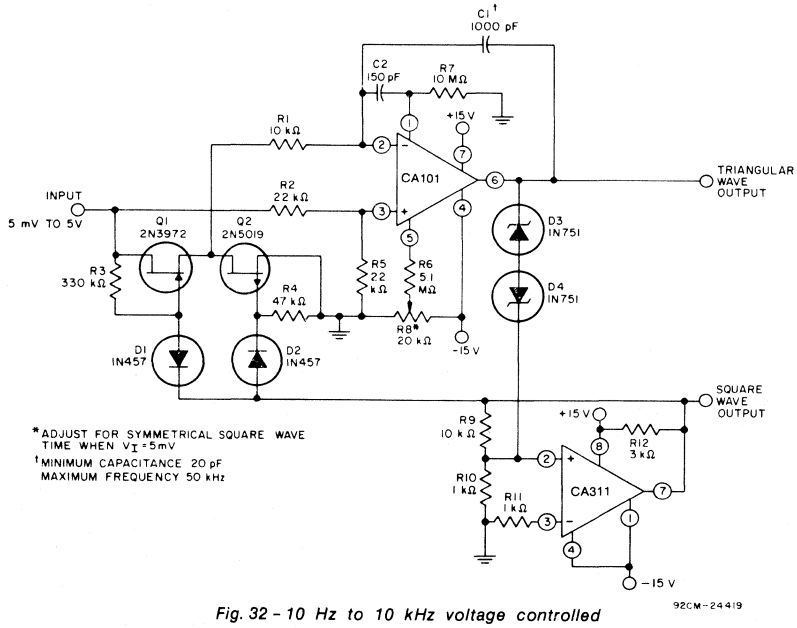


Fig. 32 – 10 Hz to 10 kHz voltage controlled oscillator.

TYPICAL APPLICATIONS (cont'd)

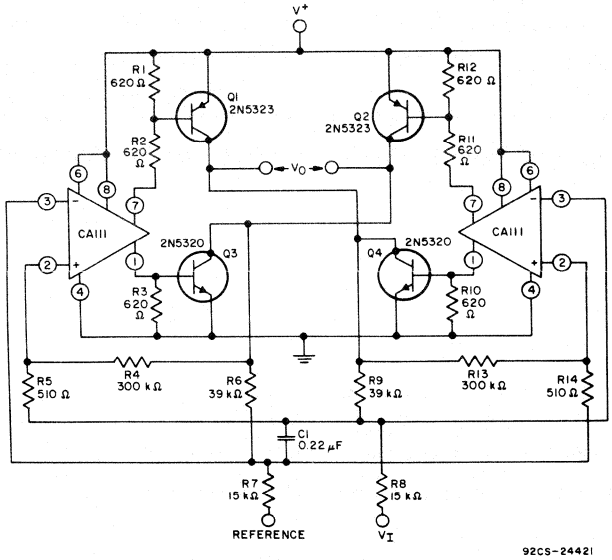
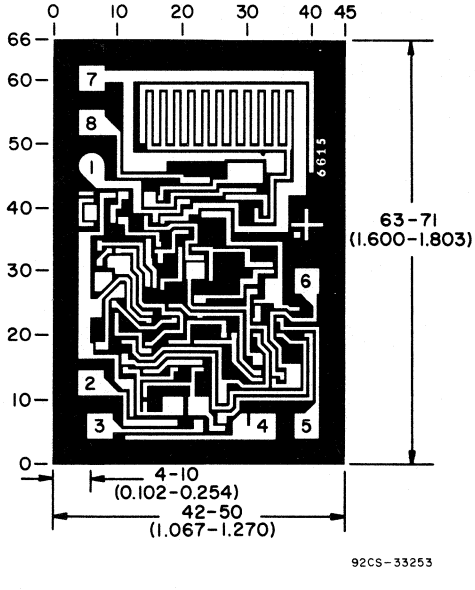


Fig. 33 - Switching power amplifier.



Dimensions and pad layout for CA311H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

CA3098

Programmable Schmitt Trigger - With Memory

Dual-Input Precision Level Detectors

Features:
- *Programmable operating current*
- *Micropower standby dissipation*
- *Direct control of currents up to 150 mA*
- *Low input on/off current of less than 1 nA for programmable bias current of 1 μA*
- *Built-in hysteresis: 20 mV max.*

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

Applications:
- *Control of relays, heaters, LEDs, lamps photosensitive devices, thyristors, solenoids, etc.*
- *Signal reconditioning*
- *Phase and frequency modulators*
- *On/off motor switching*
- *Schmitt triggers, level detectors*
- *Time delays*
- *Overvoltage, overcurrent, over-temperature protection*
- *Battery-operated equipment*
- *Square and triangular-wave generators*

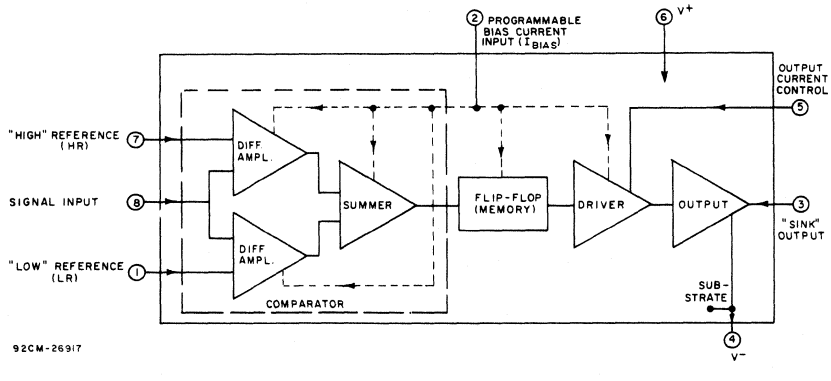


Fig. 1 - Block diagram of CA3098 programmable Schmitt trigger.

File Number **896**

2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and output stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$ Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input Offset Voltage: "Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V, I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V, I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff: "Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, $V_{CE}(SAT)$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}: "ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}: $I_{B(p\text{-}n\text{-}p)}$	V_I = 4 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n\text{-}p\text{-}n)}$	V_I = 8 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times: Delay, t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	18	–	600	–	ns
Fall, t_f			–	50	–	ns
Rise, t_r			–	500	–	ns
Storage, t_s			–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

CA3098

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C Derate linearly at	6.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

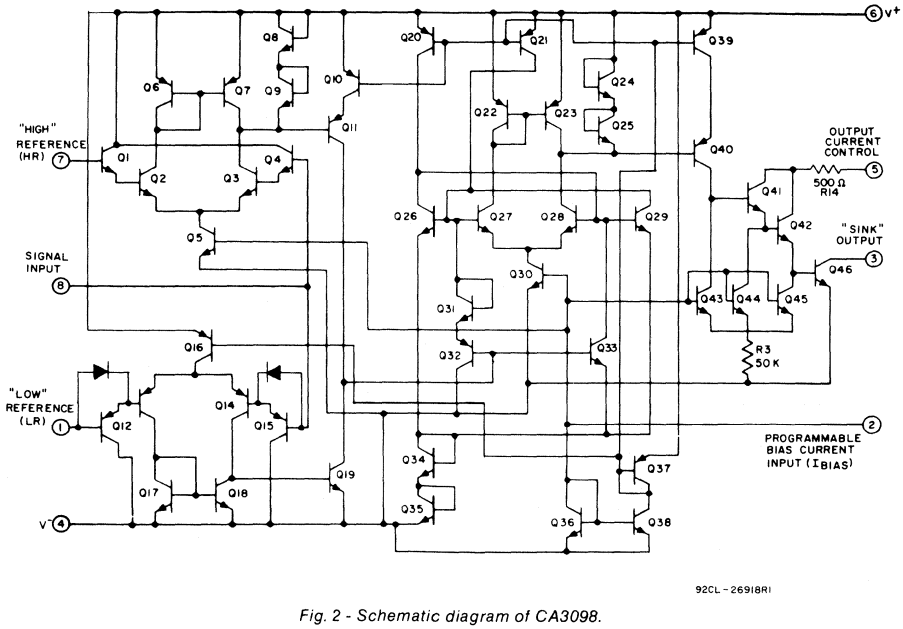


Fig. 2 - Schematic diagram of CA3098.

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

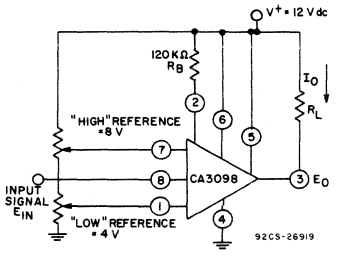


Fig. 3 - Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geqslant E_{IN} > 0$	0
2	$8 \geqslant E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geqslant E_{IN} > 4$	12
1	$4 \geqslant E_{IN} > 0$	0

Fig. 4 - Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

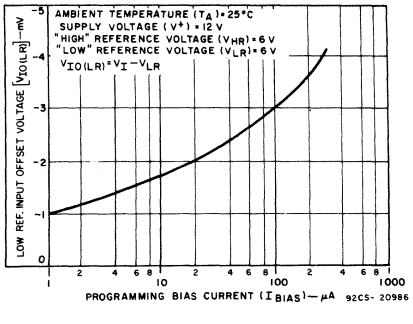


Fig. 5 - Input-offset voltage ("low" reference) vs. programming bias current.

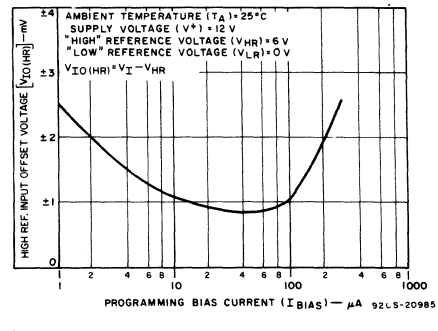


Fig. 6 - Input-offset voltage ("high" reference) vs. programming bias current.

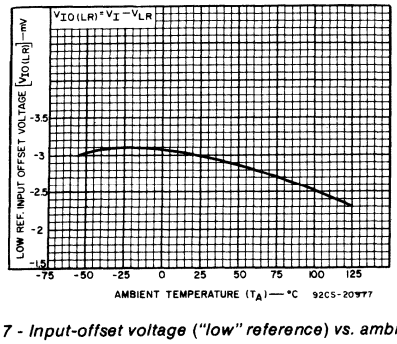


Fig. 7 - Input-offset voltage ("low" reference) vs. ambient temperature.

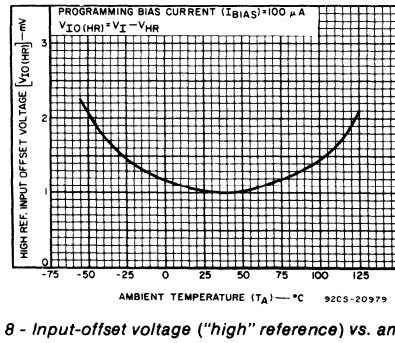


Fig. 8 - Input-offset voltage ("high" reference) vs. ambient temperature.

CA3098

TYPICAL CHARACTERISTIC CURVES (Cont'd)

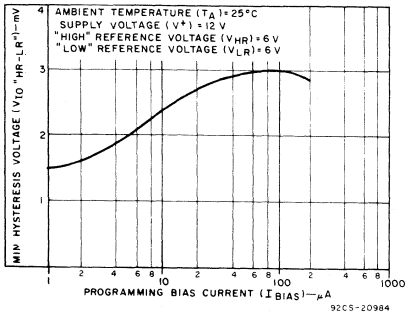


Fig. 9 - Min. hysteresis voltage vs. programming bias current.

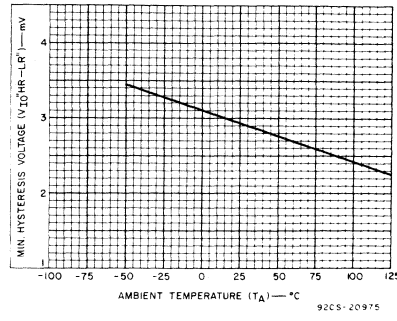


Fig. 10 - Min. hysteresis voltage vs. ambient temperature.

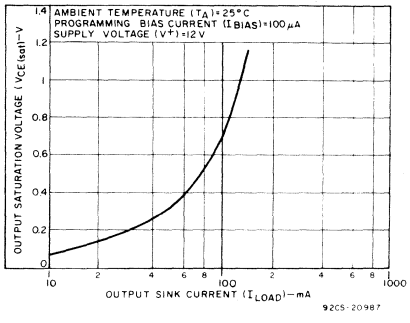


Fig. 11 - Output saturation voltage vs. output sink current.

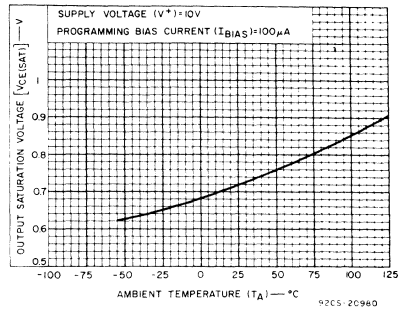


Fig. 12 - Output saturation voltage vs. ambient temperature.

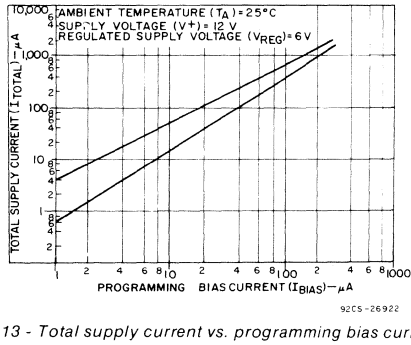


Fig. 13 - Total supply current vs. programming bias current.

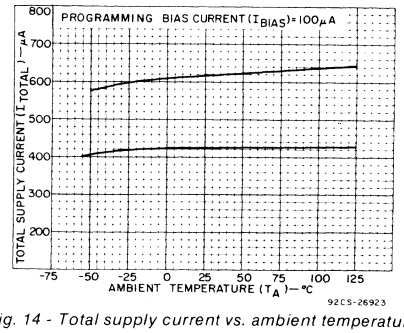


Fig. 14 - Total supply current vs. ambient temperature.

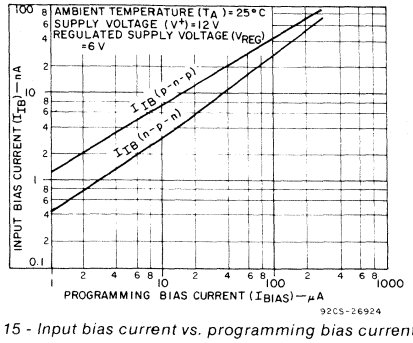


Fig. 15 - Input bias current vs. programming bias current.

TEST CIRCUITS

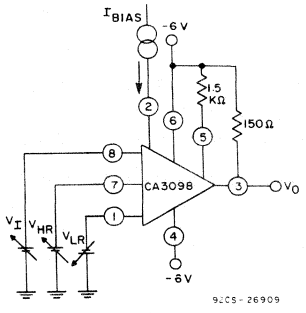


Fig. 16 - Input-offset voltage test circuit.

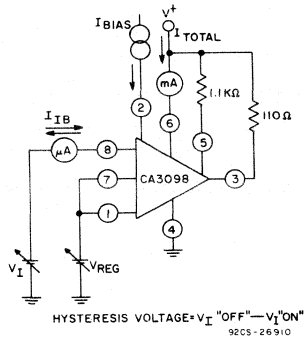


Fig. 17 - Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

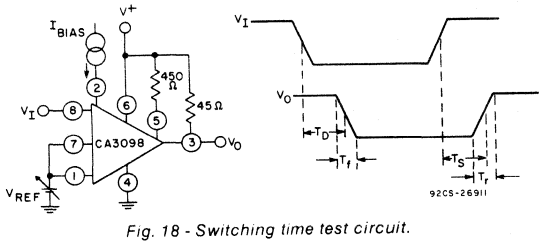


Fig. 18 - Switching time test circuit.

TYPICAL APPLICATIONS

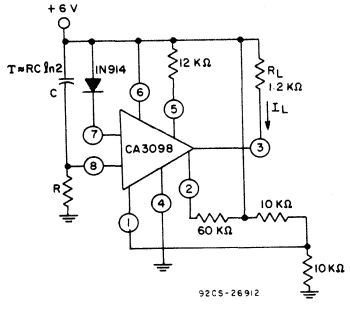


Fig. 19 - Time delay circuit: Terminal 3 "sinks" after τ seconds.

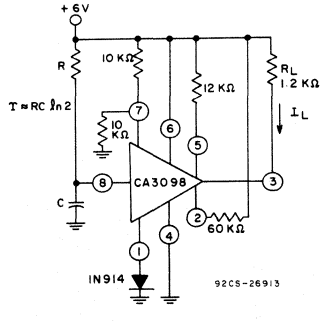


Fig. 20 - Time delay circuit: "sink" current interrupted after τ seconds.

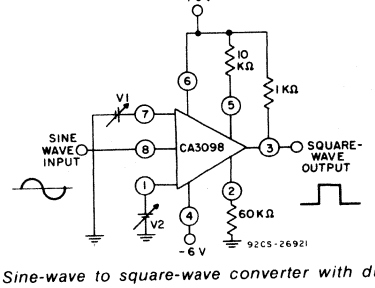
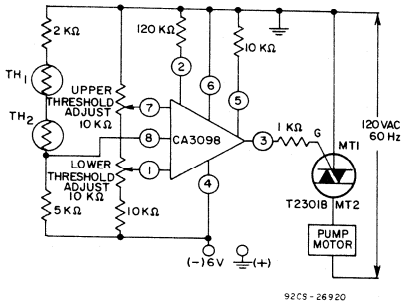


Fig. 21 - Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).

CA3098

TYPICAL APPLICATIONS (Cont'd)



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.
(b) Motor pump remains "ON" until water level falls below thermistor TH_1.
(c) Thermistors, operate in self-heating mode.

Fig. 22(a) - Water-level control.

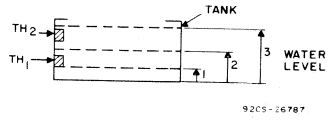


Fig. 22(b) - Water level diagram for circuit of Fig. 22(a).

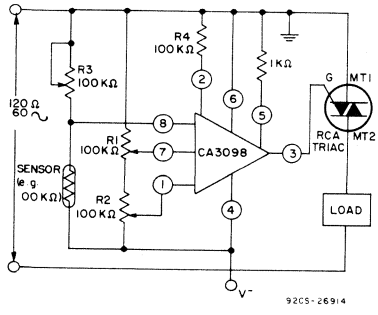


Fig. 23 - OFF/ON control of triac with programmable hysteresis.

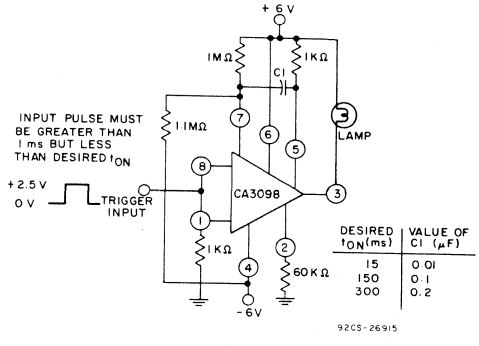
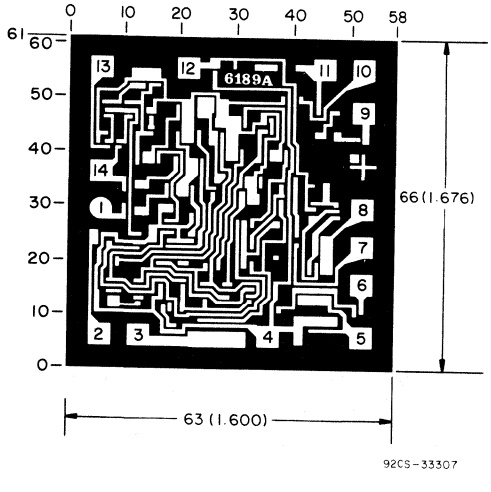


Fig. 24 - One-shot multivibrator.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for the CA3098H.

CA3099

rogrammable Comparator - - With Memory

atures:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V^+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

A-CA3099E* Programmable Comparator is a monolithic con integrated circuit designed to control high-operating-rent loads such as thyristors, lamps, relays, etc. The 3099E can be operated with either a single power supply h maximum operating voltage of 16 volts, or a dual wer supply with a maximum operating voltage of ± 8 volts. can directly control currents up to 150 mA. It operates with crowatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

*Formerly Developmental No. TA6189.

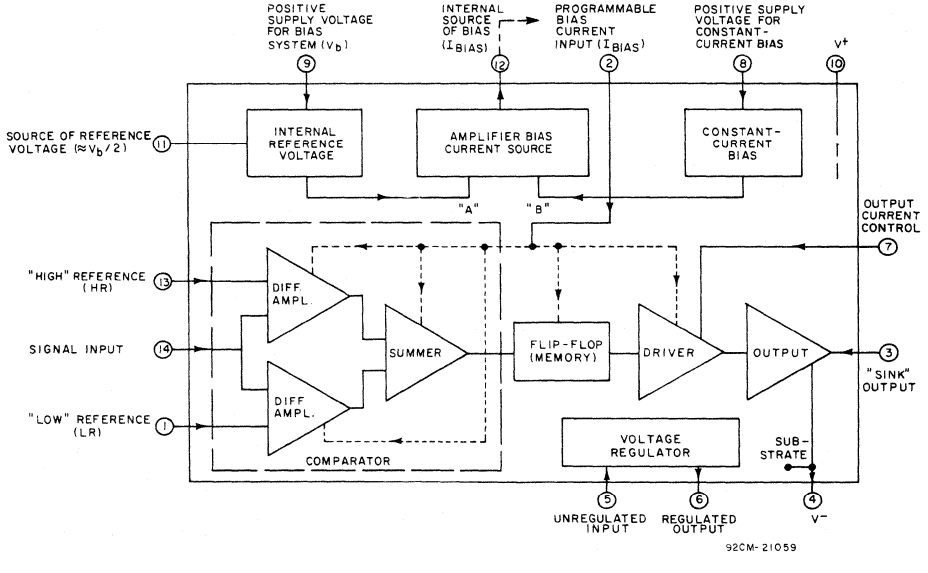


Fig. 1—Block diagram of CA3099E programmable comparator.

File Number **620**

CA3099

Major Circuit-Function Features (Cont'd)

2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_h). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

Maximum Ratings, *Absolute-Maximum Values at $T_A = 25^oC$*

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16
Output Voltage Between Terminals 7 and 4, and 3 and 4	16
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10
Operating Voltage Range:	
Term. 14	0 V to
Term. 13	2.0 V to
Term. 1	0 V to V^+ minus 2.
Load Current (Term. 3)	150
Input Current to Voltage Regulator (Term. 5)	25
Programming Bias Current (Term. 2)	1
Output Current Control (Term. 7)	15
Power Dissipation:	
Up to $T_A = 55^oC$	750
Above $T_A = 55^oC$ Derate Linearly at	6.67 mW
Ambient Temperature Range:	
Operating	−55 to +125
Storage	−65 to +150
Lead Termperature (During Soldering):	
At distance not less than 1/32 inch (3.17 mm) from seating plane for 10 s maximum	+265

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$ *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$ Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	μV/°C
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/°C
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 μA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 μA	20, 7	−5	±1	5	
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	μV/°C
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	μV/°C
Output Saturation Voltage	$V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	600	710	800	μA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,14,15	420	560	750	
Input Bias Current: $I_{B(p\text{-}n\text{-}p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	33	200	nA
$I_{B(n\text{-}p\text{-}n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	21,16,17	–	20	60	
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	μA
Internal Bias Current	I_{IBC}		18,19	120	200	280	
Switching Times:							ns
Delay	t_d	I_C = 100 μA, I_{BIAS} = 100 μA, V^+ = 5 V, V_{REG} = 2.5 V	22	–	600	–	
Fall	t_f		22	–	50	–	
Rise	t_r		22	–	500	–	
Storage	t_s		22	–	4.5	–	

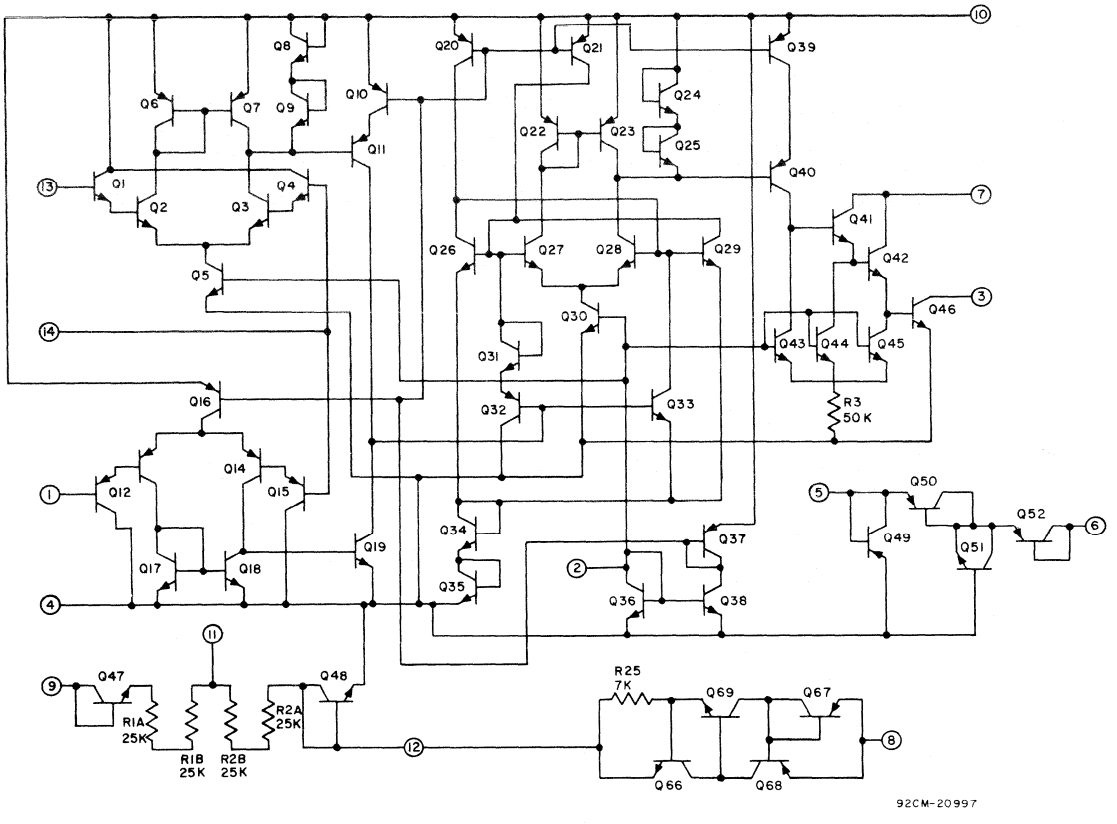


Fig.2–Schematic diagram of CA3099E.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

CA3099

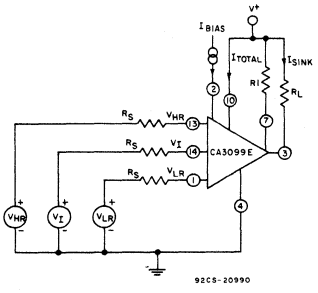


Fig.3—Functional diagram.

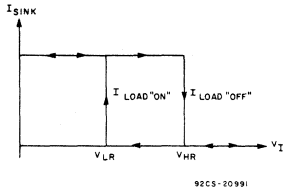


Fig.4—Logic diagram.

TYPICAL CHARACTERISTIC CURVES

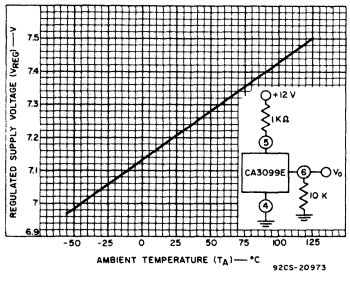


Fig.5—Regulated supply voltage vs. ambient temperature.

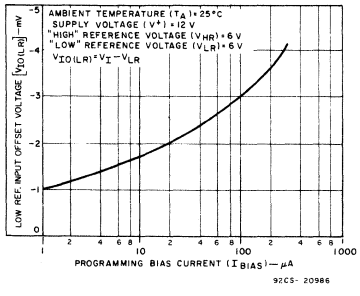


Fig.6—Input-offset voltage ("low" reference) vs. programming bias current.

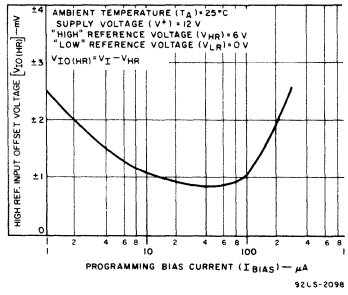


Fig.7—Input-offset voltage ("high" reference vs. programming bias current.

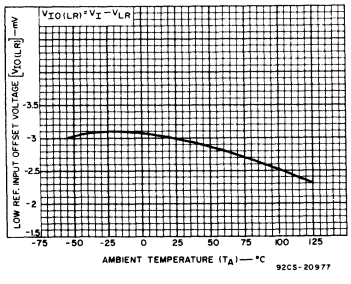


Fig.8—Input-offset voltage ("low" reference) vs. ambient temperature.

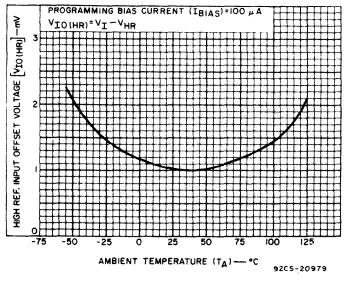


Fig.9—Input-offset voltage ("high" reference) vs. ambient temperature.

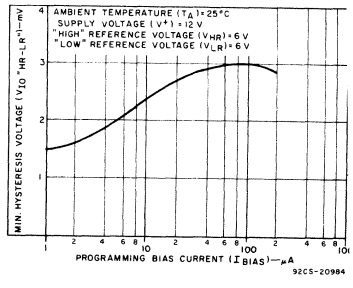


Fig.10—Min. hysteresis voltage vs. programmin bias current.

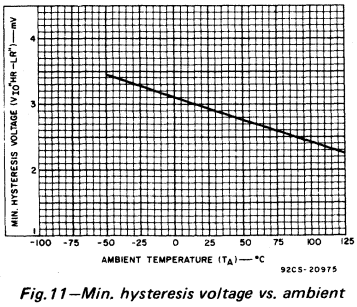


Fig.11—Min. hysteresis voltage vs. ambient temperature.

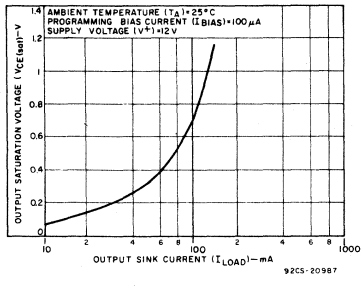


Fig.12—Output saturation voltage vs. output sink current.

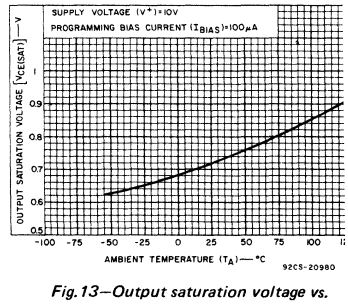


Fig.13—Output saturation voltage vs. ambient temperature.

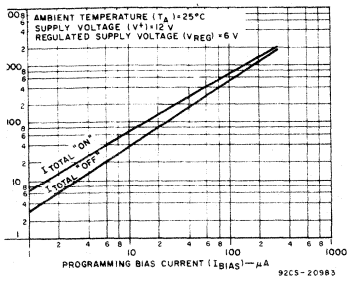


Fig.14—Total supply current vs. programming bias current.

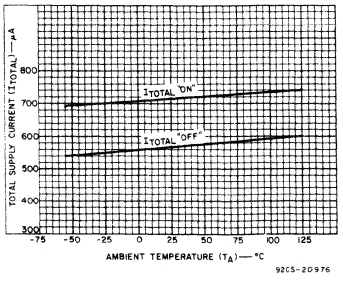


Fig.15—Total supply current vs. ambient temperature.

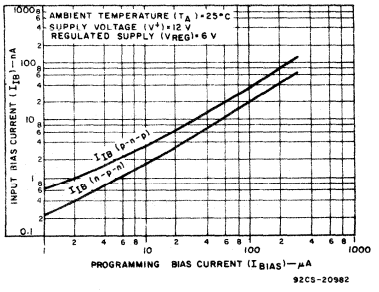


Fig.16—Input bias current vs. programming bias current.

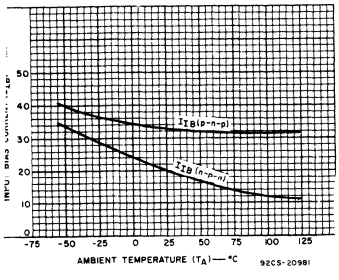


Fig.17—Input bias current vs. ambient temperature.

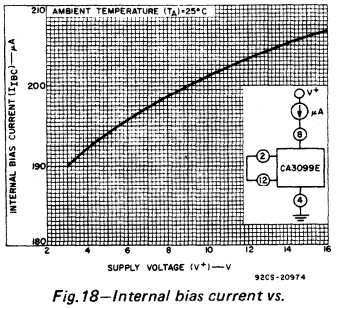


Fig.18—Internal bias current vs. supply voltage.

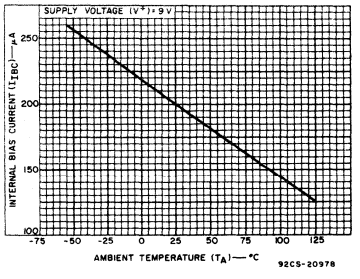


Fig.19—Internal bias current vs. ambient temperature.

TEST CIRCUITS

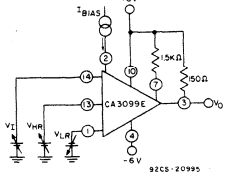


Fig.20—Input-offset voltage test circuit.

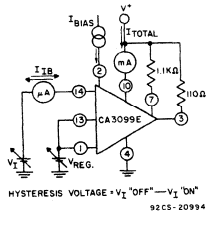


Fig.21—Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

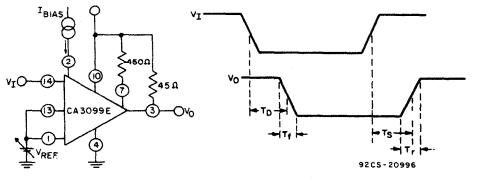


Fig.22—Switching time test circuit.

TYPICAL APPLICATIONS

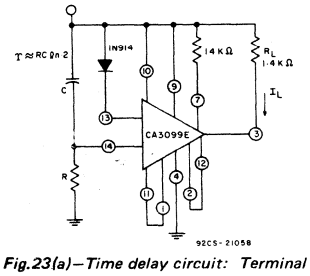


Fig.23(a)—Time delay circuit: Terminal 3 "sinks" after τ seconds.

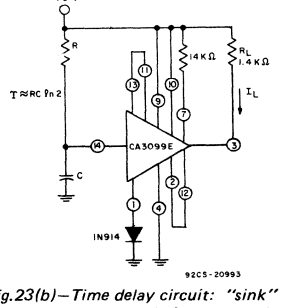


Fig.23(b)—Time delay circuit: "sink" current interrupted after τ seconds.

CA3099

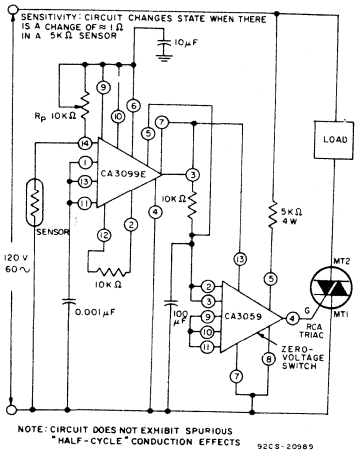


Fig.24—Sensitive temperature control.

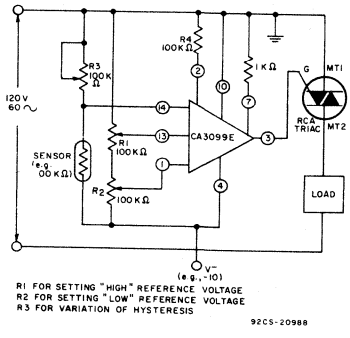


Fig.25—OFF/ON control of triac with programmable hysteresis.

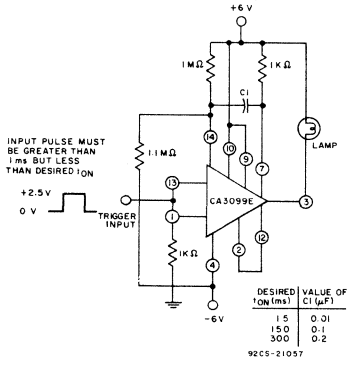


Fig.26—One-shot multivibrator.

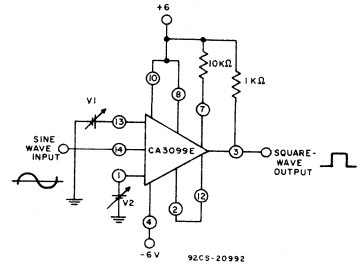


Fig.27—Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).

CA3290A, CA3290

BiMOS Dual Voltage Comparators

With MOSFET Input, Bipolar Output

- *MOSFET input stage:*
  (a) Very high input impedance (Z_{IN}) - 1.7 TΩ typ.
  (b) Very low input current - 3.5 pA typ. at +5 V supply voltage
  (c) Wide common-mode input-voltage range (V_{ICR}) - can be swung 1.5 V (typ.) below negative supply-voltage rail
  (d) Virtually eliminates errors due to flow of input currents
- *Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS logic systems*

The RCA-CA3290A and CA3290 types consist of a dual voltage-comparator on a single monolithic chip. The common-mode input voltage range includes ground when operated from a single supply. The low supply-current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

Applications:

- *High-source-impedance voltage comparators*
- *Long time delay circuits*
- *Square-wave generators*
- *A/D converters*
- *Window comparators*

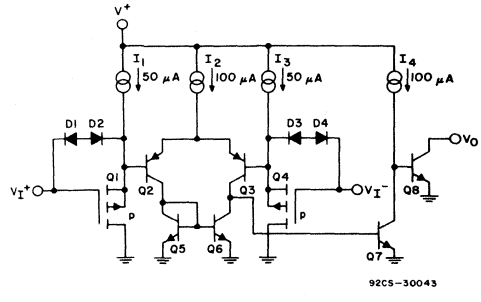


Fig. 1 — Basic CA3290 comparator.

SELECTION CHART

Selection	Characteristic				Package & Suffix			
					TO-5		Plastic	
	Max. V_{IO} (mV)	Max. I_I (pA)	Min. A_{OL}	V^+ (V)	Std.	DIL-CAN	8-Ld.	14-Ld.
CA3290A	10	40	25K	36	T	S	E	E1
CA3290	20	50	25K	36	T	S	E	E1

The CA3290 is also available in chip form (H suffix)

File Number **1049**

CA3290A, CA3290

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
Single Supply:	
CA3290A, CA3290	+36 V
Dual Supply:	
CA3290A, CA3290	±18 V
DIFFERENTIAL INPUT VOLTAGE	±36 V or ±[(V^+−V^-)+5 V] (whichever is less)
COMMON-MODE INPUT VOLTAGE	V^++5 V to V^-−5 V
DEVICE DISSIPATION:	
Up to 55°C	630 mW
Above 55°C	Derate linearly at 6.67 mW/°C
OUTPUT-TO-V^- SHORT CIRCUIT DURATION*	CONTINUOUS
TEMPERATURE RANGE, ALL TYPES:	
Operating	−55 to +125°C
Storage	−65 to +150°C
INPUT TERMINAL CURRENT	1 mA
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16±1/32 INCH (1.59±0.79 MM)	
FROM CASE FOR 10 SECONDS MAX.	265°C

*Short circuits from the output to V^+ can cause excessive heating and eventual destruction of the device.

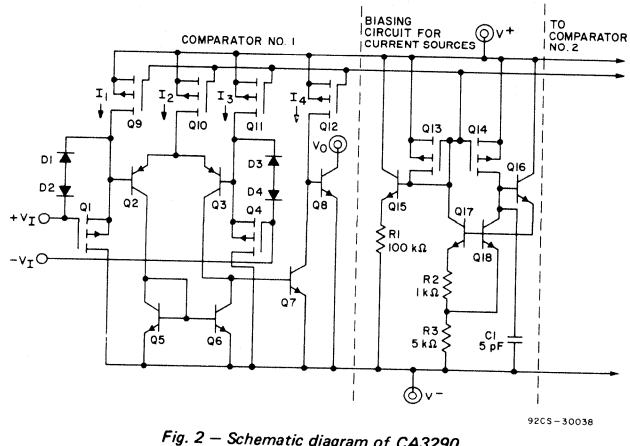


Fig. 2 – Schematic diagram of CA3290 (only one is shown).

CIRCUIT DESCRIPTION

The Basic Comparator

Fig. 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry-type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror-connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input-signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V^+.

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I_1 through I_4, respectively. Their gate-source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

ELECTRICAL CHARACTERISTICS at T_A = −55 to +125°C

CHARACTERISTIC	TEST CONDITIONS		VALUES				UNITS
			CA3290A		CA3290		
		V^+	Typ.	Max.	Typ.	Max.	
Input Offset Voltage, V_{IO}	V_{CM}=1.4 V, V_O=1.4 V	5 V	4.5	—	8.5	—	mV
	V_{CM}=0 V, V_O=0 V	±15 V	8.5	—	8.5		
Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$			8	—	8	—	μV/°C
Input Offset Current, I_{IO}	V_{CM}=1.4 V	5 V	2	28	2	32	nA
	V_{CM}=0 V	±15 V	7	28	7	32	
Input Current, I_I▲	V_{CM}=1.4 V	5 V	2.8	45	2.8	55	nA
	V_{CM}=0 V	±15 V	13	45	13	55	
Supply Current, I^+*	$R_L = \infty$	5 V	0.85	1	0.85	**1.6**	mA
		30 V	1.62	3	1.62	**3.5**	
Voltage Gain, A_{OL}	R_L=15 kΩ	±15 V	150	—	150	—	V/mV
			103	—	103	—	dB
Saturation Voltage I_{SINK} = 4 mA	V^+=5 V, $+V_I$=0 V, $-V_I$=1 V	+125°C	0.22	0.7	0.22	0.7	V
		−55°C	0.1	—	0.1	—	
Output Leakage Current, I_{OL}		15 V	65	—	65	—	nA
		36 V	130	1k	130	1k	

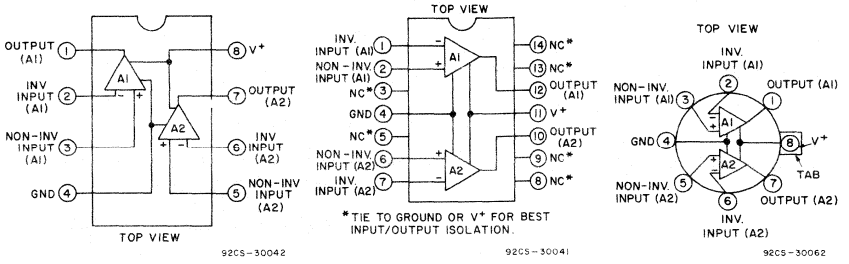
▲At T_A = +125°C
*At T_A = −55°C

CA3290A, CA3290

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

CHARACTERISTIC	TEST COND.	LIMITS						UNITS
		CA3290A			CA3290			
	V^+	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO} V_{CM}=1.4 V, V_O=1.4 V	5 V	–	4	10	–	7.5	20	mV
V_{CM}=0 V, V_O=0 V	±15 V	–	4	10	–	7.5	20	mV
Input Current, I_I V_{CM}=1.4 V	5 V	–	3.5	40	–	3.5	50	pA
V_{CM}=0 V	±15 V	–	12	40	–	12	50	pA
Input Offset Current, I_{IO} V_{CM}=1.4 V	5 V	–	2	25	–	2	30	pA
V_{CM}=0 V	±15 V	–	7	25	–	7	30	pA
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5 V^-	V^+–3.1 V^-–1.5	–	V^+–3.5 V^-	V^+–3.1 V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8 V^-	V^+–3.4 V^-–1.6	–	V^+–3.8 V^-	V^+–3.4 V^-–1.6	–	V
Supply Current, I^+ $R_L = \infty$	30 V	–	1.35	3	–	1.35	3	mA
	5 V	–	0.8	1.4	–	0.8	1.4	mA
Voltage Gain, A_{OL} R_L=15 kΩ	±15 V	25	800	–	25	800	–	V/mV
		88	118	–	88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, I_{SINK} = 4 mA	5 V	–	0.12	0.4	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	–	100	–	pA
	36 V	–	500	–	–	500	–	pA
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	–	1.2	–	μs
Falling Edge		–	200	–	–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	562	–	44	562	μV/V
	5 V	–	100	562	–	100	562	μV/V
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	–	500	–	ns
	5 V	–	400	–	–	400	–	ns

TERMINAL ASSIGNMENTS



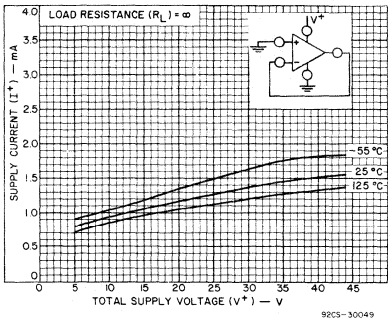


Fig. 3 — Supply current as a function of supply voltage (both amplifiers).

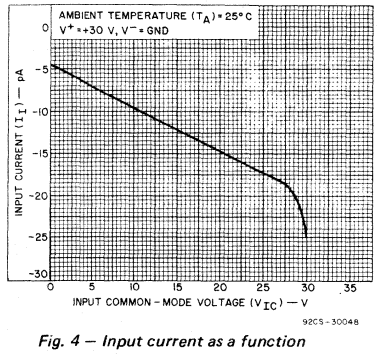


Fig. 4 — Input current as a function of input common-mode voltage.

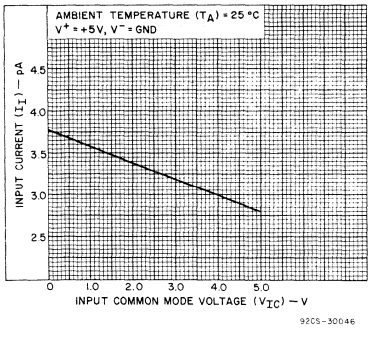


Fig. 5 — Input current as a function of input common-mode voltage.

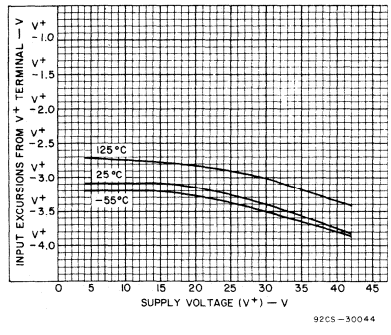


Fig. 6 — Positive common-mode input voltage range as a function of supply voltage.

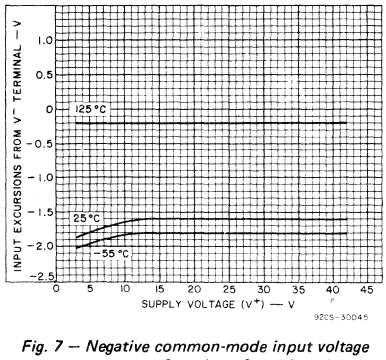


Fig. 7 — Negative common-mode input voltage range as a function of supply voltage.

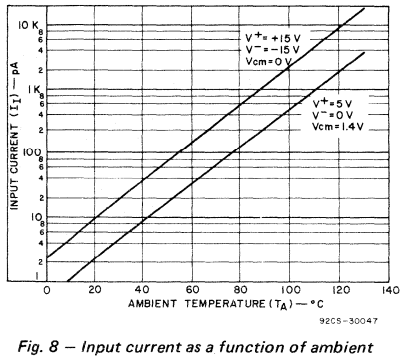


Fig. 8 — Input current as a function of ambient temperature.

CA3290A, CA3290

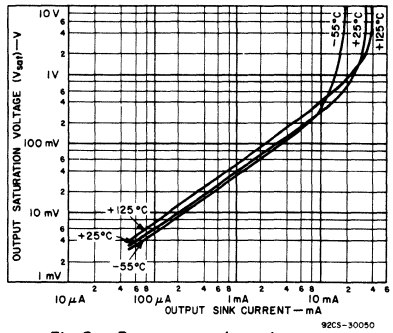
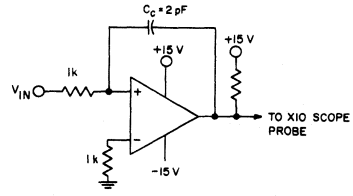
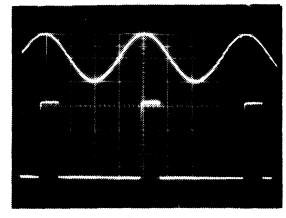


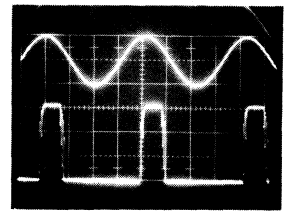
Fig. 9 — Output saturation voltage as a function of output sink current.





WITH C_C

TOP TRACE ≈ 4.5 mV/DIV = V_{IN}
BOTTOM TRACE = 10 V/DIV = V_{OUT}
H = 5 μs/DIV

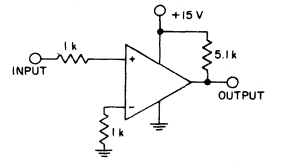


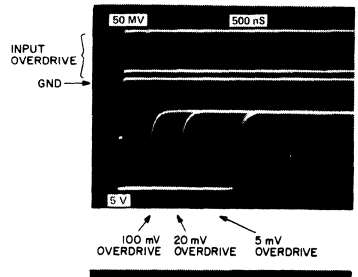
WITHOUT C_C

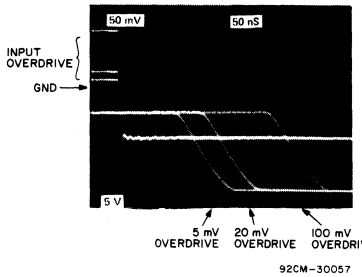
TOP TRACE ≈ 4.5 mV/DIV
BOTTOM TRACE = 10 V/DIV
H = 5 μs/DIV

92CM-30059R1

Fig. 10 — Parasitic-oscillations test circuit and associated waveforms.

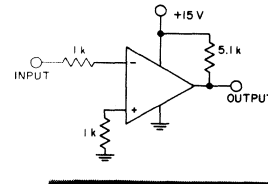


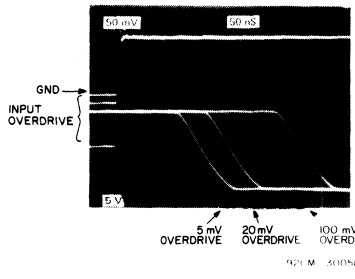




92CM-30057

Fig. 11 — Non-inverting comparator response-time test circuit and waveforms.





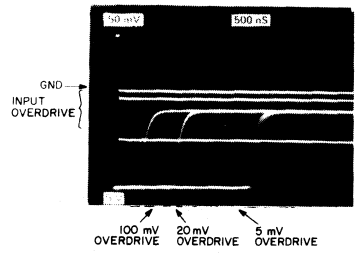


Fig. 12 — Inverting comparator response-time test circuit and waveforms.

OPERATING CONSIDERATIONS

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra-high input impedance (≅ 1.7 TΩ);
2. The availability of common-mode rejection for input signals at potentials below that of the negative power-supply rail;
3. Retention of the in-phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input-terminal currents should not exceed 1 mA. Appropriate series-connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel-connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V^+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra-high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1 to 10 mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8-lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1 pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, toggling rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1 kΩ a capacitor (≥ 1-2 pF) be connected between the appropriate input terminal and the output terminal. (See Fig. 10.)

The CA3290A and CA3290 are also supplied in a 14-lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V^+ or V^- supply rail. If either comparator is unused, its input terminals should also be tied to either the V^+ or V^- supply rail.

TYPICAL APPLICATIONS

Light-Controlled One-Shot Timer

In Fig. 13 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

Low-Frequency Multivibrator

In this application, one-half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading.

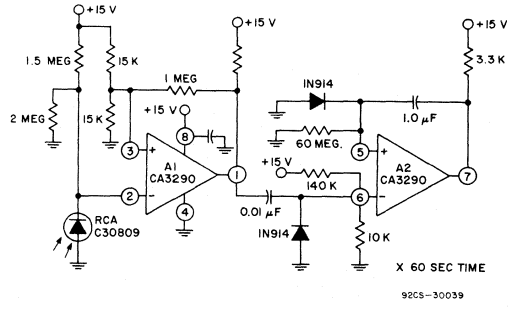


Fig. 13 – Light-controlled one-shot timer.

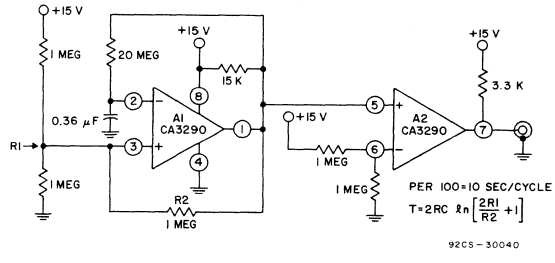


Fig. 14 – Low-frequency multivibrator.

Window Comparator

Both halves of the CA3290 can be used in a high input-impedance window comparator as shown in Fig. 15. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

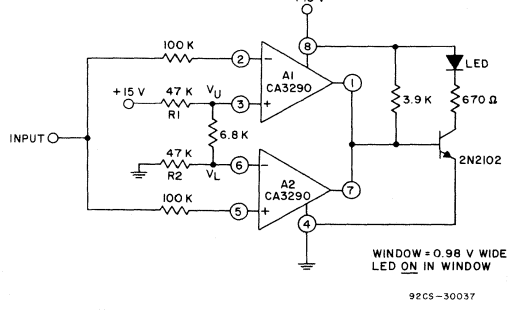


Fig. 15 – Window comparator.

LED Bar Graph Driver

The circuit in Fig. 16 demonstrates the use of the CA3290 in a bar graph display. The non-inverting inputs of both comparators are tied to the voltage divider reference and the input signal is applied to both of the inverting inputs. The LED for a particular comparator will be turned "on" when the input voltage reaches the voltage on the resistor divider reference. The CA3290 is ideal for this application where input-signal loading is critical even though many comparator inputs are driven in parallel.

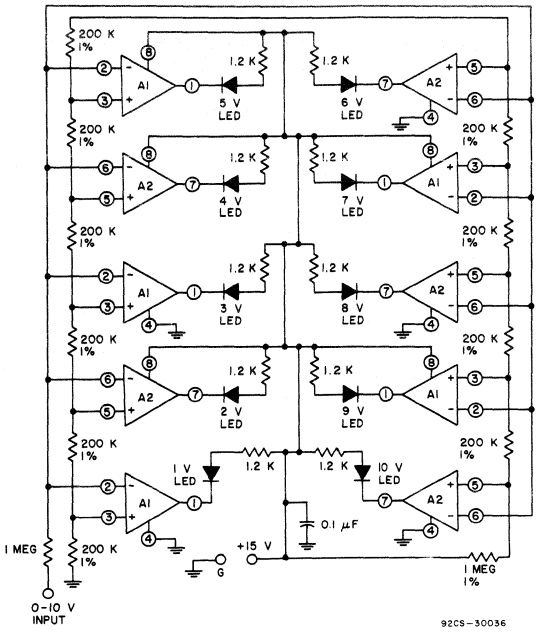
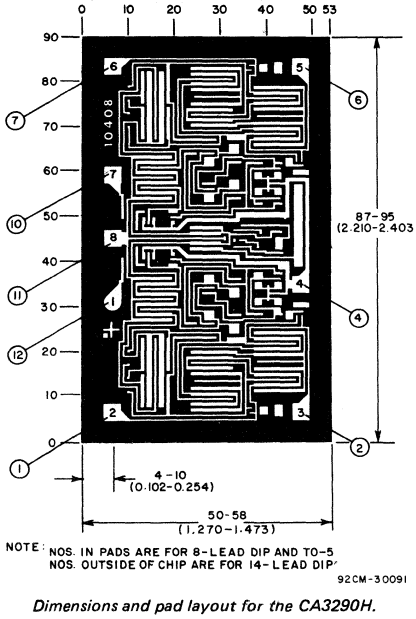


Fig. 16 – LED bar-graph driver.



Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Differential Amplifiers

Differential Amplifier Circuits — Technical Data

DC Amplifier

Features:

- *Designed for use in Communication, Telemetry, Instrumentation, and Data-Processing Equipment*
- *Balanced differential-amplifier configuration with controlled constant-current source to provide outstanding versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Companion Application Note, ICAN 5030 "Applications of RCA CA3000 Integrated Circuit DC Amplifier" covers characteristics of different operating modes, frequency considerations, 10 MHz narrow band tuned amplifier design, crystal oscillator design, and many other application aids*
- *Input impedance - 195 kΩ typ.*
- *Voltage gain - 37 dB typ.*
- *Common-mode rejection ratio - 98 dB typ.*
- *Input offset voltage - 1.4 mV typ.*
- *Push-pull input and output*
- *Frequency capability - DC to 30 MHz (with external C and R)*
- *Wide AGC range - 90 dB typ.*

Applications

- *Schmitt trigger*
- *RC-coupled feedback amplifier*
- *Mixer*
- *Comparator*
- *Modulator*
- *Crystal oscillator*
- *Sense amplifier*

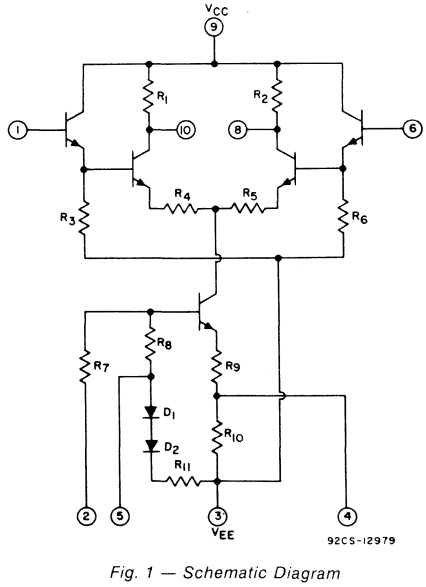


Fig. 1 — Schematic Diagram

File Number **121**

CA3000

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_A = 25°C

Indicated voltage limits for each terminal can be used under specified voltage conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2	+2	2	0
			3	-6
			6	0
			9	+6
2	-8	0	1	0
			3	-8
			6	0
			9	+6
3	-10	0	1	0
			2	0
			6	0
			9	+6
4	-8	0	1	0
			2	0
			6	0
			9	+6
5	-6	0	1	0
			2	0
			3	-6
			6	0
			9	+6
6	-2	+2	1	0
			2	0
			3	-6
			9	+6
7	NO CONNECTION			
8	0	+6	1	0
			2	0
			3	-6
			6	0
9	0	+10	1	0
			2	0
			3	-6
			6	0
10	0	+6	1	0
			2	0
			3	-6
			6	0
CASE	Internally Connected to Terminal No.3 (Substrate) DO NOT GROUND			

OPERATING TEMPERATURE RANGE	-55°C to +125°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ±1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C
MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE	± 4 V
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE	± 2.5 V
MAXIMUM DEVICE DISSIPATION:	
-55 to 85°C	450 mW
Above 85°C	Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V, unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 & No.5 Not Connected Unless Specified		TEST CIRCUITS	LIMITS TYPE CA3000				TYPICAL CHARACTERISTICS CURVES
				Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS									
Input Offset Voltage	V_{IO}				-	1.4	5	mV	2
Input Offset Current	I_{IO}				-	1.2	10	μA	2
Input Bias Current	I_{IB}				-	23	36	μA	3
Quiescent Operating Voltage	V_8 or V_{IO}	TERMINALS							
		4	5						
		NC	NC		-	2.6	-	V	4
		NC	VEE		-	4.2	-	V	4
		VEE	NC		-	-1.5	-	V	4
		VEE	VEE		-	0.6	-	V	4
Device Dissipation	P_D	NC	NC		-	30	-	mW	NONE
DYNAMIC CHARACTERISTICS									
Differential Voltage Gain Single-Ended Input	A_{DIFF}	Single-Ended Output f = 1 kHz		9	28	32	-	dB	5
		Double-Ended Output f = 1 kHz		9	-	38	-	dB	5
Bandwidth at -3 dB Point	BW	V_i = 10 mV, R_s = 1 kΩ			-	650	-	kHz	7
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	f = 1 kHz		9	-	6.4	-	V(P-P)	NONE
Common-Mode Rejection Ratio	CMRR	f = 1 kHz		13	70	98	-	dB	8
Single-Ended Input Impedance	Z_{IN}	f = 1 kHz		15	70K	195K	-	Ω	10
Single-Ended Output Impedance	Z_{OUT}	f = 1 kHz		17	5.5K	8K	10.5K	Ω	12
Total Harmonic Distortion	THD	R_S=1kΩ f = 1 kHz V_O=42V_{p-p}			-	0.2	5	%	14
AGC Range (Maximum Voltage Gain to Complete Cutoff)	AGC	f = 1 kHz		20	80	90	-	dB	NONE

STATIC CHARACTERISTICS

INPUT OFFSET VOLTAGE AND CURRENT vs TEMPERATURE

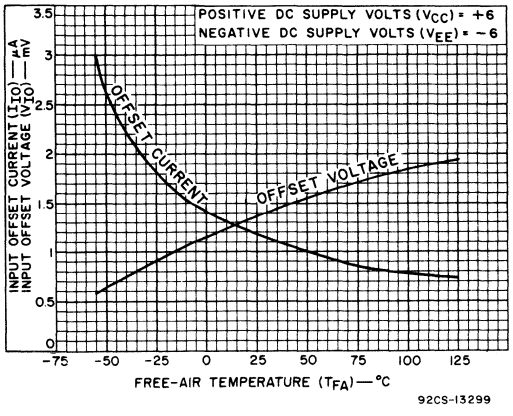


Fig.2

INPUT BIAS CURRENT vs TEMPERATURE

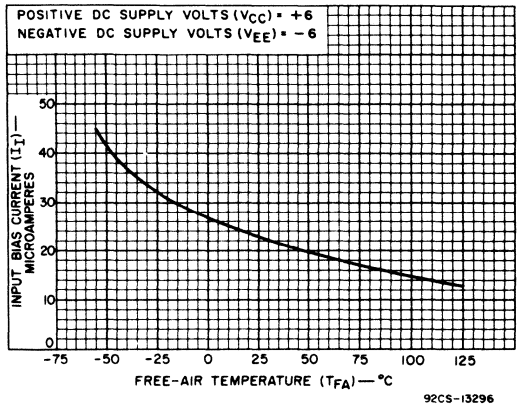


Fig.3

STATIC CHARACTERISTICS

QUIESCENT OPERATING VOLTAGE vs TEMPERATURE

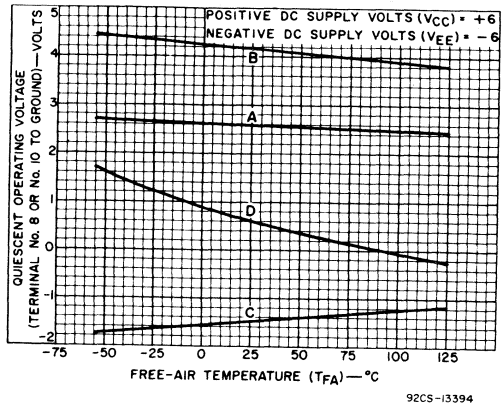


Fig. 4

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT FOR TYPE CA3000

DIFFERENTIAL VOLTAGE GAIN vs TEMPERATURE

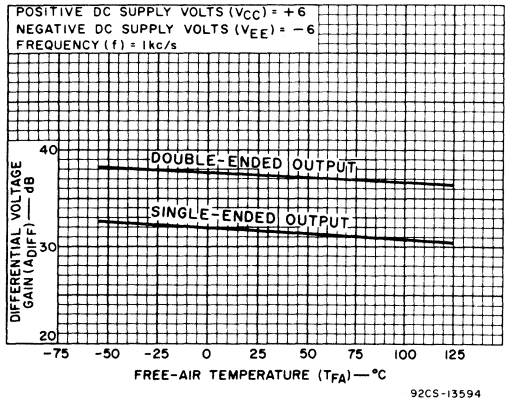


Fig. 5

DIFFERENTIAL VOLTAGE GAIN AND MAXIMUM OUTPUT VOLTAGE SWING TEST CIRCUIT

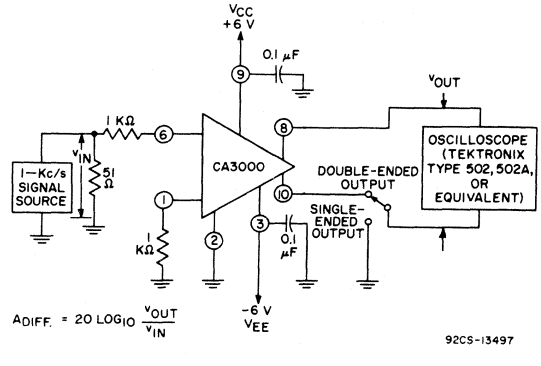


Fig. 6

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

BANDWIDTH AT -3 dB POINT vs TEMPERATURE

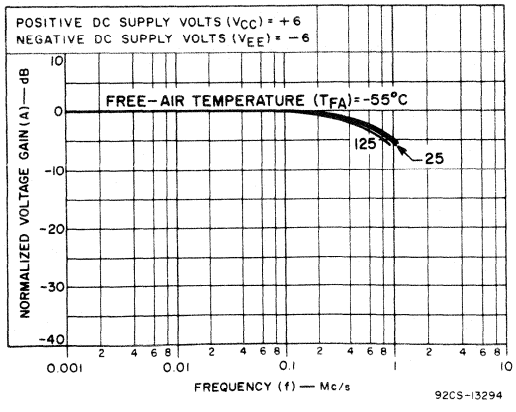


Fig. 7

COMMON-MODE REJECTION RATIO vs TEMPERATURE

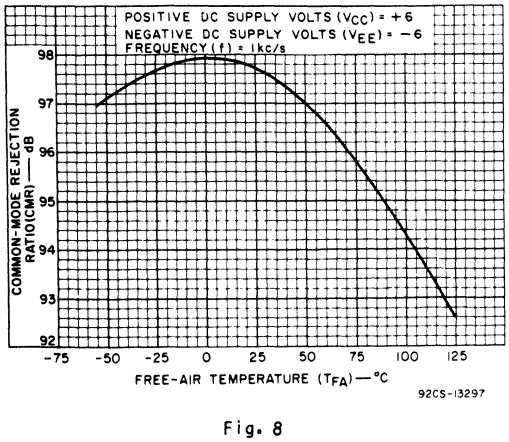
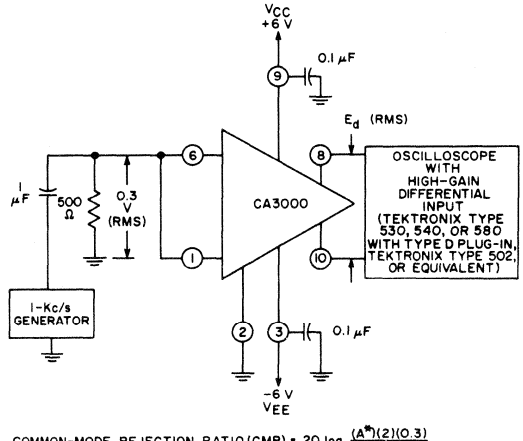


Fig. 8

COMMON-MODE REJECTION RATIO TEST CIRCUIT



COMMON-MODE REJECTION RATIO(CMR) = $20 \log \frac{(A^*)(2)(0.3)}{E_d\,(RMS)}$

*A = SINGLE-ENDED VOLTAGE GAIN

92CS-12983RI

Fig. 9

CA3000

DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPE CA3000

SINGLE-ENDED INPUT IMPEDANCE vs TEMPERATURE

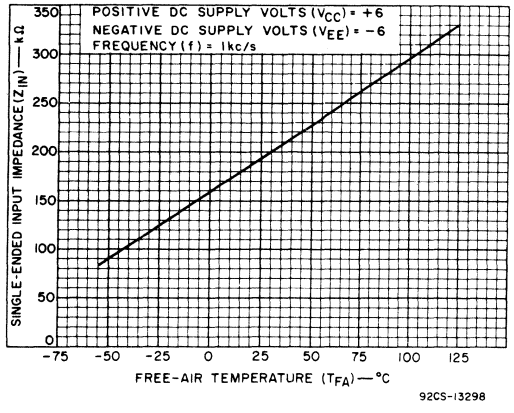


Fig. 10

SINGLE-ENDED INPUT IMPEDANCE TEST CIRCUIT

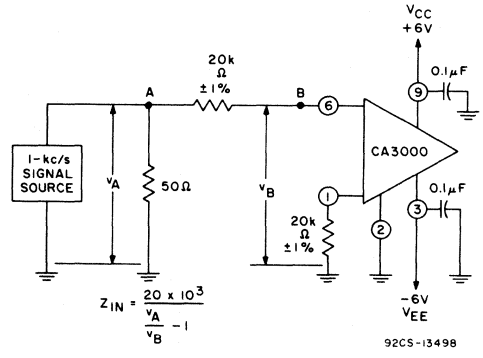


Fig. 11

SINGLE-ENDED OUTPUT IMPEDANCE vs TEMPERATURE

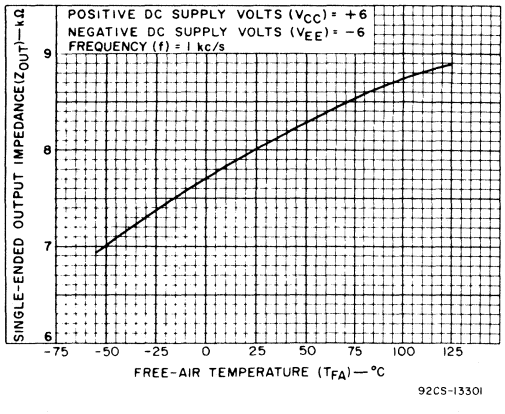
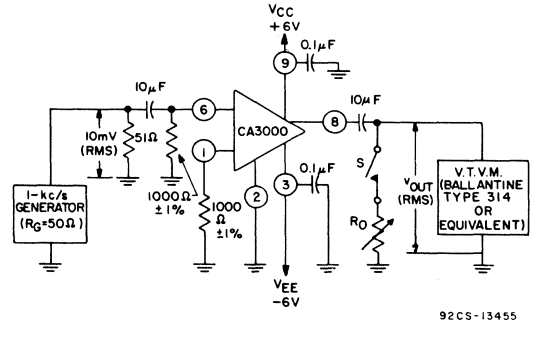


Fig. 12

SINGLE-ENDED OUTPUT IMPEDANCE TEST CIRCUIT



1. With Switch S open, record reference voltage V_{OUT}(rms).
2. Close Switch S, and adjust R_O until
   $V_{OUT} = \frac{\text{Reference Voltage}}{2}$
3. Record value of R_O as Z_{OUT}.

Fig. 13

DYNAMIC CHARACTERISTICS AND TEST CIRCUIT

TOTAL HARMONIC DISTORTION vs TEMPERATURE

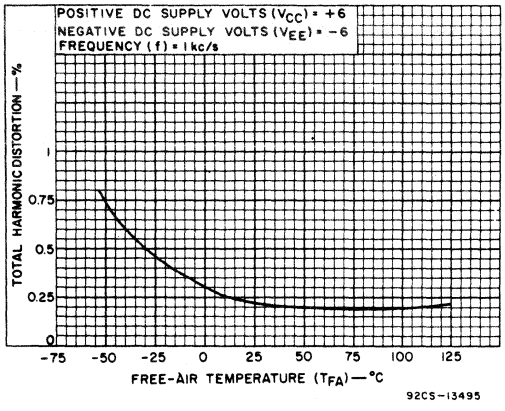
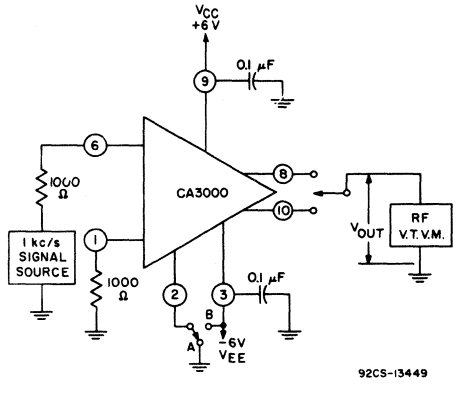


Fig. 14

AGC RANGE TEST CIRCUIT



$$\text{AGC Range} = 20 \log_{10} \frac{\text{A with S in Position A}}{\text{A with S in Position B}}$$

Fig. 15

CA3001

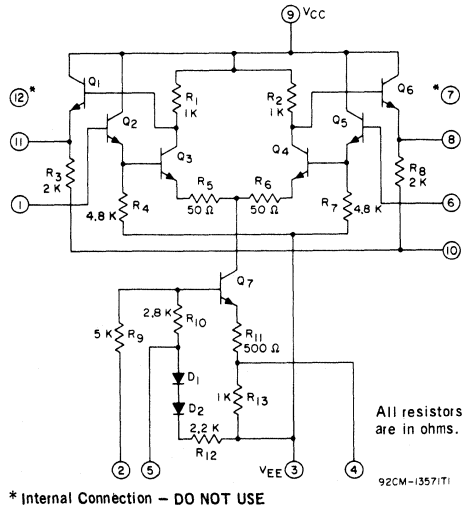
Video and Wide-band Amplifier

Features:

- *Designed for use in video systems and communication equipment*
- *Balanced differential amplifier configuration with controlled constant-current source provides outstanding versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Emitter follower input & output*
- *Companion Application Note ICAN5038 "Application of the RCA-CA3001 Integrated-Circuit Video Amplifier", covers different operating modes, gain control, distortion, swing capability, 3 stage amplifier design, and a Schmitt trigger study.*
- *Push-pull input & output*
- *AGC range - 60 dB typ.*
- *Bandwidth - 29 MHz*
- *Input resistance - 150 kΩ typ.*
- *Output resistance - 45 Ω typ.*
- *Voltage gain - 19 dB typ.*
- *Input offset voltage - 1.5 mV typ.*

Applications

- *Schmitt trigger*
- *Mixer*
- *Modulator*
- *DC, IF & video amplifier*



* Internal Connection – DO NOT USE

Fig. 1 — Schematic Diagram.

File Number **122**

ELECTRICAL CHARACTERISTICS, AT T_A = 25°C, V_{CC} = +6V, V_{EE} = -6V

CHARACTERISTICS (See Page 2 for Definitions of Terms)	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.4 and No.5 Not Connected Unless Specified			TEST CIRCUITS	LIMITS TYPE CA3001				TYPICAL CHARACTERISTICS CURVES
					Fig.	Min.	Typ.	Max.	Units	Fig.
STATIC CHARACTERISTICS:										
Input Offset Voltage	V_{IO}				4	-	1.5	-	mV	2
Input Offset Current	I_{IO}				5	-	1	10	μA	2
Input Bias Current	I_I				5	-	16	36	μA	3
Output Offset Voltage	V_{OO}	R_S = 1 kΩ				-	54	300	mV	6
Quiescent Operating Voltage	V_8 OR V_{11}	TERMINALS MODE	4	5						
		A	NC	NC		3.8	4.4	5	V	7
		B	NC	V_{EE}		-	4.8	-	V	7
		C	V_{EE}	NC		-	2.7	-	V	7
		D	V_{EE}	V_{EE}		-	4	-	V	7
Device Dissipation	P_D	A	NC	NC		60	78	120	mW	8
		B	NC	V_{EE}		-	71	-	mW	8
		C	V_{EE}	NC		-	110	-	mW	8
		D	V_{EE}	V_{EE}		-	86	-	mW	8
DYNAMIC CHARACTERISTICS:										
Differential Voltage Gain (Single-ended input and output)	A_{DIFF}	f = 1.75 MHz f = 20 MHz				16 10	19 14	-	dB dB	9 A, 9 B 9 B
Bandwidth at -3 dB Point	BW	R_S = 50Ω				16	29	-	MHz	NONE
Maximum Output Voltage Swing	$V_{OUT(P-P)}$	R_S = 50Ω f = 1.75 MHz				-	5	-	V_{P-P}	NONE
Noise Figure	NF	f = 1.75 MHz, R_S = 1 KΩ			14	-	5	8	dB	10
		f = 11.7 MHz, R_S = 1 KΩ			14	-	7.7	-	dB	10
Common-Mode Rejection Ratio	CMRR	f = 1 KHz			16	70	88	-	dB	12
Input Impedance Components:										
Parallel Input Resistance	R_{IN}	f = 1.75 MHz				50	140	-	KΩ	14
Parallel Input Capacitance	C_{IN}	f = 1.75 MHz				-	3.4	7	pF	14
Output Resistance	R_{OUT}	f = 1.75 MHz				-	45	70	Ω	NONE
AGC Range (Maximum voltage gain to complete cutoff)	AGC	f = 1.75 MHz			19	55	60	-	dB	NONE

TYPICAL STATIC CHARACTERISTICS

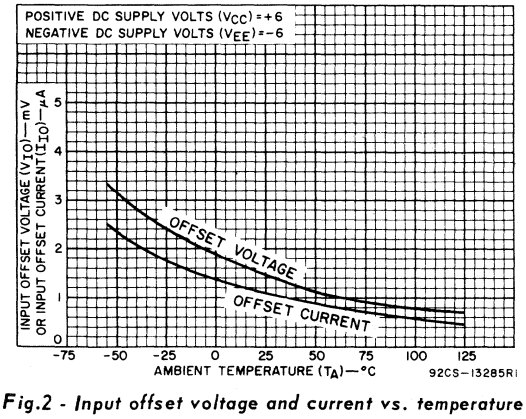


Fig.2 - Input offset voltage and current vs. temperature.

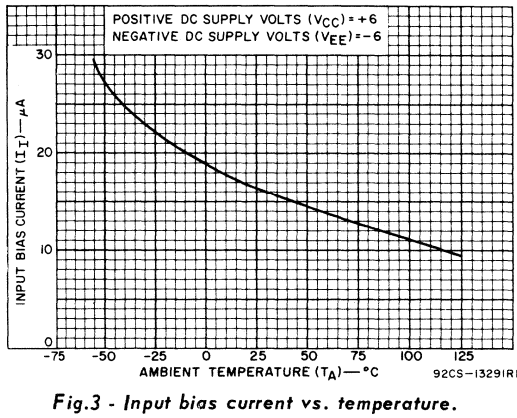


Fig.3 - Input bias current vs. temperature.

CA3001

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS at T_A = 25°C

Indicated voltage or current limits for each terminal can be applied under the specified conditions for other terminals.
All Voltages are with respect to ground (common terminal of Positive and Negative DC Supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-2.5	+2.5	2, 6 3, 10 9	0 -6 +6
2	-8.5	0	1, 6 3, 10 9	0 -8.5 +6
3	-10	0	1, 2, 6 9 10	0 +6 -6
4	-8.5	0	1, 2, 6 9 10	0 +6 -6
5	-6	0	1, 2, 6 3, 10 9	0 -6 +6
6	-2.5	+2.5	1, 2 3, 10 9	0 -6 +6
7	INTERNAL CONNECTION DO NOT USE			

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
8	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.8 & No.10	0 -6 +6
9	0	+10	1, 2, 6, 10 3	0 -6
10	-10	0	1, 2, 6 3 9	0 -6 +6
11	25 mA		1, 2, 6, 10 3 9 200-Ω RESISTOR CONNECTED BETWEEN TERMINALS No.10 & No.11	0 -6 +6
12	INTERNAL CONNECTION DO NOT USE			
CASE	INTERNALLY CONNECTED TO TERMINAL No.3 (SUBSTRATE) DO NOT GROUND			

OPERATING TEMPERATURE RANGE ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE ..... -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ±1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

MAXIMUM SINGLE-ENDED INPUT-SIGNAL VOLTAGE ..... ± 4 V

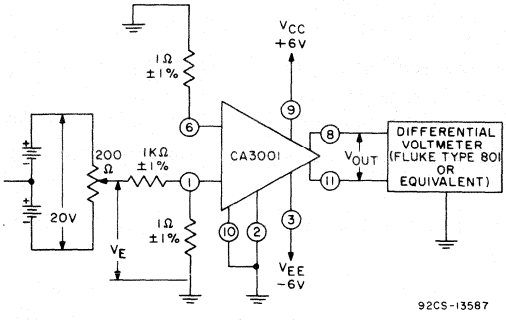
MAXIMUM COMMON-MODE INPUT-SIGNAL VOLTAGE ..... ± 2.5 V

MAXIMUM DEVICE DISSIPATION:

-55 to 85°C ..... 450 mW

Above 85°C ..... Derate linearly 5 mW/°C

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS



Adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ V 2. Measure V_E and record input offset voltage (V_{IO}) in mV as $V_{IO} = \frac{V_E}{1000}$

Fig.4 - Input offset voltage test circuit.

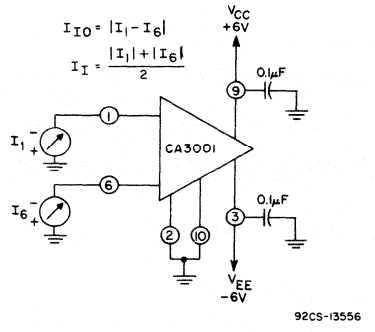


Fig.5 - Input offset current and input bias current test circuit.

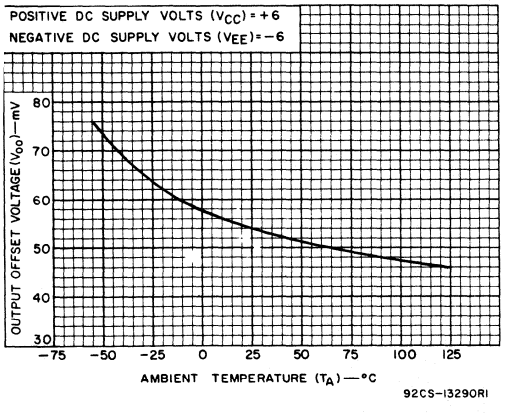


Fig.6 - Output offset voltage vs. temperature.

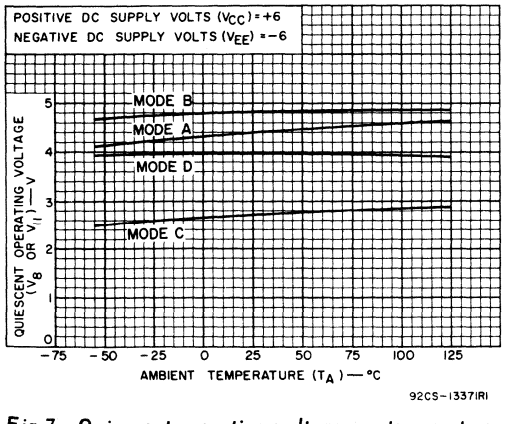


Fig.7 - Quiescent operating voltage vs. temperature.

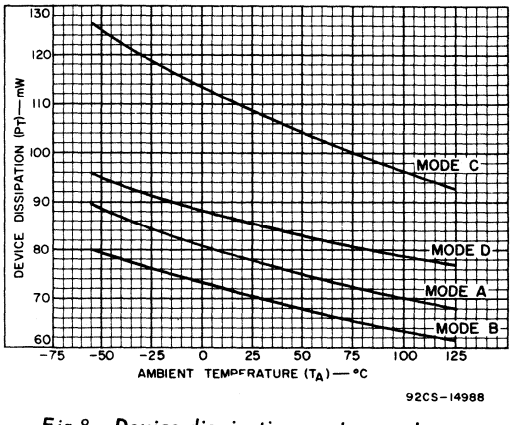


Fig.8 - Device dissipation vs. temperature.

CA3001

TYPICAL DYNAMIC CHARACTERISTICS

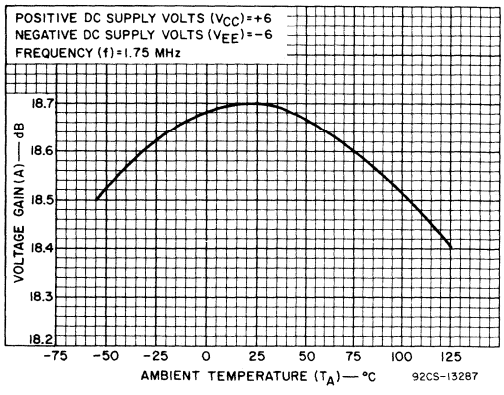


Fig.9 a - Differential voltage gain vs. temperature.

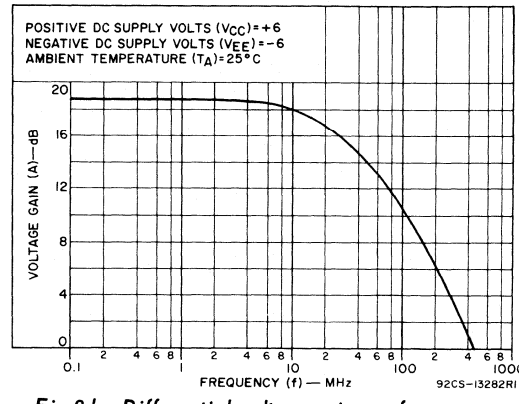


Fig.9 b - Differential voltage gain vs. frequency.

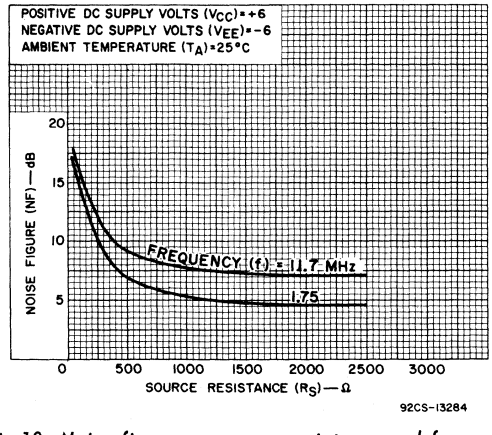
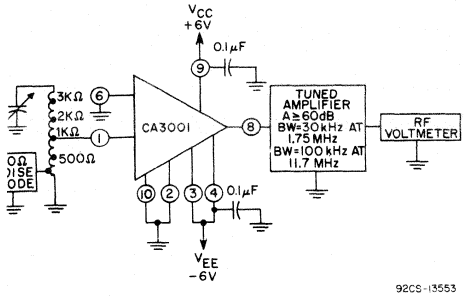


Fig.10 - Noise figure vs. source resistance and frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS



arate tuned input circuits are used for 1.75 MHz and 11.7 MHz. rce-resistance matching taps adjusted with circuit tuned to ɔnance and with 50-ohm resistor connected to simulate se diode.

Fig.11 - Noise figure test circuit.

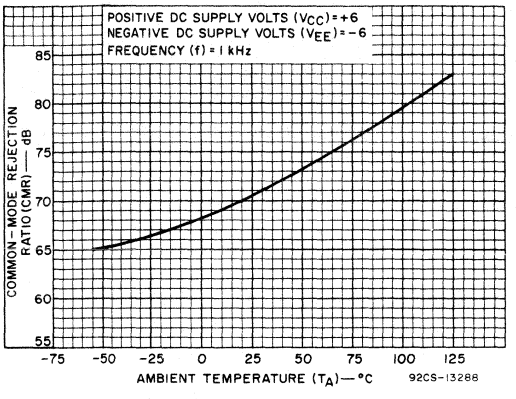


Fig.12 - Common-mode rejection ratio vs. temperature.

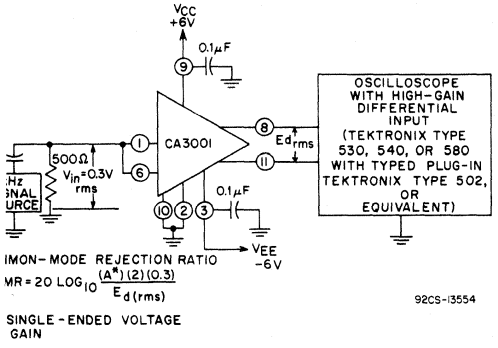


Fig.13 - Common-mode rejection ratio test circuit.

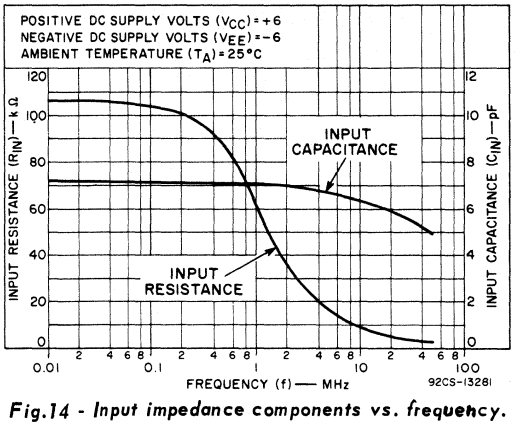


Fig.14 - Input impedance components vs. frequency.

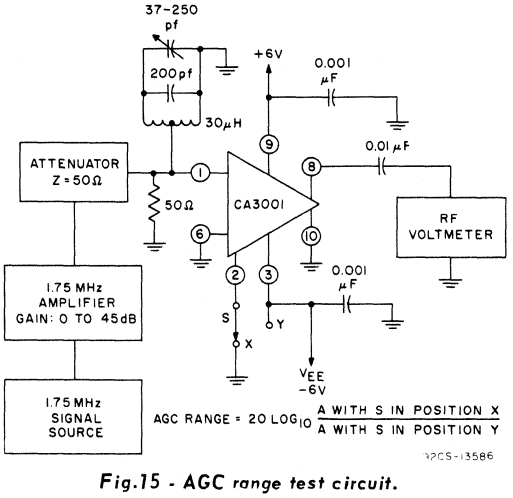


Fig.15 - AGC range test circuit.

CA3002

IF Amplifier

For Use in Communication Equipment

Features:

- *Input resistance - 100 kΩ typ.*
- *Output resistance - 70 Ω typ.*
- *Voltage gain - 24 dB typ. @ 1.75 MHz*
- *Push-pull input, single-ended output*
- *-3 dB bandwidth - 11 MHz typ.*
- *AGC range - 80 dB typ.*
- *Useful frequency range DC to 15 MHz.*

The RCA-CA3002 integrated-circuit IF amplifier is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled IF amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

The CA3002 is supplied in the 10-lead hermetic TO-5 style package.

Applications:

- *Product detector*
- *IF & video amplifier*
- *AM detector*
- *Schmitt trigger*

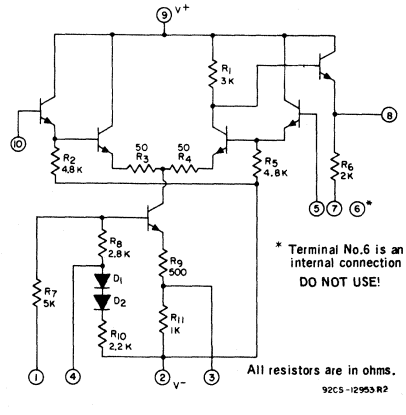


Fig. 1 — Schematic diagram.

File Number **123**

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

COMMON-MODE INPUT SIGNAL VOLTAGE . . . . . ±2 V
MAXIMUM POWER SUPPLY VOLTAGE . . . . . 16 V or ±8 V
OPERATING-TEMPERATURE RANGE . . . . . −55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . . . −65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE . . . . . ±4 V
MAXIMUM DEVICE DISSIPATION:
−55 to 85°C . . . . . 450 mW
Above 85°C . . . . . Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V

CHARACTERISTICS	SPECIAL TEST CONDITIONS TERMINALS No. 3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002			UNITS
		Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS						
Input Unbalance Voltage V_{IU}		4	–	2.2	–	mV
Input Unbalance Current I_{IU}		5	–	2.2	10	μA
Input Bias Current I_I		5	–	20	36	μA
Quiescent Operating Voltage	MODE A: TERMINAL 2 = V_{EE}, 4 = NC	7a	–	2.8	–	V
	MODE B: TERMINAL 2 = V_{EE}, 4 = V_{EE}	8b	–	3.9	–	V
Device Dissipation P_T		4	–	55	–	mW
DYNAMIC CHARACTERISTICS						
Differential Voltage Gain A_{DIF} (Single-Ended Input and Output)	f = 1.75 MHz	10	19	24	–	dB
Bandwith at −3 dB Point BW	–	10	–	11	–	MHz
Maximum Output Voltage Swing V_{OUT}(P-P)	–	10	–	5.5	–	V_{P-P}
Noise Figure NF	f = 1.75 MHz R_S = 1 kΩ	12	–	4	8	dB
Input Impedance Components: Parallel Input Resistance R_{IN}	f = 1.75 MHz	None	–	100k	–	Ω
Parallel Input Capacitance C_{IN}	f = 1.75 MHz	None	–	4	–	pF
Output Resistance R_{OUT}	f = 1.75 MHz	14	–	70	–	Ω
3rd Harmonic Intermodulation Distortion IMD	–	16	−30	−40	–	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff AGC	f = 1.75 MHz	18	60	80	–	dB

CA3002

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$) or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	−8 V	0 V	2, 7 5, 10 9	−8 0 +6
2	−10 V	0 V	1, 5, 10 9	0 +6
3	−8.5 V	0 V	1, 5, 10 7 9	0 −6 +6
4	−8 V	0 V	1, 5, 10 2, 7 9	0 −8 +6
5	−3.5 V	+3.5 V	1, 10 2, 7 9	0 −6 +6
6	INTERNAL CONNECTION DO NOT USE			
7	−12 V	0 V	1, 5, 10 2 9	0 −6 +6
8	20 mA		1, 5, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 −6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 −6
10	−3.5 V	+3.5 V	1, 5 2, 7 9	0 −6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

STATIC CHARACTERISTICS

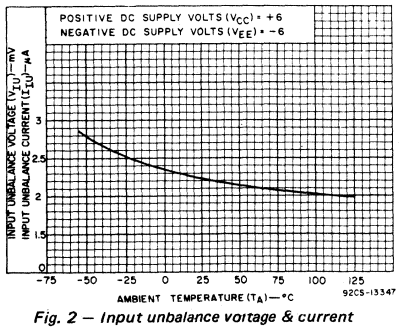


Fig. 2 — Input unbalance voltage & current vs temperature.

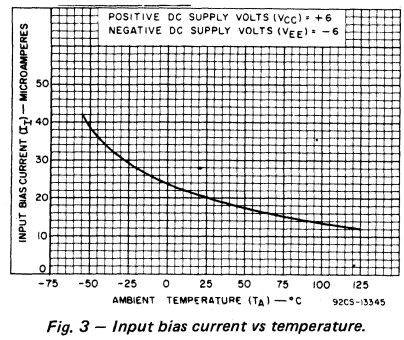


Fig. 3 — Input bias current vs temperature.

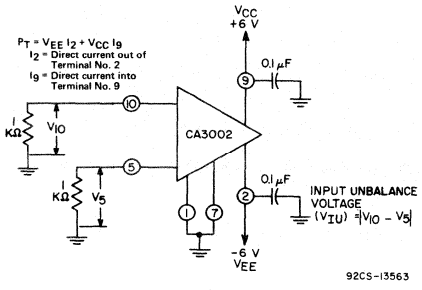


Fig. 4 – Input unbalance voltage and device dissipation test circuit.

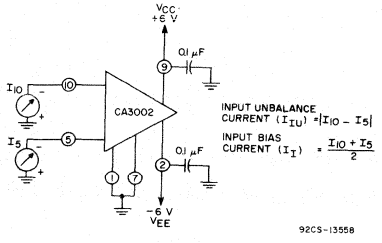


Fig. 5 – Input unbalance current & bias current test circuit.

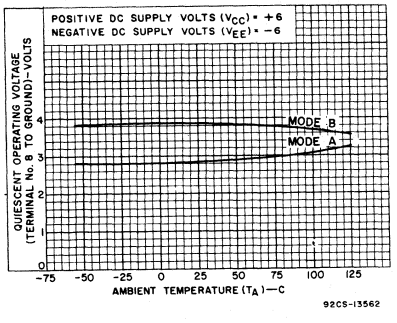


Fig. 6 – Quiescent operating voltage vs temperature.

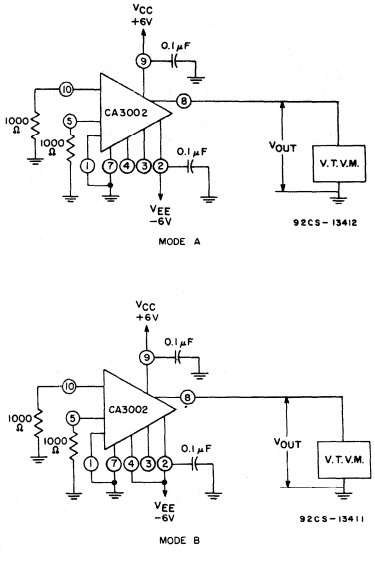


Fig. 7 – Quiescent operating voltage.

DYNAMIC CHARACTERISTICS

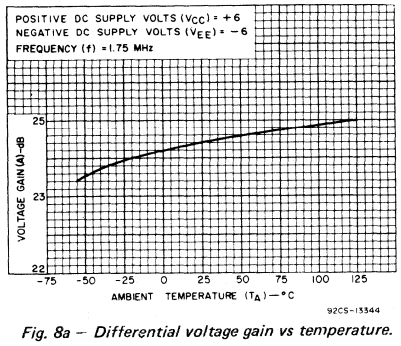


Fig. 8a – Differential voltage gain vs temperature.

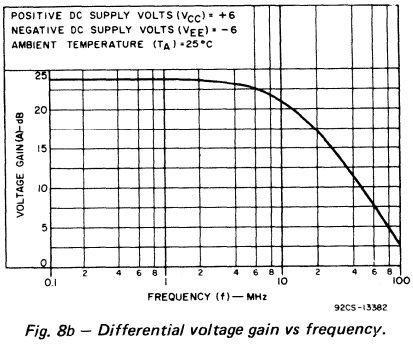


Fig. 8b – Differential voltage gain vs frequency.

CA3002

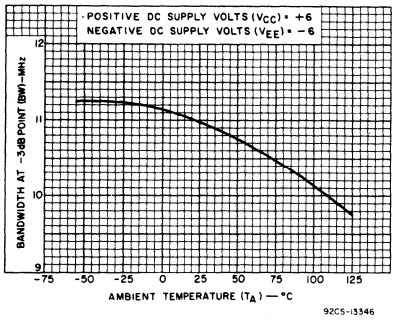


Fig. 9 — Bandwidth of −3 dB point vs temperature.

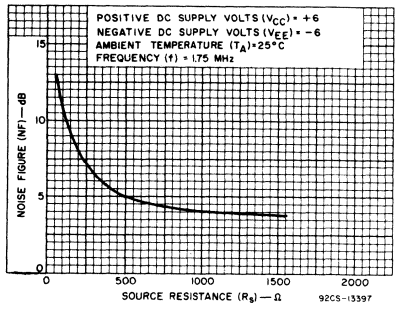


Fig. 11 — Noise figure vs source resistance.

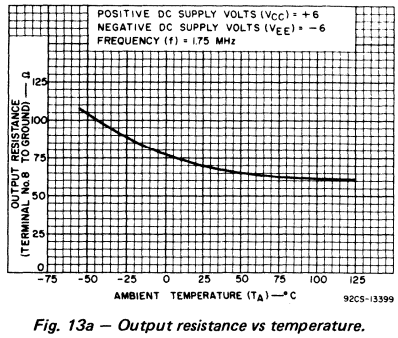


Fig. 13a — Output resistance vs temperature.

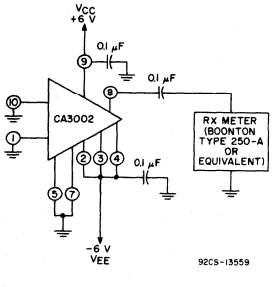


Fig. 14 — Output resistance.

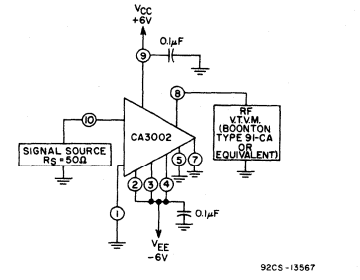
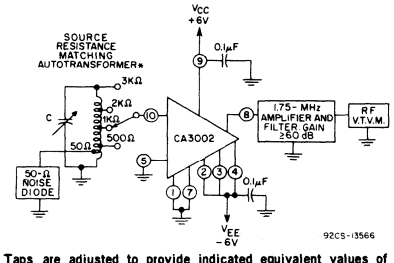


Fig. 10 — Differential voltage gain, −3 dB bandwidth, and maximum output voltage swing.



*** Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.**

Fig. 12 — Noise figure.

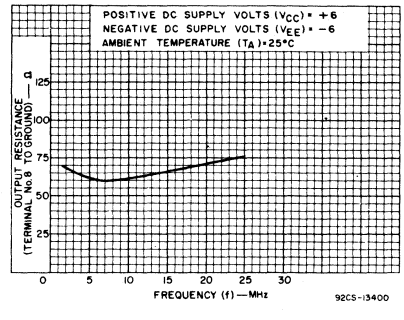


Fig. 13b — Output resistance vs frequency.

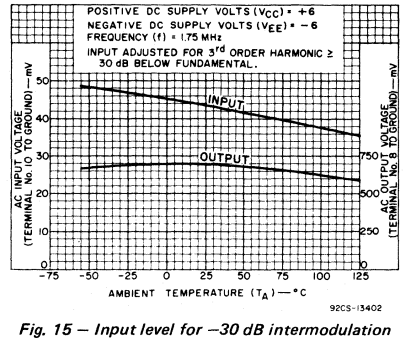
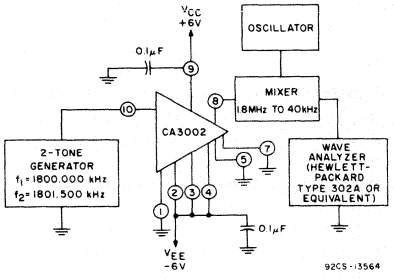


Fig. 15 — Input level for −30 dB intermodulation vs temperature.



1) Increase both input-signal tones until the $2f_2$-$f1$ and $2f_1$-$f2$ output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 16 – Intermodulation circuit.

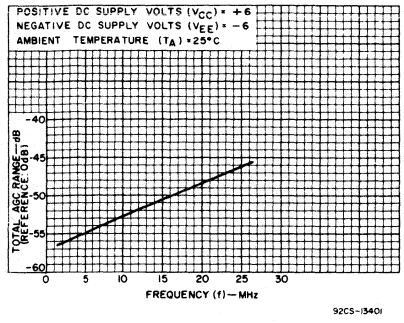
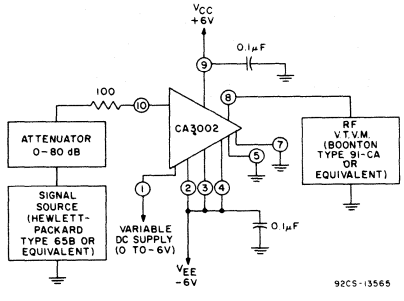


Fig. 17 – AGC range vs frequency.



1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

Fig. 18 – AGC range.

CA3005, CA3006
RF Amplifiers

Features:

- *Designed for use in communications equipment*
- *Balanced differential amplifier configuration with controlled constant-current source to provide unexcelled versatility*
- *Built-in temperature stability for operation from −55° C to +125° C*
- *Companion Application Note, ICAN 5022 "Application of RCA CA3004, CA3005, and CA3006 Integrated Circuit RF Amplifiers", covers characteristics of different operating modes, noise performance, cross-modulation, mixer, AGC limiter, detector, and amplifier design considerations.*

Applications:

- *Push-pull input and output*
- *Wide and narrow band amplifier*
- *AGC*
- *Detector*
- *RF, IF, and video frequency capability*
- *Operation from DC to 100 MHz*
- *Mixer*
- *Limiter*
- *Modulator*
- *Cascade Amplifier*

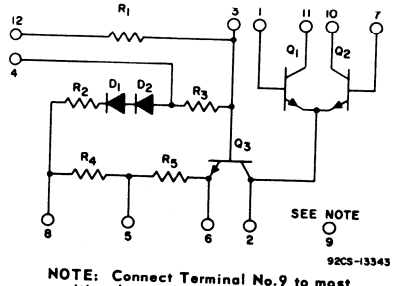


Fig. 1 — Schematic Diagram for CA3005 and CA3006.

ABSOLUTE-MAXIMUM VOLTAGE LIMITS, at T_{FA} = 25°C

Voltage limits shown for each terminal can be applied under the indicated voltage conditions for other terminals.
All voltages are with respect to GROUND (common terminal of Positive and Negative DC Supplies)

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3.5	+3.5	7 8 9 10 11 12	0 -6 +6 +6 +6 0
2	TEST POINT: DO NOT APPLY VOLTAGE FROM EXTERNAL SOURCE			
3	-9.5	0	1 7 8 9 10 11 12	0 0 -9.5 +6 +6 +6 0
4	-6	0	1 7 8 9 10 11 12	0 0 -6 +6 +6 +6 0
5	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
6	-6	0	1 7 9 10 11 12	0 0 +6 +6 +6 -6
7	-3.5	+3.5	1 8 9 10 11 12	0 -6 +6 +6 +6 0
8	-12	0	1 7 9 10 11 12	0 0 +6 +6 +6 0
9	0	+12	1 7 8 10 11 12	0 0 -6 +6 +6 0
10	0	+12	1 7 8 9 11 12	0 0 -6 +6 +6 0
11	0	+12	1 7 8 9 10 12	0 0 -6 +6 +6 0
12	-9.5	0	8 9 10 11	-9.5 +6 +6 +6
CASE	Internally connected to Terminal No.8 (substrate) DO NOT GROUND			

OPERATING-TEMPERATURE RANGE . . . . . -55°C to +125°C

STORAGE-TEMPERATURE RANGE . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

MAXIMUM SINGLE-ENDED INPUT-
SIGNAL VOLTAGE . . . . . ±3.5 V

MAXIMUM COMMON-MODE INPUT-
SIGNAL VOLTAGE . . . . . -2.5 V, +3.5 V

MAXIMUM DEVICE DISSIPATION . . . . . 300 mW

CA3005, CA3006

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V_{CC} = +6V$, $V_{EE} = -6V$

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS Terminals No.3,4,5, and 6 Not Connected Except Where Noted	TEST CIRCUITS	LIMITS							TYPI CHAR TERIS CURV
				TYPE CA3005			TYPE CA3006				
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig
STATIC CHARACTERISTICS											
Input Offset Voltage	V_{IO}		Fig.3	–	2.6	5	–	0.8	1	mV	Fig.
Input Offset Current	I_{IO}		Fig.4	–	1.4	–	–	1.4	–	μA	Fig.
Input Bias Current	I_{IB}		Fig.4	–	19	40	–	19	40	μA	Fig.
Quiescent Operating Current	I_{10} or I_{11}	TERMINALS 4 / 5									
		NC / NC	Fig.8	–	1	–	–	1	–	mA	Fig.
		NC / $-V_{EE}$	Fig.8	–	2.7	–	–	2.7	–	mA	NON
		$-V_{EE}$ / NC	Fig.8	–	0.45	–	–	0.45	–	mA	NON
		$-V_{EE}$ / $-V_{EE}$	Fig.8	–	1.25	–	–	1.25	–	mA	Fig.
Quiescent Operating Current Ratio	$\frac{I_{10}}{I_{11}}$		Fig.8	–	1.05	–	–	1.05	–	–	Fig.
Device Dissipation	P_T		Fig.8	–	26	–	–	26	–	mW	NONE
DYNAMIC CHARACTERISTICS											
Power Gain	G_p	f = 100 MHz, Cascode Configuration	Fig.10	16	20	–	16	20	–	dB	Fig.9
		f = 100 MHz, Differential-Ampl. Configuration	Fig.12	14	16	–	14	16	–	dB	Fig.1
Noise Figure	NF	f = 100 MHz, Cascode Configuration	Fig.10	–	7.8	9	–	7.8	9	dB	Fig.1
		f = 100 MHz, Differential Ampl. Configuration	Fig.12	–	7.8	9	–	7.8	9	dB	Fig.14
Common-Mode Rejection Ratio	CMR	f = 1 kHz	Fig.16	–	101	–	–	101	–	dB	Fig.15
AGC Range (Max. Voltage Gain to Complete Cutoff)	AGC	f = 1.75 MHz	Fig.17	-60	–	–	-60	–	–	dB	NONE

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

INPUT OFFSET VOLTAGE AND CURRENT

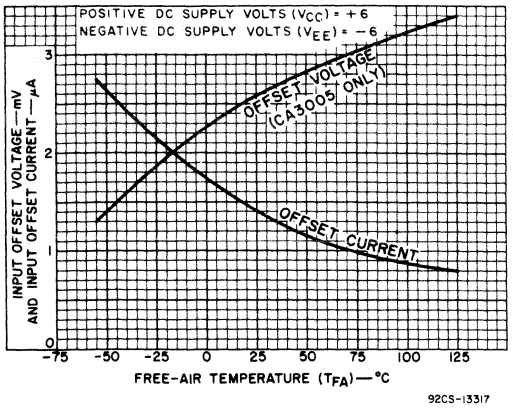


Fig. 2

INPUT OFFSET VOLTAGE TEST CIRCUIT

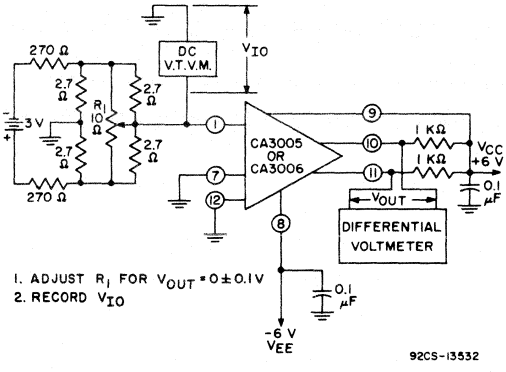


Fig. 3

INPUT BIAS CURRENT

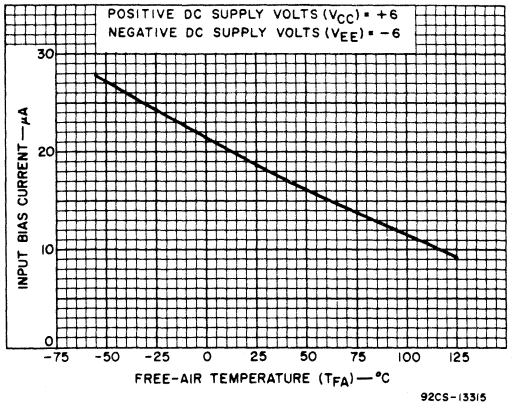


Fig. 4

QUIESCENT OPERATING CURRENT

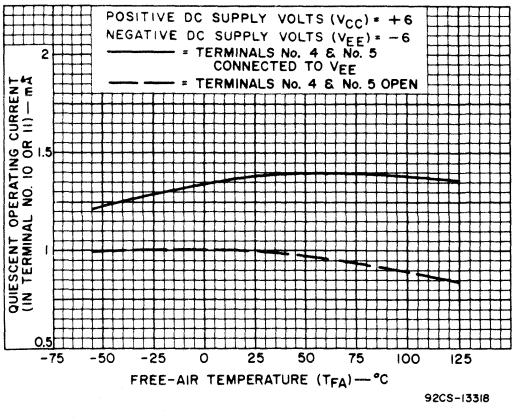


Fig. 5

QUIESCENT OPERATING CURRENT RATIO

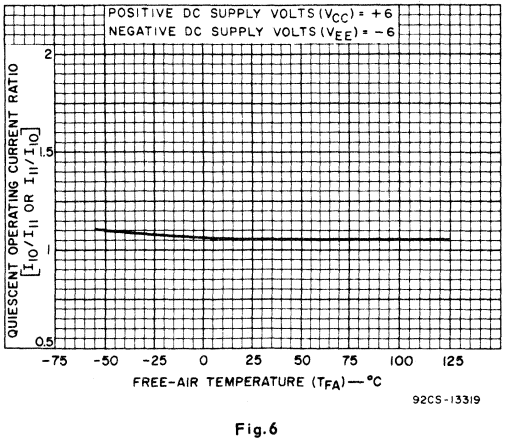


Fig. 6

CA3005, CA3006

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS FOR TYPES CA3005 AND CA3006

POWER-GAIN (CASCODE CONFIGURATION)

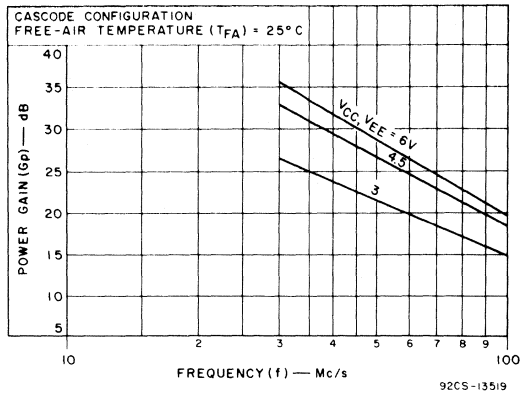


Fig.7

POWER-GAIN (DIFFERENTIAL-AMPLIFIER CONFIGURATION)

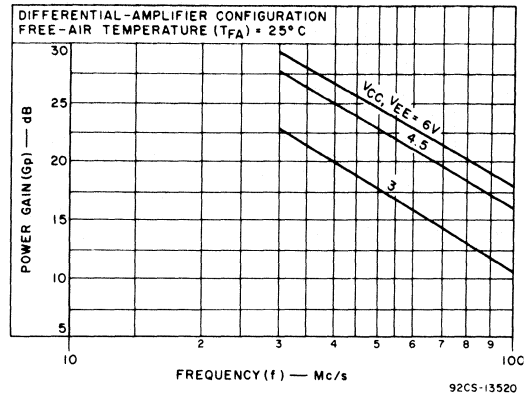
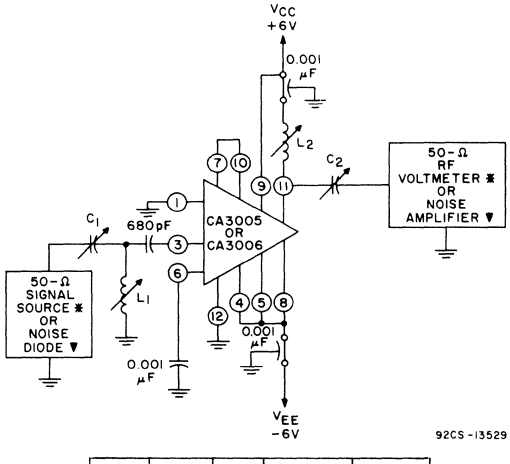


Fig.9

NOISE FIGURE AND POWER GAIN TEST CIRCUIT (CASCODE CONFIGURATION)



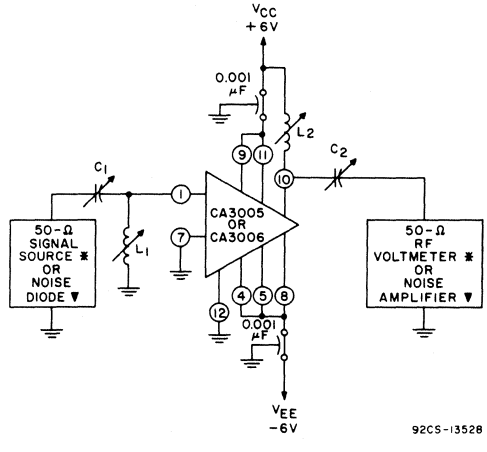
f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	14-150	5-40	0.3-0.6	0.8-1.4
100	5-40	5-40	0.07-0.12	0.15-0.3

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 8

NOISE FIGURE AND POWER-GAIN TEST CIRCUIT (DIFFERENTIAL AMPLIFIER CONFIGURATION)



f Mc/s	C_1 pF	C_2 pF	L_1 μH	L_2 μH
30	5-40	1.5-20	1.2-2	1.2-2
100	1-12	1-12	0.4-0.7	0.25-0.5

* FOR POWER-GAIN TEST

▼ FOR NOISE-FIGURE TEST

Fig. 10

TYPICAL DYNAMIC CHARACTERISTICS FOR TYPES CA3005 AND CA3006

100-Mc/s NOISE FIGURE VS. V_{EE} (CASCODE CONFIGURATION)

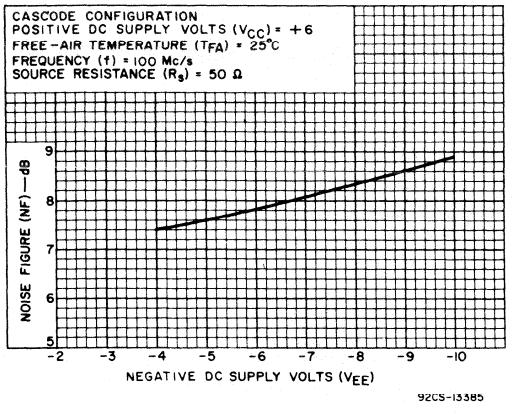


Fig. 11

100 Mc/s NOISE FIGURE VS. V_{EE} (DIFFERENTIAL AMPLIFIER CONFIGURATION)

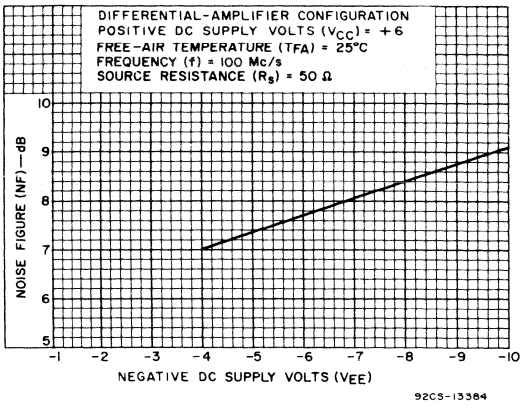


Fig. 12

COMMON-MODE-REJECTION RATIO

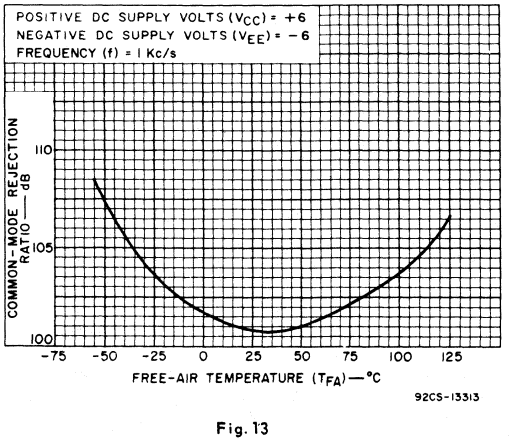


Fig. 13

CA3005, CA3006

TYPICAL DYNAMIC TEST CIRCUITS FOR TYPES CA3005 AND CA3006

COMMON-MODE REJECTION RATIO TEST CIRCUIT

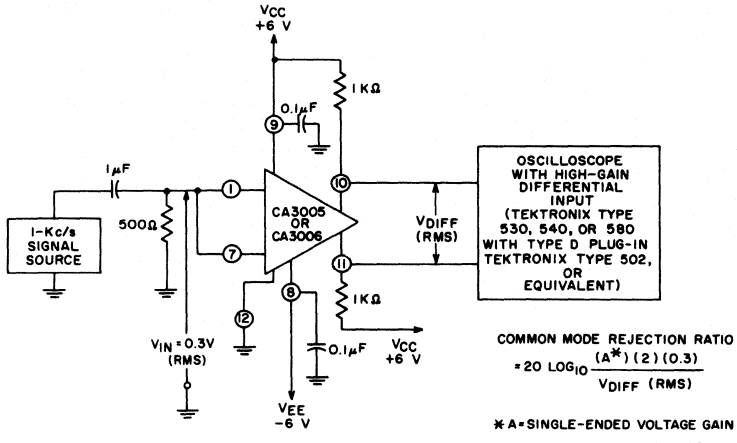


Fig. 14

AGC RANGE TEST CIRCUIT

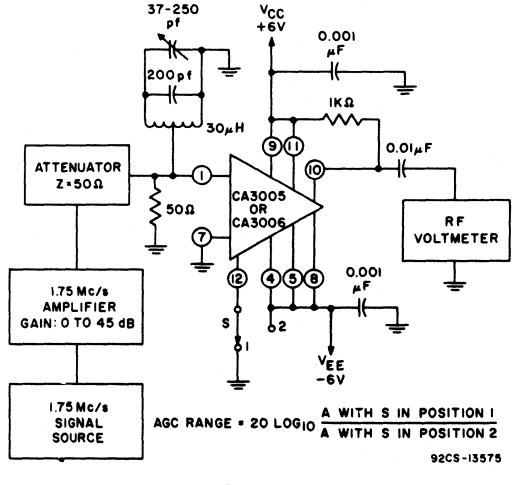


Fig. 15

CA3026, CA3054

ransistor Array - Dual Independent ifferential Amplifiers

or Low Power Applications
t Frequencies from DC to 120 MHz

eatures

Two differential amplifiers on a common substrate
Independently accessible inputs and outputs
Maximum input offset voltage - ± 5 mV
Full military temperature-range capability - −55° C to +125° C
Limited temperature range - 0° C to 85° C for CA3054

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general-purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3026 is supplied in a hermetic 12-lead TO-5-style package and is rated for full military operating-temperature range of −55° C to +125° C.

The CA3054 is supplied in a 14-lead plastic dual-in-line package with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility.

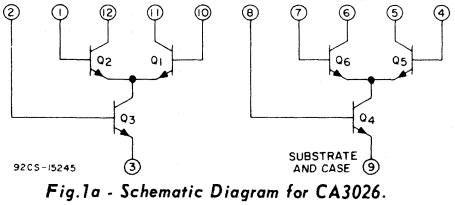


Fig.1a - Schematic Diagram for CA3026.

Applications

- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Multifunction combinations - RF/Mixer/Oscillator; Converter/IF*
- *IF amplifiers (differential and/or cascode)*
- *Product detectors*
- *Doubly balanced modulators and demodulators*
- *Balanced quadrature detectors*
- *Cascade limiters*
- *Synchronous detectors*
- *Pairs of balanced mixers*
- *Synthesizer mixers*
- *Balanced (push-pull) cascode amplifiers*

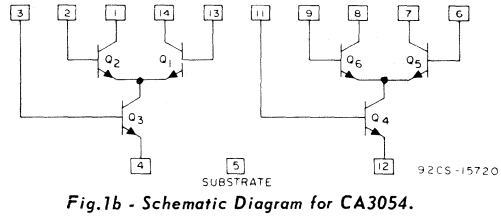


Fig.1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

File Number **338**

CA3005, CA3006

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

Power Dissipation, P:	CA3026	CA3054	
Any one transistor	300	300	mW
Total package	600	750	mW
For T_A > 55°C	Derate at 5	6.67	mW/°C
Temperature Range:			
Operating	-55 to + 125	-40 to +85	°C
Storage	-65 to + 150	-65 to +150	°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained a signal (AC) ground by means of a suitable grounding capacitor, to avoi undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1† and horizontal terminal 3† is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →		13	14	1	2	3	4	6	7	8	9	11	12	5
↓	CA3026 → TERMINAL No. ↓	10	11	12	1	2	3	4	5	6	7	8	Note 1 9	Note 1 9
13	10		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14	11			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1	12				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2	1					*	+15 -5	*	*	*	*	*	*	*
3	2						+1 -5	*	*	*	*	*	*	*
4	3							*	*	*	*	*	*	*
6	4								0 -20	*	+5 -5	*	+15 -5	*
7	5									*	*	*	*	+20 0
8	6										+20 0	*	*	+20 0
9	7											*	+15 -5	*
11	8												+1 -5	*
12	9													*
5	9													Ref Sub-strate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4, the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No.●	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

● Terminal No.10 of CA3054 is not used

CA3026, CA3054

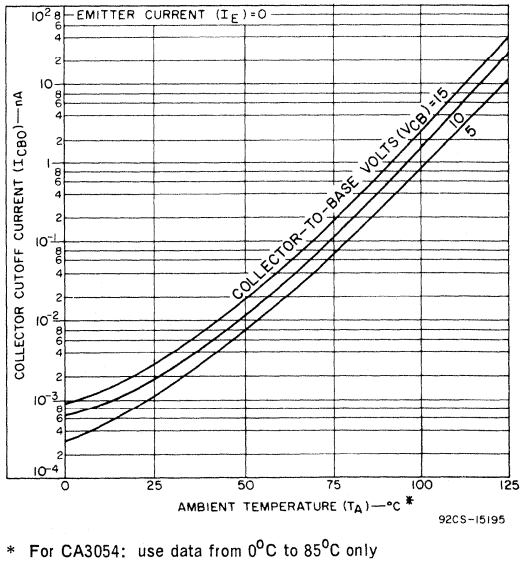
ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT FIG.	CA3026 CA3054 LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} 3 V, I_C = 50 μA	-	-	0.630	0.700	V	6
		1 mA	-	-	0.715	0.800		
		3 mA	-	-	0.750	0.850		
		10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_X = -3.3 V f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

CA3026, CA3054

DYNAMIC CHARACTERISTICS CONT'D.								
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

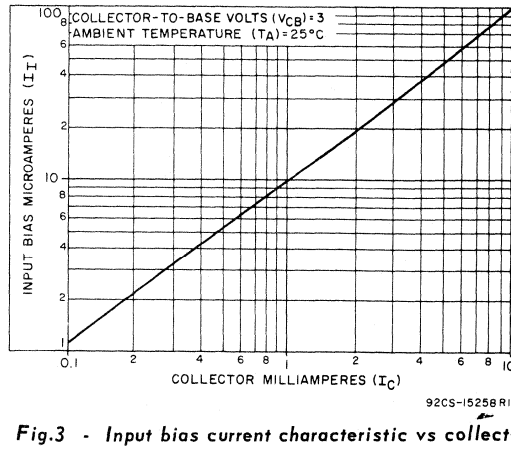


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL STATIC CHARACTERISTICS

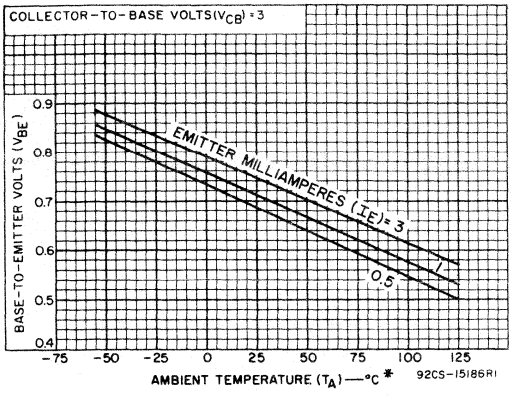


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

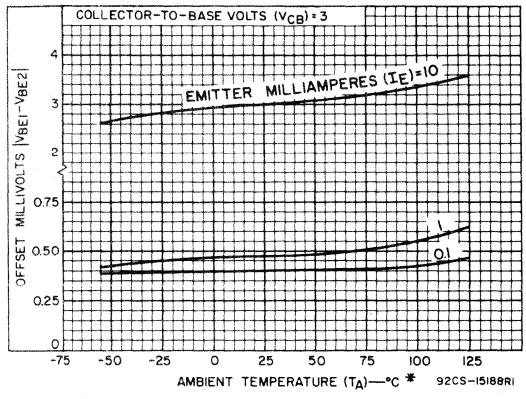


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

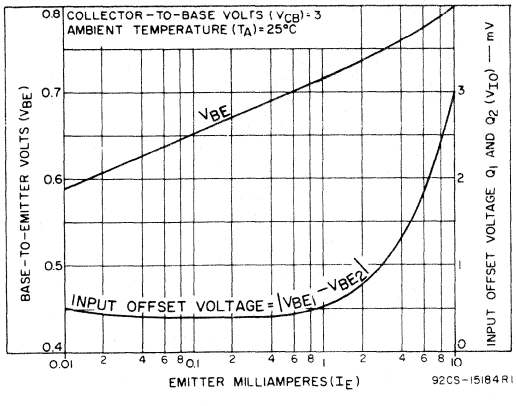


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

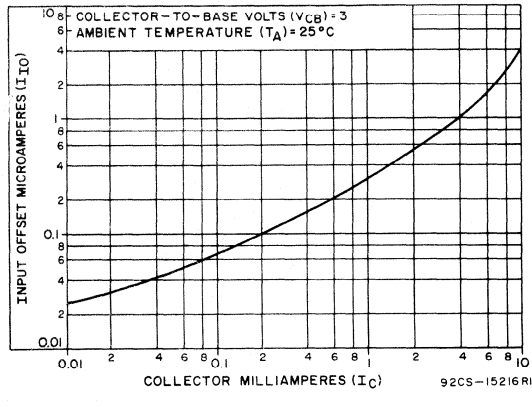


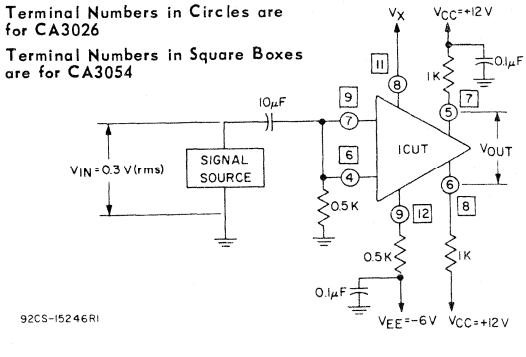
Fig.7 - Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

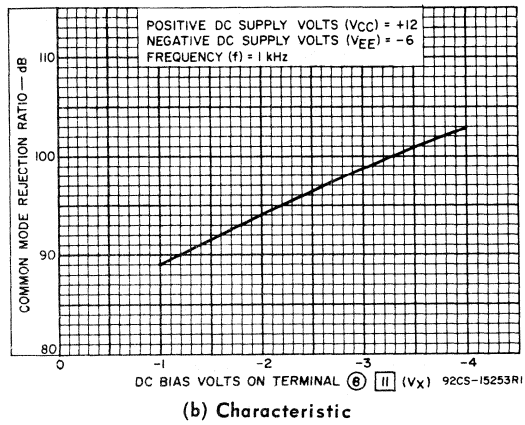
COMMON MODE REJECTION RATIO

Terminal Numbers in Circles are for CA3026

Terminal Numbers in Square Boxes are for CA3054



(a) Test setup



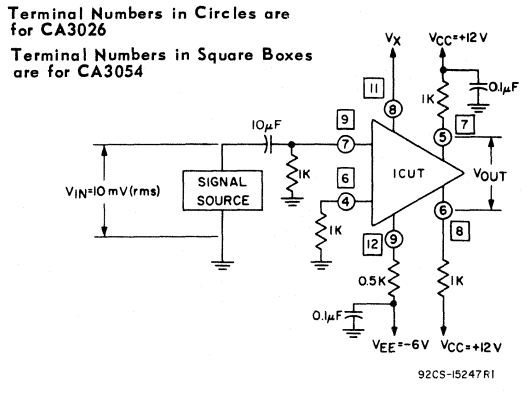
(b) Characteristic

Fig.8

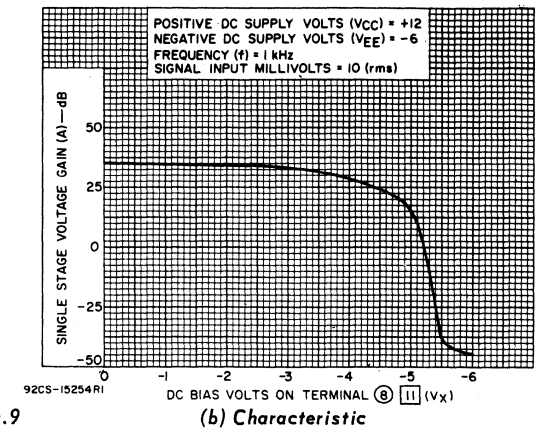
CA3026, CA3054

TYPICAL DYNAMIC CHARACTERISTICS (cont'd)

SINGLE-STAGE VOLTAGE GAIN



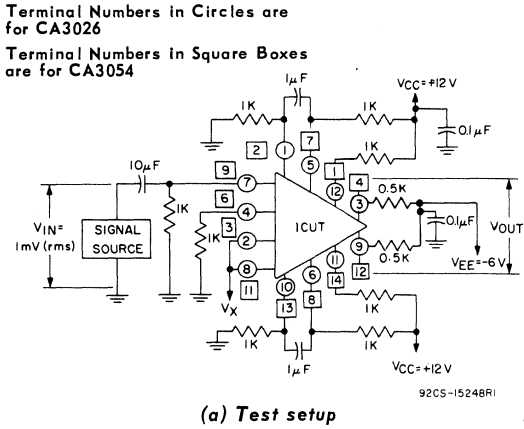
(a) Test setup



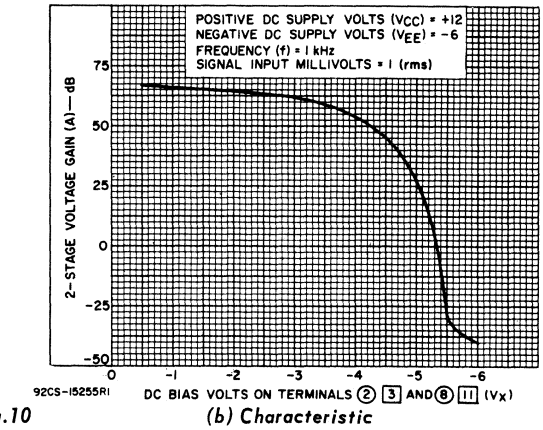
(b) Characteristic

Fig.9

TWO-STAGE VOLTAGE GAIN



(a) Test setup



(b) Characteristic

Fig.10

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

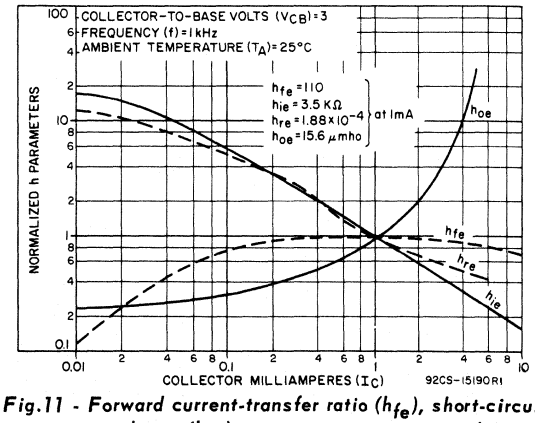


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

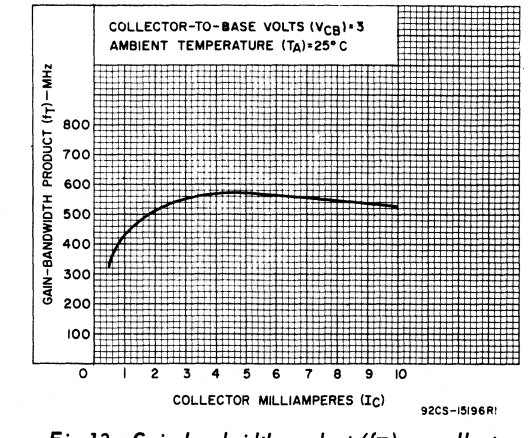


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

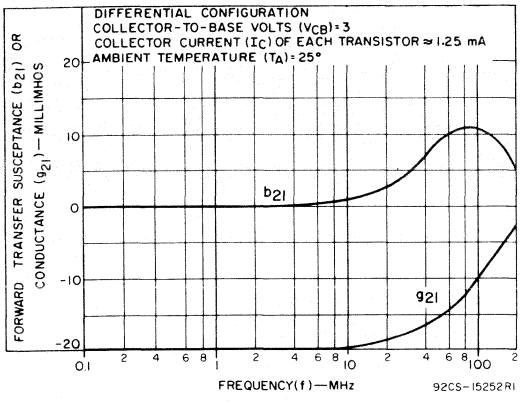


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

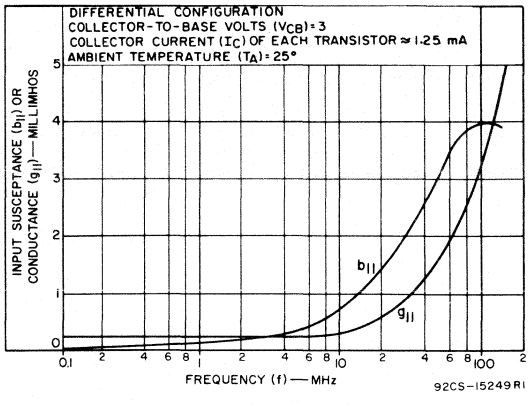


Fig.13(b) - Input admittance (Y_{11}).

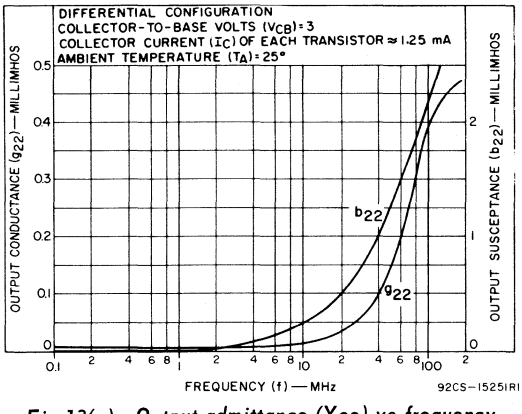


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

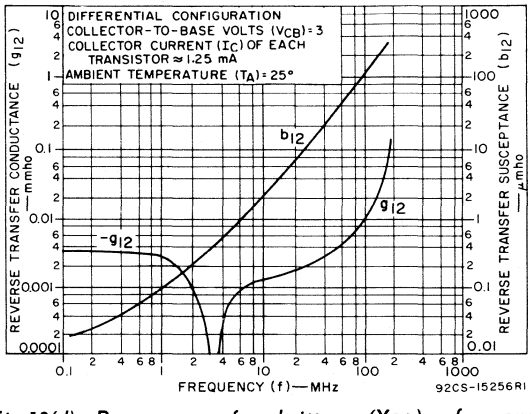


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

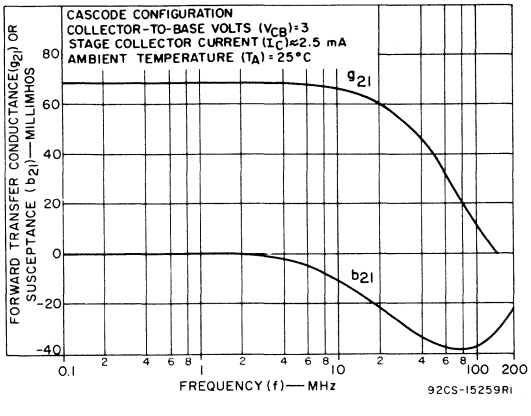


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

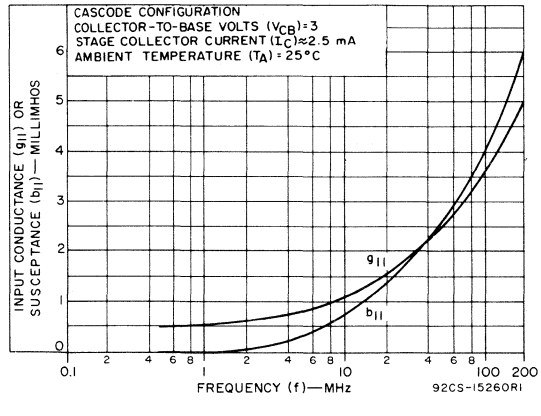


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

CA3026, CA3054

TYPICAL CHARACTERISTICS FOR EACH CASCODE AMPLIFIER (cont'd)

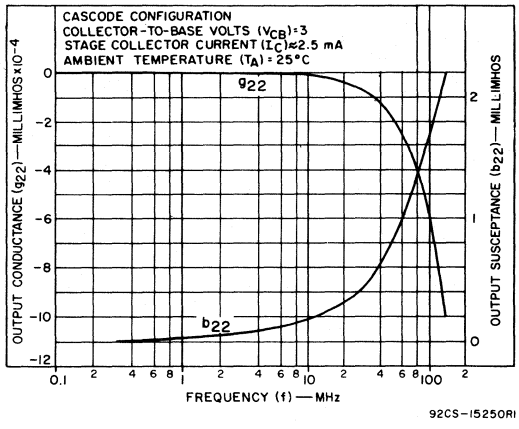


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

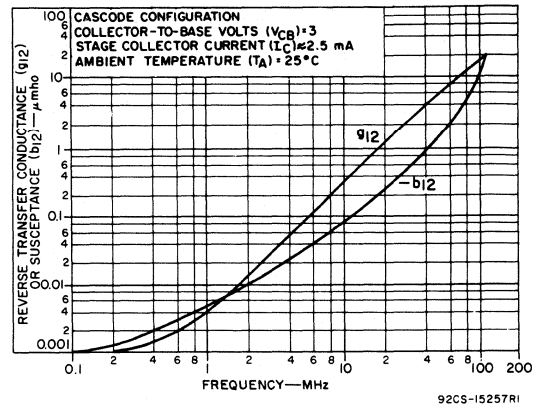


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency

CA3028A, CA3028B, CA3053

Differential/Cascode Amplifiers

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

Features:

- *Controlled for input offset voltage, input offset current, and input bias current (CA3028 series only)*
- *Balanced differential amplifier configuration with controlled constant-current source*
- *Single- and dual-ended operation*

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are available in 8-lead packages as shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

Package/Lead Options

Base Part Number	Straight-Lead TO-5	Dual-In-Line Formed-Lead TO-5	Dual-In-Line Plastic (MINI-DIP)
CA3028A	CA3028A *	CA3028AS	CA3028AE
CA3028B	CA3028B *	CA3028BS	CA3028BE
CA3053	CA3053 *	CA3053S	CA3053E

* Most RCA types in a straight-lead TO-5 package carry a "T" suffix. This one does not. Order type number as shown.

Applications:

- *RF and IF amplifiers (differential or cascode)*
- *DC, audio, and sense amplifiers*
- *Converter in the commerical FM band*
- *Oscillator*
- *Mixer*
- *Limiter*
- *Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.*

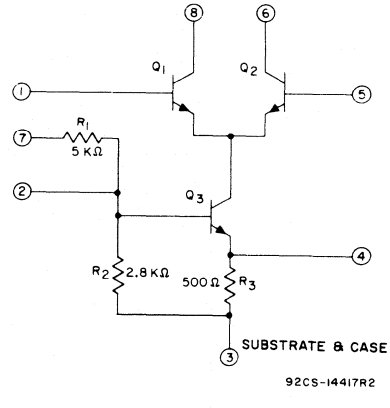


Fig. 1 - Schematic diagram for CA3028A, CA3028B and CA3053.

CA3028A, CA3028B, CA3053

ABSOLUTE MAXIMUM RATINGS at T_A = 25° C

DISSIPATION:
- At T_A Up to 85° C (CA3028A, CA3028B, CA3053) ..... 450 mW
- At T_A 85° C (CA3028A, CA3028B, CA3053) ..... Derate linearly 5 mW/° C

AMBIENT-TEMPERATURE RANGE:
- Operating ..... -55° C to +125° C
- Storage ..... -65° C to +150° C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15◆ to 0	*	+15◆ to 0	*
3‡				+10 to 0	+15◆ to 0	+30● to 0	+15◆ to 0	+30● to 0
4					+15◆ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053

⊕ Limit is +15V for CA3053

◆ Limit is +12V for CA3053

● Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	μA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	μA	5a
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} =+9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

CA3028A, CA3028B, CA3053

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARAC-TERISTICS CURVE
		Fig.			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
DYNAMIC CHARACTERISTICS															
Power Gain	G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	-	-	-	dB	10b
		11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-	-	-	-		11b,e
		10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	35	39	-	dB	10b *
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-	28	32	-		11b *
Noise Figure	NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	-	-	-	dB	10c
		11a,d	V_{CC} = +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9	-	-	-		11c,e
Input Admittance	Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-				mmho	12
		-		Diff.-Ampl.				-	0.5 + j 0.5	-					13
Reverse Transfer Admittance	Y_{12}	-		Cascode				-	0.0003 - j0	-				mmho	14
		-		Diff.-Ampl.				-	0.01 - j0.0002	-					15
Forward Transfer Admittance	Y_{21}	-		Cascode				-	99 - j18	-				mmho	16
		-		Diff.-Ampl.				-	-37 + j0.5	-					17
Output Admittance	Y_{22}	-		Cascode				-	0. + j0.08	-				mmho	18
		-		Diff.-Ampl.				-	0.04 + j0.23	-					19
Power Output (Untuned)	P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	mW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	-	-	-	dB	21b
Voltage Gain	at f = 10.7 MHz	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	-	40	-	dB	22b
		22c	V_{CC} = +0V R_L = 1 kΩ	Diff.-Ampl.	-	30	-	-	30	-	-	30	-		22d
	Differential at f = 1 kHz	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	-	-	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	40	42.5	45	-	-	-		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V_o(P-P)	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	-	-	-	V_{P-P}	-
			V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	15	23	-	-	-	-		
Bandwidth at -3 dB point	BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	-	-	-	MHz	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	-	8	-	-	-	-		
Common-Mode Input-Voltage Range	V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V V_{CC} = +12V, V_{EE} = -12V		-	-	-	-2.5	(-3.2 - 4.5)	4	-	-	-	V	-
					-	-	-	-5	(-7 - 9)	7	-	-	-		
Common-Mode Rejection Ratio	CMR	24	V_{CC} = +6V, V_{EE} = -6V V_{CC} = +12V, V_{EE} = -12V		-	-	-	60	110	-	-	-	-	dB	-
					-	-	-	60	90	-	-	-	-		
Input Impedance at f = 1 kHz	Z_{IN}		V_{CC} = +6V, V_{EE} = -6V V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	5.5	-	-	-	-	kΩ	-
					-	-	-	-	3	-	-	-	-		
Peak-to-Peak Output Current	I_{P-P}		V_{CC} = +9V	f = 10.7 MHz	2	4	7	2.5	4	6	2	4	7	mA	-
			V_{CC} = +12V	e_{in} = 400 mV Diff.-Ampl.	3.5	6	10	4.5	6	8	3.5	6	10		

* Does not apply to CA3053

CA3028A, CA3028B, CA3053

DEFINITION OF TERMS

AGC Bias Current

The current drawn by the device from the AGC-voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

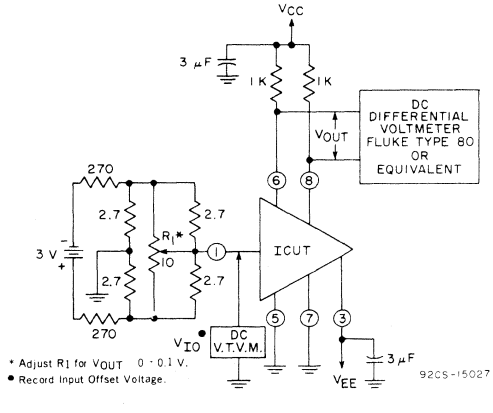


Fig. 2 - Input offset voltage test circuit for CA3028B.

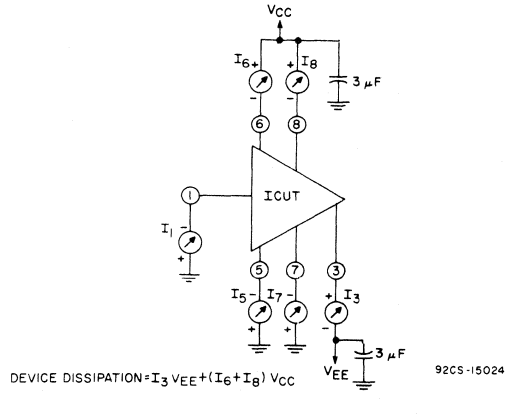


Fig. 3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

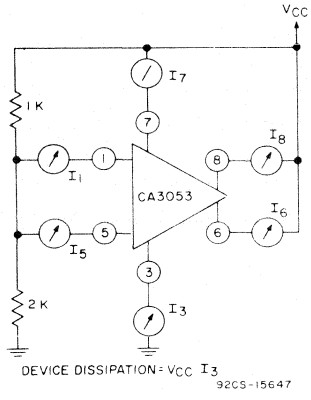


Fig. 3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

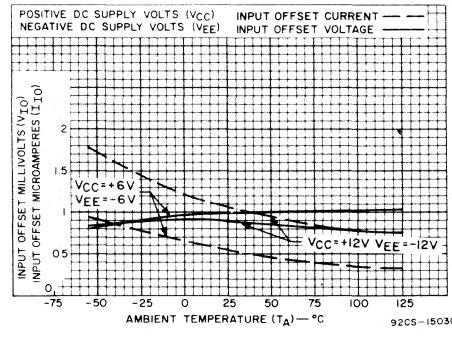


Fig. 4 - Input offset voltage and input offset current for CA3028B.

TYPICAL CHARACTERISTICS

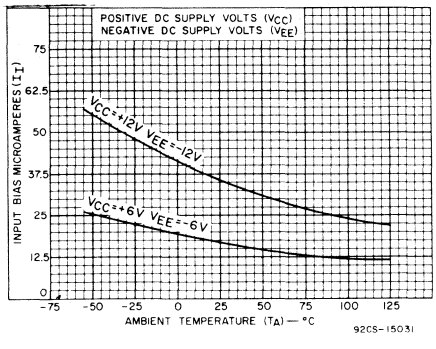


Fig. 5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

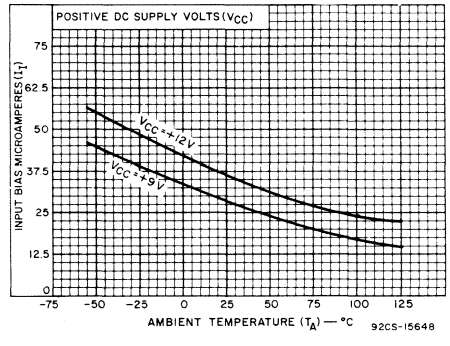


Fig. 5b - Input bias current vs. ambient temperature for CA3053.

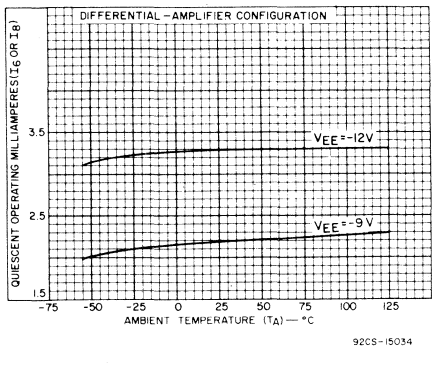


Fig. 6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

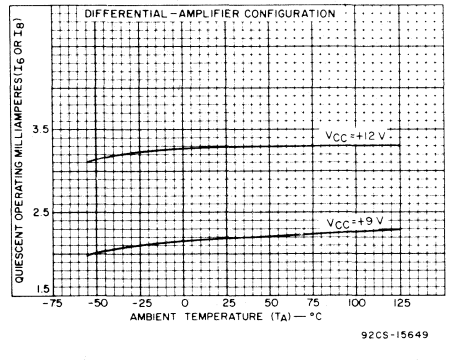


Fig. 6b - Quiescent operating current vs. ambient temperature for CA3053

CA3028A, CA3028B, CA3053

TYPICAL CHARACTERISTICS (Continued)

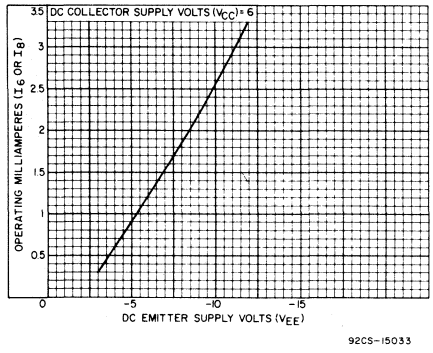


Fig. 7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

TYPICAL CHARACTERISTICS AND TEST CIRCUITS

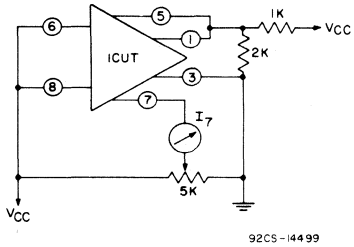


Fig. 8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

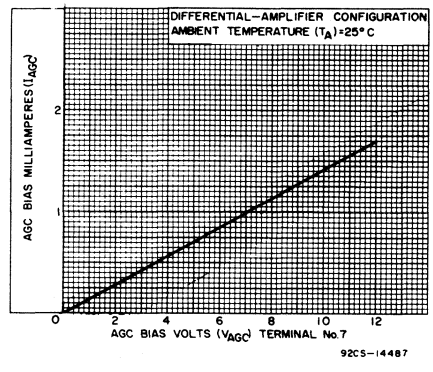


Fig. 8b - AGC bias current vs. bias volts (terminal No. 7) for CA3028A and CA3028B.

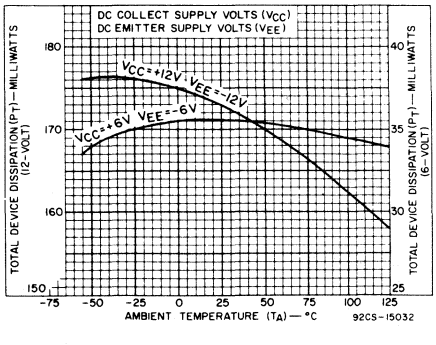
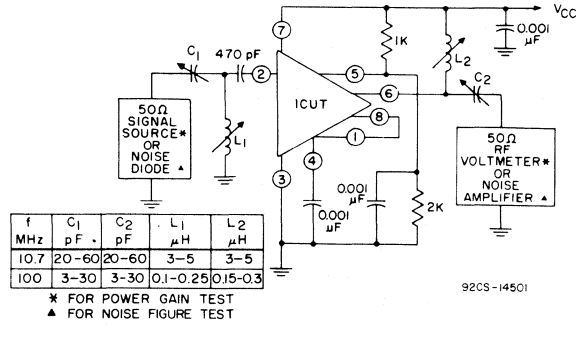


Fig. 9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig. 10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

** 10.7 MHz Power Gain Test Only.*

TYPICAL CHARACTERISTICS AND TEST CIRCUITS (Continued)

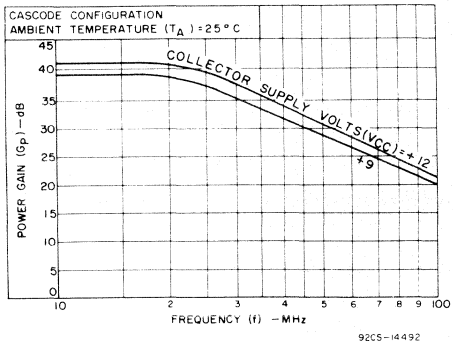


Fig. 10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

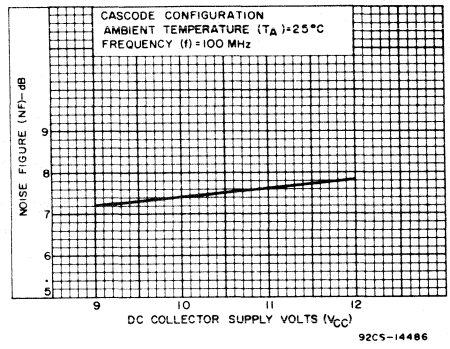
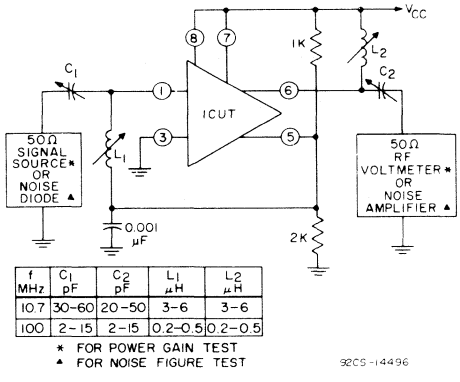


Fig. 10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig. 11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No. 7 connected to V_{CC}) for CA3028A, CA3028B and CA3053*

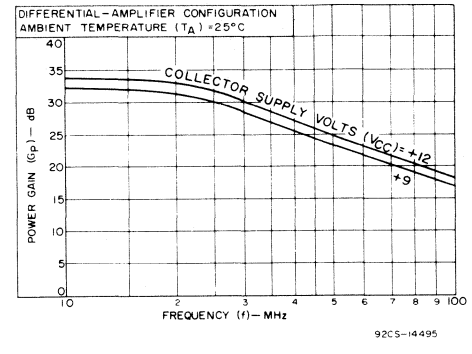


Fig. 11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.

* 10.7 MHz Power Gain Test Only.

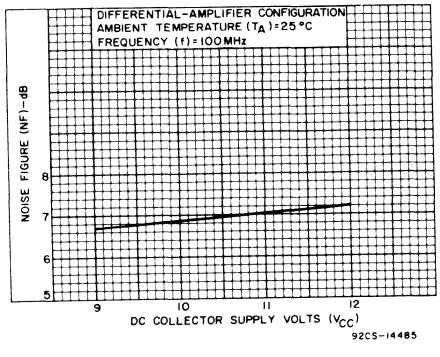
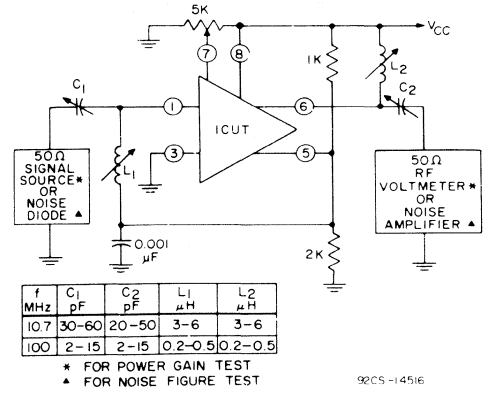


Fig. 11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig. 11d - Power gain and noise figure test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

CA3028A, CA3028B, CA3053

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS (Continued)

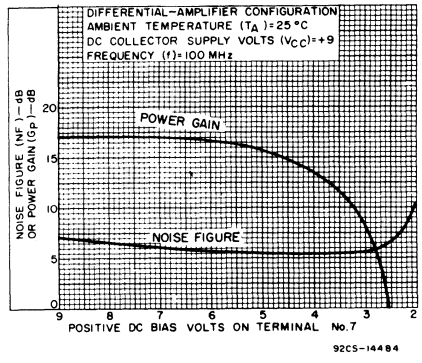


Fig. 11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No. 7) for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

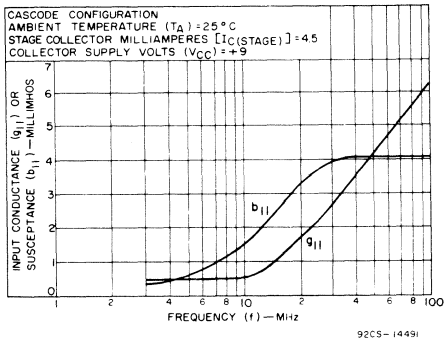


Fig. 12 - Input admittance (Y_{11}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

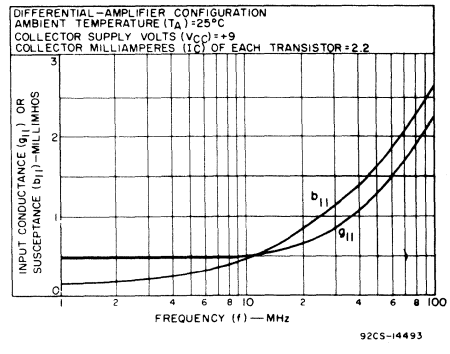


Fig. 13 - Input admittance (Y_{11}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

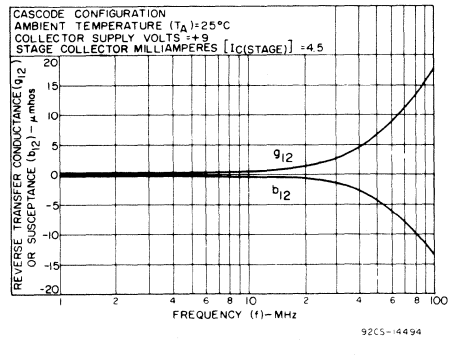


Fig. 14 - Reverse transadmittance (Y_{12}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

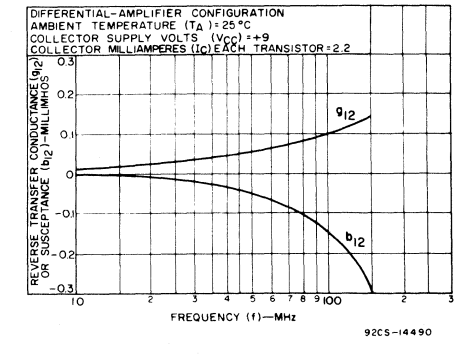


Fig. 15 - Reverse transadmittance (Y_{12}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL ADMITTANCE PARAMETERS (Continued)

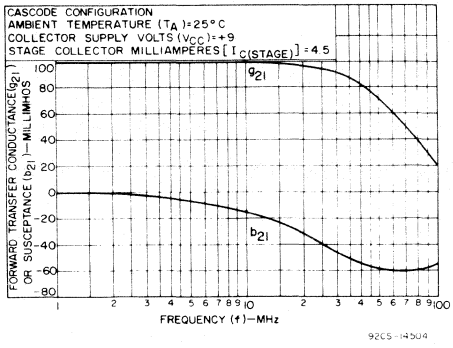


Fig. 16 - Forward transadmittance (Y_{21}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

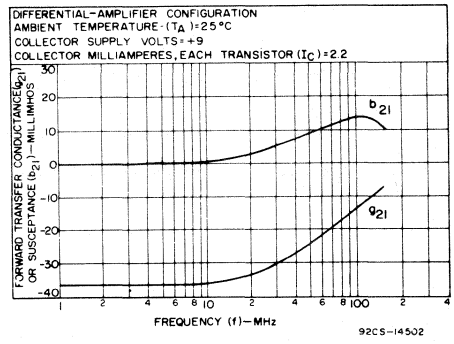


Fig. 17 - Forward transadmittance (Y_{21}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

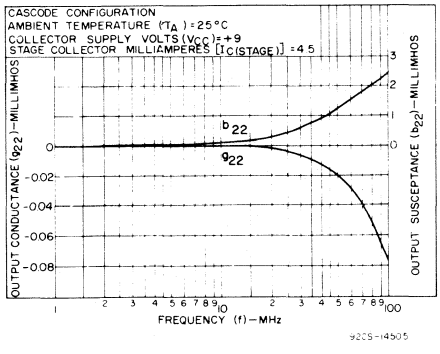


Fig. 18 - Output admittance (Y_{22}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

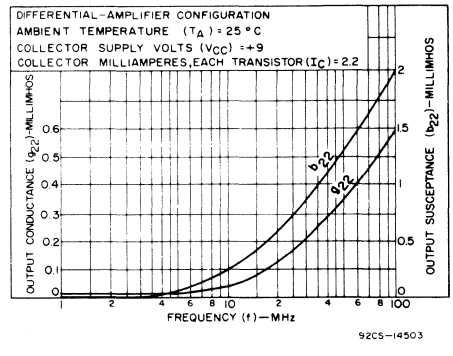


Fig. 19 - Output admittance (Y_{22}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

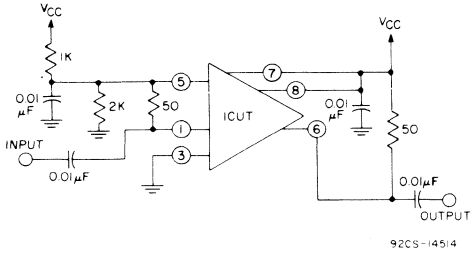


Fig. 20a - Output power test circuit for CA3028A and CA3028B.

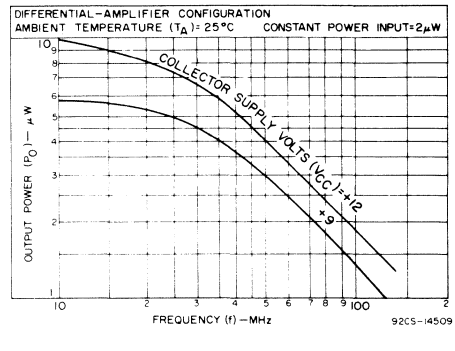
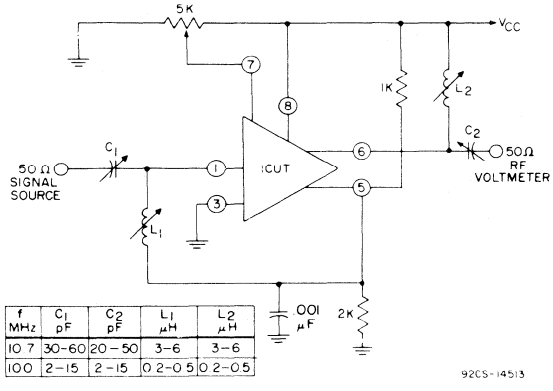


Fig. 20b - Output power vs. frequency - 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.

CA3028A, CA3028B, CA3053

TYPICAL TEST CIRCUITS AND CHARACTERISTICS (Continued)



f MHz	C1 pF	C2 pF	L1 μH	L2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig. 21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

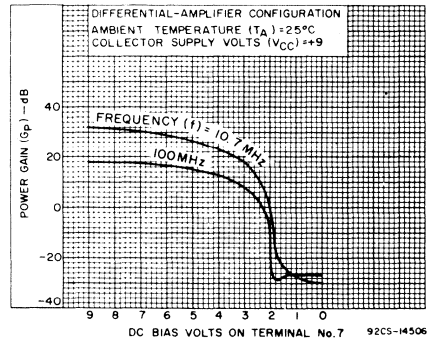


Fig. 21b - AGC characteristics for CA3028A and CA3028B.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

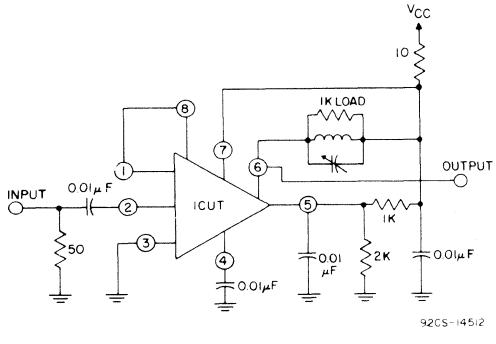


Fig. 22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

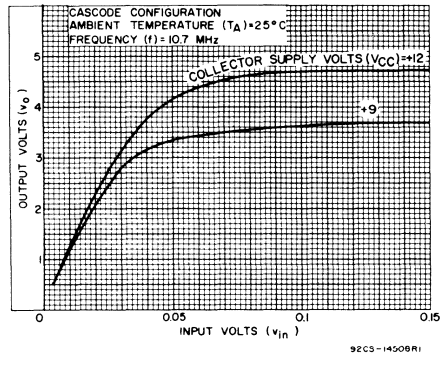


Fig. 22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

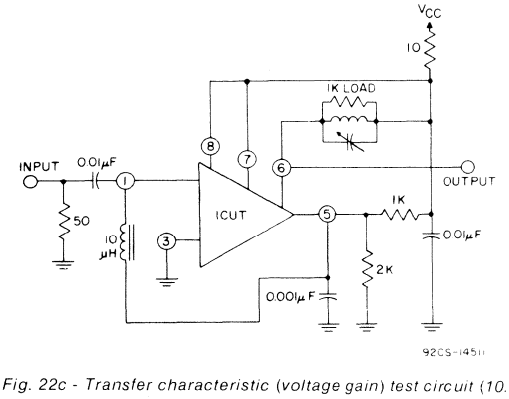


Fig. 22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

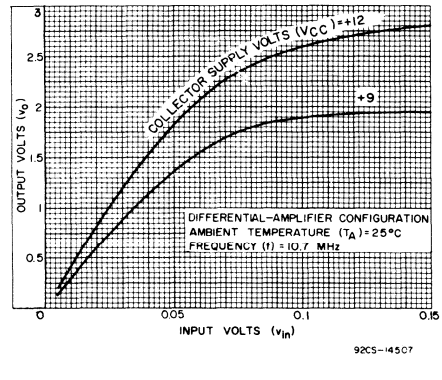
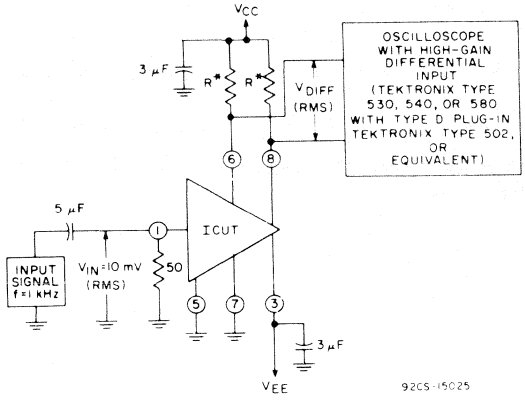


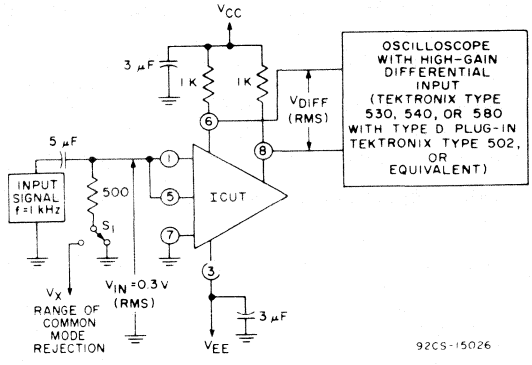
Fig. 22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS (Continued)



* For R = 1.6 kΩ – (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ – (V_{CC} = 6 V, V_{EE} = -6V)

Fig. 23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



For CMR test: S_1 to ground
For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)\ (2)\ (0.3)}{V_{DIFF}\ (RMS)}$

* A = Single-ended voltage gain.

Fig. 24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

CA3040

Video and Wide-band Amplifier

For Industrial and Commercial
Equipment at Frequencies up to 200 MHz

Features:

- *High differential push-pull voltage gain - 37 dB typ.*
- *Single-ended voltage gain - 31 dB typ.*
- *Wide [3dB] bandwidth - 55 MHz typ.*
- *Balanced input and output*
- *High input resistance - 150 kΩ typ.*
- *Low output resistance - 125 Ω typ.*
- *Bias options for temperature compensation:*
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain

Applications

- *Video amplifier*
- *Schmitt trigger*
- *Modulator*
- *IF Amplifier*
- *Mixer*
- *DC Amplifier*
- *Sense Amplifier*

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of −55 to +125° C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ± 2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ± 0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

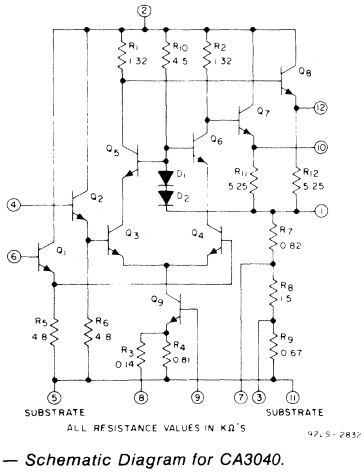


Fig. 1 — Schematic Diagram for CA3040.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

File Number **363**

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * . . . . . 450 mW
Derating factor for $T_A > 85^oC$ . . . . . 5 mW/°C
TEMPERATURE RANGE:
Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

Limitation imposed by the thermal resistance of package.

MAXIMUM VOLTAGE RATINGS at $T_A = 25^oC$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

CA3040

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits Fig.	Special Test Conditions	Limits CA3040 Min.	Typ.	Max.	Units	Typica Characteri: Curves Fig.
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V							
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V	9
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V	-
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V	-
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	-	+1	V	9
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	15	45	μA	-
Input Unbalance Current	$\lvert I_6 - I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	-	6	μA	-
Power Supply Current Drain	I_2 or $I_5 + I_{11}$	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA	10
	I_2 or $I_5 + I_8 + I_{11}$	2(b)	Mode B Switch open or closed					
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V							
Differential Voltage Gain								-
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz R_S = 50 Ω	34	37	-	dB	-
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz R_S = 50 Ω	28	31	-	dB	4,5
-3 dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	-	MHz	4,7
Differential Voltage Gain Balance	$A_{DIFF(SE)10} - A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB	-
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz R_S = 50 Ω	-	0.5	-	V_{RMS}	7
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz R_S = 400 Ω	-	7.5	9	dB	8
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ	-
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF	-
Output Resistance	R_O	3(a)		-	125	-	Ω	-
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: -55°C ≤ T_A ≤ +125°C								
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	3(a)	Bias Mode A	-	0	-	mV/°C	9
		3(b)	Bias Mode B	-	6.4	-	mV/°C	
Power Supply Current Drain	ΔI_2/°C	3(a)	Bias Mode A	-	5	-	μA/°C	11
Differential Voltage Gain	A_{DIFF}/°C	3(a)	Bias Mode A	-	0.0166	-	dB/°C	12
		3(b)	Bias Mode B	-	0	-		

Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Term. 1 and 6 with suitable chokes so that reactance at 30 MH_z exceeds 5

ATIC CHARACTERISTICS TEST CIRCUITS FOR CA3040

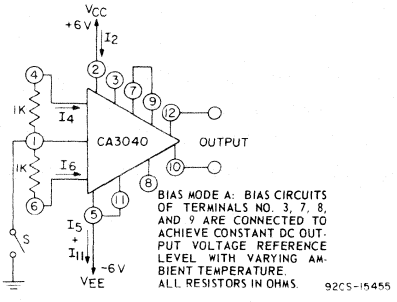


Fig.2(a) - Bias Mode A

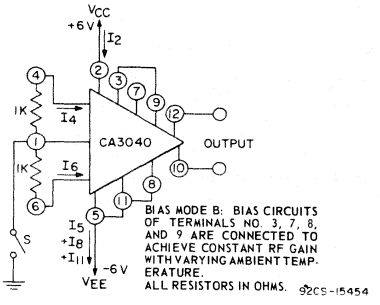
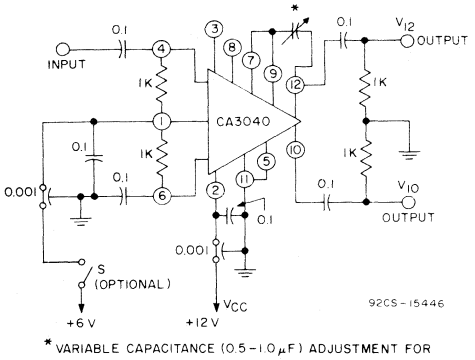


Fig.2(b) - Bias Mode B

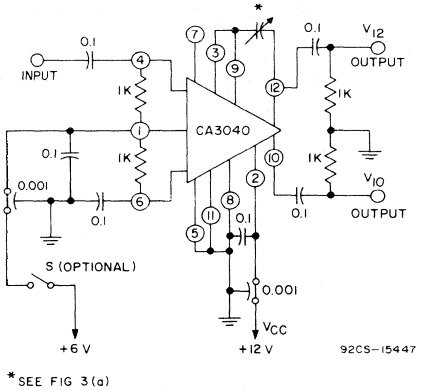
YNAMIC CHARACTERISTICS TEST CIRCUITS FOR CA3040



* VARIABLE CAPACITANCE (0.5-1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.

ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).
BIAS MODE A IS AS DEFINED IN FIG. 2 (a)

Fig.3(a) - Bias Mode A



* SEE FIG 3 (a)

BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

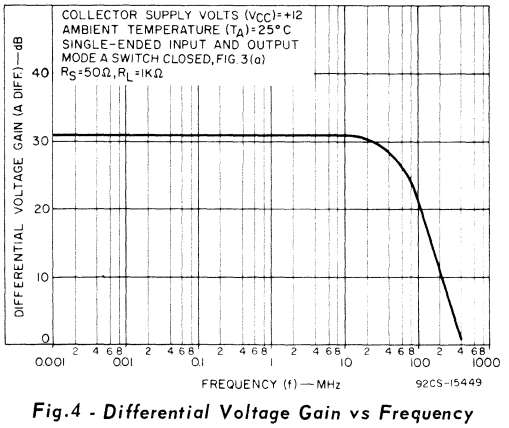


Fig.4 - Differential Voltage Gain vs Frequency

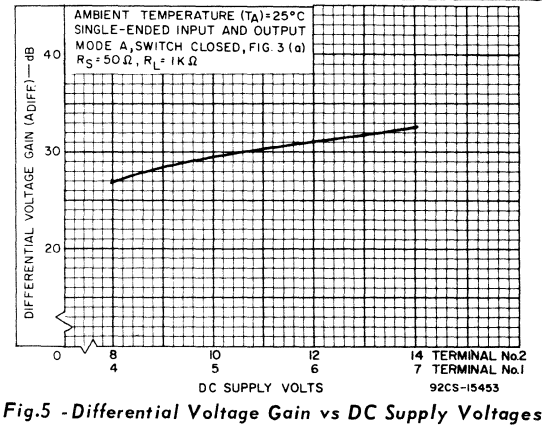


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

CA3040

OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal cc siderations of shielding, parts layout, and isolatic the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, wh used, must provide shielding within the pin circl The socket shown in the chassis of Fig.6 is Barnes MG-1201, or equivalent, modified by drilli a 1/8" hole in the center and inserting a ground brass pin.
2. Do not bypass Terminal No.9 in normal operatio Fig.3 shows the use of neutralization betwe Terminal No.9 and one output to balance the amplifi at high frequencies. Experience shows that stabl operation, while possible, is difficult to achie if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors shoul be soldered directly to the socket Terminals No. and No.6 to suppress parasitic oscillations. A current carrying connections are made at the oth end of the resistors. Direct sensing of Termina No.4 or No.6 voltage should not be attempted.

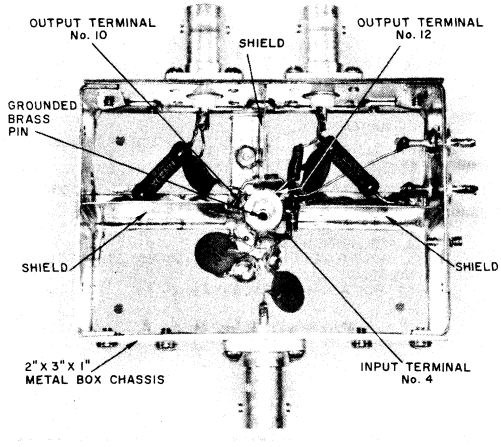


Fig.6 - Test Circuit Layout

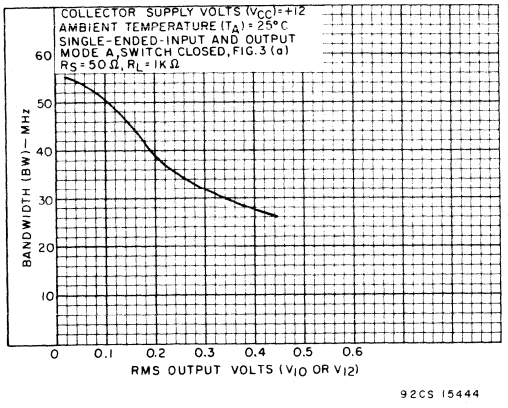


Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

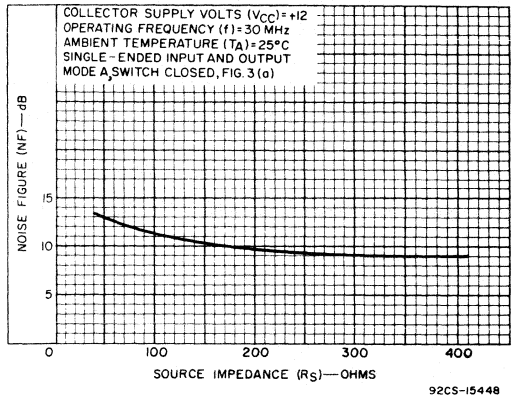


Fig.8 - Noise Figure (NF) vs Source Impedance

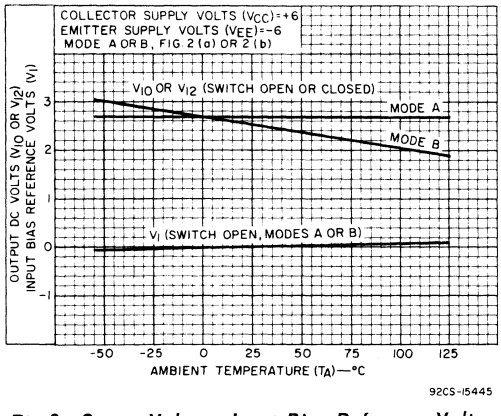


Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

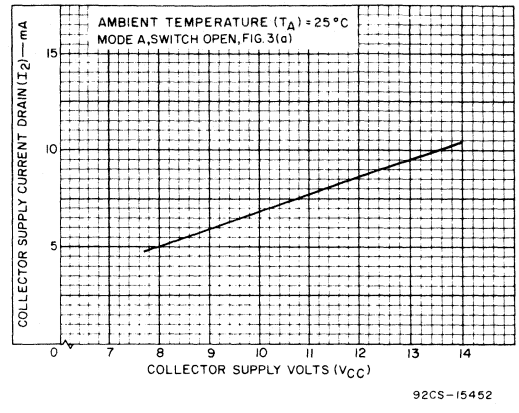


Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

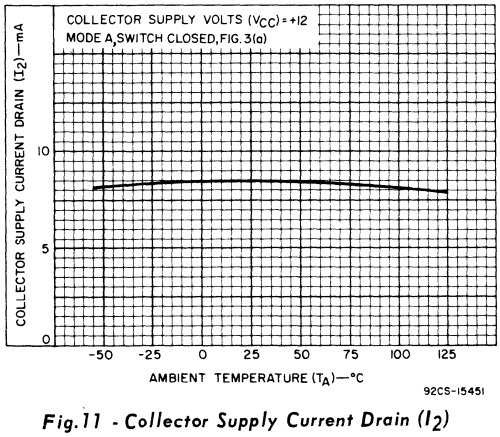


Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

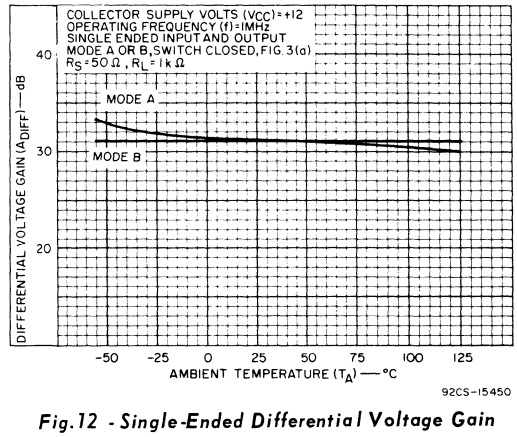


Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

CA3049, CA3102

Dual High-Frequency Differential Amplifiers

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- **Power Gain 23 dB (typ.) at 200 MHz**
- **Noise Figure 4.6 dB (typ.) at 200 MHz**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Full military-temperature-range capability- (–55°C to + 125°C) for the CA3102E and for the CA3049T**

RCA-CA3049T and CA3102E* consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

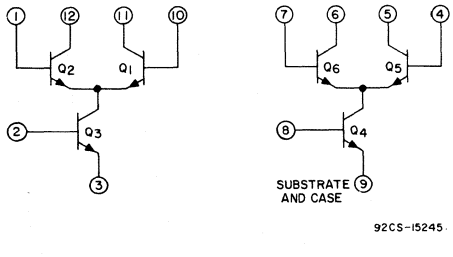
The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

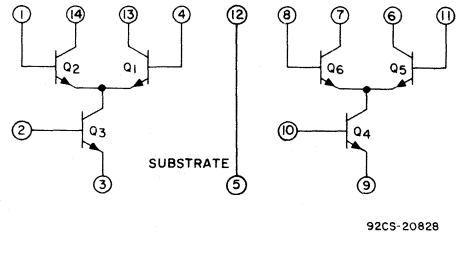
Applications

- **VHF amplifiers**
- **VHF mixers**
- **Multifunction combinations – RF/Mixer/Oscillator Converter/IF**
- **IF amplifiers (differential and/or cascode)**
- **Product detectors**
- **Doubly balanced modulators and demodulators**
- **Balanced quadrature detectors**
- **Cascade limiters**
- **Synchronous detectors**
- **Balanced mixers**
- **Synthesizers**
- **Balanced (push-pull) cascode amplifiers**
- **Sense amplifiers**

*Formerly Developmental No. TA6228.



Schematic Diagram for CA3049T



Schematic Diagram for CA3102E

File Number **611**

CA3049, CA3102

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25°C$*

Power Dissipation, P:	CA3049T	CA3102E	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	CA3102E LIMITS MIN.	CA3102E LIMITS TYP.	CA3102E LIMITS MAX.	CA3049T LIMITS MIN.	CA3049T LIMITS TYP.	CA3049T LIMITS MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS												
For Each Differential Amplifier												
Input Offset Voltage	V_{IO}			1	---	0.25	5	---	0.25	---	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9 = 2$ mA		1	---	0.3	3	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1	---	13.5	33		13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	---	1.1	---	---	1.1	---	μV/°C	4
For Each Transistor												
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CE} = 6$ V, $I_C = 1$ mA		---	674	774	874	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CE} = 6$ V, $I_C = 1$ mA		---	---	-0.9	---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$		---	---	0.0013	100	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$		---	15	24	---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10$ μA, $I_E = 0$		---	20	60	---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10$ μA, $I_B = 0$, $I_E = 0$		---	20	60	---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10$ μA, $I_C = 0$		---	5	7	---	5	7	---	V	---
DYNAMIC CHARACTERISTICS												
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, $R_S = 500\ \Omega$, $I_C = 1$ mA		---	---	1.5	---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 6$ V, $I_C = 5$ mA		---	---	1.35	---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	$I_C = 0$, $V_{CB} = 5$V	*	---	---	0.28	---	---	0.28	---	pF	8
			**	---	---	0.15	---	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	$I_C = 0$, $V_{CI} = 5$V			---	1.65	---	---	1.65	---	pF	8
For Each Differential Amplifier												
Common-Mode Rejection Ratio	CMR	$I_3 = I_9 = 2$ mA		---	---	100	---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22	---	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	---	23	---	dB	---
Noise Figure	NF	$V_{CC} = 12$V	Cascode	3	---	4.6	---	---	4.6		dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9 = 2$ mA	Cascode	---	---	1.5 + j 2.45	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9 = 4$mA (each collector $I_C \simeq 2$mA)	Cascode	---	---	0 - j 0.008	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

CA3049, CA3102

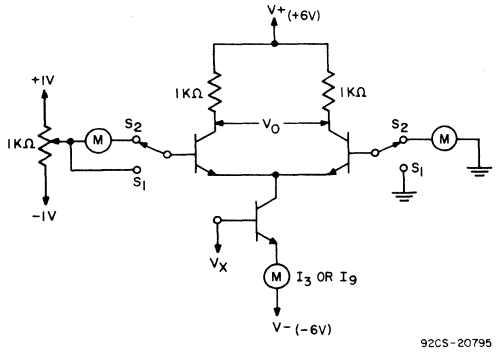


Fig.1—Static characteristics test circuit for CA3102E.

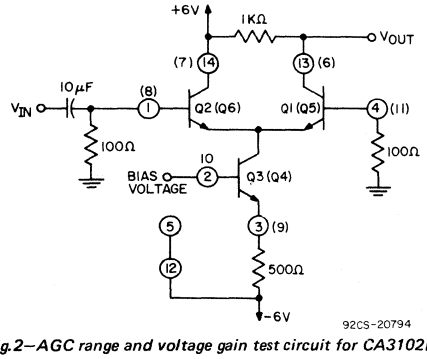
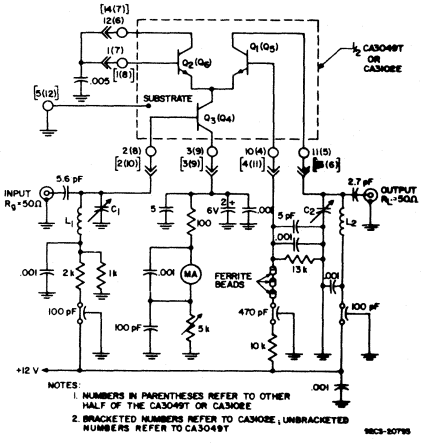


Fig.2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig.3—200 MHz cascode power gain and noise figure test circuit.

Typical Characteristics for CA3049T and CA3102E

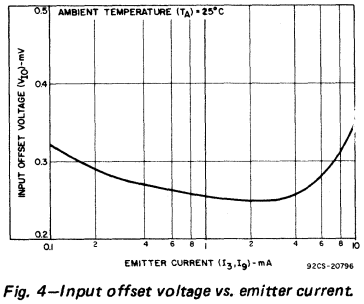


Fig. 4—Input offset voltage vs. emitter current.

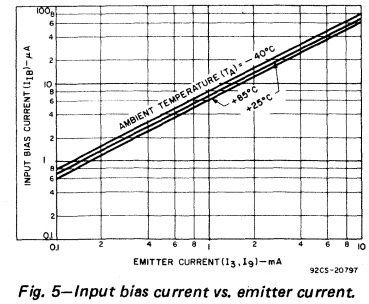


Fig. 5—Input bias current vs. emitter current.

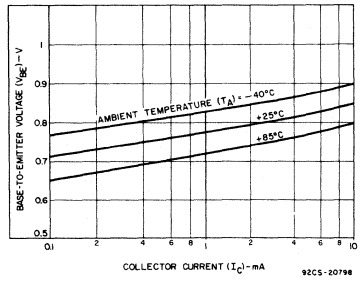


Fig. 6—Base-to-emitter voltage vs. collector current.

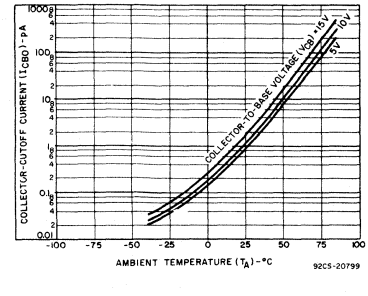


Fig. 7—Collector-cutoff current vs. temperature.

Typical Characteristics for CA3049T and CA3102E (cont'd)

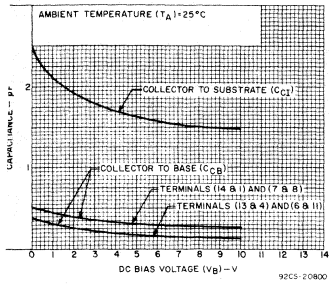


Fig. 8—Capacitance vs. dc bias voltage.

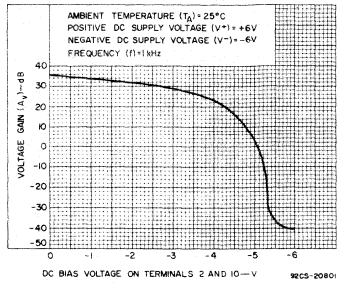


Fig. 9—Voltage gain vs. dc bias voltage.

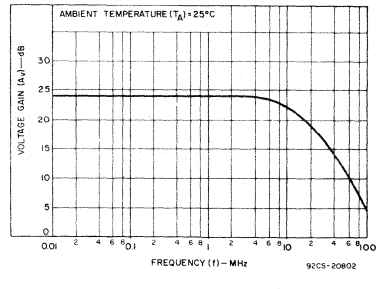


Fig. 10—Voltage gain vs. frequency.

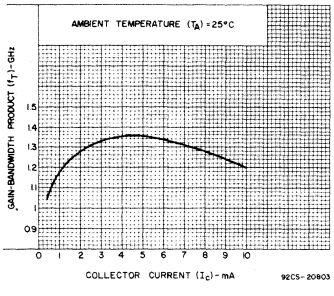


Fig. 11—Gain-bandwidth product vs. collector current.

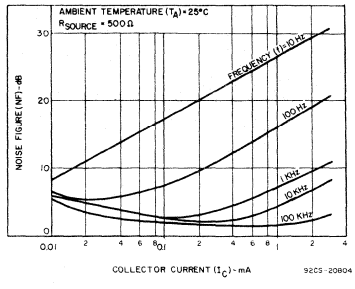


Fig. 12—1/f noise figure vs. collector current.

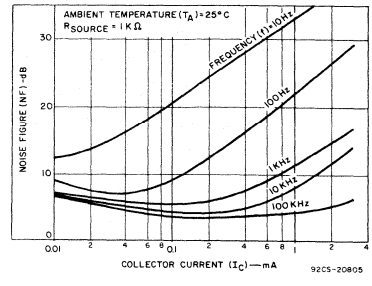


Fig. 13—1/f noise figure vs. collector current.

Typical Input Admittance Characteristics for CA3049T and CA3102

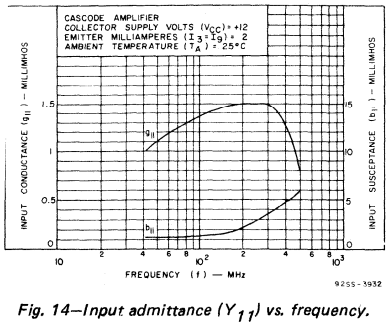


Fig. 14—Input admittance (Y_{11}) vs. frequency.

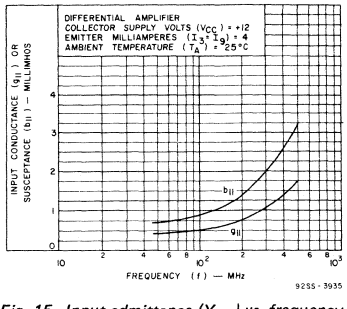


Fig. 15—Input admittance (Y_{11}) vs. frequency.

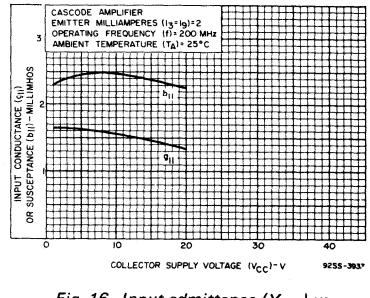


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

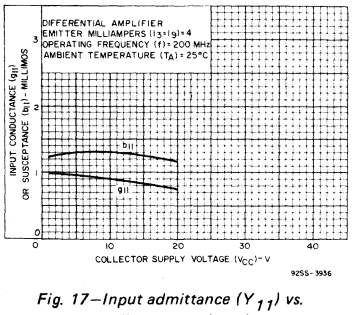


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

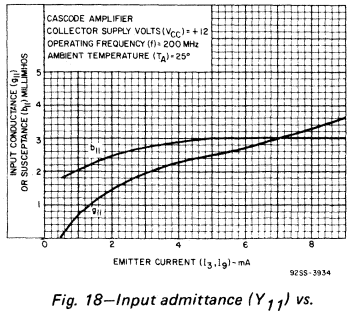


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

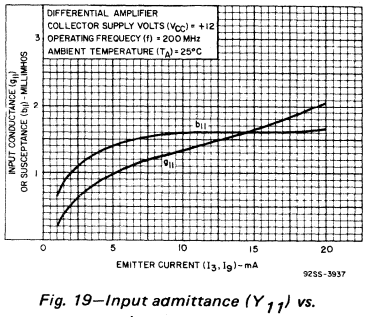


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

CA3049, CA3102

Typical Output Admittance Characteristics for CA3049T and CA3102E

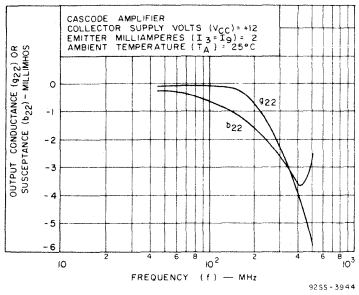


Fig. 20—Output admittance (Y_{22}) vs. frequency.

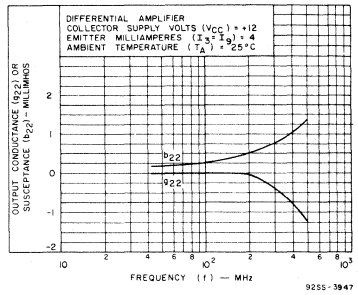


Fig. 21—Output admittance (Y_{22}) vs. frequency.

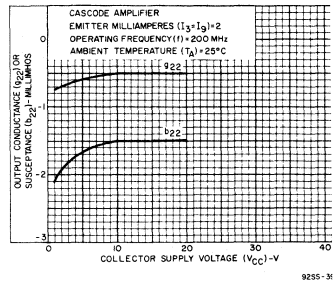


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

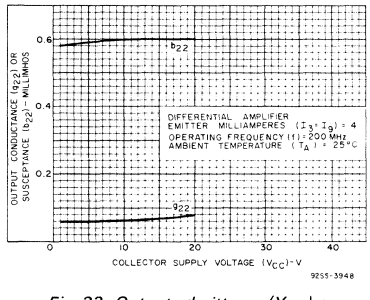


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

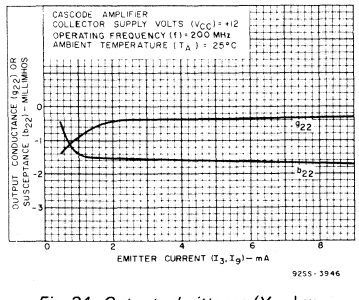


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

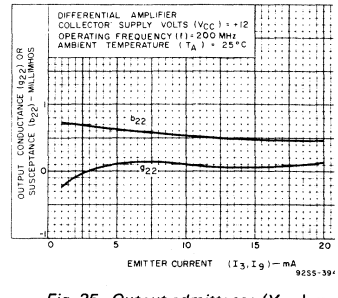


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

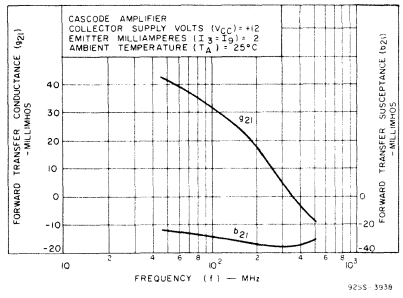


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

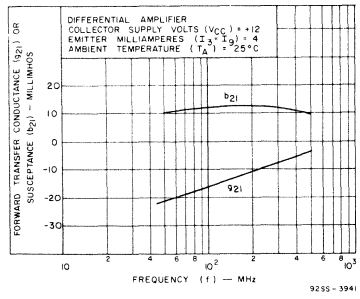


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

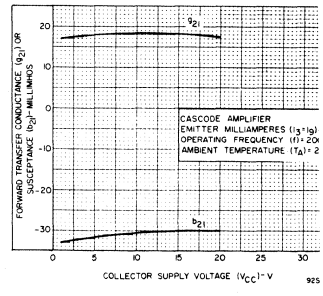


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

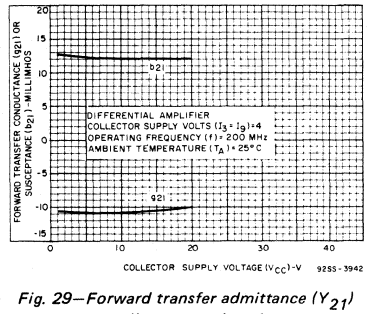


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

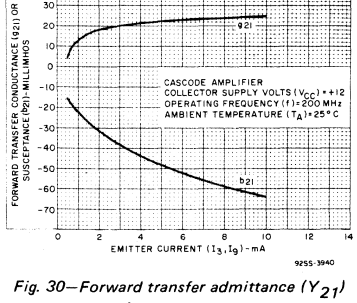


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

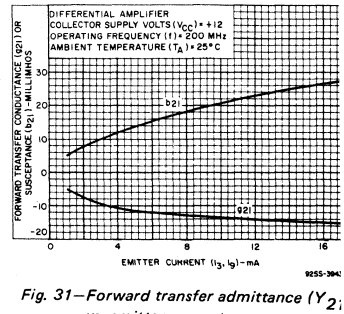


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.

CA3050, CA3051

Dual Differential Amplifiers

Two Darlington-Connected Differential Amplifiers with Diode Bias String

For Low-Power Applications at Frequencies from DC to 20 MHz

Features:

- *Input offset current - 70 nA max.*
- *Input bias current - 500 nA max.*
- *Input offset voltage - 5 mV max.*
- *Input impedance - 460 kΩ typ.*
- *Independently accessible inputs and outputs*

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

The CA3050 is supplied in an hermetic 14-lead Dual-In-Line ceramic package rated for operation over the full military temperature range of −55° C to +125° C.

The CA3051 is supplied in a Dual-In-Line plastic package for applications requiring only a limited temperature range of −25° C to +85° C.

Applications

- *Matched dual amplifiers*
- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Dual multivibrators*
- *Doubly balanced detectors and modulators*
- *Balanced quadrature detectors*
- *Synthesizer mixers*
- *Product detectors*

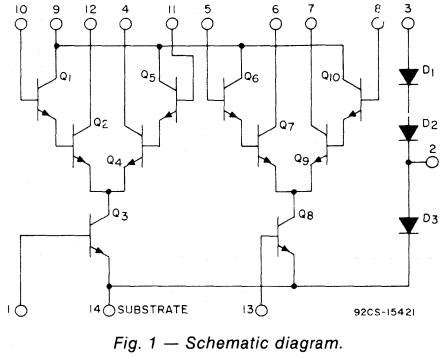


Fig. 1 — Schematic diagram.

File Number **361**

CA3049, CA3102

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For $T_A > 55°C$, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125	-40 to +85	°C
Storage	-65 to +150	-65 to +150	°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265°C		

The following ratings apply for each transistor in the device

Collector-to-Emitter Voltage, V_{CEO}	15
Collector-to-Base Voltage, V_{CBO}	20
Collector-to-Substrate Voltage, V_{CIO} *	20
Emitter-to-Base Voltage, V_{EBO}	5
Collector Current, I_C	50 r

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to -2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	–	*	*	*	*	*	*	*	*	*	*	*	*	+1 -5
2			+5 -2	*	*	*	*	*	*	*	*	*	*	+1 -1
3				*	*	*	*	*	*	*	*	*	*	+3 -1
4					*	*	*	*	*	+14 -2.5 Note 3	+14 -2.5 Note 4	*	*	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	*	*	*	*	+16 -
6							*	+14 -2.5 Note 2	*	*	*	*	*	+20 -1
7								+14 -2.5 Note 2	*	*	*	*	*	+20 -1
8									+1 -20	*	*	*	*	+16 -
9										+20 -1	+20 -1	*	*	+20 -1
10											+10 -10	+2.5 -14 Note 3	*	+16 -
11												+2.5 -14 Note 4	*	+16 -
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0 1
2	50	50
3	50	1
4	50	1
5	5	0 1
6	50	1
7	50	1
8	5	0 1
9	50	1
10	5	0 1
11	5	0.1
12	50	1
13	5	0 1
14	100	5

Note 1: This rating is important only when terminal 5 is more positive than terminal 8.

Note 2: This rating is important only when terminal 8 is more positive than terminal 5.

Note 3: This rating is important only when terminal 10 is more positive than terminal 11.

Note 4: This rating is important only when terminal 11 is more positive than terminal 10.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

LECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3050/CA3051			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_I		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})\ \text{or}\ (I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800		
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850		
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_{IN}	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_{OUT}	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	JB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

CA3050, CA3051

TYPICAL STATIC CHARACTERISTICS

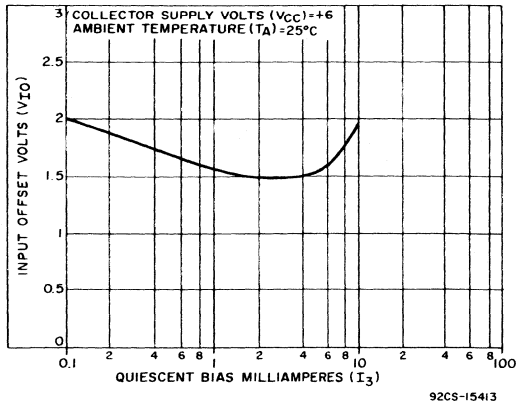


Fig.2(a) - Typical input offset voltage vs quiescent bias current.

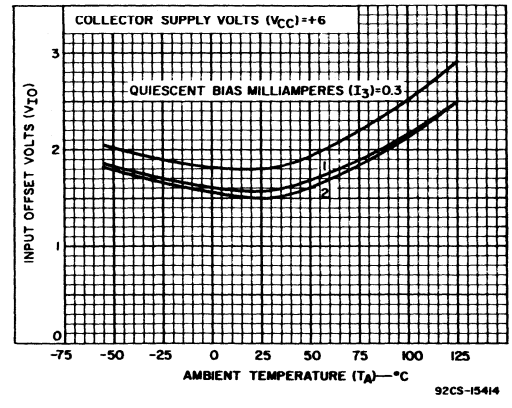


Fig.2(b) - Typical input offset voltage vs ambient temperature.

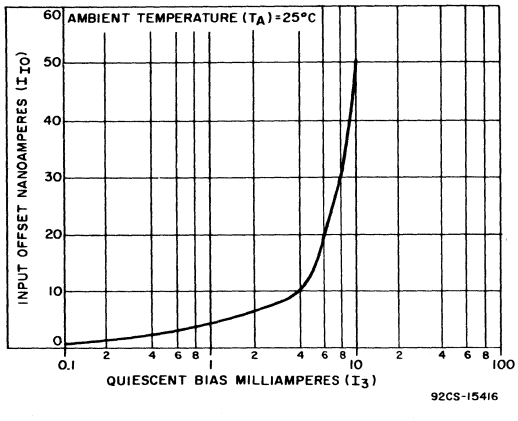


Fig.3(a) - Typical input offset current vs quiescent bias current.

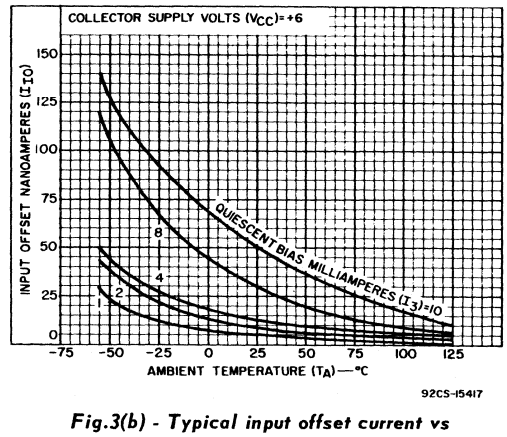


Fig.3(b) - Typical input offset current vs ambient temperature.

STATIC CHARACTERISTICS

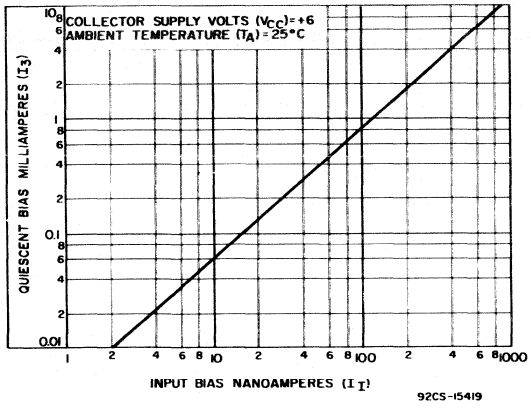


Fig.4(a) - Typical quiescent bias current vs input bias current.

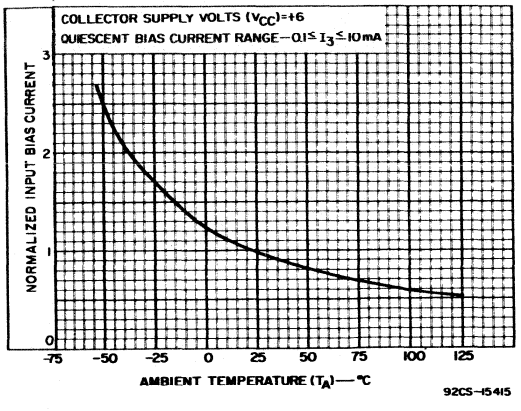


Fig.4(b) - Typical normalized input bias current vs ambient temperature.

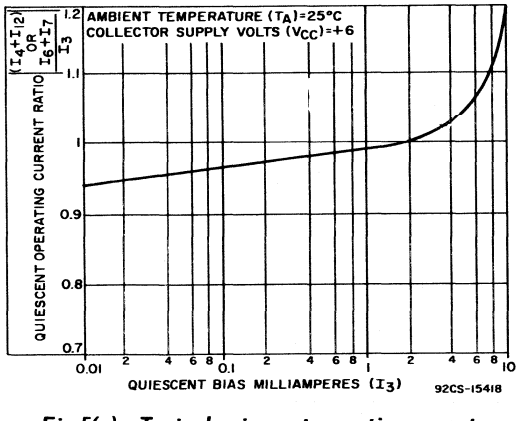


Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

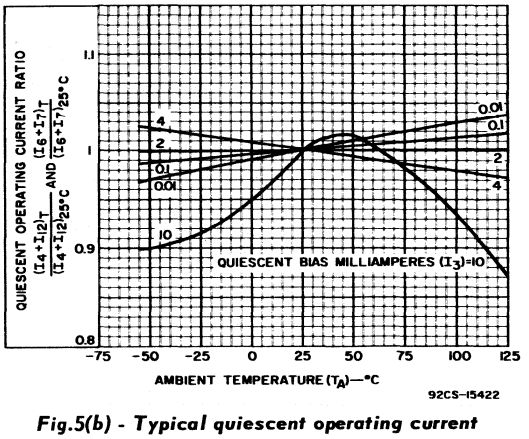


Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

CA3050, CA3051

STATIC CHARACTERISTICS

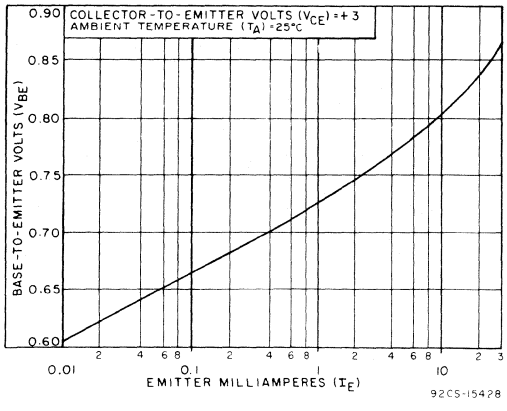


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

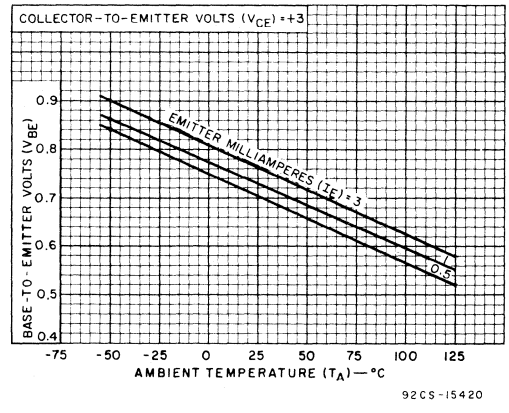


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

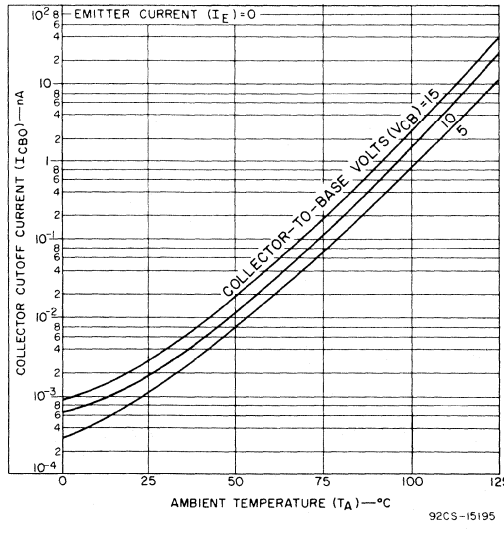


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

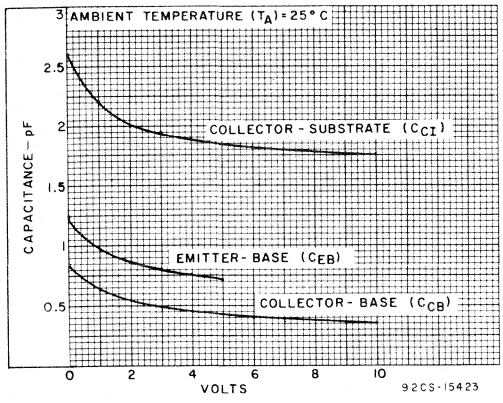


Fig.9 - Typical capacitance for each transistor.

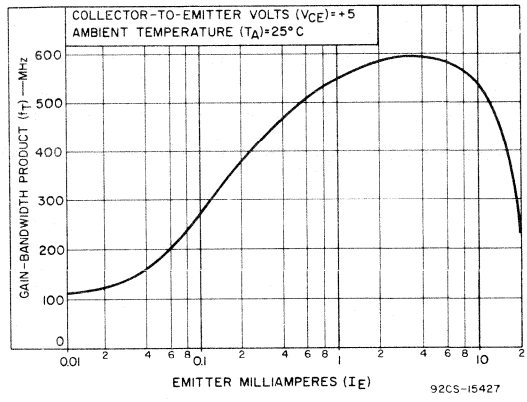
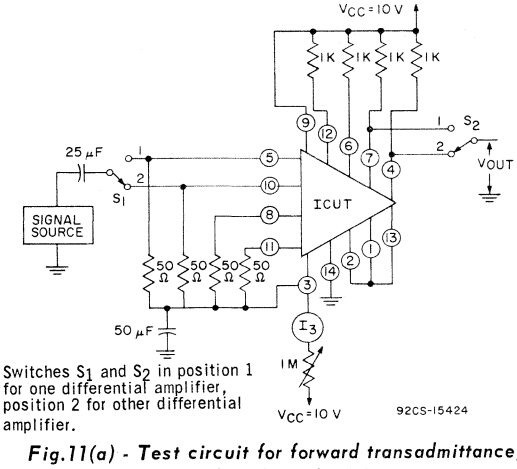


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

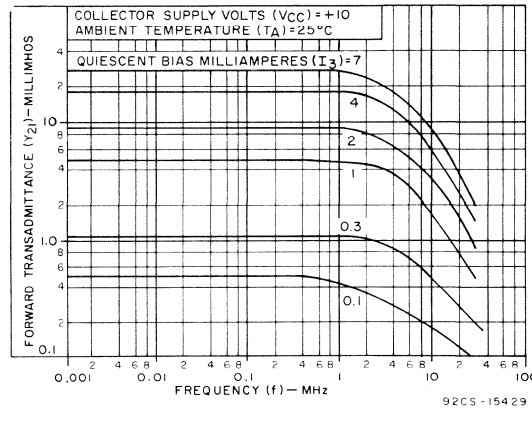


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.

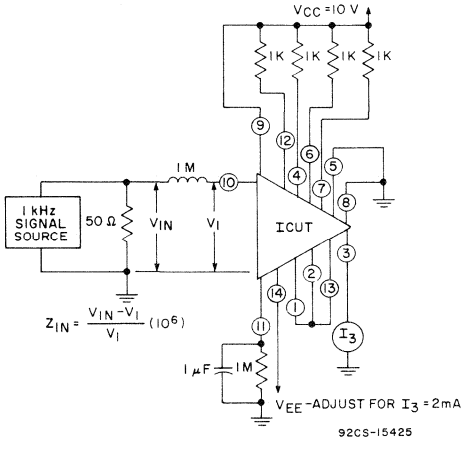


Fig.12(a) - Test circuit for input impedance.

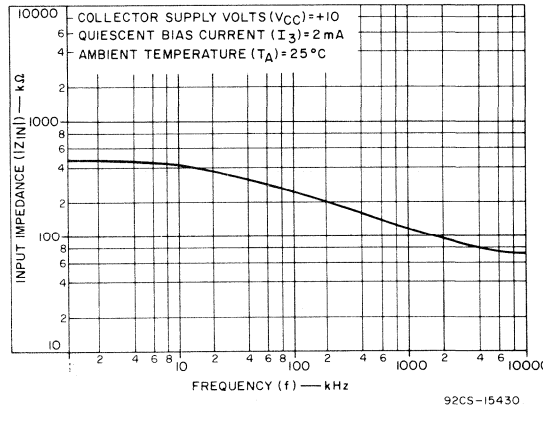
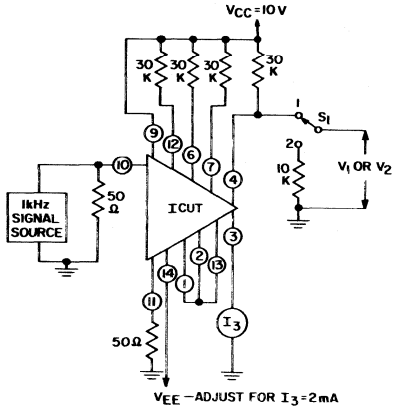


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.

CA3050, CA3051

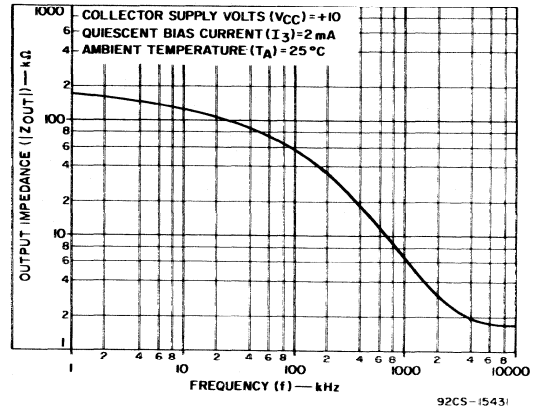
DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K+10K)-10K}$$

92CS-15426

Fig.13(a) - Test circuit for output impedance.



92CS-15431

Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

Power Control Circuits — Technical Data

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

CA723, CA723C

Voltage Regulators

For Regulated Output Voltages Adjustable from 2 V to 37 V at Output Currents up to 150 mA Without External Pass Transistors

Features:
- *Up to 150 mA output current*
- *Positive and negative voltage regulation*
- *Regulation in excess of 10 A with suitable pass transistors*
- *Input and output short-circuit protection*
- *Load and line regulation: 0.03%*
- *Direct replacement for 723 and 723C industry types*
- *Adjustable output voltage: 2 to 37 V*

RCA-CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

Applications:
- *Series and shunt voltage regulator*
- *Floating regulator*
- *Switching voltage regulator*
- *High-current voltage regulator*
- *Temperature controller*

The CA723 and CA723C are supplied in the 10-lead TO-5-style package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All types are rated for operation over the full military-temperature range of −55° C to +125° C.

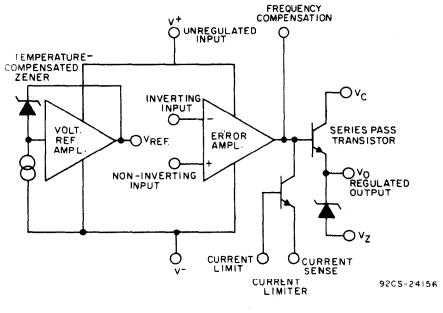


Fig. 1 — Functional diagram of the CA723 and CA723C.

File Number **788**

CA723, CA723C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT–OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE:		
Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:		
Up to T_A = 25°C –		
CA723T, CA723CT	800	mW
CA723E, CA723CE	1000	mW
Above T_A = 25°C –		
CA723T, CA723CT		
Derate linearly	6.3	mW/°C
CA723E, CA723CE		
Derate linearly	8.3	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

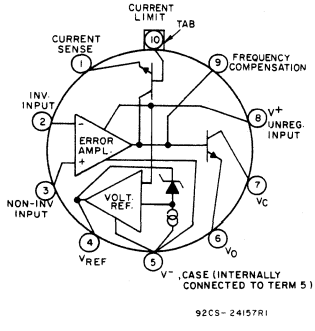


Fig. 2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

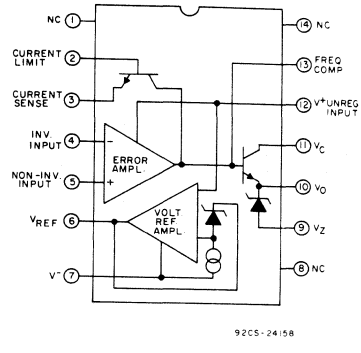


Fig. 3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

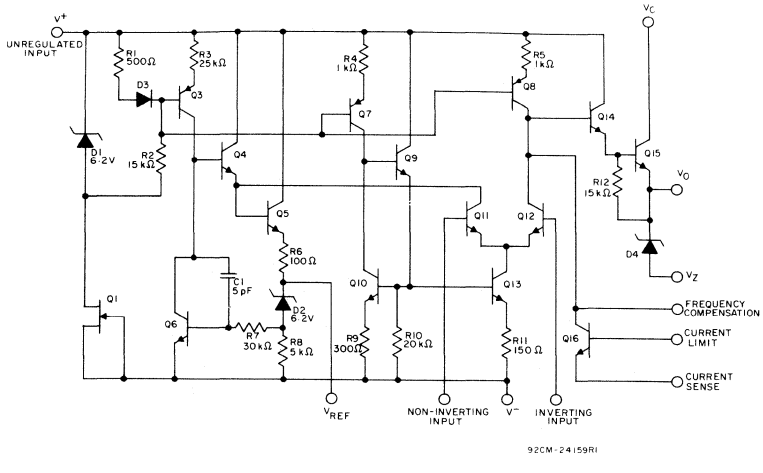


Fig. 4 – Equivalent schematic diagram of the CA723 and CA723C.

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, $V^- = 0$, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, $C_{REF} = 0$, $R_{SCP} = 0$, unless otherwise specified. Divider impedance $\frac{R_1R_2}{R_1+R_2}$ at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	$I_L = 0$, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_i		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, $V_I - V_O$		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = O to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, $\triangle V_O$	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	

CA723, CA723C

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

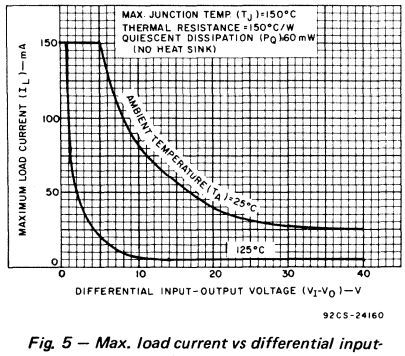


Fig. 5 — Max. load current vs differential input-output voltage.

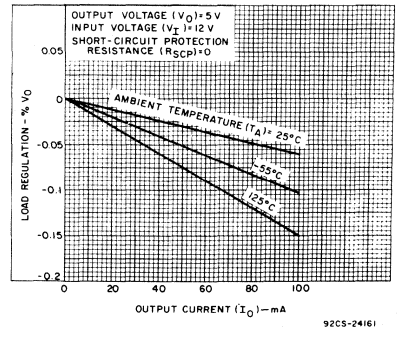


Fig. 6 — Load regulation without current limiting.

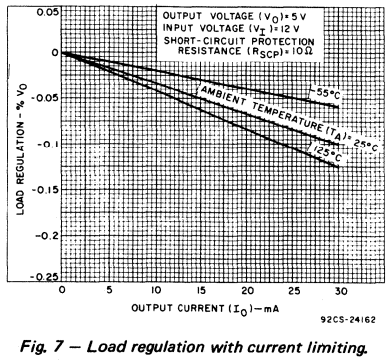


Fig. 7 — Load regulation with current limiting.

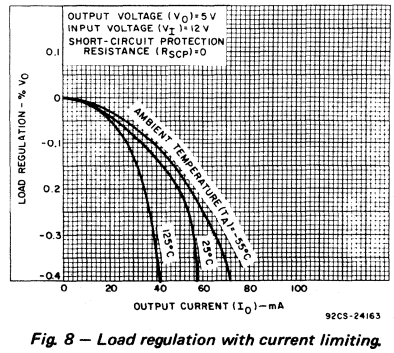


Fig. 8 — Load regulation with current limiting.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Cont'd)

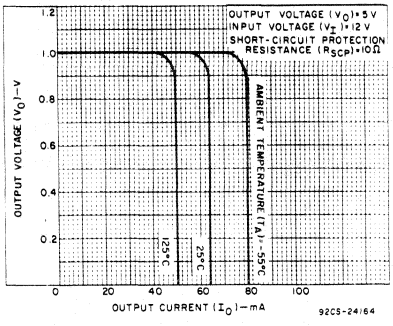


Fig. 9 – Current limiting characteristics.

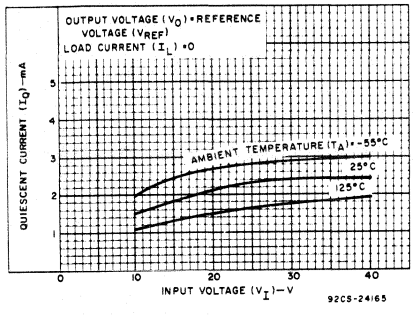


Fig. 10 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

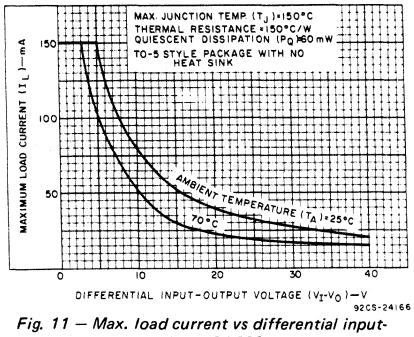


Fig. 11 – Max. load current vs differential input-output voltage CA723CT.

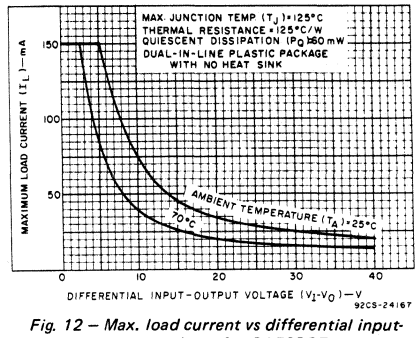


Fig. 12 – Max. load current vs differential input-output voltage for CA723CE.

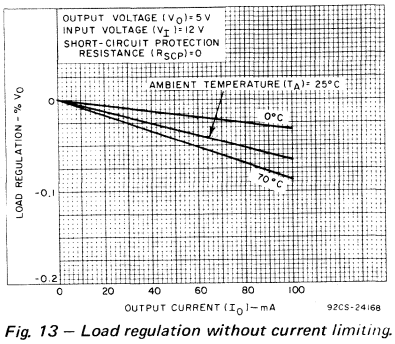


Fig. 13 – Load regulation without current limiting.

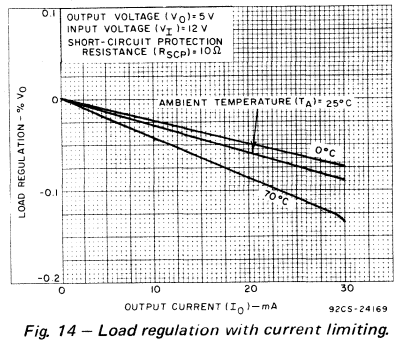


Fig. 14 – Load regulation with current limiting.

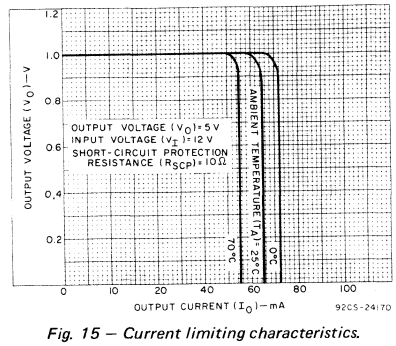


Fig. 15 – Current limiting characteristics.

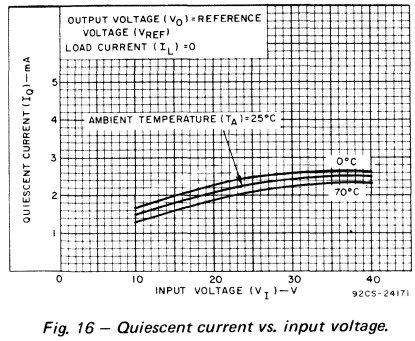


Fig. 16 – Quiescent current vs. input voltage.

CA723, CA723C

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

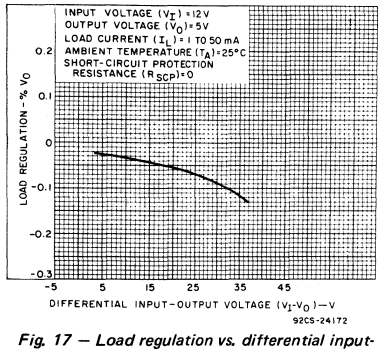


Fig. 17 — Load regulation vs. differential input-output voltage.

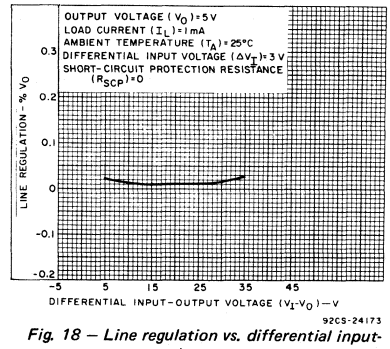


Fig. 18 — Line regulation vs. differential input-output voltage.

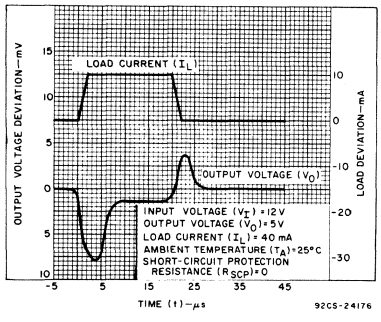


Fig. 19 — Line transient response.

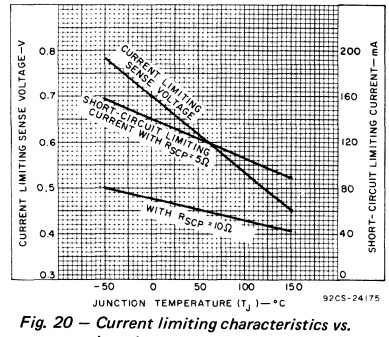


Fig. 20 — Current limiting characteristics vs. junction temperature.

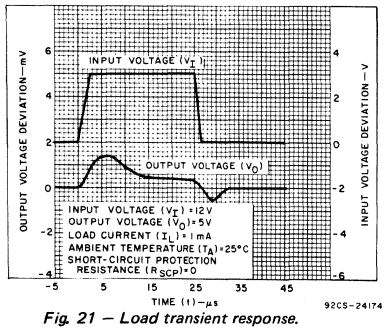


Fig. 21 — Load transient response.

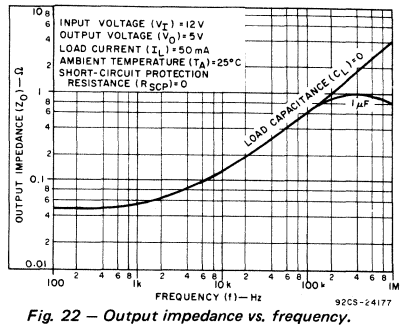


Fig. 22 — Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS

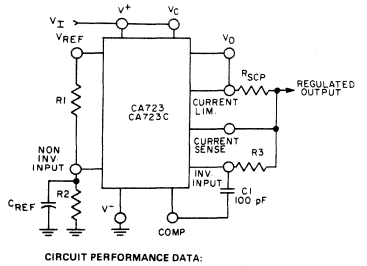


Fig. 23 — Low-voltage regulator circuit (V_O = 2 to 7 volts).

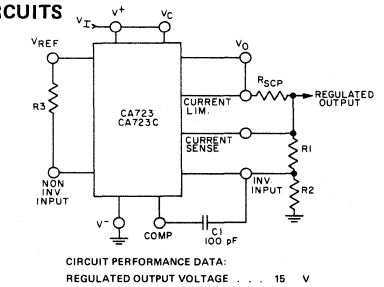
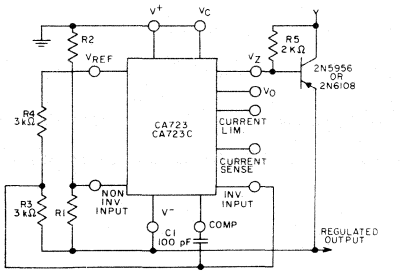


Fig. 24 — High-voltage regulator circuit (V_O = 7 to 37 volts).

TYPICAL APPLICATION CIRCUITS (Cont'd)



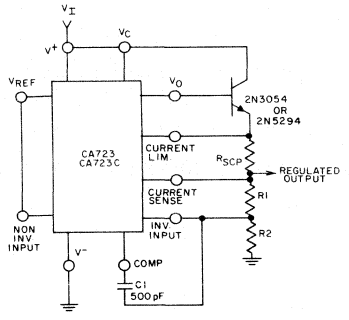
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−15 V
LINE REGULATION (ΔV_I = 3 V)	1 mV
LOAD REGULATION (ΔI_L = 100 mA)	2 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24180R1

Fig. 25 — Negative-voltage regulator circuit.

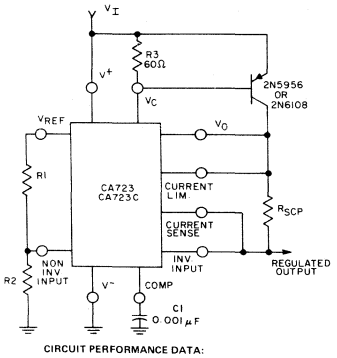


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 1 A)	15 mV

92CS-24181R1

Fig. 26 — Positive-voltage-regulator circuit (with external n-p-n pass transistor).

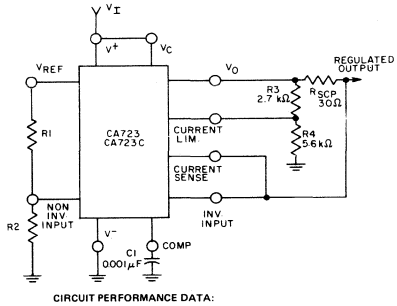


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 1 A)	5 mV

92CS-24182R1

Fig. 27 — Positive voltage-regulator circuit (with external p-n-p pass transistor).

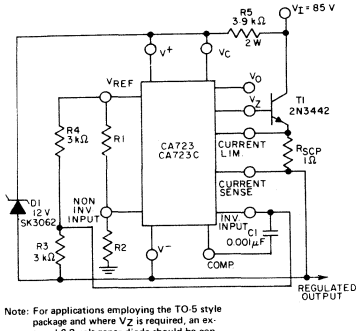


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 10 mA)	1 mV
SHORT-CIRCUIT CURRENT	20 mA

92CS-24183

Fig. 28 — Foldback current-limiting circuit.



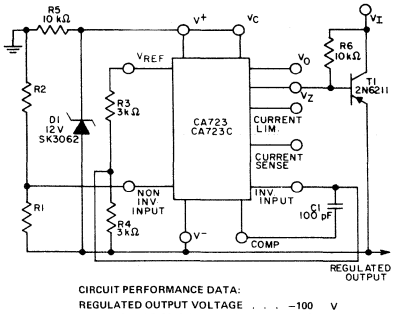
Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50 V
LINE REGULATION (ΔV_I = 20 V)	15 mV
LOAD REGULATION (ΔI_L = 50 mA)	20 mV

92CS-24184

Fig. 29 — Positive-floating regulator circuit.



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−100 V
LINE REGULATION (ΔV_I = 20 V)	30 mV
LOAD REGULATION (ΔI_L = 100 mA)	20 mV

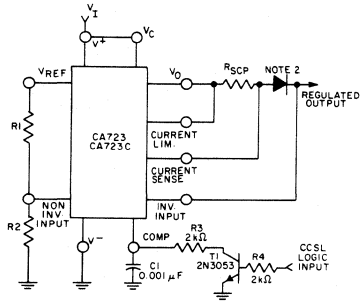
Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24185

Fig. 30 — Negative-floating regulator circuit.

CA723, CA723C

TYPICAL APPLICATION CIRCUITS (Cont'd)



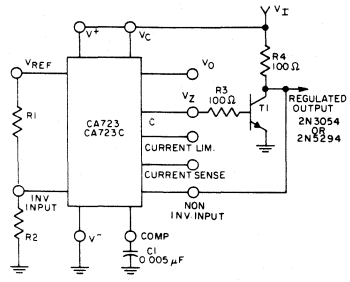
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	1.5 mV

Note 1: A current limiting transistor may be used for shutdown if current limiting is not required.
Note 2: Add a diode if $V_O > 10$ V.

92CS-24186R1

Fig. 31 – Remote shutdown regulator circuit with current limiting.



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 10 V)	0.5 mV
LOAD REGULATION (ΔI_L = 100 mA)	1.5 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

92CS-24187R1

Fig. 32 – Shunt regulator circuit.

Advance Information/
Preliminary Data

CA1523

Voltage Regulator Control Circuit For Variable Switching Regulator

Features:

- *Operates up to 200 kHz*
- *Pins ESD protected*
- *Remote ON/OFF*
- *Slow start with reset*
- *Overcurrent sensing*
- *Lower peak currents than PWM regulator: Less prone to magnetic saturation*

The RCA CA1523* monolithic silicon integrated circuit is a variable interval pulse regulator designed to provide the control circuitry for use in switching regulator circuits. It operates from 11 to 15 volts.

* Formerly RCA Developmental Type No. TA11977

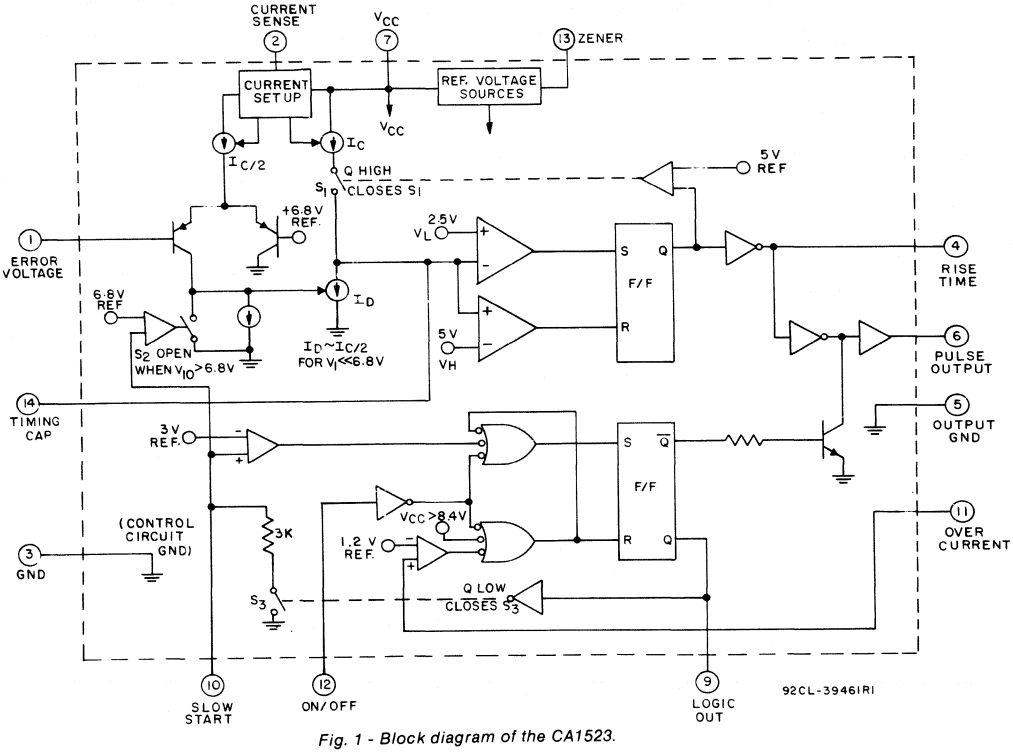


Fig. 1 - Block diagram of the CA1523.

File Number **1785**

CA1523

The regulator provides a single output drive capable of 300mA source/200mA sink. The maximum operating frequency is better than 200 kHz. An attractive feature of the CA1523 is that the timing capacitor charge and discharge current is set up externally via a single resistor. The ratio of charge to discharge current is internally set at a maximum of 2 to 1 allowing simultaneous change in output pulse width with increased frequency at higher load. The pulse width variation at higher frequencies effectively compensates for the losses in magnetics and thereby increases the power supply efficiency at higher load end by as much as 20 percent.

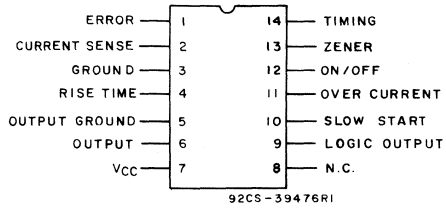
Other desirable features along with various circuit block function explanations are listed below.

- The **Oscillator** is a sawtooth generator whose charge (rise) cycle determines the output pulse width and discharge which is continuously variable from very low to maximum of I_{charge}.
  Charge $I_{charge} = I_o - I_{Discharge}$ giving 2 to 1 pulse-width control
  Discharge $I_{Discharge}$ = approximately 0 to 1/2 I_o to frequency control
- **Pulse Shaping:** Applied to the oscillator output via RS Flip-Flop with parallel inhibit controlled by slow-start overcurrent sense, supply voltage monitor and ON/OFF functions.
- **Pulse Rise Time:** Modified to meet RFI requirements by external slow-down capacitor.
- **Slow Start with Reset:** Externally programmed against internal 3V reference. Reset is initiated upon Inhibit ensuring soft start at power up and restart.
- **Over Current Sense:** Internal stable thresholds of 1.2V.
- **Supply Voltage Monitors:** Locks out the drive until V_{supply} has reached 8-9V.
- **ON/OFF:** Activates regulator independent of raw DC.
- **Error Amplifier:** Compares output against a stable 6.8V internal reference and controls the discharge current sink on the timing capacitor.
- **Band-Gap:** Reference voltage (internal) provides temperature compensated 1.2V and 6.8V references.
- **Separate GND:** The power GND is separated from circuit ground for improved noise.
- **ESD Protection:** Pins are protected against ESD.

The CA1523 is supplied in a 14-lead dual-in-line plastic package (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 15 V
SUPPLY CURRENT:
$I_{6(max.)}$ ..... ±50 mA
$I_{6(max.)}$, 1 μs, 1800 pF Load ..... +300, -200 mA
DEVICE DISSIPATION:
Up to T_A = 70°C ..... 530 mW
Above T_A = 70°C ..... Derate linearly at 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to 70°C
Storage ..... -55 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± in (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



CA1523
TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS, T_A = 25°C
Refer to the condition shown in the test circuit; V_7 = 13 V, V_1 = 5.9 V unless otherwise stated

CHARACTERISTIC	PIN	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Power Supply, V_{CC} (Pin 7)						
Supply Voltage	7	—	9.5	13	—	V
Supply Current	7	V_{CC} = +13 V	20	27	34	mA
Zener Voltage	13	—	7.8	8.4	8.9	V
Output Pulse (Pin 6)						
Maximum Pulse Width	6	Measured at 6 V Threshold Level	5.5	6.5	7.5	μs
Minimum Pulse Width	6	Measured at 6 V Threshold Level	2	3	4	μs
Output High Voltage	6	I_6 = 0 mA, V_4 = 0 V	11.1	12	12.6	V
Output Low Voltage	6	I_6 = 50 mA, V_{12} = 0 V	0.6	1	1.3	V
Rise Time	6	Measured at 1.8 and 10 V Threshold Levels	250	600	1250	ns
Fall Time	6	Measured at 1.8 and 10 V Threshold Levels	50	200	350	ns
Error Voltage Range (Pin 1)						
Error Voltage Reference	1	Adjust R_T; Observe Pin 6 Min./Max. Freq. Range	5.9	6.8	7.5	V
Change Current (Pin 14)						
Charge Current	14	Adjust R_T, V_1 = 7.5 V; Set V_{14} = 0 V, Then V_{14} = 2.5 V	190	220	250	μA
Discharge Current	14	Adjust R_T, = 5.9 V; Set V_{14} = 5.5 V, Then 5 V	95	110	125	μA
Slow Start Discharge Current	14	Maintain V_{14} = 5 V, V_{10} = 5.5 V Set V_{10} = 5.5 V, Meas. I_{14} (Hi) Set V_{10} = 4 V, Meas. I_{14} (Lo) Limits = $\frac{I_{14}(Hi) - I_{14}(Lo)}{1.5}$	20	30	40	μA/V
Logic Tests						
Discharge Voltage	10	Pin 12 = 1k Ω to Gnd	1.7	2.4	3.2	V
Output Inhibit Voltage	7	Increase V_7 until $V_9 \geq 2$ V	7.9	8.4	9.1	V
Overcurrent Trip Voltage	11	V_{12} = 5 V; V_{10} = 0 V; Increase V_{11} until $V_9 \leq 0.5$ V	1.1	1.25	1.4	V

CA1523

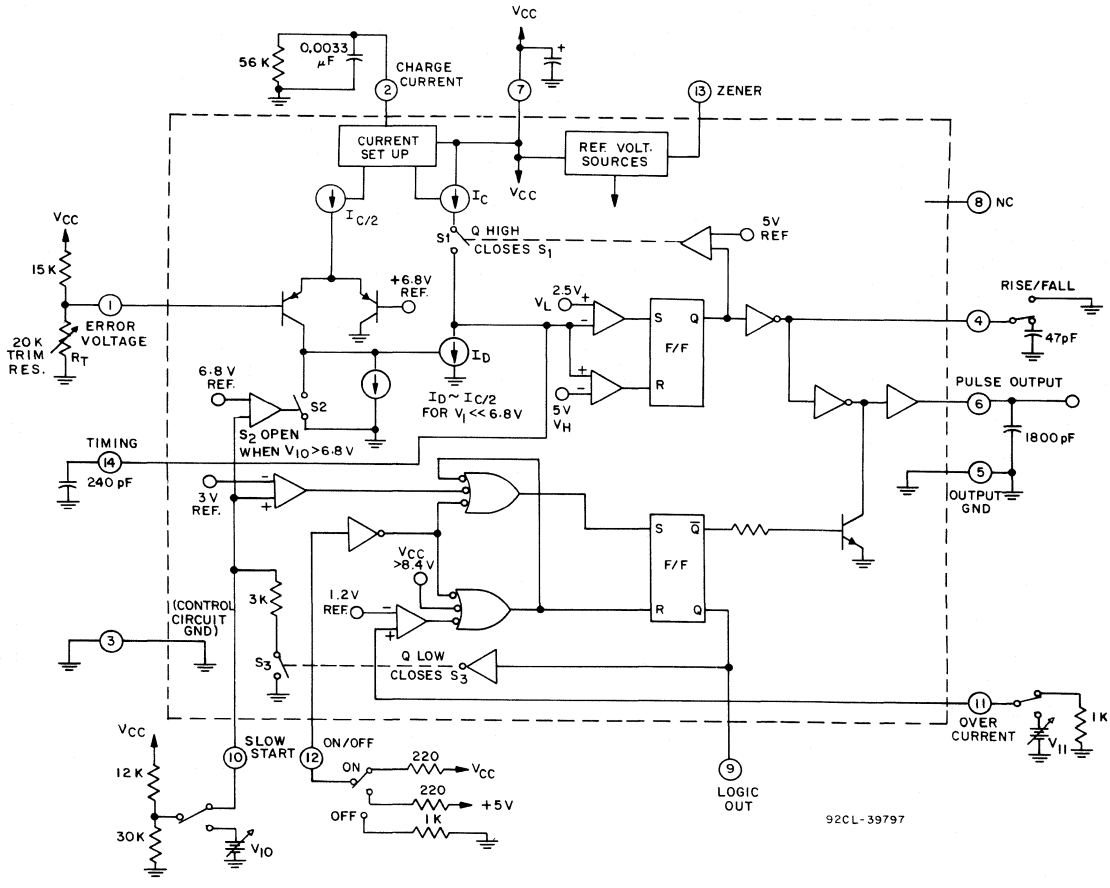


Fig. 2 - Test circuit for the CA1523.

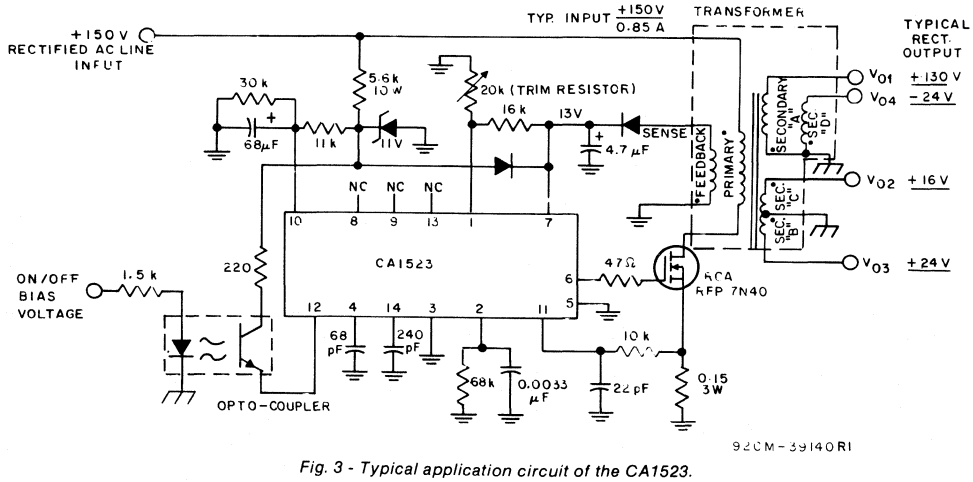


Fig. 3 - Typical application circuit of the CA1523.

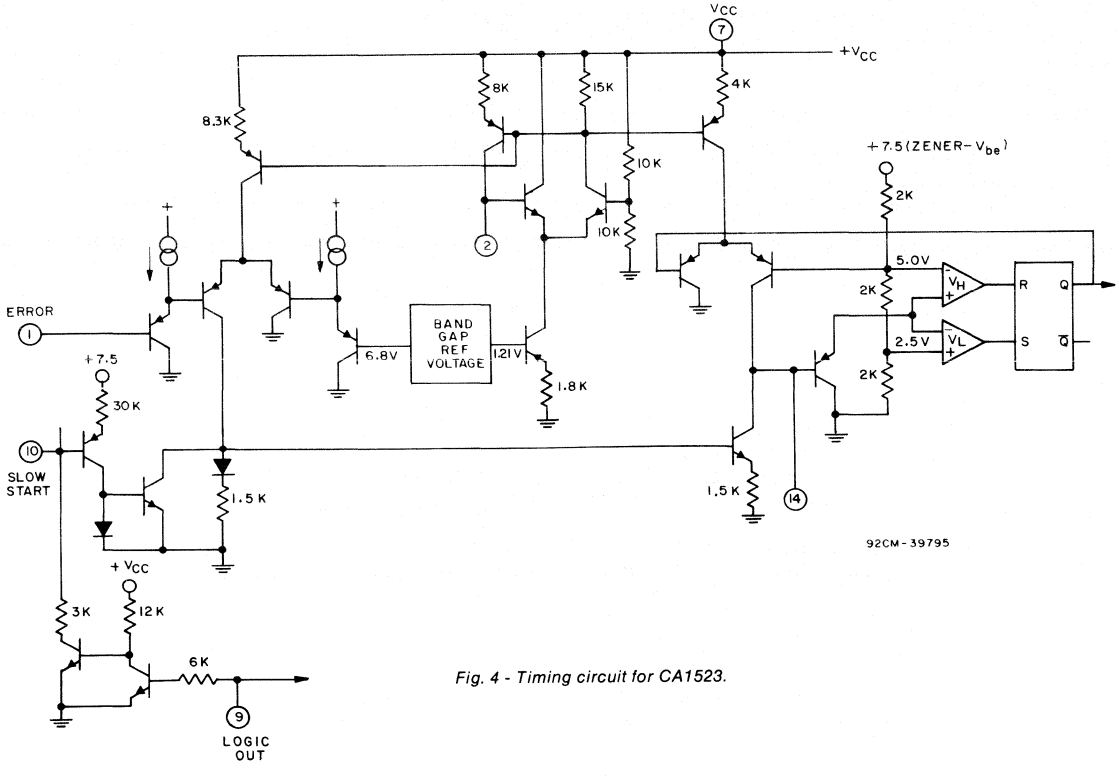


Fig. 4 - Timing circuit for CA1523.

CA1524, CA2524, CA3524

Regulating Pulse Width Modulator

Features:
- *Complete PWM power control circuitry*
- *Separate outputs for single-ended or push-pull operation*
- *Line and load regulation of 0.2% typ.*
- *Internal reference supply with 1% max. oscillator and reference voltage variation over full temperature range*
- *Standby current of less than 10 mA*
- *Frequency of operation beyond 100 kHz*
- *Variable-output dead time of 0.5 to 5 μs*
- *Low V_{CE}(sat) over the temperature range*

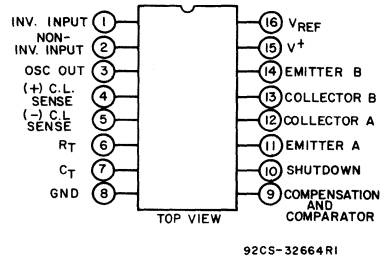
The RCA-CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524, respectively. A block diagram of the CA1524 series is shown in Fig. 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converters, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converters, as well as other power-control applications.

The CA1524 is specified for the military temperature range of −55° C to +125° C.

The CA2524 and CA3524 are specified for the commercial temperature range of 0° C to 70° C. All types operate over a supply voltage range of 8 to 40 V, have a rated operating temperature range of −55° C to +125° C, and are supplied in 16-lead, dual-in-line plastic packages (E suffix, and dual-in-line frit-seal hermetic packages (F suffix). The CA3524 is available in chip form (H suffix).

Applications:
- *Positive and negative regulated supplies*
- *Dual-output regulators*
- *Flyback converters*
- *DC-DC transformer-coupled regulating converters*
- *Single-ended DC-DC converters*
- *Variable power supplies*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

INPUT VOLTAGE (BETWEEN V_{IN} AND GROUND TERMINALS)	40 V
OPERATING VOLTAGE RANGE (V_{IN} TO GROUND)	8 to 40 V
OUTPUT CURRENT EACH OUTPUT: (TERMINALS 11, 12 or 13, 14)	100 mA
OUTPUT CURRENT (REFERENCE REGULATOR)	50 mA
OSCILLATOR CHARGING CURRENT	5 mA
DEVICE DISSIPATION:	
Up to T_A = 25° C	1 W
Above $T_A \doteq$ 25° C	Derate linearly 8 mW/° C
OPERATING TEMPERATURE RANGE	−55 to +125° C
STORAGE TEMPERATURE RANGE	−65 to +150° C

File Number **1239**

CA1524, CA2524, CA3524

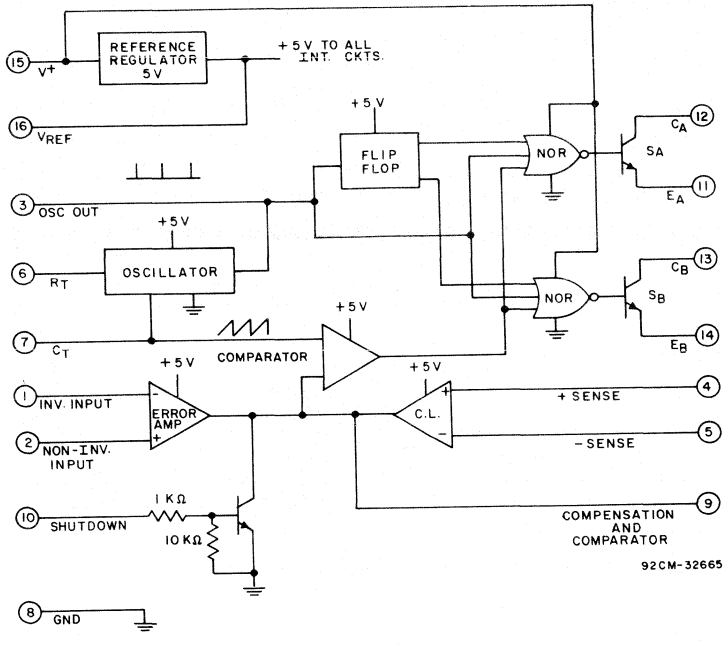


Fig. 1 - Functional block diagram of CA1524 series.

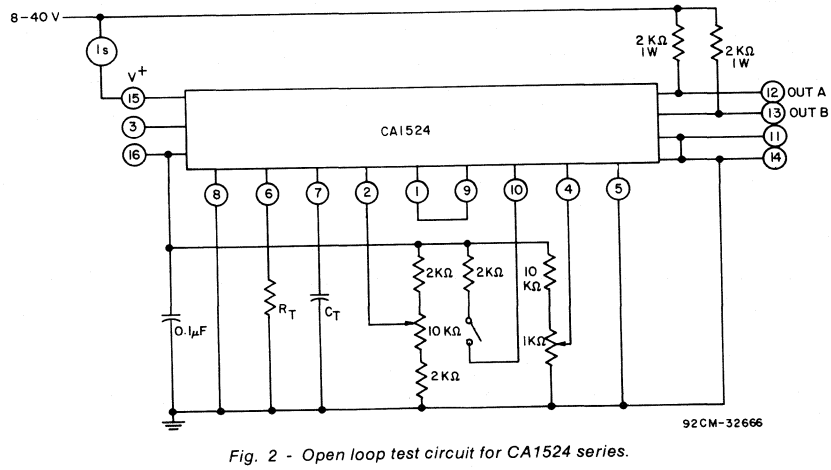
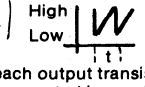


Fig. 2 - Open loop test circuit for CA1524 series.

CA1524, CA2524, CA3524

ELECTRICAL CHARACTERISTICS at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V+=20 V and f=20 kHz, unless otherwise stated.

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section:								
Output Voltage		4.8	5	5.2	4.6	5	5.4	V
Line Regulation	V+=8 to 40 V	—	10	20	—	10	30	mV
Load Regulation	I_L=0 to 20 mA	—	20	50	—	20	50	mV
Ripple Rejection	f=120 Hz, T_A=25°C	—	66	—	—	66	—	dB
Short Circuit Current Limit	V_{REF}=0, T_A=25°C	—	100	—	—	100	—	mA
Temperature Stability	Over Operating Temperature Range	—	0.3	1	—	0.3	1	%
Long Term Stability	T_A=25°C	—	20	—	—	20	—	mV/khr
Oscillator Section:								
Maximum Frequency	C_T=0.001 μF, R_T=2 KΩ	—	300	—	—	300	—	kHz
Initial Accuracy	R_T and C_T constant	—	5	—	—	5	—	%
Voltage Stability	V+=8 to 40 V, T_A=25°C	—	—	1	—	—	1	%
Temperature Stability	Over Operating Temperature Range	—	—	2	—	—	2	%
Output Amplitude	Terminal 3, T_A=25°C	—	3.5	—	—	3.5	—	V
Output Pulse Width (Pin 3)	C_T=0.01 μF, T_A=25°C	—	0.5	—	—	0.5	—	μs
* Ramp Voltage Low	Pin 7	—	0.6	—	—	0.6	—	V
* Ramp Voltage High	Pin 7	—	3.5	—	—	3.5	—	V
Capacitor Charging Current Current Range	Pin 7 (5-2 V_{BE})/RT	0.03	—	2	0.03	—	2	mA
Timing Resistance Range	Pin 6	1.8	—	120	1.8	—	120	KΩ
Charging Capacitor Range	Pin 7	0.001	—	0.1	0.001	—	0.1	μF
Dead Time Expansion Capacitor on Pin 3 (when a small osc. cap is used)	Pin 3	100	—	1000	100	—	1000	pF
Error Amplifier Section:								
Input Offset Voltage	V_{CM}=2.5 V	—	0.5	5	—	2	10	mV
Input Bias Current	V_{CM}=2.5 V	—	1	10	—	1	10	μA
Open Loop Voltage Gain		72	80	—	60	80	—	dB
Common Mode Voltage	T_A=25°C	1.8	—	3.4	1.8	—	3.4	V
Common Mode Rejection Ratio	T_A=25°C	—	70	—	—	70	—	dB
Small Signal Bandwidth	A_V= 0 dB, T_A=25°C	—	3	—	—	3	—	MHz
Output Voltage	T_A=25°C	0.5	—	3.8	0.5	—	3.8	V
Amplifier Pole		—	250	—	—	250	—	Hz
Pin 9 Shutdown Current	External Sink	—	200	—	—	200	—	μA
Comparator Section:								
Duty Cycle	% Each Output On	0	—	45	0	—	45	%
Input Threshold	Zero Duty Cycle	—	1	—	—	1	—	V
Input Threshold	Max. Duty Cycle	—	3.5	—	—	3.5	—	V
Input Bias Current		—	1	—	—	1	—	μA
Current Limiting Section:								
Sense Voltage For 25% Output Duty Cycle	Terminal 9=2 V with Error Amplifier Set for Max Out, T_A=25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		—	0.2	—	—	0.2	—	mV/°C
Common Mode Voltage		-1	—	+1	-1	—	+1	V
Rolloff Pole of R51 C3 + Q64		—	300	—	—	300	—	Hz

*Ramp voltage at Pin 7 

where t = OSC period in microseconds
$t \cong R_T C_T$ with C_T in microfarads and R_T in ohms.

Output frequency at each output transistor is half OSC frequency when each output is used separately and is equal to the OSC frequency when each output is connected in parallel.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Section: (Each Output)								
Collector-Emitter Voltage		40	—	—	40	—	—	V
Collector Leakage Current	V_{CE}=40 V	—	0.1	50	—	0.1	50	μA
Saturation Voltage	V+=40 V, I_C=50 mA	—	0.8	2	—	0.8	2	V
Emitter Output Voltage	V+=20 V	17	18	—	17	18	—	V
Rise Time	R_C=2 KΩ, T_A=25°C	—	0.2	—	—	0.2	—	μs
Fall Time	R_C=2 KΩ, T_A=25°C	—	0.1	—	—	0.1	—	μs
Total Standby Current:* I_S	V+=40 V	—	4	10	—	4	10	mA

*Excluding oscillator charging current, error and current limit dividers, and with outputs open.

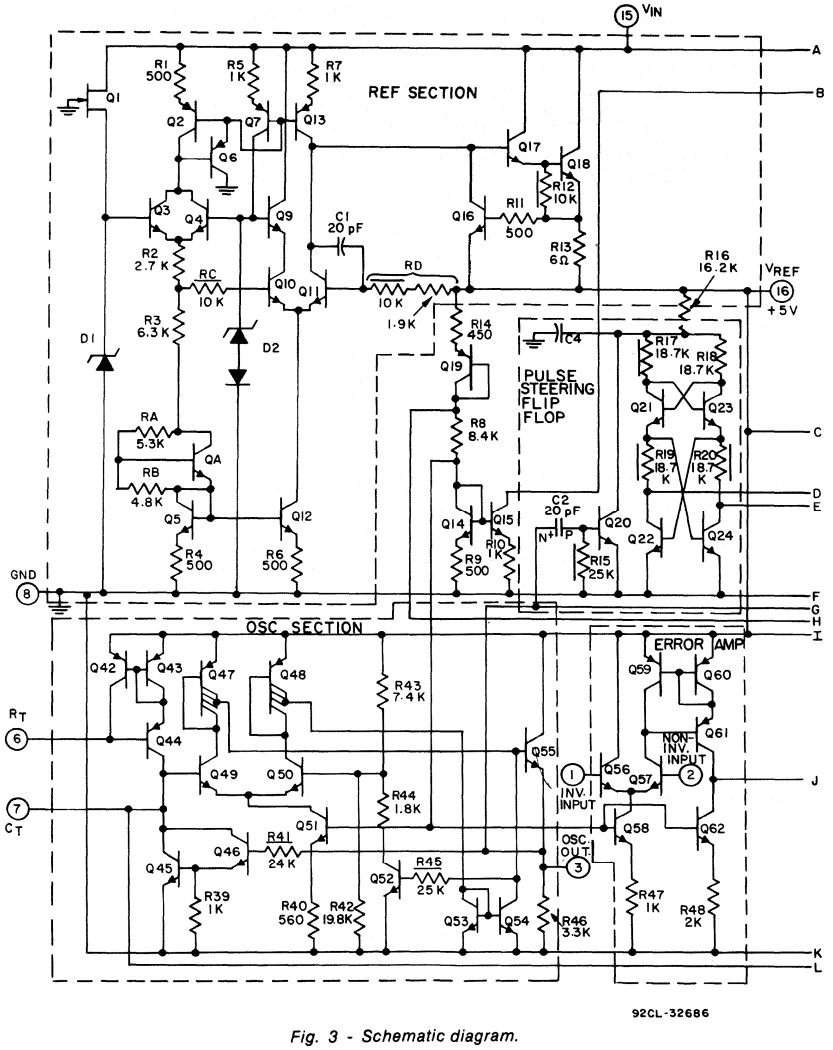


Fig. 3 - Schematic diagram.

CA1524, CA2524, CA3524

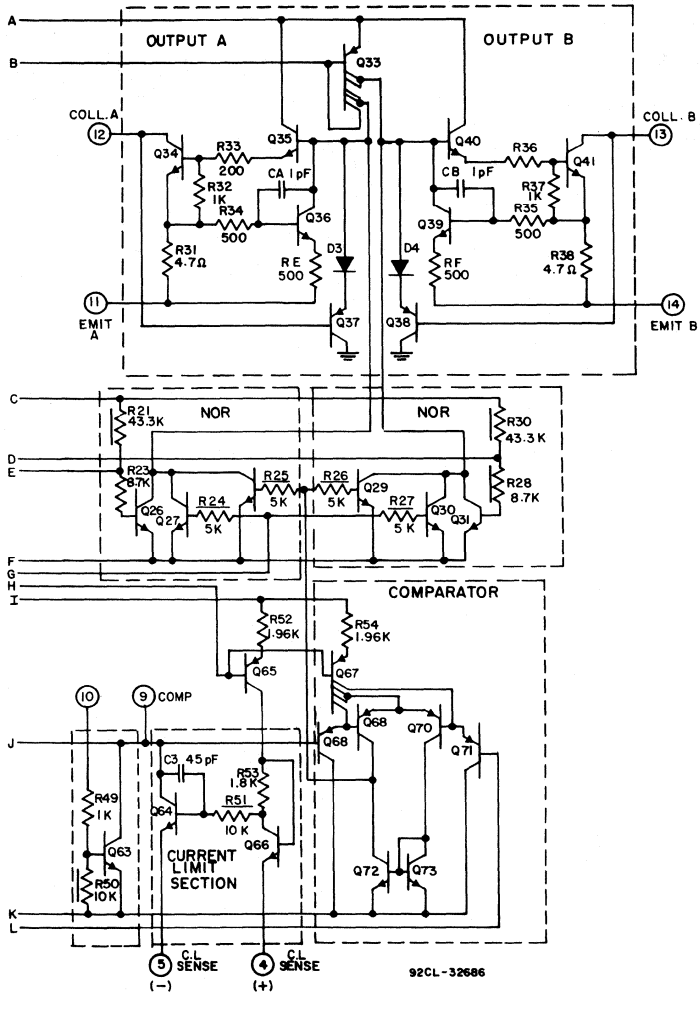


Fig. 3 - Schematic diagram (cont'd).

CA1524, CA2524, CA3524

CIRCUIT DESCRIPTION

Voltage Reference Section

The CA1524 series contains an internal series voltage regulator employing a zener reference to provide a nominal 5-volt output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50-mA output current.

Fig. 4 shows the temperature variation of the reference voltage with supply voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 5 and 6, respectively.

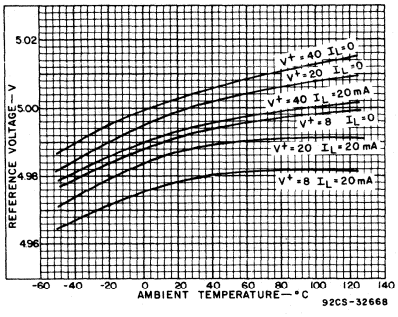


Fig. 4 - Typical reference voltage as a function of ambient temperature.

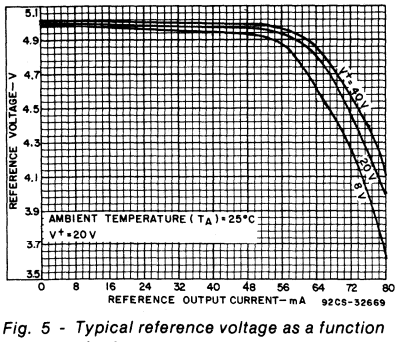


Fig. 5 - Typical reference voltage as a function of reference output current.

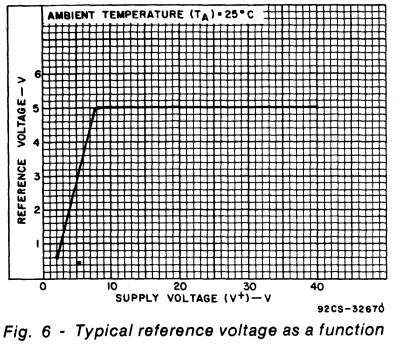


Fig. 6 - Typical reference voltage as a function of supply voltage.

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to $(5-2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30 μA to 2 mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5 μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control of blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Fig. 7. Pulse widths less than 0.5 μs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

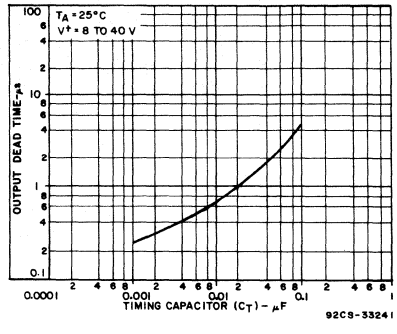


Fig. 7 - Typical output stage dead time as a function of timing capacitor value.

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF but no greater than 1000 pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2-KΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable.

The oscillator period is determined by R_T and C_T, with an approximate value of $t=R_TC_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals. Fig. 8 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 10. To synchronize two or more CA1524's, one must be designated as master, with

CA1524, CA2524, CA3524

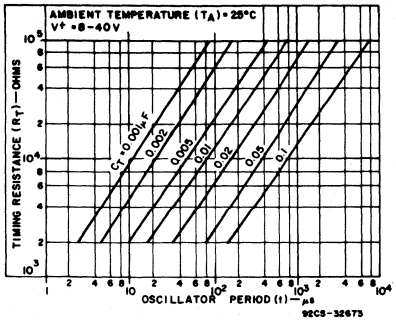


Fig. 8 - Typical oscillator period as a function of R_T and C_T.

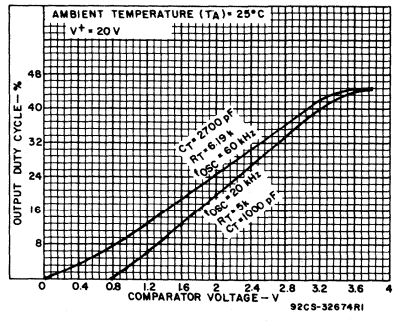


Fig. 10 - Typical duty cycle as a function of comparator voltage (at terminal 9).

R_TC_T set for the correct period. Each of the remaining units (slaves) must have a C_T of ½ the value used in the master and approximately a 10% longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{out}, terminal 9, is very high (≅ 5 MΩ).

The gain is:

$$A_V = g_m R = 8\, I_C\, R/2KT = 10^4,$$

where $R = \dfrac{R_{out}\, R_L}{R_{out}+R_L}$, $R_L = \infty$, $A_V \propto 10^4$

Since R_{out} is extremely high, the gain can be easily reduced from a nominal 10^4 (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 9.

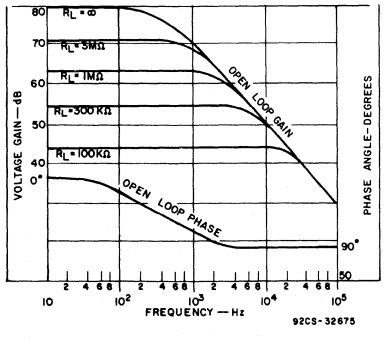


Fig. 9 - Open-loop error amplifier response characteristics.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Fig. 10. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000-pF capacitor and a variable series 50-KΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200 μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 11. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

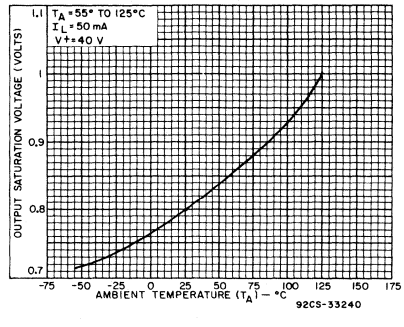


Fig. 11 - Typical output saturation voltage as a function of ambient temperature.

Output Section

The CA1524 series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 11 and 12, respectively.

There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

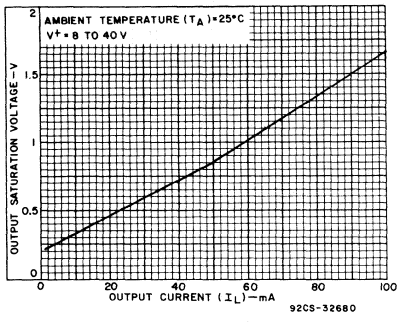


Fig. 12 - Typical output saturation voltage as a function of output current.

Device Application Suggestions

For higher currents, the circuit of Fig. 13 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5-volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

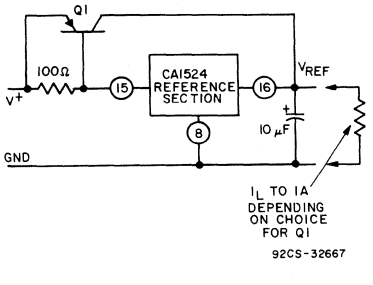


Fig. 13 - Circuit for expanding the reference current capability.

The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 14. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

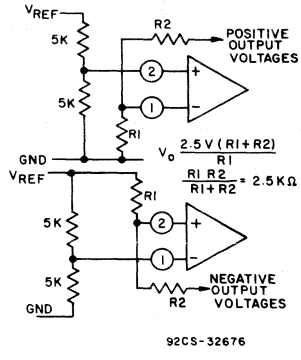


Fig. 14 - Error amplifier biasing circuits.

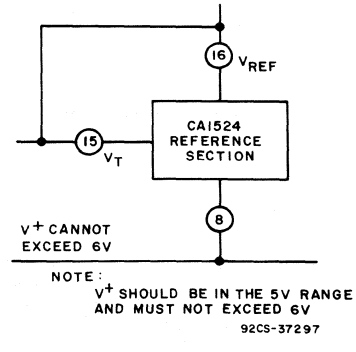


Fig. 15 - Circuit to allow external bypass of the reference regulation.

To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 16 may be used.

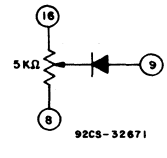


Fig. 16 - Circuit for expansion of dead time, without using a capacitor on pin 3 or when a low value oscillator capacitor is used.

CA1524, CA2524, CA3524

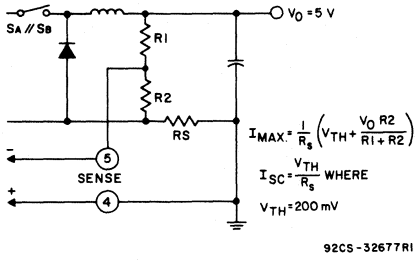


Fig. 17 - Foldback current-limiting circuit used to reduce power dissipation under shorted output conditions.

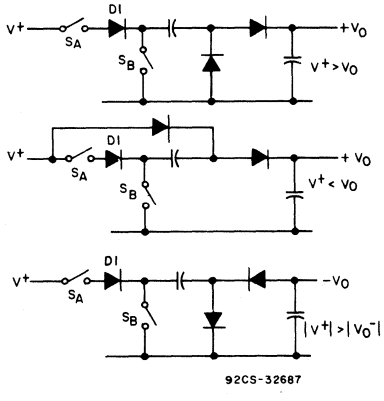


Fig. 18 - Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch S_A).

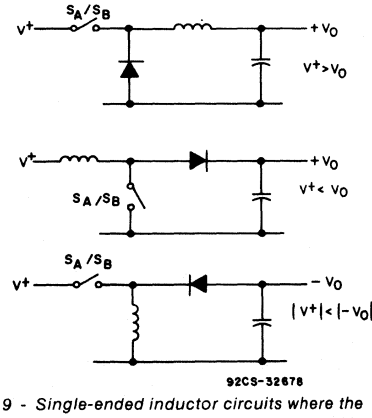


Fig. 19 - Single-ended inductor circuits where the two outputs of the 1524 are connected in parallel.

Table I - Input vs. Output voltage, and Feedback Resistor Values for I_L=40 mA (For capacitor-diode output circuit in Fig. 21)

V_O (V)	R2 (KΩ)	V+ (Min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

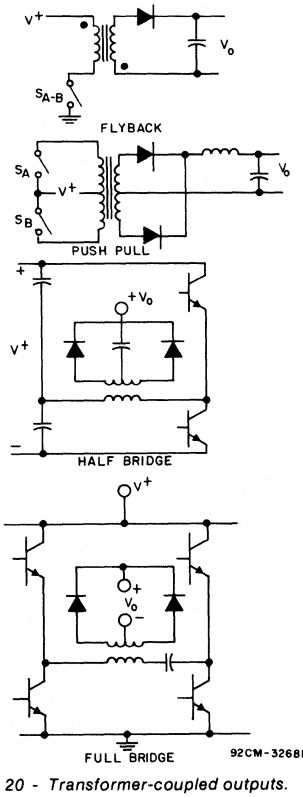


Fig. 20 - Transformer-coupled outputs.

APPLICATIONS*

A capacitor-diode output filter is used in Fig. 22 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 21 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5 V to -20 V with an output current of 40 mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 22 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

*For additional information on the application of this device and a further explanation of the circuits below, see RCA Application Note ICAN-6915 "Application of the CA1524 series PWM IC".

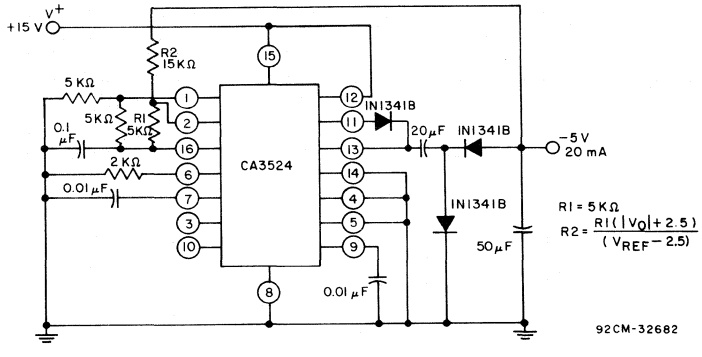


Fig. 21 - Capacitor-diode output circuit.

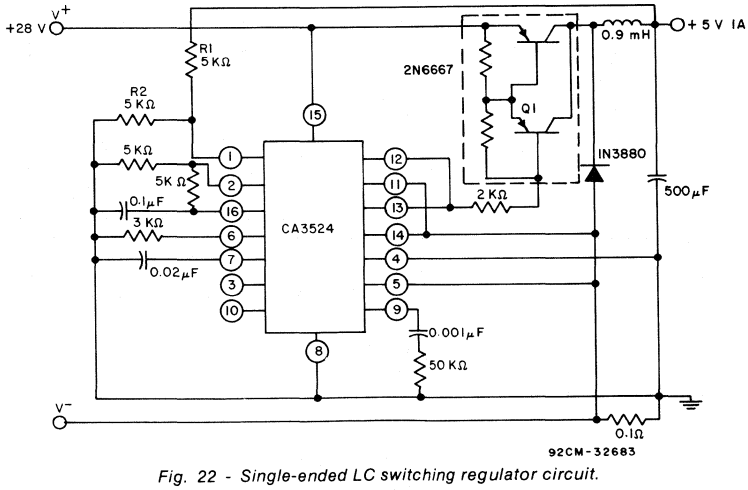


Fig. 22 - Single-ended LC switching regulator circuit.

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Flyback Converter

Fig. 23 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 24. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low-Frequency Pulse Generator

Fig. 25 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5-V (or 2.5-V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz, respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R1; R2 controls duty cycle.

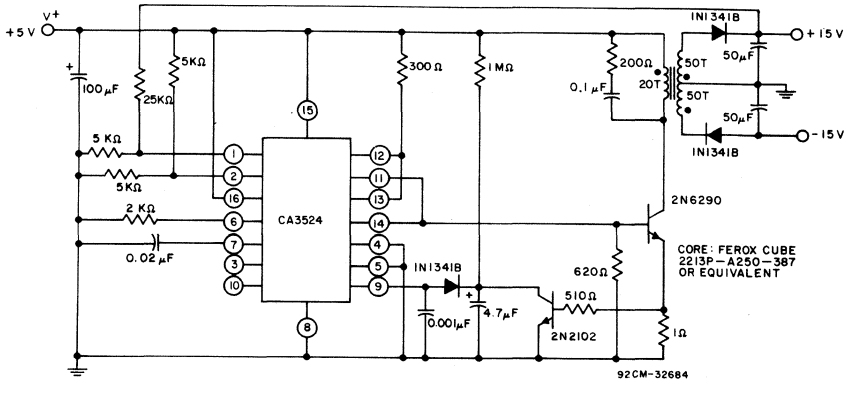


Fig. 23 - Flyback converter circuit.

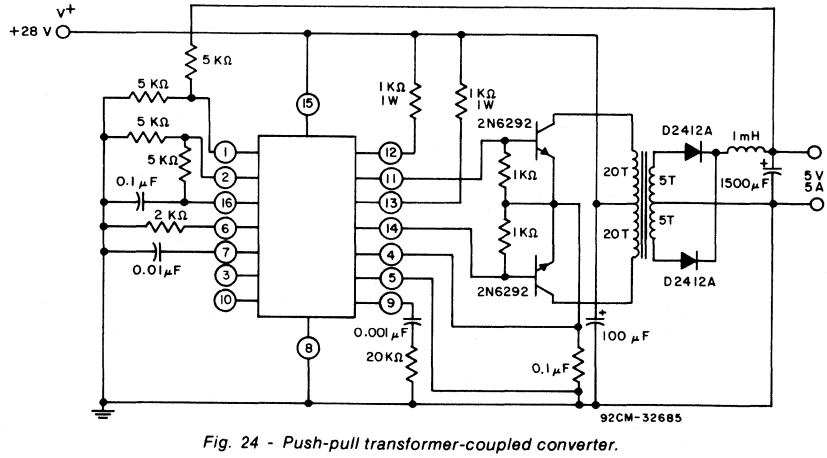


Fig. 24 - Push-pull transformer-coupled converter.

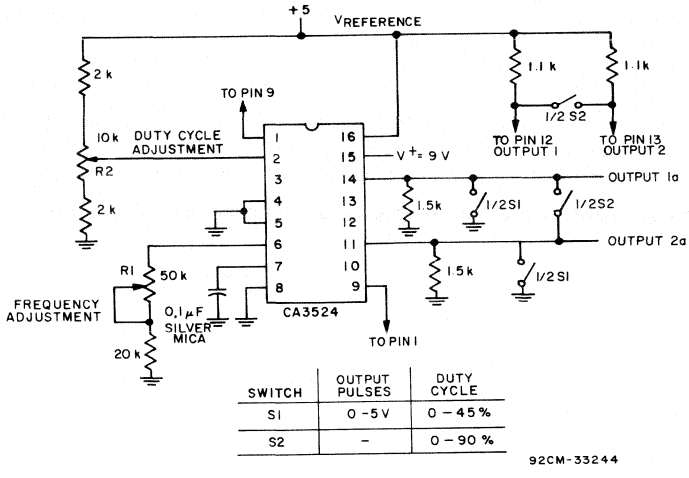


Fig. 25 - Low-frequency pulse generator.

The Variable Switcher

The circuit diagram of the CA1524, used as a variable-output-voltage power supply is shown in Fig. 26. By connecting the two output transistors in parallel, the duty cycle is doubled, i.e., 0-90%.

As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage.

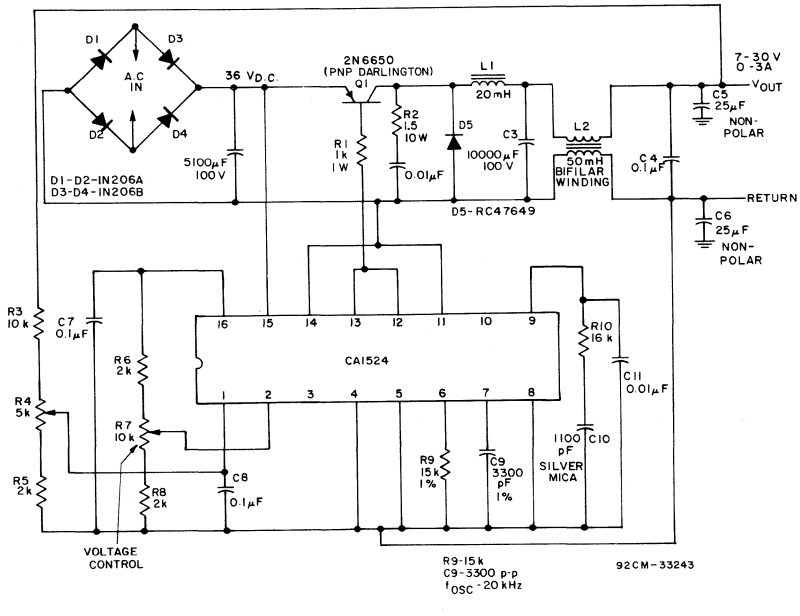


Fig. 26 - The CA1524 used as a 0-5 A, 7-30 V laboratory supply.

CA1524, CA2524, CA3524

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 27 and 28 uses half (Q2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

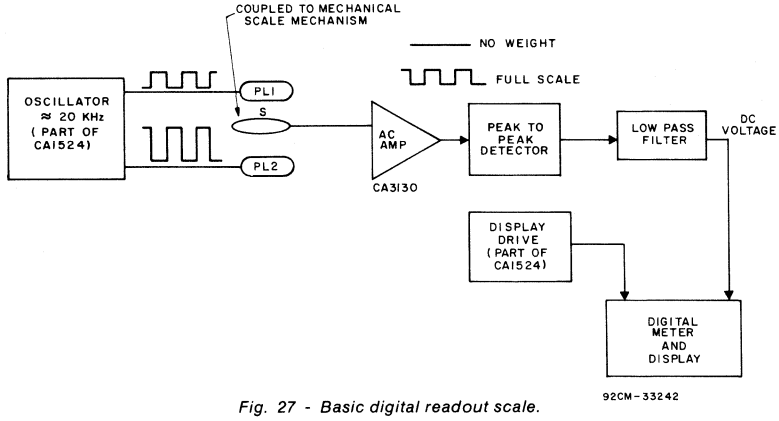


Fig. 27 - Basic digital readout scale.

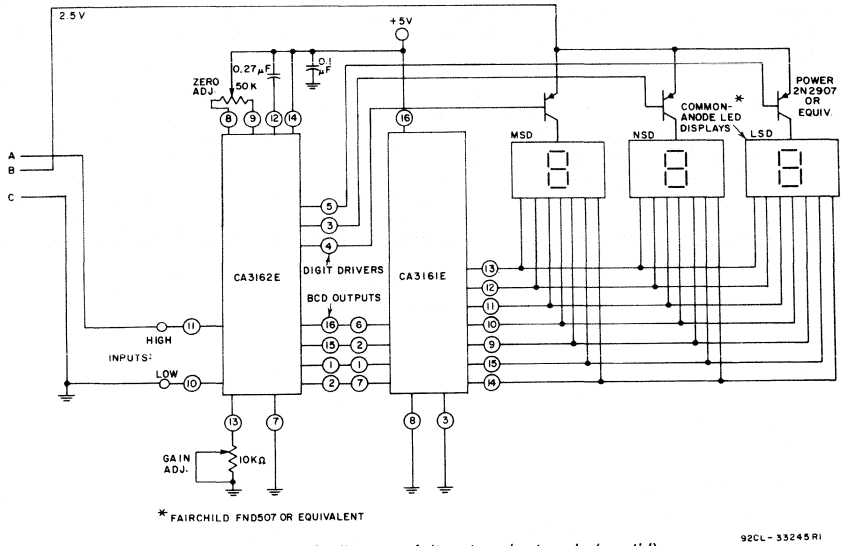


Fig. 28 - Schematic diagram of digital readout scale (cont'd).

CA1524, CA2524, CA3524

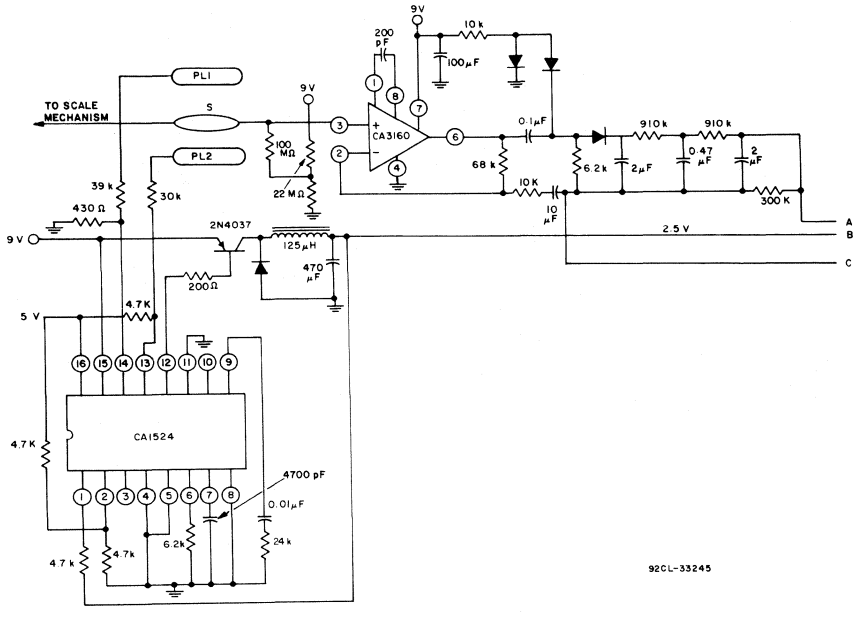
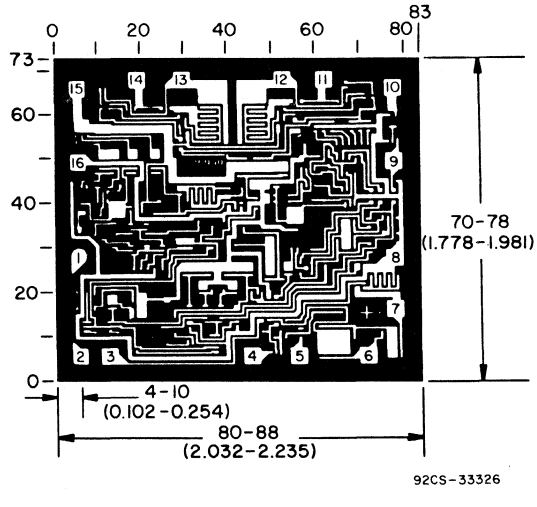


Fig. 28 - Schematic diagram of digital readout scale.



Dimensions and pad layout for CA3524H chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3020, CA3020A

lultipurpose Wide-Band ower Amplifiers

ır Military, Industrial,
d Commercial Equipment
Frequencies up to 8 MHz

atures:

- **High power output — class B amplifier. . .**
  CA3020 — 0.5 W typ. at V_{CC} = +9 V
  CA3020A — 1.0 W typ. at V_{CC} = +12 V
- **Wide frequency range. . .**
  Up to 8 MHz with resistive loads
  High power gain. . .75 dB typ.
- **Single power supply for class B operation with transformer. . .**
  CA3020 — 3 to 9 V
  CA3020A — 3 to 12 V
- **Built-in temperature-tracking voltage regulator provides stable operation over -55° C to +125° C temperature range**

e RCA-CA3020 and CA3020A are integrated-circuit, multi-ge, multipurpose, wide-band power amplifiers on a single nolithic silicon chip. They employ a highly versatile and ble direct-coupled circuit configuration featuring wide fre-ency range, high voltage and power gain, and high power tput. These features plus inherent stability over a wide nperature range make the CA3020 and CA3020A extremely ɜful for a wide variety of applications in military, industrial, d commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt dc supply with a typical power gain of 75 dB. The CA3020 provides 0.5-watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

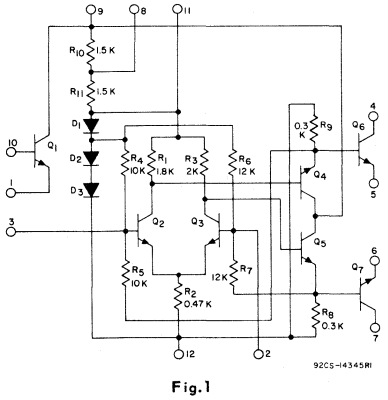


Fig.1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Applications:

- **AF power amplifiers for portable and fixed sound and communications systems**
- **Servo-control amplifiers**
- **Wide-band linear mixers**
- **Video power amplifiers**
- **Transmission-line driver amplifiers (balanced and unbalanced)**
- **Fan-in and fan-out amplifiers for computer logic circuits**
- **Lamp-control amplifiers**
- **Motor-control amplifiers**
- **Power multivibrators**
- **Power switches**
- **Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"**

File Number **339**

CA3020, CA3020A

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK		WITH HEAT SINK	
At T_A = 25°C	1 W	At T_C = 25°C	2 W
Above T_A = 25°C	derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C	2 W
		Above T_C = 55°C	derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -55°C to +125°C
Storage . . . . . -65°C to +150°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

▲ Higher value is for CA3020A.

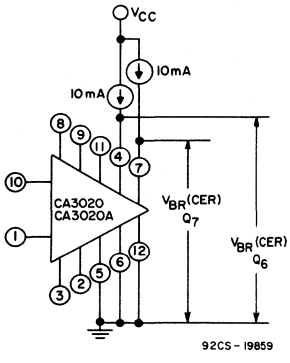
ECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE								
		FIG.	V_{CC1}	V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
lector-to-Emitter eakdown Voltage, Q_6 & Q_7 10 mA	$V_{(BR)CER}$	2_a	-	-	18	-	-	25	-	-	V
lector-to-Emitter eakdown Voltage, Q_1 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	8	9.0	2.0	-	5.5	-	-	5.5	-	mA
ık Output Currents, $_6$ & Q_7	I_4PK I_7PK	8	9.0	2.0	140	-	-	180	-	-	mA
off Currents, $_6$ & Q_7	I_4 CUTOFF I_7 CUTOFF	8	9.0	2.0	-	-	1.0	-	-	1.0	mA
feretial Amplifier urrent Drain	I_{CC1}	8	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
tal Current Drain	I_{CC1} + I_{CC2}	8	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
ferential Amplifier put Terminal Voltages	V_2 V_3	8	9.0	2.0	-	1.11	-	-	1.11	-	V
gulator Terminal Voltage	V_{11}	8	9.0	2.0	-	2.35	-	-	2.35	-	V
Cutoff (Leakage) Currents: ollector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
mitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
ollector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
rward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
ndwidth at -3 dB Point	BW	9	6.0	6.0	-	8	-	-	8	-	MHz
aximum Power Output	$P_{O(MAX)}$	10	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
nsitivity for P_{OUT} = 400 mW	e_{IN}	10	9.0	9.0	-	35[a]	55	-	-	-	mV
nsitivity for P_{OUT} = 800 mW	e_{IN}	10	9.0	12.0	-	-	-	-	50[b]	100	mV
put Resistance---- Terminal 3 to Ground	R_{IN3}	11	6.0	6.0	-	1000	-	-	1000	-	Ω
unction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

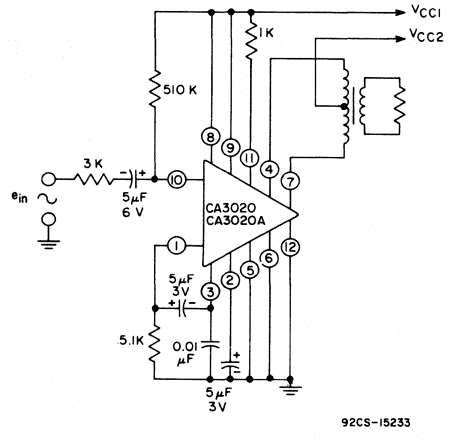
R_{CC} = 130 Ω

R_{CC} = 200 Ω

CA3020, CA3020A



a. Collector-to-Emitter Breakdown Voltage (Q_6 and Q_7) Circuit



b. Typical Audio Amplifier Circuit Utilizing the CA3020 or CA3020A As An Audio Preamplifier and Class B Power Amplifier

Fig.2

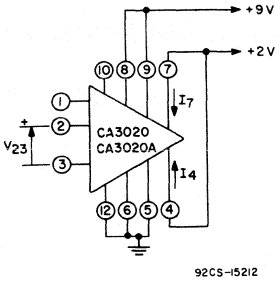
TYPICAL PERFORMANCE DATA*

An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%	P_O	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

* Refer to Figs.8 through 12 for Measurement and Symbol Information.

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

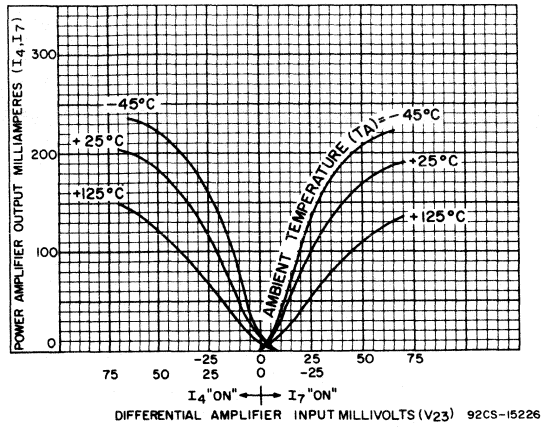
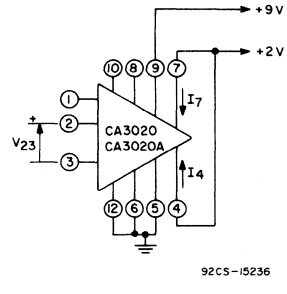


Fig.3 b. Characteristics with R_{10} shorted out



a. Test Setup

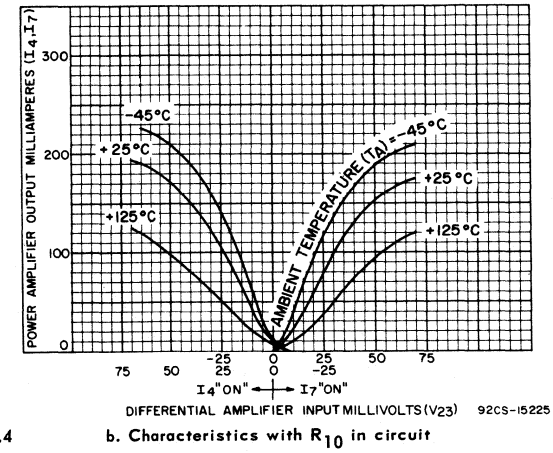
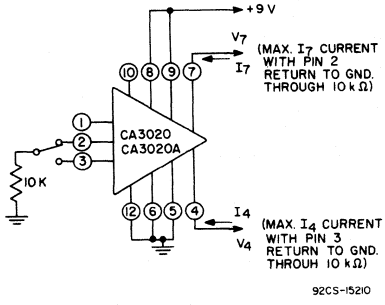


Fig.4 b. Characteristics with R_{10} in circuit

"MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup

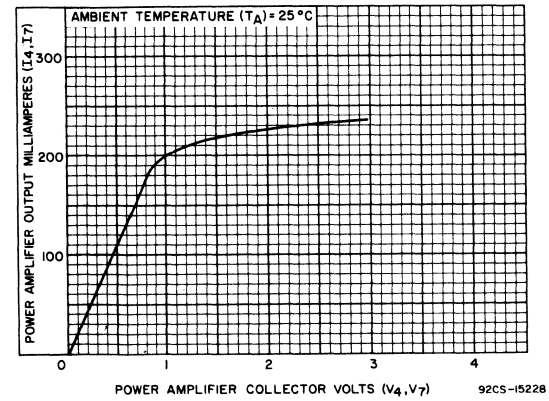
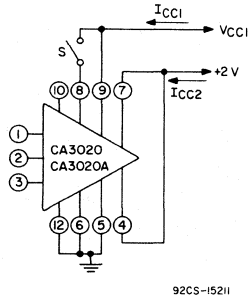


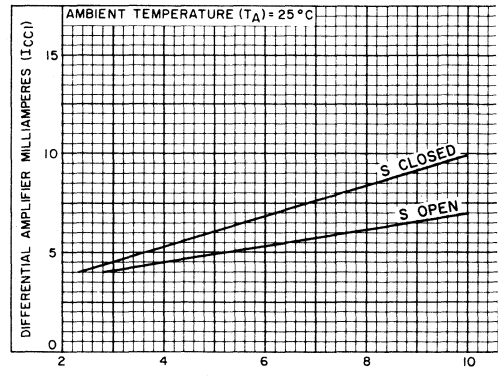
Fig.5 b. Characteristic

CA3020, CA3020A

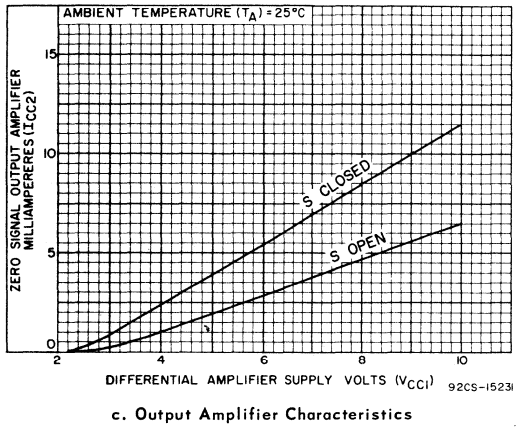
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



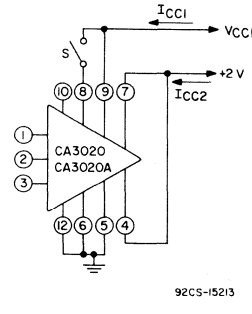
b. Differential Amplifier Characteristics



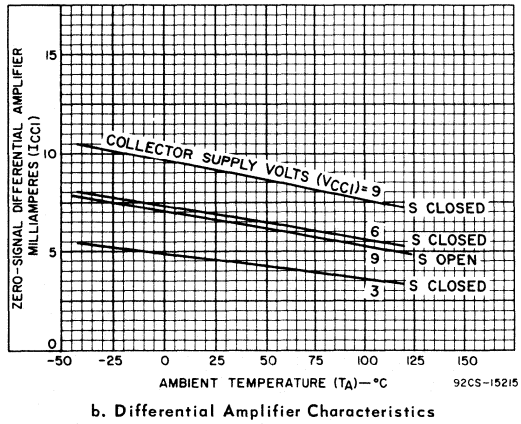
c. Output Amplifier Characteristics

Fig.6

ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE

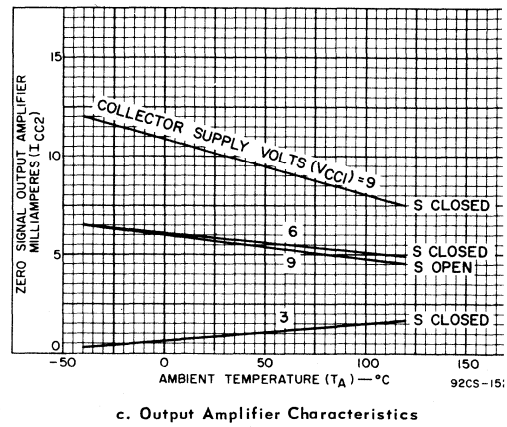


a. Test Setup



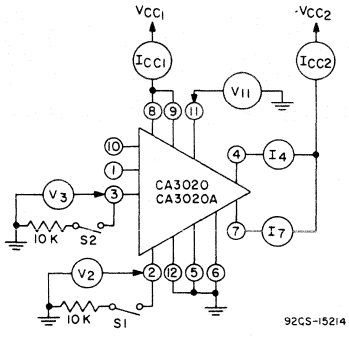
b. Differential Amplifier Characteristics

Fig.7



c. Output Amplifier Characteristics

STATIC CURRENT AND VOLTAGE TEST CIRCUIT



CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.8

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

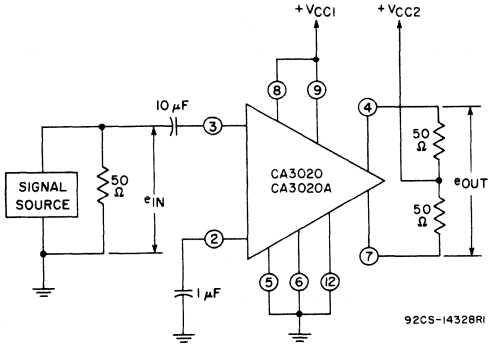


Fig.9

PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN

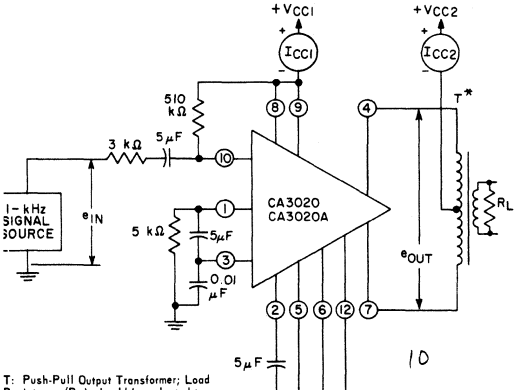


Fig.10

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100 \frac{P_{OUT}}{V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}}$$

where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) = $\dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

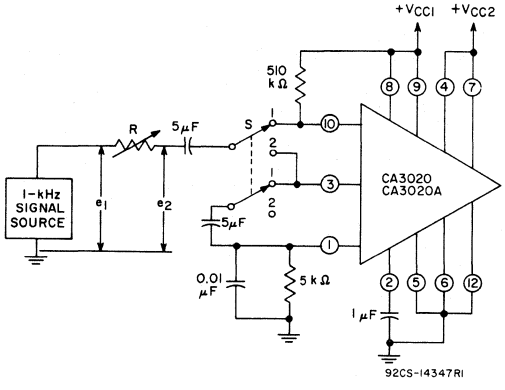
PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

CA3020, CA3020A

MEASUREMENT OF INPUT RESISTANCE



PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

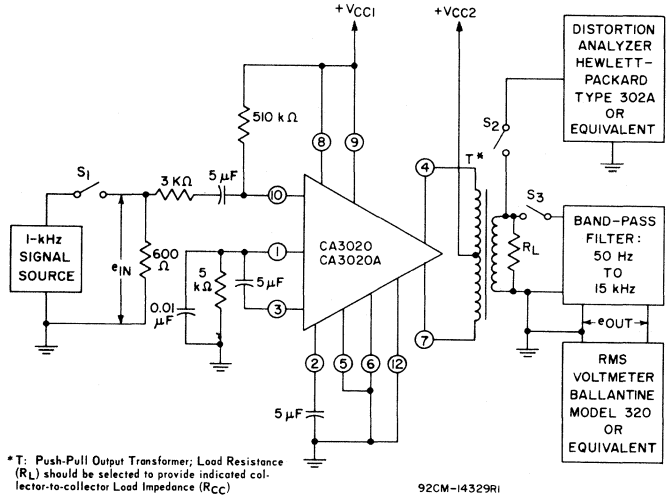
1. Apply desired value of V_{CC_1} and V_{CC_2} and set S Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

Fig.11

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10}\frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

Fig.12

CA3059, CA3079

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

Applications:

Relay control
Valve control
Synchronous switching of flashing lights
On-off motor switching
Differential comparator with self-contained power supply for industrial applications
Photosensitive control
Power one-shot control
Heater control
Lamp control

The RCA-CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

Limiter-Power Supply — Permits operation directly from an AC line.

Differential On/Off Sensing Amplifier — Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.

Zero-Crossing Detector — Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.

Triac Gating Circuit — Provides high-current pulses to the gate of the power controlling thrysistor.

In addition, the CA3059 provides the following important auxiliary functions (see Fig. 1):

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations, page 11. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3059 and CA3079)".

The CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages. The CA3079 is also available in chip form (H suffix).

Features	CA3059	CA3079
■ *24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation*	√	√
■ *Differential Input*	√	√
■ *Low Balance Input Current (max.) -μA*	1	2
■ *Built-in Protection Circuit for opened or shorted sensor (Term. 14)*	√	
■ *Sensor Range (Rx) - kΩ*	2 to 100	2 to 50
■ *DC Mode (Term 12)*	√	
■ *External Trigger (Term 6)*	√	
■ *External Inhibit (Term 1)*	√	
■ *DC Supply Volts (max.)*	14	10
■ *Operating Temperature Range - °C*	-55 to +125	

File Number **490**

CA3059, CA3079

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
- CA3059 14
- CA3079 10

DC SUPPLY VOLTAGE, (BETWEEN TERMS. 2 AND 8):
- CA3059 14
- CA3079 10

PEAK SUPPLY CURRENT (TERMS. 5 AND 7) ..... ± 50 m
OUTPUT PULSE CURRENT (TERM. 4) ..... 150 m
POWER DISSIPATIONS:
- Up to TA = 55°C - CA3059, CA3079 ..... 700 m
- Above TA = 55°C - CA3059, CA3079 ..... Derate linearly 6.67 mW/°

AMBIENT TEMPERATURE RANGE:
- Operating ..... -55 to +125°
- Storage ..... -65 to +150°

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	MAXIMUM CURRENT RATINGS I_{IN} mA	MAXIMUM CURRENT RATINGS I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0▲ -14	0▲ -14	0 -14	0 -14	0 -14	*	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

Note 1 — Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

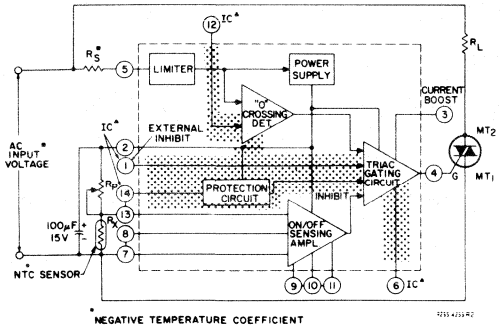
Note 2 — Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 — For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to −10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

CA3059, CA3079



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:

Circuitry, within shaded areas, not included in CA3079

- See chart
- ▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1 - Functional block diagram of CA3059 and CA3079.

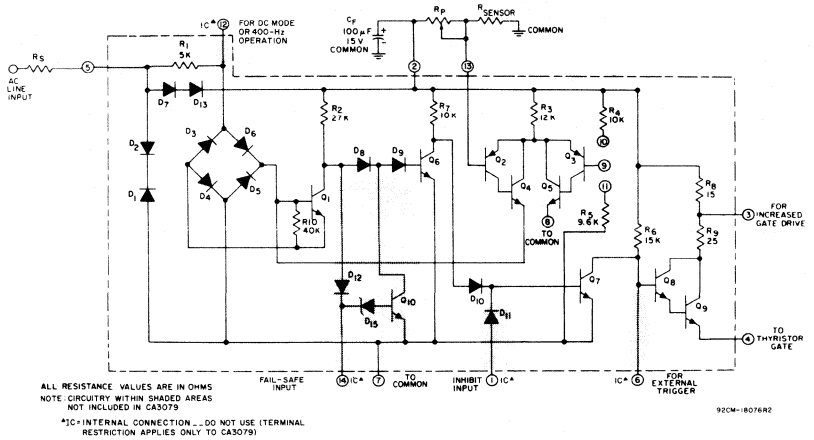


Fig. 2 - Schematic diagram of CA3059, and CA3079.

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)

All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S					
Inhibit Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6.1	6.5	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	—	6.8	—	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	—	6.4	—	V
Pulse Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6	6.4	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	—	6.7	—	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	—	6.3	—	V
At 50/60 Hz (CA3058) *See Fig. 3*	R_S = 8 kΩ, I_L = 0 T_A = −55 to +125°C	5.5	—	7.5	V

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
Gate Trigger Current, I_{GT}[4] *See Figs. 4, 5(a)*	Terms. 3 and 2 connected, V_{GT} = 1 V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}[4] With Internal Power Supply	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
With External Power Supply *See Figs. 5, 6*	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
Inhibit Input Ratio, V_9/V_2 *See Fig. 7*	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
Total Gate Pulse Duration:* For positive dv/dt, t_P 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz	C_{EXT} = 0, R_{EXT} = ∞	–	12	–	μs
For negative dv/dt, t_N 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz *See Fig. 8*	C_{EXT} = 0, R_{EXT} = ∞	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz): For positive dv/dt, t_{P1}	C_{EXT} = 0 R_{EXT} = ∞	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*		–	60	–	μs
Output Leakage Current, I_4 Inhibit Mode: *See Fig. 9*		–	0.001	10	μA
Input Bias Current, I_I CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, $\Delta V_{13}^{\neq}$ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

$^{\neq}$Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

* Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

● The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

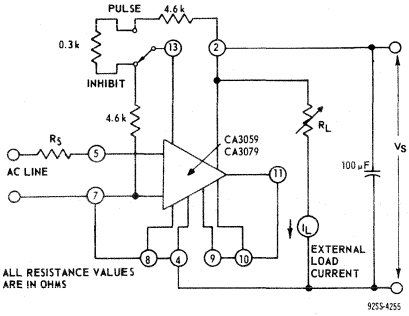


Fig. 3(a)—DC supply voltage test circuit for CA3059 and CA3079.

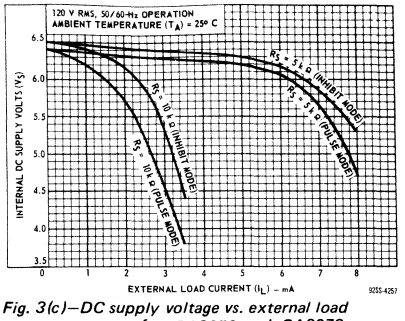


Fig. 3(c)—DC supply voltage vs. external load current for CA3059 and CA3079.

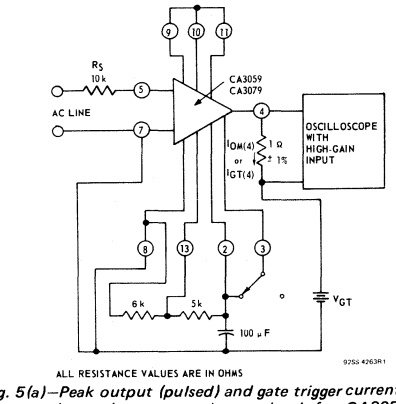


Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3059 and CA3079.

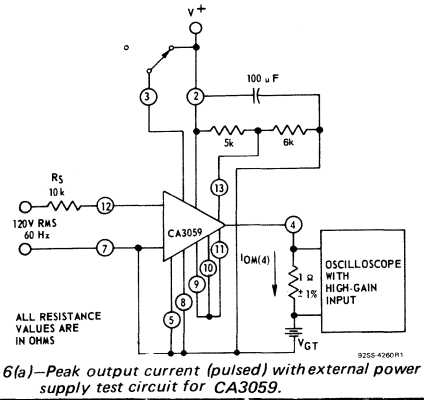


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3059.

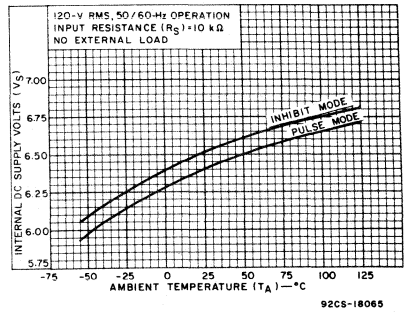


Fig. 3(b)—DC supply voltage vs. ambient temperature for CA3059 and CA3079.

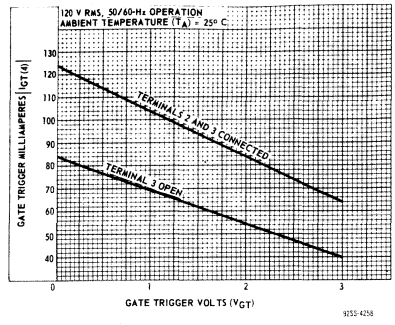


Fig. 4—Gate trigger current vs. gate trigger voltage for CA3059 and CA3079.

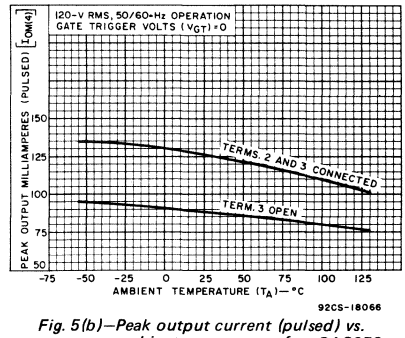


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3059 and CA3079.

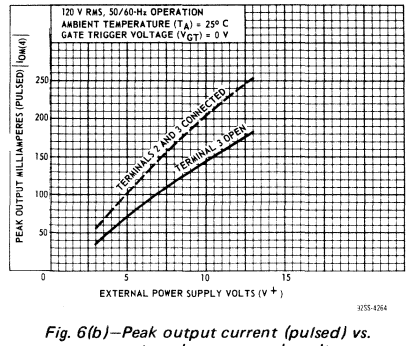


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3059.

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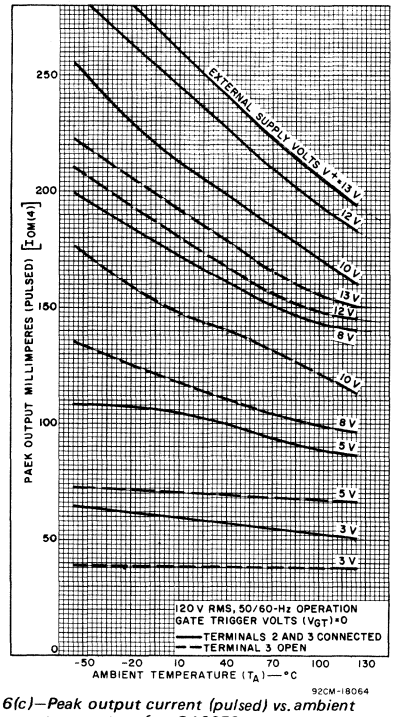


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3059.

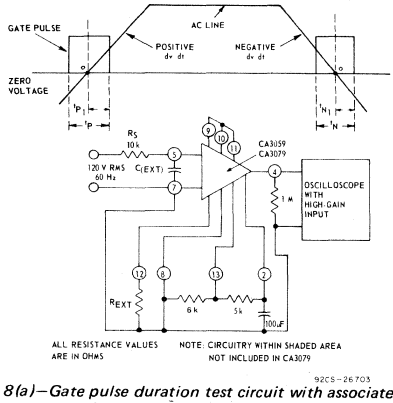


Fig. 8(a)—Gate pulse duration test circuit with associated waveform for CA3059 and CA3079.

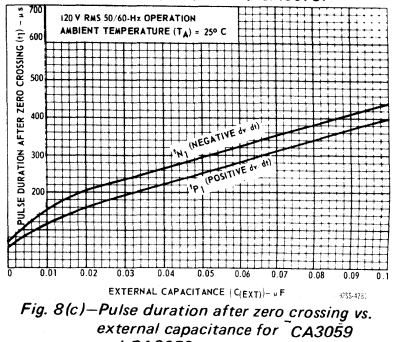


Fig. 8(c)—Pulse duration after zero crossing vs. external capacitance for CA3059 and CA3079.

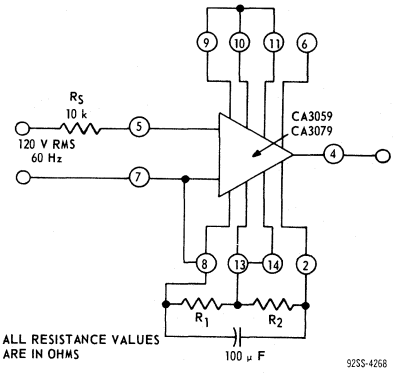


Fig. 7(a)—Input inhibit voltage ratio test circuit for CA3059 and CA3079.

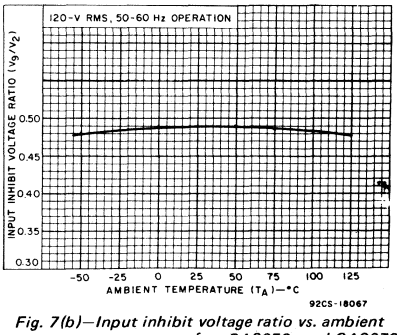


Fig. 7(b)—Input inhibit voltage ratio vs. ambient temperature for CA3059 and CA3079.

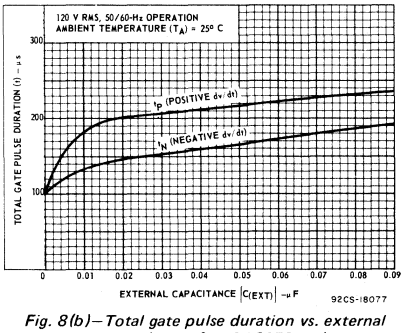


Fig. 8(b)—Total gate pulse duration vs. external capacitance for CA3059 and CA3079.

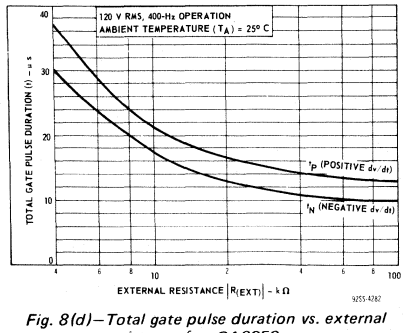


Fig. 8(d)—Total gate pulse duration vs. external resistance for CA3059.

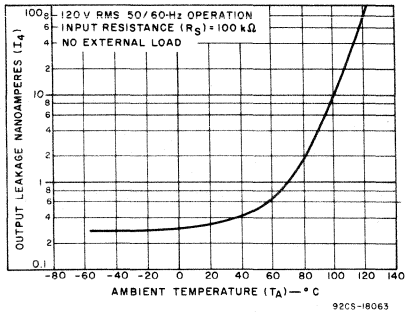


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3059 and CA3079.

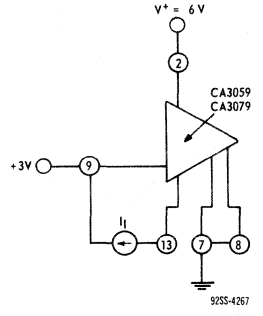
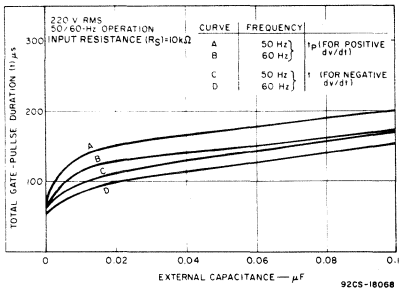
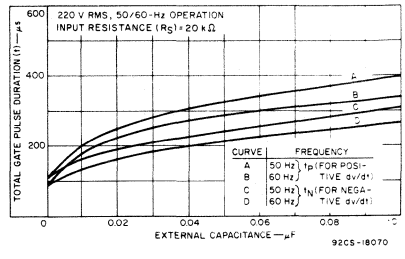


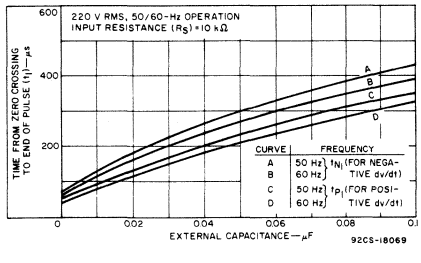
Fig. 10—Input bias current test circuit for CA3059 and CA3079.



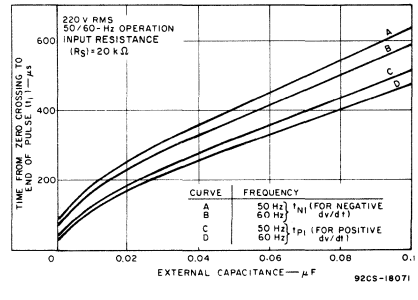
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3059 and CA3079.

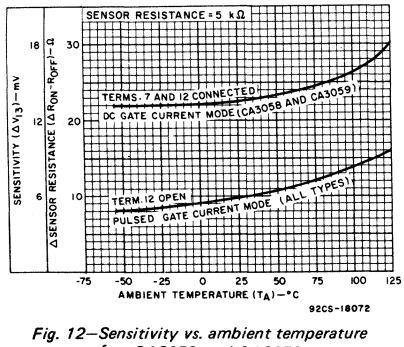


Fig. 12—Sensitivity vs. ambient temperature for CA3059 and CA3079.

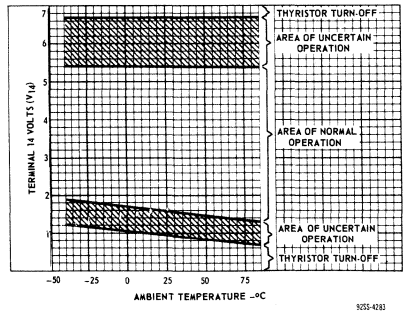


Fig. 13—Operating regions for built-in protection circuit for CA3059.

CA3059, CA3079

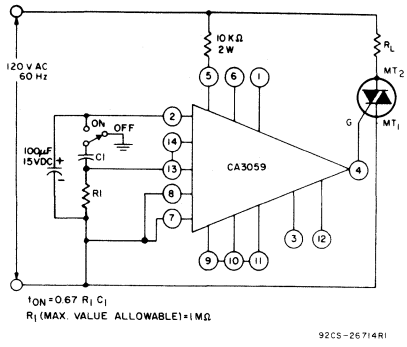


Fig. 14—Line-operated one-shot timer.

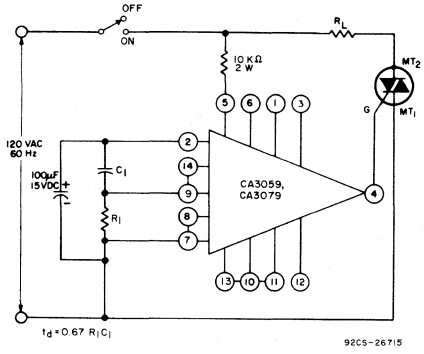


Fig. 15—Line-operated thyristor control time delay turn-on circuit.

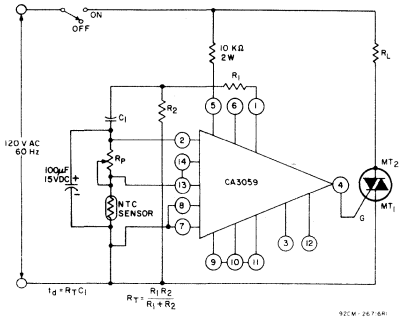


Fig. 16—On/off temperature control circuit with delayed turn-on.

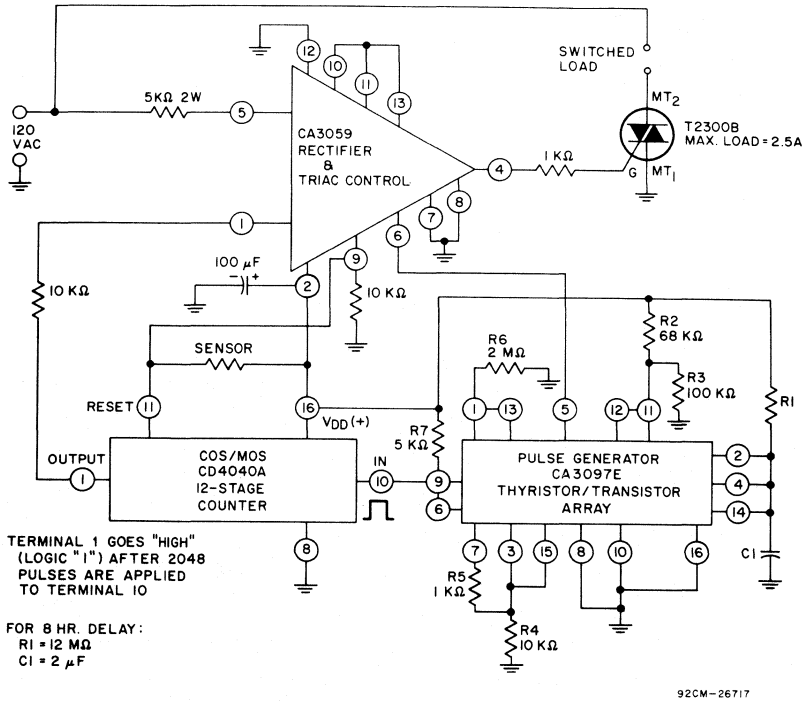


Fig. 17(a)—Line-operated IC timer for long time periods.

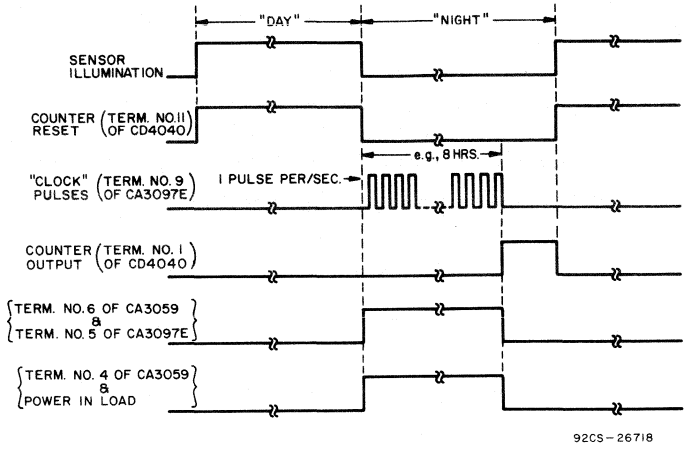


Fig. 17(b)—Timing diagram for Fig. 17(a).

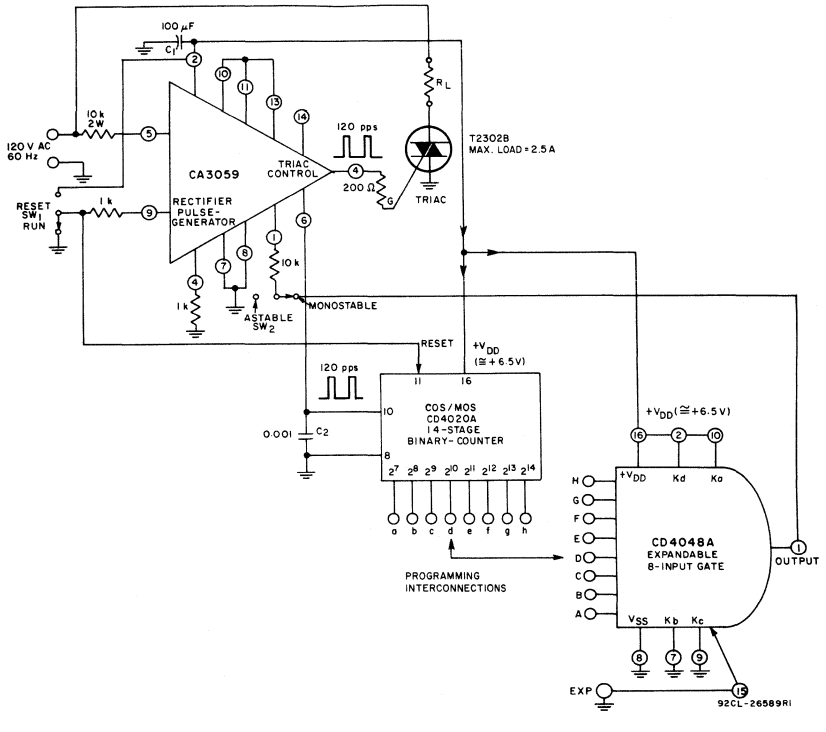


Fig. 18(a)—Programmable ultra-accurate line-operated timer. (Programmable over the range from 0.5333 seconds to 2 minutes, 16 seconds in 0.5333-second increments)

Time Periods (t = 0.5333 s)	1 t	2 t	4 t	8 t	16 t	32 t	64 t	128 t	t_o
Terminals									
CD4020A	a	b	c	d	e	f	g	h	
CD4048A	A	B	C	D	E	F	G	H	
	C	NC	NC	NC	NC	NC	NC	NC	1 t
	NC	C	NC	NC	NC	NC	NC	NC	2 t
	C	C	NC	NC	NC	NC	NC	NC	3 t
	NC	NC	C	NC	NC	NC	NC	NC	4 t
	C	NC	C	NC	NC	NC	NC	NC	5 t
	NC	C	C	NC	NC	NC	NC	NC	6 t
	C	C	C	NC	NC	NC	NC	NC	7 t
	NC	NC	NC	C	NC	NC	NC	NC	8 t
	C	NC	NC	C	NC	NC	NC	NC	9 t
	NC	C	NC	C	NC	NC	NC	NC	10 t
	C	C	NC	C	NC	NC	NC	NC	11 t
	NC	NC	C	C	NC	NC	NC	NC	12 t
	C	NC	C	C	NC	NC	NC	NC	13 t
	NC	C	C	C	NC	NC	NC	NC	14 t
	C	C	C	C	NC	NC	NC	NC	15 t
	C	C	C	C	NC	C	C	NC	111 t
	NC	NC	NC	NC	C	C	C	NC	112 t
	C	NC	NC	NC	C	C	C	NC	113 t
	C	C	C	C	C	C	C	C	255 t

Notes:

t_o = Total time delay = $n_1 t + n_2 t + \ldots n_n t$.

C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.

NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

Fig. 18(b)—"Programming" table for Fig. 18(a).

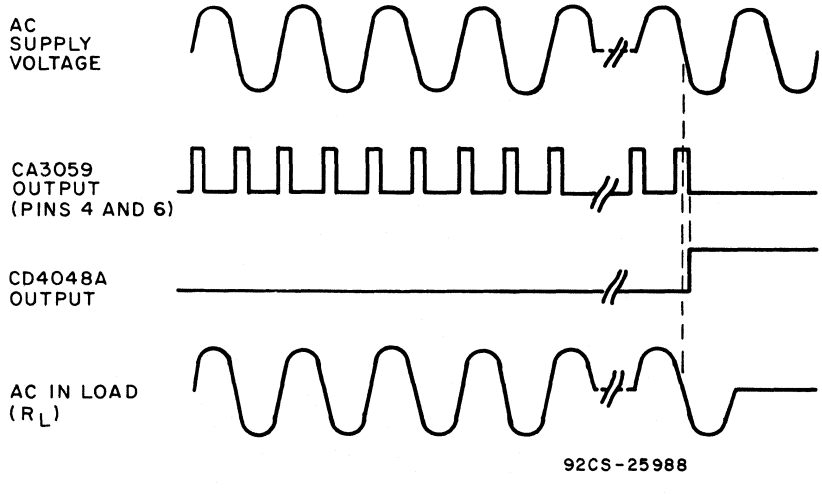


Fig. 18(c)—Timing diagram for Fig. 18(a).

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

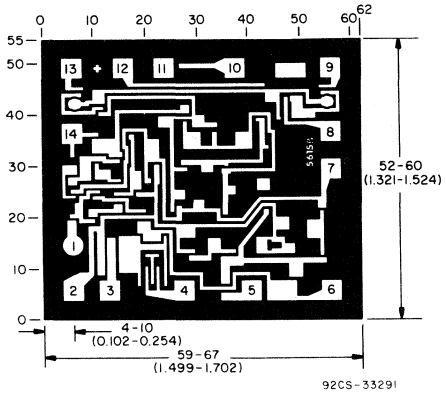
External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

For a list of RCA thyristors, see RCA Thyristor Data Bulletin, File No. 406, dated 5-75.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CA3059H.

CA3085, CA3085A, CA3085B

Positive Voltage Regulators

For Regulated Voltages from 1.7V to 46V at Currents up to 100mA

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

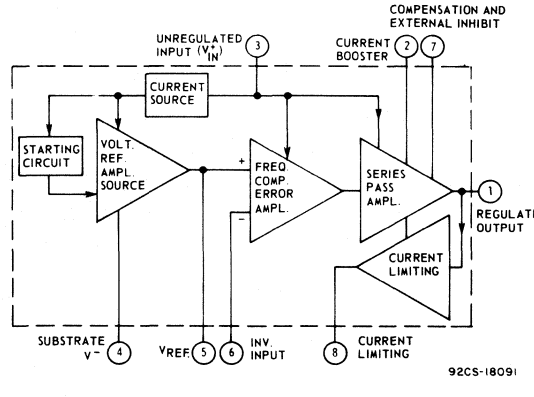


Fig. 1—Block diagram of CA3085 Series.

File Number **491**

CA3085, CA3085A, CA3085B

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK	WITH HEAT SINK (TO-5 ONLY)
up to T_A = 55°C ..... 630 mW	up to T_C = 55°C .... 1.6 W
above T_A = 55°C derate linearly @6.67 mW/°C	above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:

CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	•	•	•	•	•	+10 0
6	–	–	•	•	•	•	•	•
7	–	–	–	+3 −10	+3 −10	•	•	+‡ 0
8	–	–	–	–	+5 −1	•	•	•
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

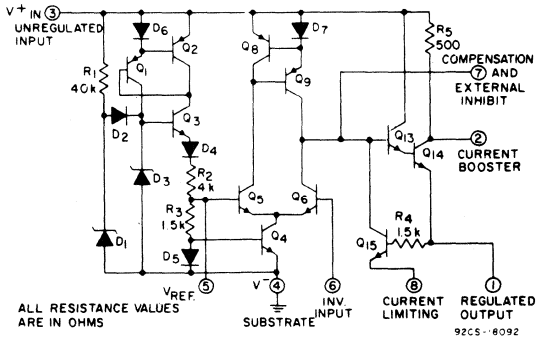


Fig.2—Schematic diagram of CA3085 Series.

CA3085, CA3085A, CA3085B

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C [Unless indicated otherwise]		LIMITS: CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNIT
Reference Voltage	V_{REF}	4	V^+_{IN} = 15V		1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	4	V^+_{IN} = 30V		–	3.3	4.5	—	–	–	–	–	–	mA
			V^+_{IN} = 40V		–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V		–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–		7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	4	V^+_{IN} = 30, 40, 50V#; R_L = 365Ω; Term. No. 6 to Gnd.		26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	4	V^+_{IN} = 30V		–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–		4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	7	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6Ω		–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0		–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0		–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1 mA, R_{SCP} = 0		–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage	V_{NOISE}	11	V^+_{IN} = 25V	C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
				C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	12	V^+_{IN} = 25V f = 1kHz	C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
				C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	12	V^+_{IN} = 25V, f = 1kHz		–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	–	I_L = 0, V_{REF} = 1.6V		–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	16	V^+_{IN} = 25V, +50mA Step		–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step		–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step		–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–			–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* R_{SCP}: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

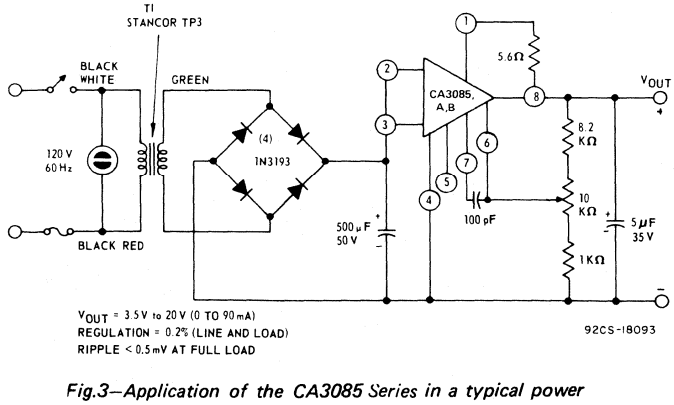
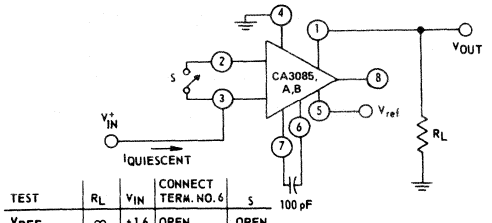


Fig.3—Application of the CA3085 Series in a typical power supply.

CA3085, CA3085A, CA3085B

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
$V_{REF.}$	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10k	+30	TERM. NO. 1	OPEN

Fig.4—Test circuit for V_{REF}, $I_{quiescent}$, V_{OUT}(max.), V_{OUT}(min.).

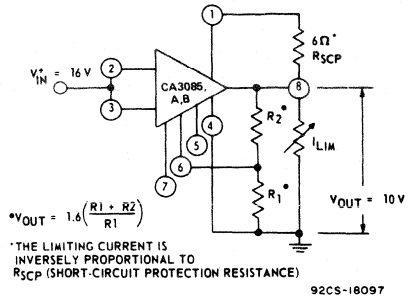


Fig.7—Test circuit for limiting current

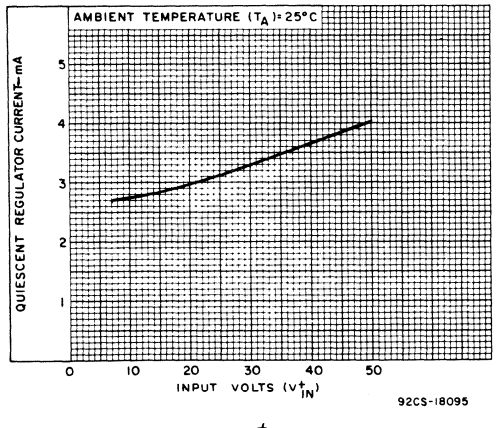


Fig.5—$I_{quiescent}$ vs. V^+_{IN}.

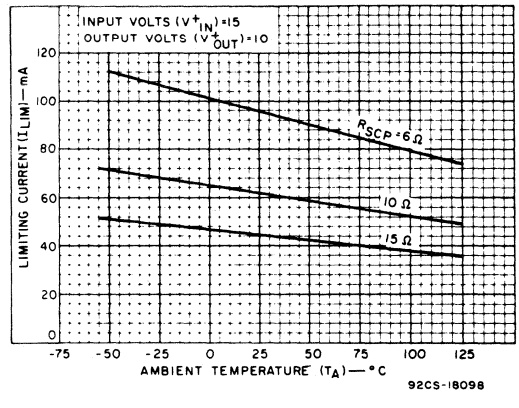


Fig.8—I_{LIM} vs. T_A.

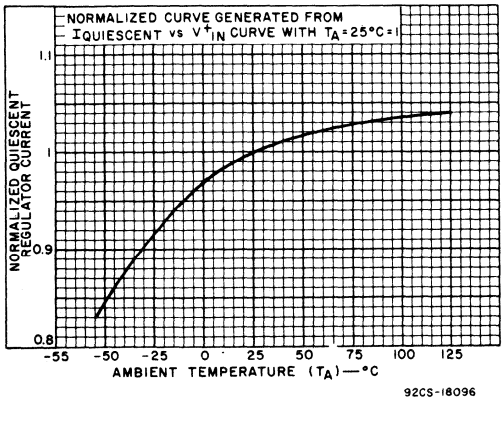


Fig.6—Normalized $I_{quiescent}$ vs. T_A.

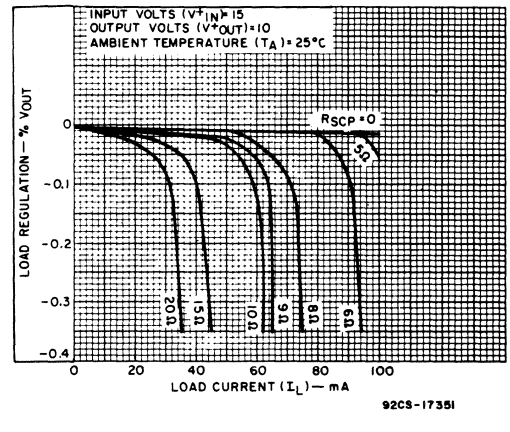


Fig.9—Load regulation characteristics.

CA3085, CA3085A, CA3085B

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

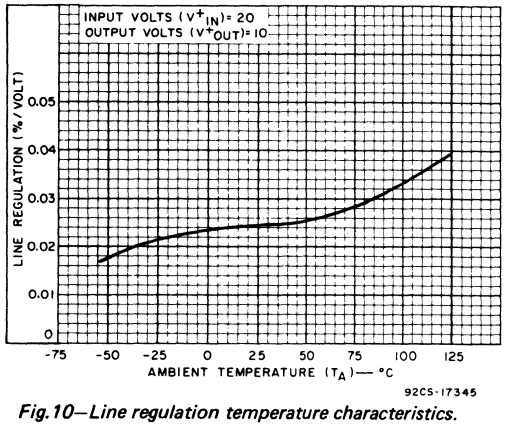


Fig.10—Line regulation temperature characteristics.

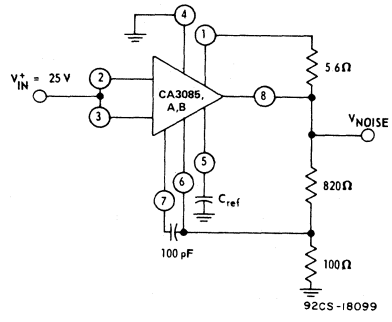


Fig.11—Test circuit for noise voltage.

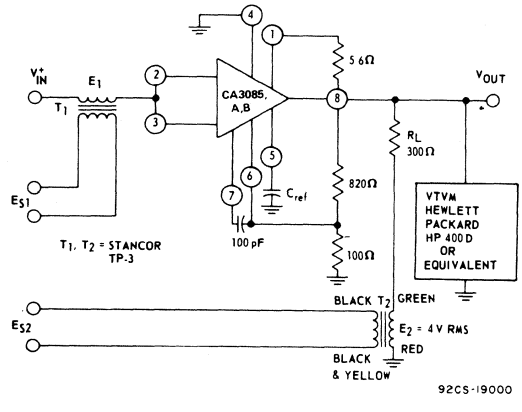


Fig.12—Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection — I

Conditions:

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection — II

Conditions:

1. Repeat Ripple Rejection I with C_{REF} = 2 μF

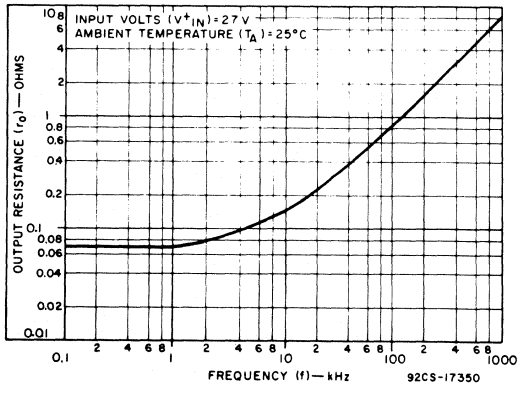


Fig.13—r_o vs. f.

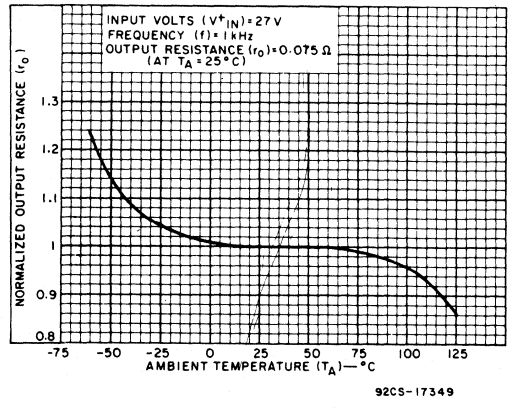


Fig.14—Normalized r_o vs. T_A.

CA3085, CA3085A, CA3085B

TEST CIRCUIT AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

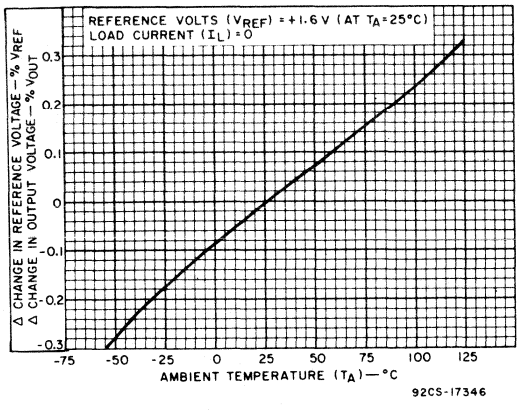


Fig.15—Temperature coefficient of V_{REF} and V_{OUT}.

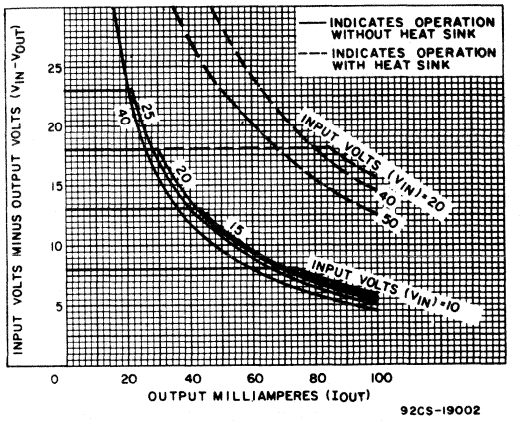


Fig.17—Dissipation limitation (V_{IN}—V_{OUT} vs. I_{OUT}).

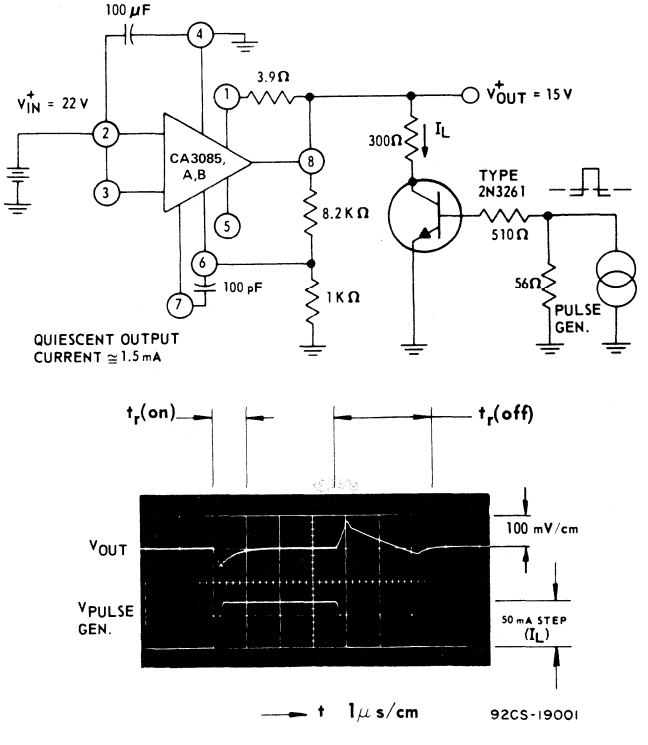


Fig.16—Turn-on and turn-off recovery time test circuit with associated waveforms.

CA3085, CA3085A, CA3085B

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

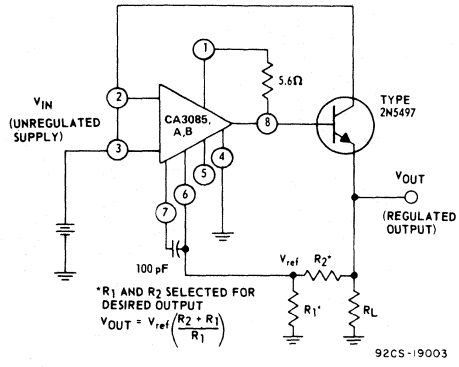


Fig. 18—Typical high-current voltage regulator circuit.

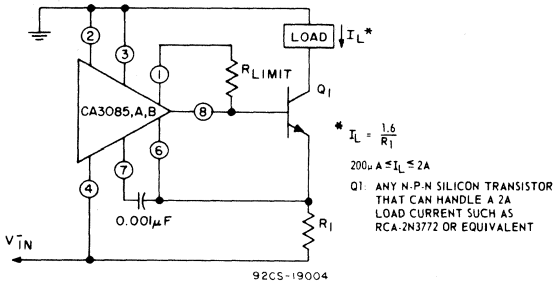


Fig. 19—Typical current regulator circuit.

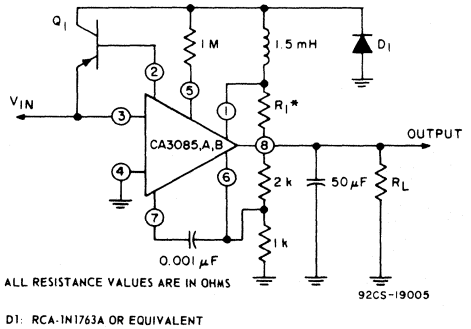


Fig. 20—Typical switching regulator circuit.

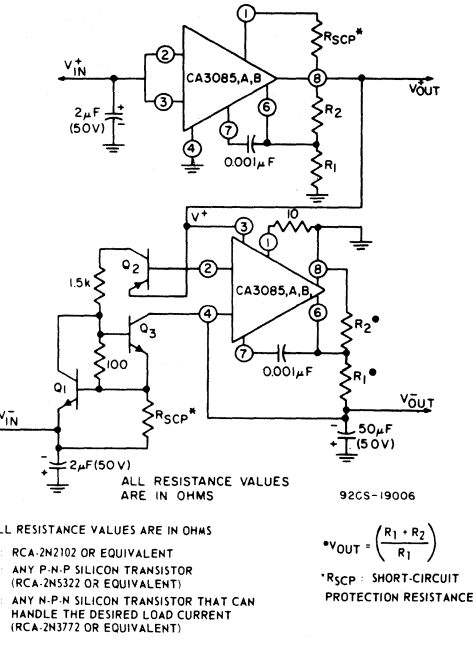


Fig. 21—Combination positive and negative voltage regulator circuit.

CA3169

Solenoid and Motor Driver (1/2 H Driver)

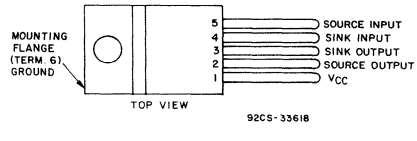
Features:
- *Chip encapsulated in a 5-lead plastic TO-220-style package (VERSA-VI)*
- *Output short-circuit protection*
- *Thermal overload protection*
- *Solenoid inductive "kick" protection with internal-clamp diodes*
- *Output sink and source capacity of 600-mA minimum overtemperature*
- *Horizontal and vertical mounting packages available*
- *Separate sink circuit and source circuit, each individually controlled*
- *Inputs can be driven by TTL logic levels and CMOS logic levels*
- *Low V_{CE}(sat)*

The RCA-CA3169 is a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCR's, and triacs are some of the solid-state devices that can be controlled by the CA3169. This device can also control relays, solenoids (latching or non-latching), motors (DC - forward and reverse) and DC stepping motors.

The CA3169 contains a separate source-driver circuit with internal current-limiting protection and a separate sink-driver circuit. The sink driver contains an energy-absorbing diode to protect the device against any inductive "kick" during state changes. The CA3169 is protected against overvoltage conditions on the output drivers and overtemperature conditions (thermal-shutdown protection).

The input operating levels are TTL compatible. The source and sink outputs are in their off condition (non-conducting) when their respective inputs are in a HI state, or open-circuited. The outputs are in their on state (conducting) when their respective inputs are LO. The VERSA-VI package is available with two lead configurations. The CA3169 has a vertical-mount lead form, and the CA3169M has a horizontal-mount lead form.

Applications:
- *Latching solenoid driver (single and multiple)*
- *Non-latching solenoid driver*
- *Relay driver*
- *Lamp controller*
- *Lamp driver*
- *Motor controller (forward and reverse)*
- *Stepper motor controller*
- *On-off logic controllers (TTL logic)*
- *Intermediate power driver*
- *Triac, SCR, and transistor drivers*



TERMINAL ASSIGNMENT

File Number **1277**

CA3169

MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY VOLTAGE (Pin 1 to GND) ..... Positive . . .41 V DC
Negative . . .1.4 V DC
SINK CURRENT ..... 1.9 A
SOURCE CURRENT ..... Controlled by Internal Current Limiting
INPUT VOLTAGE:
SINK INPUT (Pin 4 to GND) ..... 17 V
SOURCE INPUT (Pin 5 to GND) ..... 17 V
MAXIMUM FORWARD CURRENT—Diode D1 ..... 2.5 A
MAXIMUM FORWARD CURRENT—Diode D2 ..... 3 A
POWER DISSIPATION, P_D at T_A=90°C ..... 15 W
THERMAL RESISTANCE, JUNCTION TO CASE ..... 4°C/W
JUNCTION TEMPERATURE ..... 150°C
OPERATING TEMPERATURE ..... -40° to +85°C
STORAGE TEMPERATURE ..... -55° to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. ..... 265°C

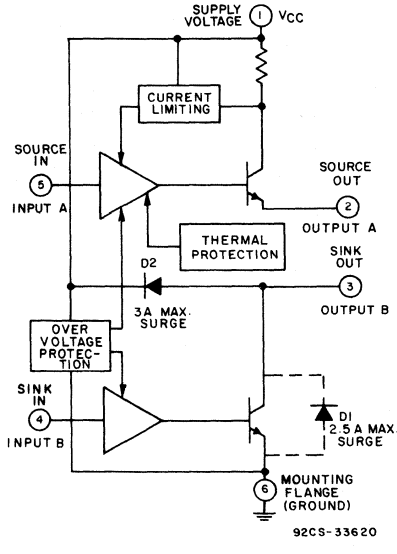
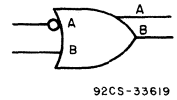


Fig. 1 - 1/2 H driver function diagram.

TRUTH TABLE FOR SOLENOID DRIVER
TTL Logic Conditions: $0 \leq V_L \leq 0.8$, $1.9 \leq V_H \leq 5.5$

INPUT A SOURCE IN	INPUT B SINK IN	OUTPUT A SOURCE OUT	OUTPUT B SINK OUT
V_L	V_L	HIGH (ON)	LOW (ON)
V_L	V_H	HIGH (ON)	(OFF)
V_H	V_L	(OFF)	LOW (ON)
V_H	V_H	(OFF)	(OFF)



ELECTRICAL CHARACTERISTICS at T_A=25°C, V_{CC}=10.5 V to 18 V
Unless otherwise specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Output Leakage Current, Pin 2 See Fig. 6	Inputs Open V_{CC}=4 V to 18 V Source and Sink Loads=20 Ω	-110	±0.5	110	μA
Output Leakage Current, Pin 3 See Fig. 6	Inputs Open V_{CC}=4 V to 18 V Source and Sink Loads=20 Ω	-110	±0.5	110	μA
Thermal Resistance, Junction to Case θ_{JC}		—	3	4	°C/W
Quiescent Current, Pin 1 See Fig. 5	Device "ON" Input Terminals Shorted, V_{CC}=14 V	—	70	100	mA
Quiescent Current, Pin 1 See Fig. 4	Device "OFF" Input Terminals Open, V_{CC}=14 V	—	17	40	mA
Thermal Shutdown Temperature	R_L=Short Circuit	128	140	162	°C
Overvoltage Shutdown-Circuit Upper Trip Point, Pin 1 Voltage See Fig. 8	R_L=20 Ω	20	25	27	V
Overvoltage Shutdown-Circuit Lower Trip Point, Pin 1 Voltage See Fig. 8	R_L=20 Ω	18	21.4	23	V
Input Logic Levels; Source Input - Pin 5, Sink Input - Pin 4					
Input Low Threshold Sink or Source V_{IL}	V_{CC}=14 V **See Note 1**	—	0.4	0.8	V
Input High Threshold Sink or Source V_{IH}	V_{CC}=14 V **See Note 2**	1.9	2.4	—	V
Input Low Current Sink or Source I_{LL}	$V_{IN} \leq$ 0.4 V	−0.9	−0.3	—	mA
Input High Current Sink or Source I_{IH}	$V_{IN} \leq$ 5.5 V	−110	−23	110	μA

NOTE 1: I_{SOURCE} or $I_{SINK} \leq$ 600 mA, $V_{OS} \leq$ 1.5 V, $V_{SINK} \leq$ 0.75 V.
NOTE 2: I_{SOURCE} or $I_{SINK} \leq$ 100 μA, V_{SOURCE} = GND, for V_{SINK} 20 Ω to V_{CC}.

CA3169

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Source Outputs					
Output Voltage, V_{OS} Pin 2 **See Note 3** See Fig. 7	Referenced to V_{CC} with I_{SOURCE}= 600 mA	—	1	1.6	V
Short-Circuit Current Limit, Pin 2 to Ground		0.65	1.11	2.6	A
Turn-On Delay to Output-On, Pin 2	C_L=100 pF, R_L=33 Ω	—	0.45	5.6	μs
Turn-Off Delay to Output-Off Pin 2	C_L=100 pF, R_L=33 Ω	—	5	55	μs
Sink Outputs					
Output Saturation Voltage V_3 **See Note 3** See Fig. 10	I_{SINK}=600 mA, $V_{IN} \leq$ 0.4 V	—	0.3	0.85	V
Output Saturation Voltage V_3 **See Note 3** See Fig. 10	I_{SINK}=1000 mA $V_{IN} \leq$ 0.4 V	—	0.8	1.65	V
Turn-On Delay to Output-On Pin 3 (T_{ON})	C_L=100 pF, R_L=33 Ω to V_{CC}	—	0.45	5.6	μs
Turn-Off Delay to Output-Off Pin 3 (T_{OFF})	C_L=100 pF, R_L=33 Ω to V_{CC}	—	0.95	25	μs

NOTE 3: Measured over temperature range of −40°C to 85°C.

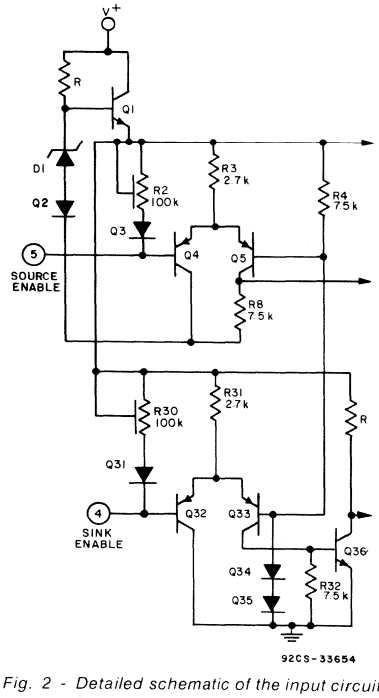


Fig. 2 - Detailed schematic of the input circuit for CA3169.

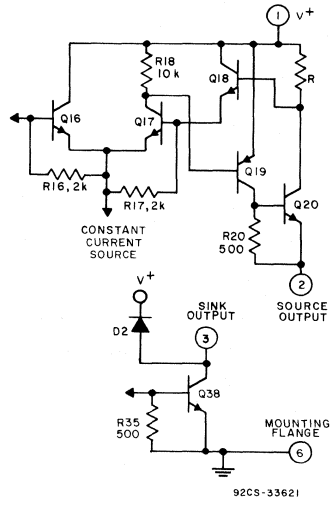


Fig. 3 - Detailed schematic of the output circuit for CA3169.

TEST CIRCUITS
(V_{CC} = V_{IN} = PIN 1 VOLTAGE)

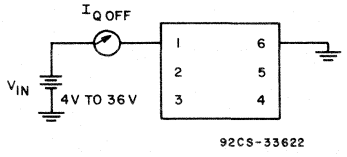


Fig. 4 - Quiescent current device "OFF"

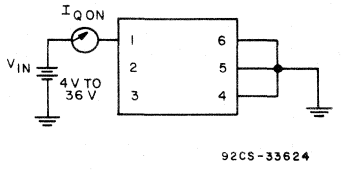


Fig. 5 - Quiescent current device "ON".

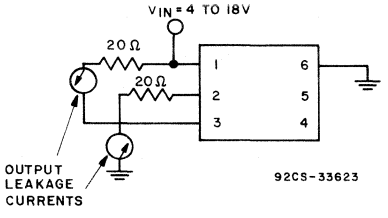


Fig. 6 - Output leakage currents.

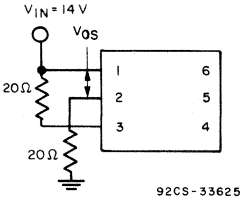
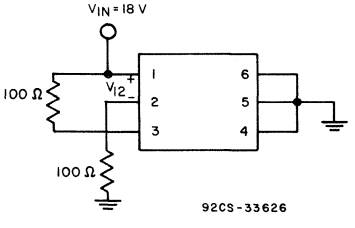


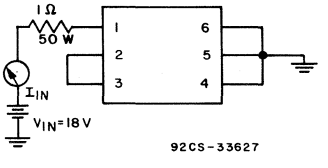
Fig. 7 - Output source voltage (referenced to V_{CC}).



PROCEDURE

1. Measure V_{12}.
2. Increase V_{CC} until $V_{12} \geq 2$ V.
3. Measure V_{CC}; this voltage is the high trip point. Pin 2 should be off; i.e., pin 3 should be high.
4. Observe and measure the voltage at pin 3.
5. Decrease V_{CC} until pin 3 switches, i.e., ≤ 18 V. The supply voltage will be the low trip point voltage.

Fig. 8 - Overvoltage protection.



When V_{CC} is turned on, I_{IN} should be equal to or greater than 1 A. Thermal shutdown will operate properly if the input current drops below 0.5 A (0.3 A typ.) in 10 to 15 seconds. Cover the unit during this test in the event that the thermal shutdown is not operating properly.

Fig. 9 - Thermal shutdown.

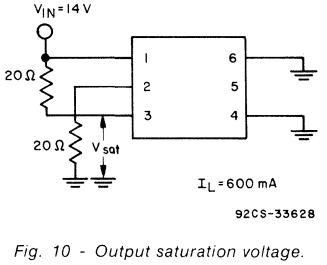
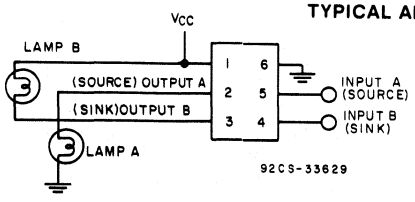


Fig. 10 - Output saturation voltage.

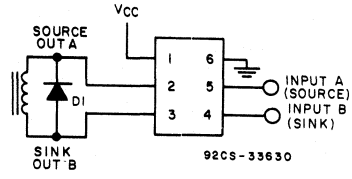
CA3169

TYPICAL APPLICATIONS



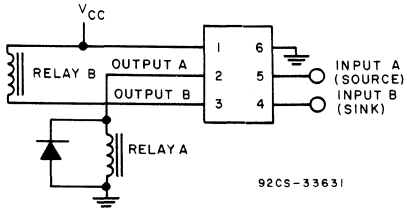
When input A goes low, lamp A will light. When input B goes low, lamp B will light.

Fig. 11 - Lamp driver.



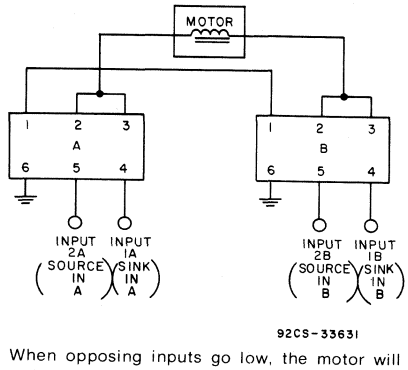
Input A and input B must both be low for the solenoid to switch.

Fig. 12 - Non-latching solenoid.



Relay A will close when input A goes low. Relay B will close when input B goes low. Both relays will close when both inputs go low.

Fig. 13 - Relay driver.



When opposing inputs go low, the motor will switch direction; if source input A and sink input B both go low, current will flow from A to B. If source input B and sink input A both go low, current will flow from B to A.

Fig. 14 - Motor driver or latching solenoid driver.

Advanced Information/
Preliminary Data

CA3177

Operational Amplifier/ Comparator

With Shutdown Control and Isolated Transistor

FEATURES:
- *Operates from single power supply*
- *High output current (50 mA max.)*
- *Output sink current or drive current capability*
- *Output disable control*

The RCA-CA3177E* is a multiple-control amplifier/ comparator monolithic integrated circuit intended for use in general purpose applications requiring comparator functions with logic override switching and control. An op-amp with differential inputs drives an output transistor with high current capability. An isolated transistor is also available for optional use.

The CA3177E is supplied in the 8-lead dual-in-line plastic (Mini-DIP) package.

*Formerly RCA Dev. Type No. TA10387.

Applications:
- *Comparator*
- *Switching and gating control*
- *Power switch/amplifier*
- *Switching regulator*
- *Pulse width modulator*
- *TV horizontal drive amplifier*

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
V1, V5, V5 ..... +15 V
INPUT CURRENT:
13, 14, 17, 18 ..... ± 1 mA
OUTPUT CURRENT:
I1 ..... 50 mA
I6 ..... 10 mA
DEVICE DISSIPATION, (Including Q14):
At $T_A \leq 25°C$ ..... 625 mW
At $T_A > 25°C$ ..... Derate linearly 5 mW/°C
Q14 DISSIPATION:
At $T_A \leq 25°C$ ..... 150 mW
At $T_A > 25°C$ ..... Derate linearly 1.2 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +70°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... 265°C

File Number **1235**

CA3177

ELECTRICAL CHARACTERISTICS *at T_A = 25°C, V+ (V5) = 15 V, except as noted*

CHARACTERISTIC	CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Operational Amplifier				
Input Offset Voltage, V_{IO}		—	100	mV
Input Bias Current, I_{IB}		—	15	μA
Common-Mode Input Voltage Range, V_{ICR}		2	12	V
Amplifier Supply Current, I5		3	10	mA
Q14 Amplifier				
DC Forward-Current Transfer Ratio, h_{FE}	V_{CE} = 10 V, I_6 = 0.1 mA V_{CE} = 10 V, I_6 = 2 mA	45 45	— —	
Collector-to-Emitter Saturation Voltage, V_{CE}(sat)	I_7 = 0.2 mA, I_6 = 2 mA	—	0.6	V
Q1 Amplifier				
Collector-to-Emitter Saturation Voltage, V_{CE}(sat)	I_8 = 0.15 mA, I_1 = 30 mA	—	0.4	V

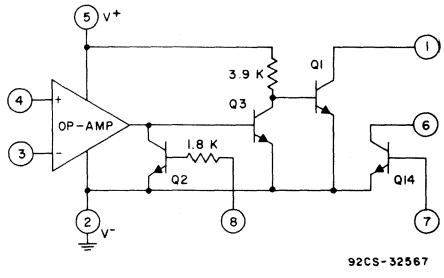
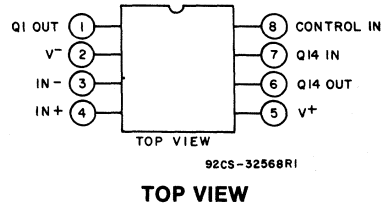


Fig. 1—Functional diagram for CA3177E.



TOP VIEW
TERMINAL ASSIGNMENT

Advance Information/
Preliminary Data

CA3219A

Quad-Gated Inverting Power Driver

For Interfacing Low-Level Logic to High Current Loads

Features:

- *Driven outputs capable of switching 600 mA load currents without spurious changes in output state*
- *Inputs compatible with TTL or 5-volt CMOS logic*
- *Suitable for resistive or inductive loads*
- *Power-Frame construction for good heat dissipation*

The RCA CA3219AE• quad power NAND driver contains four NAND-gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, ac and dc motors, heaters, incandescent displays, and vacuum fluorescent displays.

Diodes in the outputs protect the IC against voltage transients due to switching inductive loads.

To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die substrate and to the ground bond pads. In free air, junction-to-air thermal resistance (RθJA) is 50°C/W (typical).

This coefficient can be lowered to 40°C/W (typical) by suitable design of the PC board to which the CA3219E is soldered.

The CA3219AE is supplied in the 16-lead dual-in-line plastic package (E suffix).

•Formerly RCA Dev. Type No. TA11536

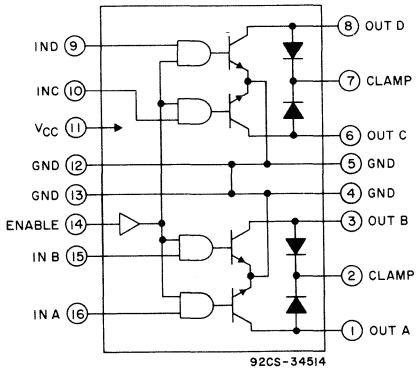


Fig. 1 - Block diagram for the CA3219AE.

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

File Number **1636**

CA3219A

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

Logic Supply Voltage (V_{CC}) ..... 7 V
Logic Input Voltage (V_{IN}) ..... 15 V
Output Voltage (V_{CEX}) ..... 50 V_{DC}
Output Sustaining Voltage (V_{CC})sus ..... 35 V_{DC}
Output Current (I_O) ..... 1 ADC
Power Dissipation (P_D)
  Up to 55° C ..... 1.5 W
  Above 55° C ..... Derate Linearly at 16.6 mW/° C
  Up to 90° C with heat sink ..... Derate Linearly at 25 mW/° C
Ambient Temperature Range:
  Operating ..... -40 to +85° C
  Storage ..... -55 to +150° C
Maximum Junction Temperature ($T\theta_J$) ..... +150° C
Maximum Thermal Resistance
  Junction-to-Air (θ_{J-A}) ..... 60° C/W
  Junction-to-Case (θ_{J-C})
    to pins 4, 5, 12, 13 at seat ..... 12° C/W
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

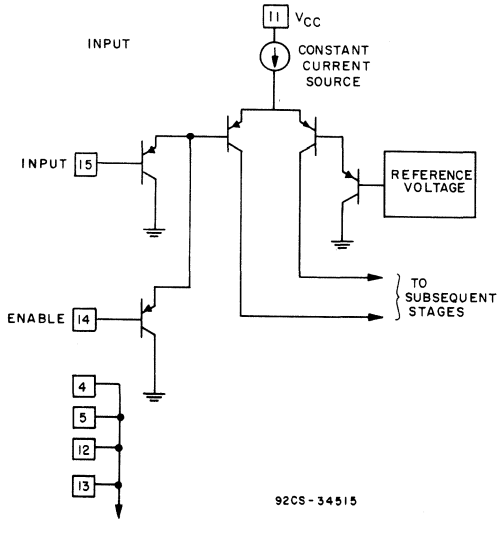


Fig. 2 - Schematic of one input section.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{CC} = 5 V

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Output Leakage Current (I_{CEX}) V_{CE} = 50 V V_{IN} = 0.8 V	—	100	μA
Output Sustaining Voltage $V_{CE(sus)}$ I_C = 100 mA V_{IN} = 0.8 V	25	—	V
Collector Emitter Saturation Voltage $V_{CE(sat)}$			
I_C = 100 mA V_{IN} = 2.4 V	—	0.3	V
I_C = 400 mA V_{IN} = 2.4 V	—	0.5	V
I_C = 600 mA V_{IN} = 2.4 V	—	0.7	V
Input Low Voltage V_{IL}	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8 V	—	+10	μA
Input High Voltage V_{IH} I_C = 600 mA	2	—	V
Input High Current I_{IH} I_C = 700 mA; V_{IN} = 5.5 V	—	40	μA
Supply Current - All Outputs ON, I_{CC}(ON) I_C = 700 mA; V_{CC} = V_{IH} = 5.5 V	—	80	mA
Supply Current - All Outputs OFF, I_{CC}(OFF)	—	5	mA
Clamp Diode Leakage Current I_R V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage V_F			
IF = 1 A	—	1.5	V
IF = 1.5 A	—	2	V
Turn-On Delay t_{PHL} Turn-Off Delay t_{PLH}		10	μs

CA3242

Advance Information/
Preliminary Data

Quad-Gated Inverting Power Driver

For Interfacing Low-Level Logic to High Current Loads

Features:

- *Driven outputs capable of switching 600 mA load currents without spurious changes in output state*
- *Inputs compatible with TTL or 5-volt CMOS logic*
- *Suitable for resistive or inductive loads*
- *Output overload protection*
- *Power-Frame construction for good heat dissipation*

The RCA CA3242E• quad-qated non-inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Output overload protection is provided when the load current (approximately 1.2A) causes the output V_{CESAT} to rise above 1.3V for more than a built-in time delay, nominally 35μsec. That output will be shut-down by its protection network without affecting the other outputs. The corresponding Input or Enable must be toggled to reset the output protection circuit.

•Formerly RCA Dev. Type No. TA11491

Diodes in the outputs protect the IC against voltage transients due to switching inductive loads.

To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance (θJ-A) is 50° C/W (typical). This coefficient can be lowered to 40° C/W (typical) by suitable design of the PC board to which the CA3242E is soldered.

The CA3242 is supplied in a 16-lead dual-in-line plastic package (E suffix).

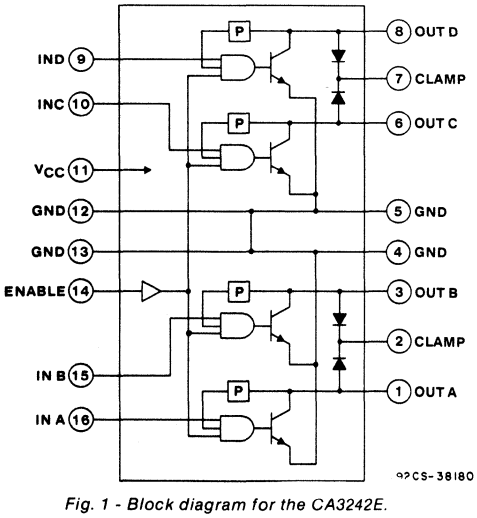


Fig. 1 - Block diagram for the CA3242E.

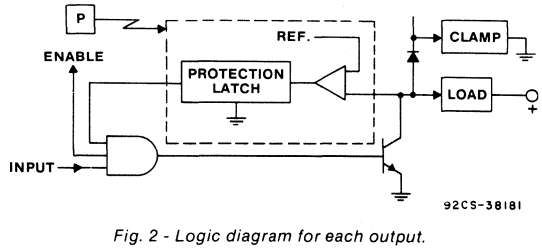


Fig. 2 - Logic diagram for each output.

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

File Number **1561**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

LOGIC SUPPLY VOLTAGE (V_{CC}) ..... 7 V
LOGIC INPUT VOLTAGE (V_{IN}) ..... 15 V
OUTPUT VOLTAGE (V_{CEX}) ..... 50 V_{DC}
OUTPUT SUSTAINING VOLTAGE (V_{CC})sus ..... 35 V_{DC}
OUTPUT CURRENT (I_O) ..... 1 ADC
POWER DISSIPATION (P_D)
Up to 55° C ..... 1.5 W
Above 55° C ..... Derate linearly at 16.6 mW/° C
Up to 90° C with heat sink ..... Derate linearly at 25 mW/° C
AMBIENT TEMPERATURE RANGE:
Operating ..... -40 to +85° C
Storage ..... -55 to +150° C
MAXIMUM JUNCTION TEMPERATURE ($T\theta_J$) ..... +150° C
MAXIMUM THERMAL RESISTANCE
Junction-to-Air (θ_{J-A}) ..... 60° C/W
Junction-to-Case (θ_{J-C}) to pins 4, 5, 12, 13 at seat ..... 12° C/W
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

ELECTRICAL CHARACTERISTICS at T_A = -40 to + 85° C, V_{CC} = 5 V

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Output Leakage Current (I_{CEX}) V_{CE} = 50 V V_{IN} = 2.4 V	—	100	μA
Output Sustaining Voltage $V_{CE(sus)}$ I_C = 100 mA V_{IN} = 2.4 V	25	—	V
Collector Emitter Saturation Voltage $V_{CE(sat)}$ I_C = 100 mA V_{IN} = 0.8 V	—	0.3	V
I_C = 400 mA V_{IN} = 0.8 V	—	0.6	V
I_C = 600 mA V_{IN} = 0.8 V	—	0.8	V
Input Low Voltage V_{IL}	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8 V	—	±10	μA
Input High Voltage V_{IH} I_C = 600 mA	2	—	V
Input High Current I_{IH} I_C = 700 mA; V_{IN} = 4.5 V	—	10	μA
Supply Current - All Outputs ON, $I_{CC(ON)}$ I_C = 700 mA; V_{CC} = V_{IH} = 5.5 V	—	80	mA
Supply Current - All Outputs OFF, $I_{CC(OFF)}$	—	5	mA
Clamp Diode Leakage Current I_R V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage V_F IF = 1 A	—	1.8	V
IF = 1.5 A	—	2.5	V
Turn-On Delay t_{PHL} Turn-Off Delay t_{PLH}	—	20	μs

CA3242

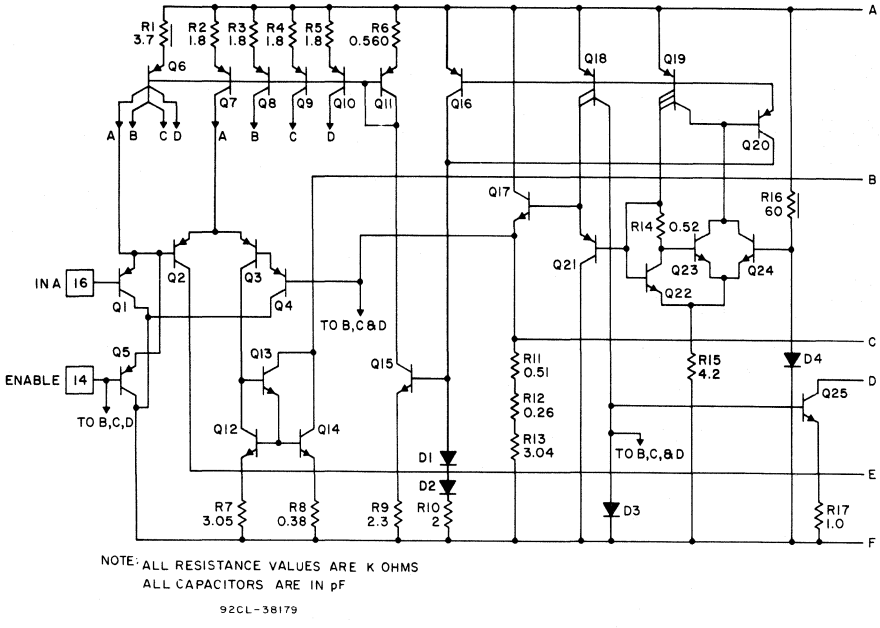


Fig. 3 - Schematic diagram of the CA3242E (Switch Section-A).
(Continued on next page).

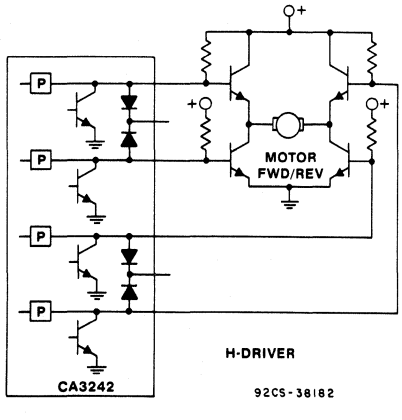


Fig. 4 - Typical applications for the RCA CA3242 Quad Driver.

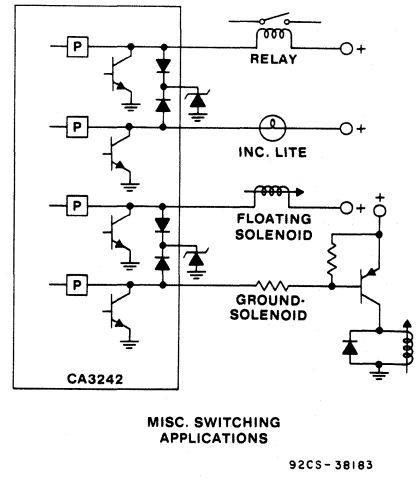


Fig. 5 - Typical applications for the RCA CA3242 Quad Driver.

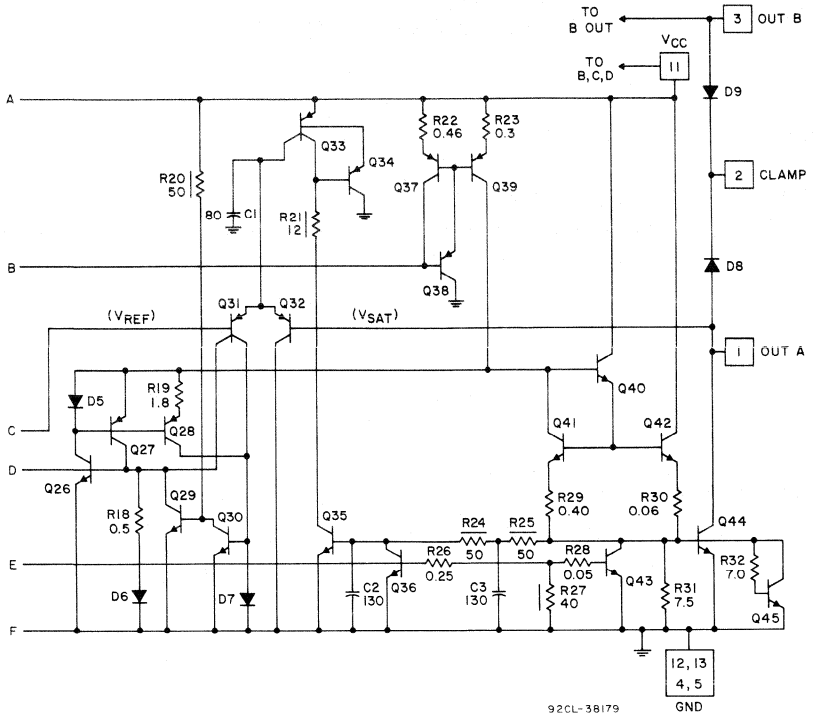


Fig. 3 - Schematic diagram of the CA3242E (Switch Section-A). (Continued from previous page).

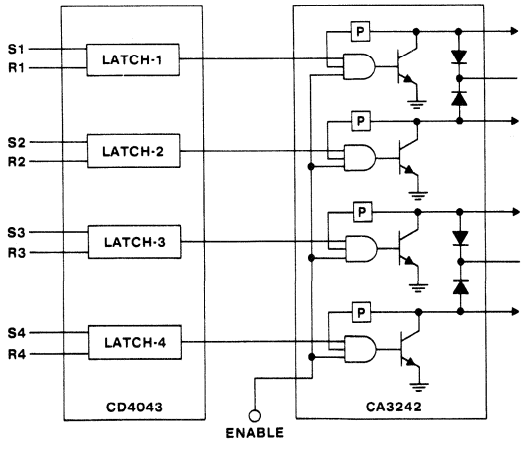


Fig. 6 - Typical applications for the RCA CA3242 Quad Driver.

CA3252

Advance Information/
Preliminary Data

Quad-Gated Non-Inverting Power Driver

For Interfacing Low-Level Logic
to High Current Loads

Features:

- *Driven outputs capable of switching 600 mA load currents without spurious changes in output state*
- *Inputs compatible with TTL or 5-volt CMOS logic*
- *Suitable for resistive or inductive loads*

The RCA CA3252E• quad-gated non-inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

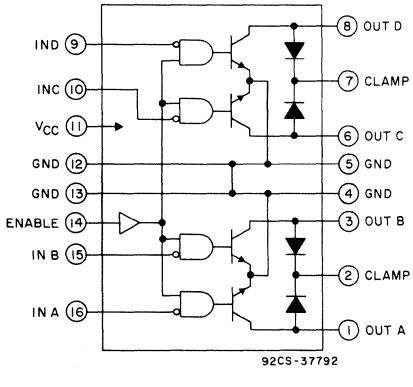
Diodes in the outputs protect the IC against voltage transients due to switching inductive loads.

•Formerly RCA Dev. Type No. TA11489.

To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance (θJ-A) is 50°C/W* (typical).

The CA3252E is supplied in the 16-lead dual-in-line plastic package with special construction for improved dissipation capability.

*This coefficient can be lowered to 40°C/W (typical) by suitable design of the PC board to which the CA3252E is soldered.



92CS-37792

TRUTH TABLE

ENABLE	IN	OUT
H	L	L
H	H	H
L	X	H

File Number **1542**

CA3252

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

LOGIC SUPPLY VOLTAGE (V_{CC}) ..... 7 V
LOGIC INPUT VOLTAGE (V_{IN}) ..... 15 V
OUTPUT VOLTAGE (V_{CEX}) ..... 50 V_{DC}
OUTPUT SUSTAINING VOLTAGE (V_{CC})sus ..... 35 V_{DC}
OUTPUT CURRENT (I_O) ..... 1 ADC
POWER DISSIPATION (P_D)
Up to 55° C ..... 1.5 W
Above 55° C ..... Derate linearly at 16.6 mW/° C
Up to 90° C with heat sink ..... Derate linearly at 25 mW/° C
AMBIENT TEMPERATURE RANGE:
Operating ..... -40 to +85° C
Storage ..... -55 to +150° C
MAXIMUM JUNCTION TEMPERATURE ($T_{\theta J}$) ..... +150° C
MAXIMUM THERMAL RESISTANCE
Junction-to-Air (θ_{J-A}) ..... 60° C/W
Junction-to-Case (θ_{J-C})
to pins 4, 5, 12, 13 at seat ..... 12° C/W

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{CC} = 5 V

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Output Leakage Current (I_{CEX}) V_{CE} = 50 V V_{IN} = 2.4 V	—	100	μA
Output Sustaining Voltage $V_{CE(sus)}$ I_C = 100 mA V_{IN} = 2.4 V	25	—	V
Collector Emitter Saturation Voltage $V_{CE(sat)}$ I_C = 100 mA V_{IN} = 0.8 V	—	0.3	V
I_C = 400 mA V_{IN} = 0.8 V	—	0.5	V
I_C = 600 mA V_{IN} = 0.8 V	—	0.7	V
Input Low Voltage V_{IL}	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8 V	—	±10	μA
Input High Voltage V_{IH} I_C = 600 mA	2	—	V
Input High Current I_{IH} I_C = 700 mA; V_{IN} = 4.5 V	—	40	μA
Supply Current — All Outputs ON, $I_{CC(ON)}$ I_C = 700 mA; V_{CC} = V_{IH} = 5.5 V	—	80	mA
Supply Current — All Outputs OFF, $I_{CC(OFF)}$	—	5	mA
Clamp Diode Leakage Current I_R V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage V_F IF = 1 A	—	1.5	V
IF = 1.5 A	—	2	V
Turn-On Delay t_{PHL} Turn-Off Delay t_{PLH}		30	μs

CA3252

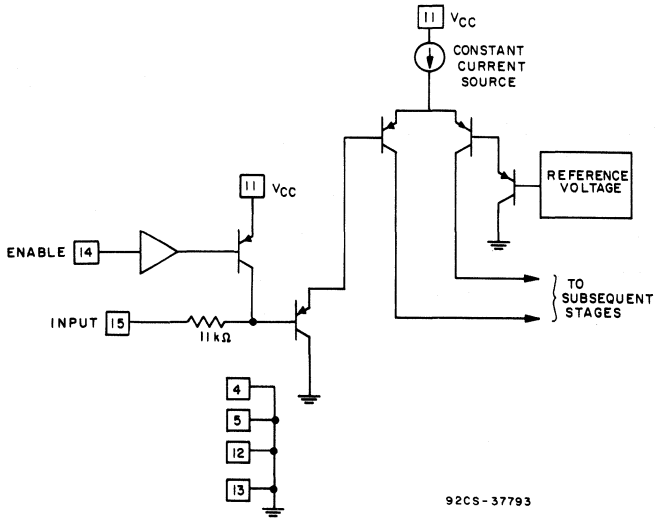


Fig. 2 - Schematic of one input section.

Special Function Circuits

Special Function Circuits — Technical Data

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

CA3091

Four-Quadrant Multiplier

Features:

- "Accuracy": ±4% (max.)
- "Linearity": 3.0% (max.)
- Feedthrough: 9 mV p-p (typ.)
- 3-db bandwidth: 4.4 MHz
- Low power operation capability: ±6.0 V, 4 mW drain
- Low power-supply sensitivity: 36 mV/V typ.
- Smooth overload characteristics — no foldback if full-scale input signal is exceeded
- Negligible warm-up drift
- Broadband operation capability (flat to 1 MHz) — both inputs have similar characteristics for reduced high-frequency phase shift between the inputs
- Low-level linearity correction circuitry minimizes low-level feedthrough for improved small-signal accuracy
- All multiplication is performed with wideband circuitry — this permits two signals of frequencies much higher than the -3 db frequency of the multiplier to produce a difference frequency that is within the multiplier's bandwidth
- High immunity to parasitic oscillation
- Essentially free from excess peaking — provides improved frequency response
- Requires no level shifting at the output — current-source operation at the output permits output signal to be referenced to ground or other levels within the output voltage swing capabilities of the multiplier
- Internal bias regulator

RCA-CA3091D*, a monolithic silicon integrated circuit, is a four-quadrant multiplier that provides an output voltage that is the product of two input (x and y) voltages.

This device functions as a multiplier, divider, squarer, square rooter, and power-series approximator. In addition, this device is useful in applications such as ideal full-wave rectifiers, automatic level controllers, RMS converters, frequency discriminators, and voltage-controlled filters and oscillators.

The CA3091D comprises five basic circuits (See Fig. 1), including: a multiplier block, two linearity compensators, a current converter, a current source for biasing, and a regulator (reference voltage). A brief description of the operation, functions and typical applications is given in the section "Operating Considerations". In addition there is a separate section on "Symbols, Terms, and Definitions" that defines the terms and symbols used throughout the data bulletin.

The CA3091D is supplied in 14-lead dual-in-line ceramic package and operates over the full military temperature range of -55°C to +125°C.

* Formerly Developmental Type TA5855A.

Applications:

- Multiplier ■ Divider ■ Squarer ■ Square Rooter
- Power-series approximator
- Full-wave rectifier
- Automatic level controller
- RMS converter
- Frequency discriminator
- Voltage-controlled filters and oscillators

File Number **534**

CA3091

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DC Supply Voltages:		
Between Terms. 12 and 1	+18	V
Between Terms. 4 and 1	−18	V
DC Supply Currents:		
At Term. 12 with DC Supply Voltage = +15 V	4	mA
At Term. 4 with DC Supply Voltage = −15 V	16	mA
Bias Current (At Term. 3)	1	mA
* Input Current	±1	mA
Output Short-Circuit Duration		No limitation
Voltage Reference Current	10	mA
Linearity Correction Currents:		
At Terminals 7 and 8	10	mA
Device Dissipation (Up to 125°C)	200	mW
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (during soldering):		
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265	°C

* External resistance is required to limit the current to the indicated ±1 mA value.

ELECTRICAL CHARACTERISTICS, For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS $T_A = 25^oC$, $I_{IB} = 0.5$ mA, $V^+ = 15$ V, $V^- = -15$ V	Circuit and/or Char. Curve	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
STATIC CHARACTERISTICS							
INPUT CIRCUIT							
Input Balance (Correction) Currents:							
At x Input	I_{IC}	x = 0	–	−20	−2.1	+20	μA
At y Input		y = 0	–	−20	−8.7	+20	μA
Feedthrough Linearity Balance (Correction) Current	I_{OC}		–	−34	−2.9	+34	μA
OUTPUT CIRCUIT							
Output Offset Current	I_{OO}	x & y = 0,	–	−10	−0.23	+10	μA
Output Offset Voltage	V_{OO}	I_{OO} thru R_L = 33kΩ	–	−0.330	−0.0076	+0.330	V
Output Peak Current Swing	$\|I_O\|$	Thru R_L = 24kΩ	3	0.41	0.45	–	mA
Output Peak Voltage Swing	$\|V_O\|$	Across R_L = 33kΩ	4	12	12.9	–	V
DC SUPPLIES & BIASING							
Current Drain (Idling):							
At Term. 4		V^- = -15 V	–	–	2.9	4.5	mA
At Term. 12		V^+ = +15 V	–	–	2.0	3.0	mA
Reference Voltage	V_{ref}	Measured across Terms. 6 & 4 at I = 1mA	–	5.5	6.1	6.7	V
DYNAMIC CHARACTERISTICS							
Output Current	I_O	With I = 0.2mA at each input	–	–	0.21	0.32	mA
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$			11	0.69	1.0	1.7	
Accuracy		Worst case at 25°C	–	–	2.6	4.0	% of 10 V
Linearity				–	1.7	3.0	
Feedthrough Voltage:							
At y = 20V p-p, x = 0			–	–	9	20	mV p-p
At x = 20V p-p, y = 0			–	–	9	20	

NOTE: See page 7 for "Symbols, Terms and Definitions".

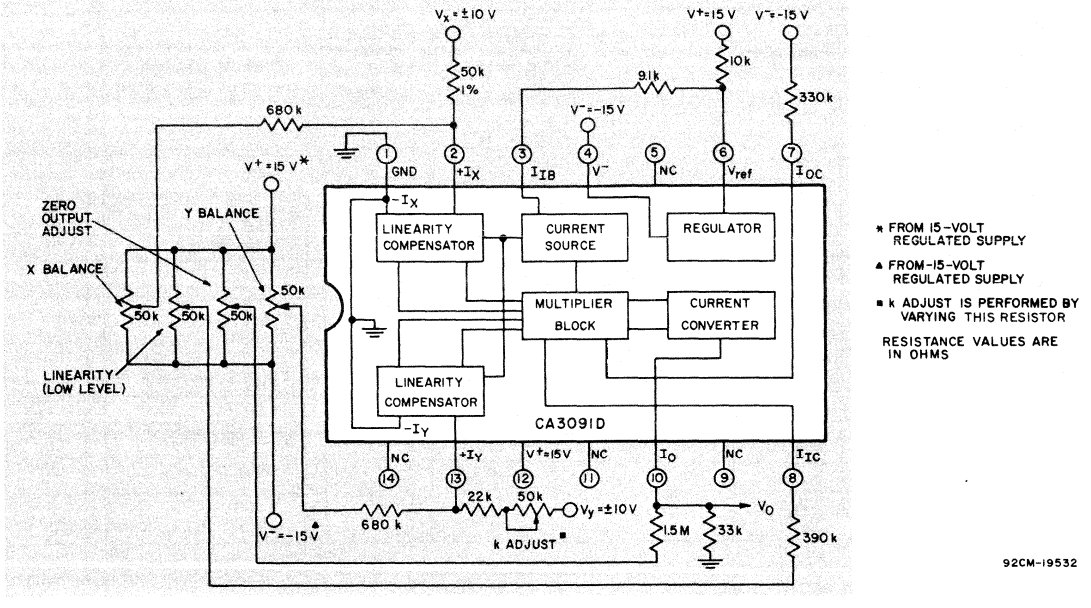
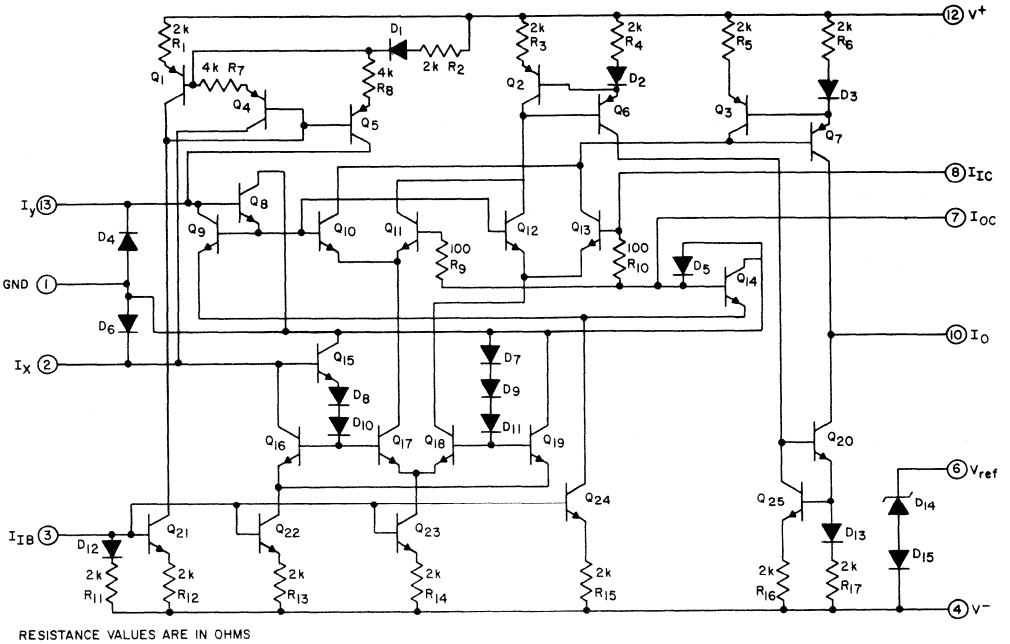


Fig.1—Functional block diagram of CA3091D with typical multiplier outboard(peripheral)circuitry.



RESISTANCE VALUES ARE IN OHMS

92CM-19534

Fig.2—Schematic diagram of the CA3091D.

CA3091

ELECTRICAL CHARACTERISTICS, Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: $T_A = 25^oC$, $I_{IB} = 0.5$ mA, $V^+ = 15$ V, $V^- = -15$ V	Circuit and/or Char. Curve	TYPICAL VALUES	UNITS
STATIC CHARACTERISTICS					
INPUT CIRCUIT					
Input Resistance:					
At x Input	R_I	$\lvert I_x \rvert \leq 0.2$ mA	5	1.3	k Ω
At y Input		$\lvert I_y \rvert \leq 0.2$ mA		0.5	k Ω
Input Capacitance:					
At x Input	C_I	at 1 MHz	–	5.8	pF
At y Input				5.8	pF
OUTPUT CIRCUIT					
Output Resistance	R_O		6	1.0	M Ω
Output Capacitance:	C_O	at 1 MHz		4.0	pF
DC Supply Voltage Sensitivity:					
At Term. 4	$\frac{\Delta V_O}{\Delta V^-}$		11	26	mV/V
At Term. 12	$\frac{\Delta V_O}{\Delta V^+}$			36	mV/V
DYNAMIC CHARACTERISTICS					
Bandwidth (At -3dB point):					
Through x Input	BW		8, 10	4.8	MHz
Through y Input			8, 9	4.4	MHz
3° Error Frequency:					
Through x Input			–	360	kHz
Through y Input				310	kHz
Maximum Slew Rate	SR	7pF in parallel with 10 MΩ load	7	27	V/μs
Temperature Coefficients:					
Output Offset Current	$\Delta I_{OO}/\Delta T$	x & y = O	–	–0.021	μA/°C
x-Input Balance Current	$\Delta I_{IC}/\Delta T$	x = O	–	–0.063	μA/°C
y-Input Balance Current		y = O	–	–0.063	μA/°C
Normalized k Factor $\left(k_N = \frac{k}{k_r}\right)$	k_N		–	–0.76	%/%/°C
Accuracy			–	0.11	%/°C
Linearity			–	0.06	%/°C
Feedthrough:					
At x = O			–	5.6	mV/°C
At y = O				5.7	mV/°C

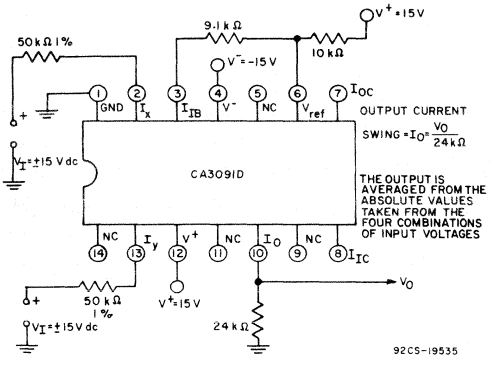


Fig.3—Test circuit for measurement of output current swing capability.

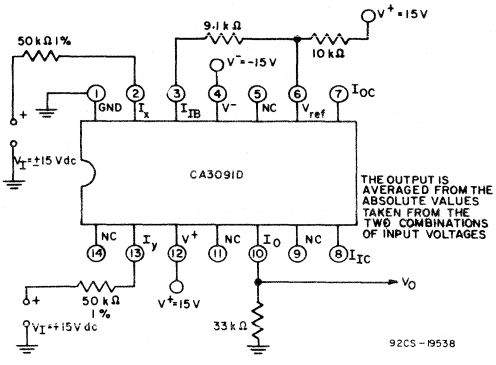


Fig.4—Test circuit for measurement of output voltage swing capability.

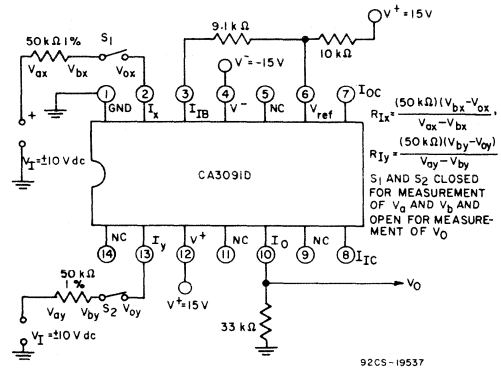


Fig.5—Test circuit for measurement of input resistance.

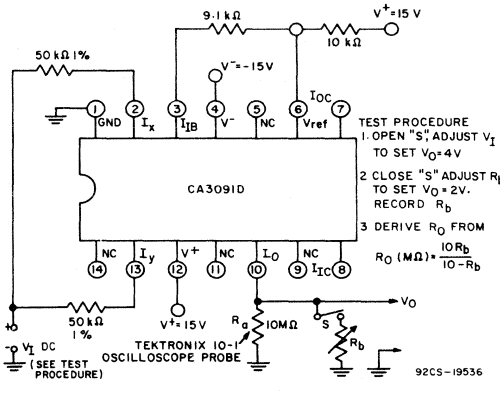


Fig.6—Test circuit for measurement of output resistance.

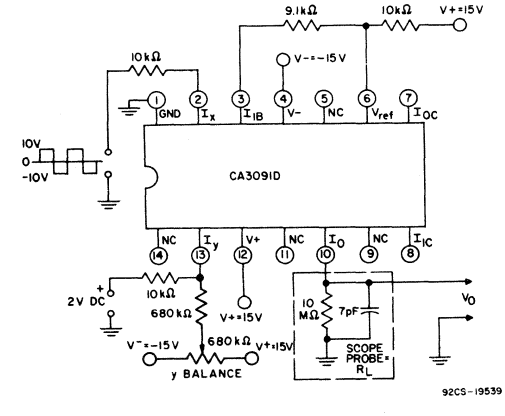


Fig.7—Test circuit for measurement of maximum slew rate.

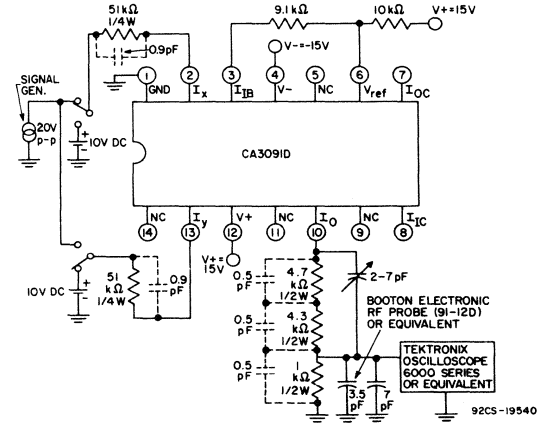


Fig.8—Test circuit for measurement of frequency response.

CA3091

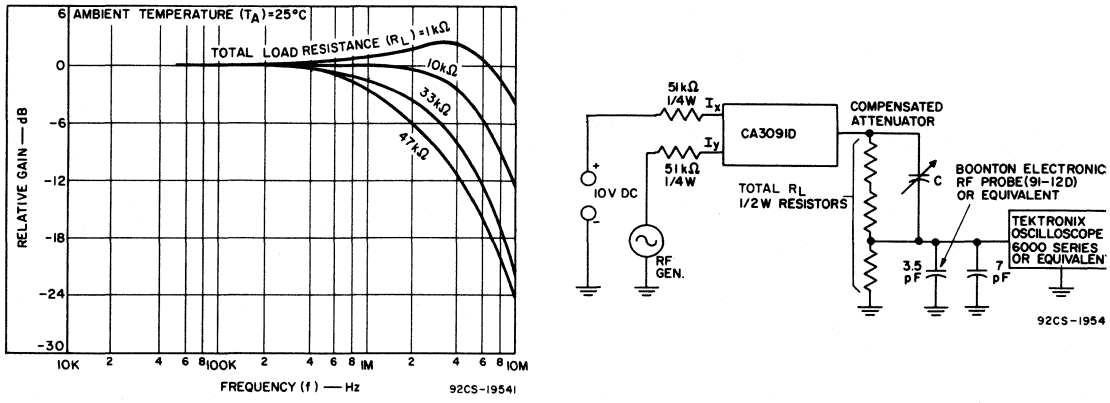


Fig.9- y–input frequency response characteristic curve with associated test circuit.

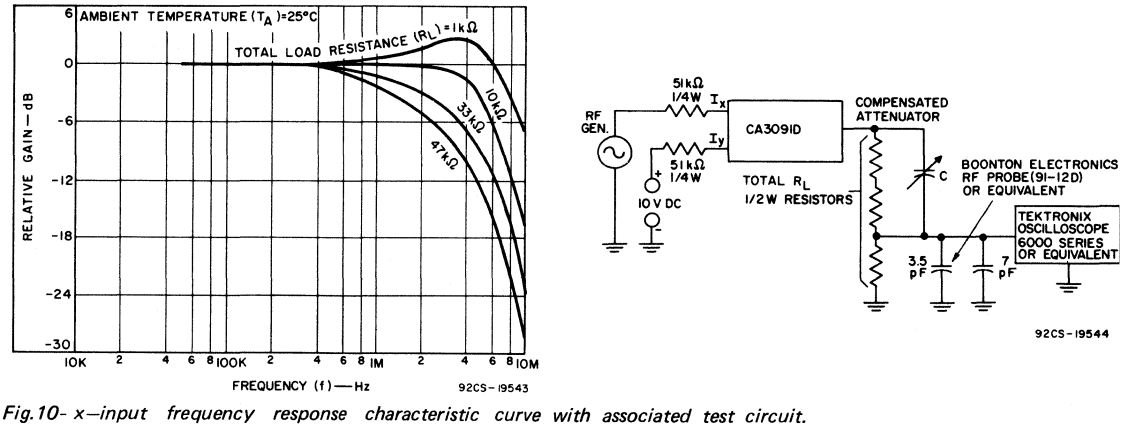


Fig.10- x–input frequency response characteristic curve with associated test circuit.

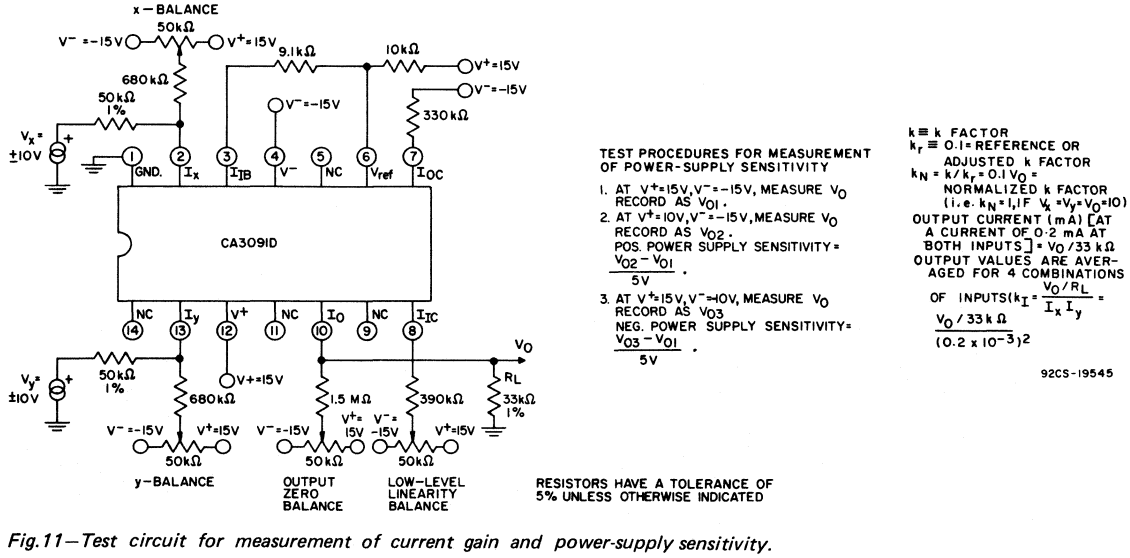
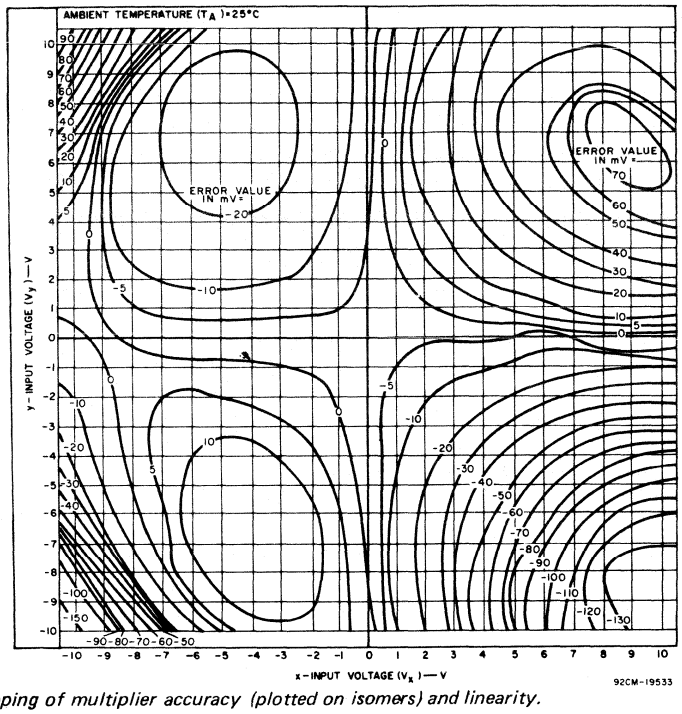


Fig.11—Test circuit for measurement of current gain and power-supply sensitivity.



Note: See "Contour Map" in "Symbols, Terms and Definitions" Section.

Fig.12—Contour mapping of multiplier accuracy (plotted on isomers) and linearity.

SYMBOLS, TERMS AND DEFINITIONS

Output Offset Current
The multiplier output current produced when both of the multiplier input signals are in the zero state.

Output Zero
Sets the output at the zero level when the x and y inputs are in the zero state. (It is implied that all other zeroing adjustments have been effected.)

R_I
Input Resistance — Converts the input voltage to an input current.

R_L
Output (Load) Resistance — Converts the output current to a voltage.

R_O
Output Resistance — See V_O and I_O for the equations associated with these properties.

Regulator Diode
A temperature compensated Zener diode, included in the multiplier circuit, to provide a stable I_{IB}.

Scale Factor or k factor (k)
Represents the basic gain of the multiplier as expressed in the equation $V_O = kV_XV_Y$

The equation indicates the ideal transfer function for the multiplier. The normalized k factor is expressed by $k_N = k/k_{ref}$ where k_{ref} is the ideal or reference k factor. The ideal factor, k_{ref} is the value at which the k factor is set when the k-factor adjust control is trimmed. Optimum operation of the CA3091D is achieved when the k-factor is 0.1.

V_{IM}
The maximum ac sine-wave voltage to be applied to the multiplier; a 20-volt p-p sine wave is the nominal maximum swing voltage recommended for use with 50-kilohm input resistors.

V_{MID}
An ac or dc voltage that approximately satisfies the equation

$$V_{MID} = V_{IM}/\sqrt{2}.$$

V_O
The output product voltage derived from the expression

$$(kV_XV_Y = V_O)$$

V_{ref}.
Temperature compensated zener connected to the −15 volt supply to provide a reference voltage as an aid in setting up a stable I_{IB}.

V_X, V_Y
The input voltages to be multiplied.

x-Balance Circuit
Sets the output to the zero level when the x-input is in the zero state.

y-Balance Circuit
Sets the output to the zero level when the y-input is in the zero state.

SYMBOLS, TERMS AND DEFINITIONS — continued

Accuracy
Accuracy defines the degree of error encountered in the operation of the multiplier. It is portrayed on a contour map by isomers (contour lines). Isomers with the highest values indicate "less-accurate" operation of the multiplier. (See illustrative Contour Map in Fig. 12.)

Contour Map
The contour map, shown in Fig. 12, is a graphical portrayal of the multiplier errors in the x, y input plane. Each contour line, termed "isomer", connects those points whose error values (in millivolts) are equal in magnitude. For example, a −20 mV contour line with points at $V_X = 5V$ and $V_Y = -3V$ indicates that the output voltage is 20 mV less than the theoretical output product (kV_XV_Y). This error voltage, presented in percent of full-scale input (±10 V), defines the "accuracy" of the device. Thus, a 20-mV error voltage represents an "accuracy" of 0.2% as derived from the equation:

$$\text{Accuracy} = 20\ \text{mV}/10 \times 100\% = 0.2\%.$$

A contour map provides a true indication of multiplier performance in each of the four quadrants. Each CA3091D is comprehensively tested and must provide the specified accuracy in the four quadrants.

Current Converter
This portion of the IC combines the multiplier's differential-amplifier output currents and converts them to a single-ended output current.

Current Sources
These circuits provide the biasing currents for the various circuits in the IC. The I_{IB} terminal provides the control current for the current-source circuit.

Feedthrough
Feedthrough occurs when an output signal is produced even though one of the input signals is zero. Consequently, feedthrough signal characteristics constitute a source of error in the operation of a multiplier. In the CA3091D, for example, the feedthrough signal output is specified to be less than 20 mV p-p when either terminal is set at 20 V p-p and the other terminal is set to zero.

I_{IB}
Circuit biasing control current.

I_{IC}
See I_{OC}.

I_O
Output product current ($k_I I_X I_Y = I_O$), where $k_I = kR_I^2 / R_L$

I_{OC}, I_{IC}
Compensatory input and output currents required to correct unlinearity along the x axis. (Optional for low-level signal use.)

I_X, I_Y
Input currents to be multiplied.

k
Voltage Scale Factor (determines the gain of the multiplier).

k_I
Current Scale Factor (k_I) = $(R_I^2 / R_L)k$.

k adjust
Scale-Factor Adjustment.

Linearity
"Linearity" indicates the degree of multiplier error (i.e. deviation from "straight-line" characteristics) along each of the four boundaries of the input x, y field. These boundaries are formed when one input is held at one of the two maximum values (10 volts or −10 volts) and the other input is swept through the voltage range. (See Contour Map for additional information.)

Linearity Adjust
An external circuit to provide vernier adjustment for optimum linearity. This control should be adjusted before adjusting the y-balance control.

Linearity Balance Circuit (Low-Level)
This circuit makes the multiplier's transfer function linear for low-level x-input signals.

Linearity Compensator
Internal circuitry that converts input current into a non-linear voltage, a requisite for producing a linear output in the differential amplifiers of the multiplier circuit.

Multiplier Circuitry
Provides the product of the two input voltages.

Multiplier Transfer Function
This function mathematically describes the interaction of the two inputs and the resulting output signal. The basic transfer function for a multiplier is

$$k(V_X + V_{Xe})(V_Y + V_{Ye}) = V_O + V_{Oe}$$

where: k = k factor and represents the basic gain of the multiplier

V_X, V_Y = the external inputs to be multiplied

V_O = the desired value of the product output signal

V_{Xe}, V_{Ye} = the "effective" errors that occur at the inputs of the multiplier and cause an output signal when either input is in a zero state.

V_{Oe} = the error voltage that develops at the output of the multiplier

DC correction factors are added to the multiplier inputs and output to compensate for the errors and offset variations. A complex linearity error term appears in the transfer function; however, this term is not included in the above equation for the purpose of clarity.

OPERATING CONSIDERATIONS

Operation of a Multiplier

A multiplier is, essentially, a gain-controlled amplifier (See Fig. 13) that multiplies the input signal (V_X) with the external gain controlling signal (V_Y) to produce the resultant output (V_O). The gain is externally adjustable by a coefficient (k). Stated simply, a multiplier produces an output voltage that is the linear product of two input voltages.

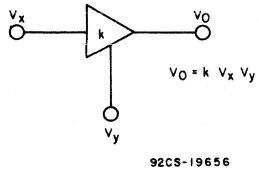
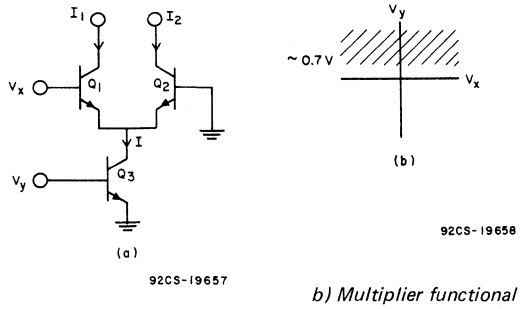


Fig.13—Gain-controlled amplifier.

The basic multiplier, shown in Fig. 14a, is a two-quadrant multiplier. The input signal (V_X) may have either a positive or negative polarity whereas, the external gain-controlling signal (V_Y) must be positive and greater than the base-to-emitter voltage (Fig. 14b). The output current ($I_1 - I_2$) of the differential amplifier, comprised of transistors Q1 and Q2, is related to both the input signal (V_X) and the current source (I). Since the current source (I) is related to the gain controlling signal (V_Y) the output current ($I_1 - I_2$), therefore, is related to both V_X and V_Y.



a) Basic circuit.

b) Multiplier functional only in shaded region.

Fig.14—Two-quadrant multiplier.

This relationship is essentially non-linear; thus an appropriate linearization circuit must be provided in the input stage to achieve the following linear relationship:

$$I_1 - I_2 = k' V_X V_Y \qquad \text{(Eq. 1)}$$

where k' is a constant

Figure 15 shows a typical arrangement of three differential amplifiers to form a four-quadrant multiplier. This arrangement incorporates the operating principles of the two-quadrant multiplier, but, in addition, it permits both of the input signals (V_X and V_Y) to have positive or negative polarities (or zero). When either input is zero, the output current ($I_1 - I_2$) must, theoretically, be zero as is shown by the following:

1. Assume $V_X = 0$,
   then $i_1 = i_2$ and $i_3 = i_4$
   therefore $i_1 + i_4 = i_2 + i_3$.
   Since $I_1 = i_1 + i_4$ and $I_2 = i_2 + i_3$,
   then $I_1 = I_2$.
   This equality is independent of V_Y
2. Now assume $V_Y = 0$,
   then $i_5 = i_6$.
   Sine $i_5 = i_1 + i_2$ and $i_6 = i_3 + i_4$,
   then $i_1 + i_2 = i_3 + i_4$.
   Since $i_1 = i_3$ and $i_2 = i_4$
   then $i_1 + i_4 = i_3 + i_2$.
   Therefore $I_1 = I_2$.
   This equality is independent of V_X.

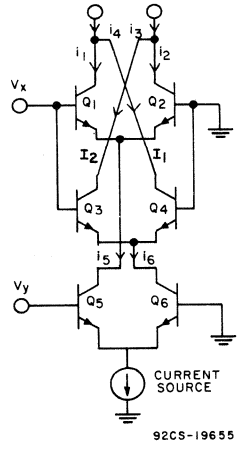


Fig.15—Basic four-quadrant multiplier.

The multiplying operation discussed in the previous section applies when neither V_X nor V_Y is zero. The output current ($I_1 - I_2$) then satisfies Equation 1,

$$I_1 - I_2 = k' V_X V_Y.$$

CA3091

The multiplying action of the four-quadrant multiplier is dependent on current unbalance in the three differential amplifiers. Ideally, the multiplying operation should not occur if either V_X or V_Y is O. However, in practical applications slight current unbalances do exist. It is necessary, therefore, to null out such unbalances with external potentiometers prior to operation.

TYPICAL OPERATING CONSIDERATIONS

The RCA-CA3091D, shown in Fig. 2, is a four-quadrant multiplier that incorporates the basic multiplier principle, previously discussed in "Operation of a Multiplier". Because the design of this multiplier is based on the multiplication of two input currents to produce an output current it is necessary to convert the input voltages to input currents and the output current to an output voltage by inserting resistors at both input and output terminals. Fig. 1 shows the four-quadrant multiplier with its peripheral circuitry for nulling current unbalances.

The Bias Current (I_{IB}) at Term. 3 sets the operating current level for the entire multiplier circuit by means of a current-source circuit. Therefore, it is essential that this bias current level remain constant under all operating conditions. To maintain this steady state, a temperature compensated zener diode is provided on the chip and connected to the Reference Voltage (Term.6).

Linearity of the differential amplifier transconductance function is accomplished by linearity compensators as shown in Fig. 1. To correct low-level signal unbalances that ma occur between Differential Amplifiers A and B, an externa potentiometer is connected to Terminals 7 and 8 (See Fig 1). The Current Converter circuit, which consists of a set o current mirrors, supplies the output current ($I_1 - I_2$). It i important that circuit unbalances be corrected prior t operation. Table I describes the alignment procedures fo correcting these unbalances.

A multifunctional circuit board (Figs. 16 and 17) is availabl for performing the four basic applications, such as, multi plying, dividing, squaring and taking the square root.

When the CA3091D is used as a multiplier (Fig. 18) or as a squarer (Fig. 18) only the basic pheripheral circuitry on the multifunctional circuit board is utilized and the general-purpose operational amplifier (CA3741T) is disabled from operation. Follow the ac alignment procedures for these two applications before operating the circuit.

When the CA3091D is used as a divider (Fig. 20), the operational amplifier is required in order to provide the proper negative feedback. The limitations for operation as a divider are that $O < V_Y \leqslant 10V$ and $-10V \leqslant V_Z \leqslant 10V$. Note, the range of V_Y is limited to the positive polarity; if V_Y was permitted to go negative, the feedback loop would go positive and, thereby, create an unstable operating condition.

Alignment of the divider (Fig. 19) differs from multiplier and squarer alignment because of the additional variances introduced by the operational amplifier. A coupling capacitor is

Table I

AC Alignment Procedures For CA3091D, Four-Quadrant Multiplier

(Refer to Fig. 16, for circuit pertaining to following alignment procedures.)

Step No.	Voltage Setting		Control Adjust	Test Equipment Used	Measure	Notes
	V_X	V_Y				
1	–	–	–	–	–	Set all potentiometers to center of range.
2	O	V_{IM}	x Balance	AC VM	V_O	Adjust for a minimum reading.
3	O	V_{IM}	Linearity	AC VM	V_O	Adjust for a minimum reading.
4	–	–	–	–	–	Repeat Steps 1 and 2 until no further improvement is noted.
5	V_{IM}	O	y Balance	AC VM	V_O	Adjust for a minimum reading.
6	O	O	Zero Output	DC VM	V_O	Adjust for zero output.
7	V_{MID}	V_{MID}	R_k	AC/DC VM	V_O	Adjust for $V_{MID}^2/10$ at the output.
8	–	–	–	–	–	Check multiplier for alignment in all four quadrants.

V_{IM} – Is the maximum AC swing of the sine wave that will be applied to the multiplier. A 20-volt p-p value is the nominal maximum swing of the AC sine wave with input resistors of 50 kilohms.

V_{MID} – An AC or DC voltage that approximately satisfies the equation $V_{MID} = V_{IM}/\sqrt{2}$. For example, if a 50-kilohm resistor is used with a 7-volt input, then R_k should be adjusted for a 4.9-volt output.

provided at the output of the divider alignment circuit in order to separate the ac signal from the dc signal and, thus, avoid interaction between the calibrating potentiometers.

The alignment procedure for the square-rooter function (Fig. 21) is identical to the alignment procedure for the divider function. The input voltage range is limited to $0 < V_I \leqslant 10V$. This limitation is necessary in order to prevent the output voltage (V_O) from latching to the negative output saturation voltage of the operational amplifier. Table II describes the divider alignment procedure.

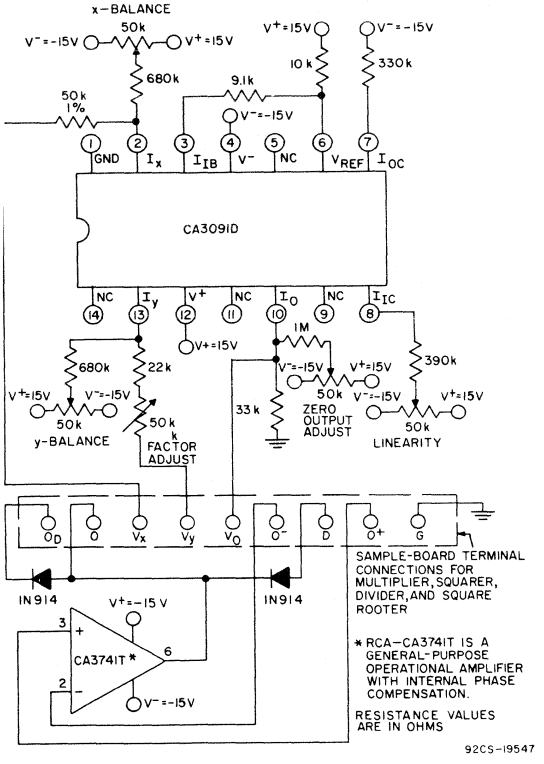
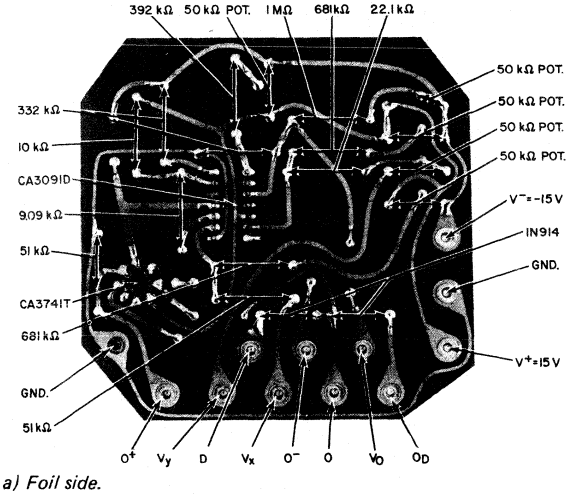
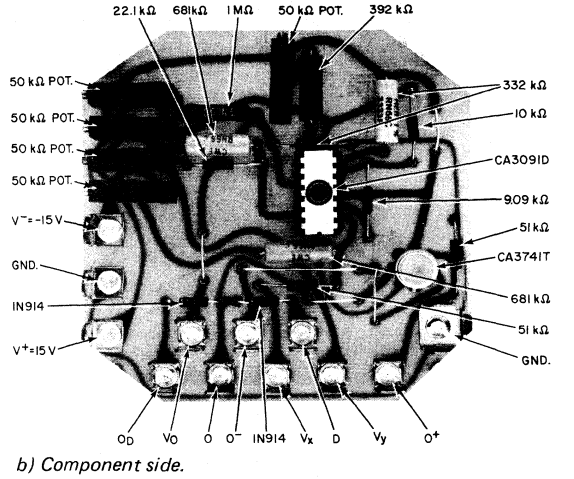


Fig.16—Typical multifunction circuit arrangement utilizing the CA3091D and CA3741T.



a) Foil side.



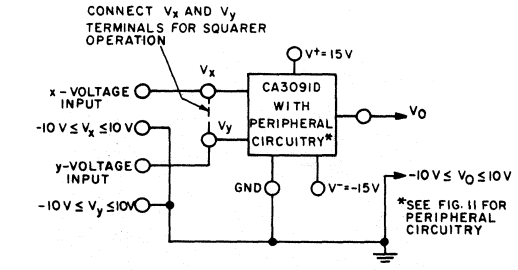
b) Component side.

Fig.17—Photographs of a printed-circuit board for multifunction applications (multiplier, squarer, divider, square rooter) utilizing the CA3091D and CA3741T.

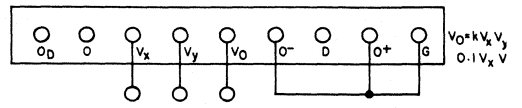
Table II — Divider Alignment Procedure

Step No.	Set V_z V	Set V_y V	Measure	Output Coupling	Test Equipment Used	Adjust	Notes
1	—	—	—	—	—	—	Set all potentiometers to center of range.
2	0	V_S	V_O	ac	ac — VM	O_{zero}	Adjust for minimum reading.
3	0	10V dc	V_O	dc	dc — VM	$x_{balance}$	Adjust for OV dc output.
4	V_S	V_S	V_O	ac	ac — VM	$y_{balance}$	Adjust for minimum reading.
5	5V dc	5V dc	V_O	dc	dc — VM	k_{adjust}	Adjust for 10V dc output.

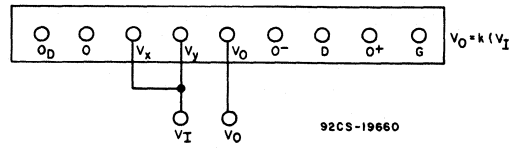
CA3091



a) Circuit arrangement for multiplier or squarer operation.



b) Terminal connections for multiplying operation.



c) Terminal connections for squarer operation.

Fig.18—Multifunction circuit-board arrangement with terminal connections for multiplier and squarer operation.

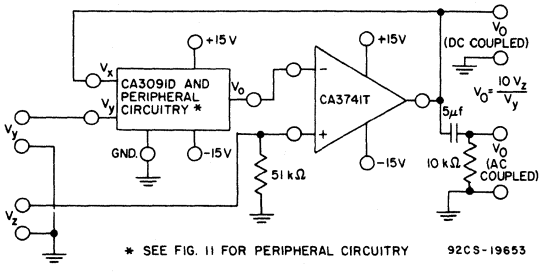


Fig.19—(a) Divider alignment circuit.

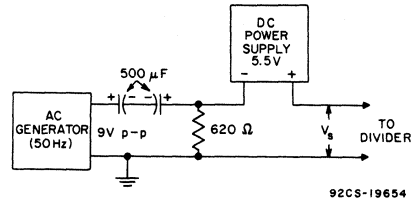
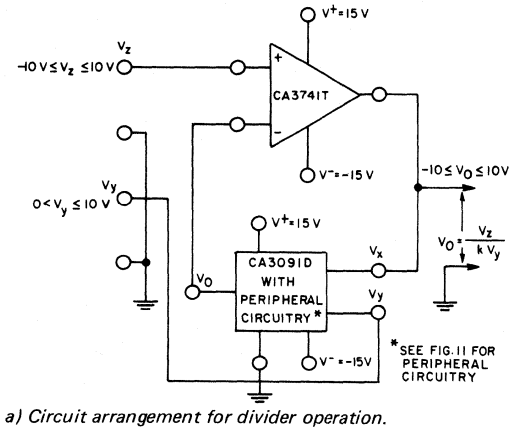
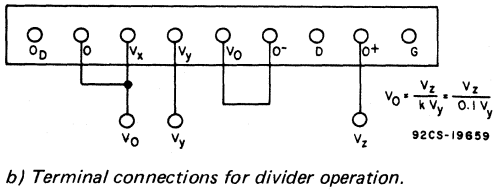


Fig.19—(b) Circuit to provide offset ac signal for use i divider alignment procedure.

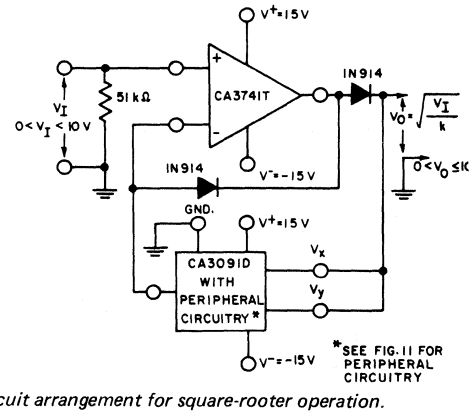


a) Circuit arrangement for divider operation.

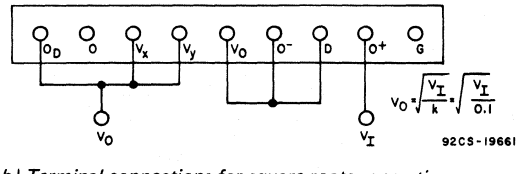


b) Terminal connections for divider operation.

Fig.20—Multifunction circuit-board arrangement with terminal connections for divider operation.



a) Circuit arrangement for square-rooter operation.



b) Terminal connections for square-rooter operation.

Fig.21—Multifunction circuit-board arrangement with terminal connections for square-rooter operation.

CA3164A

BiMOS Single-Chip Detector/Alarm System

With Integral Drivers for Mechanical and Piezoelectric Horn Alarms

Features:

- Interfaces directly with high Z sensors - no external buffer FET required
- Low input current: 1 pA max.
- Gate-protected input terminals
- On-chip beep oscillator for low battery indication

The RCA-CA3164A is a monolithic BiMOS Integrated circuit designed to meet the stringent system requirements of a battery- or line-operated alarm circuit. When used with an ionization chamber and electromechanical or piezoelectic horn, it provides a one-chip approach to smoke detection. No external active devices are required to interface with either the chamber input or horn output terminals. The CA3164A can also be used with photoelectric chambers by the addition of several external components.

The CA3164A is supplied in the 14-lead dual-in-line plastic package (E suffix).

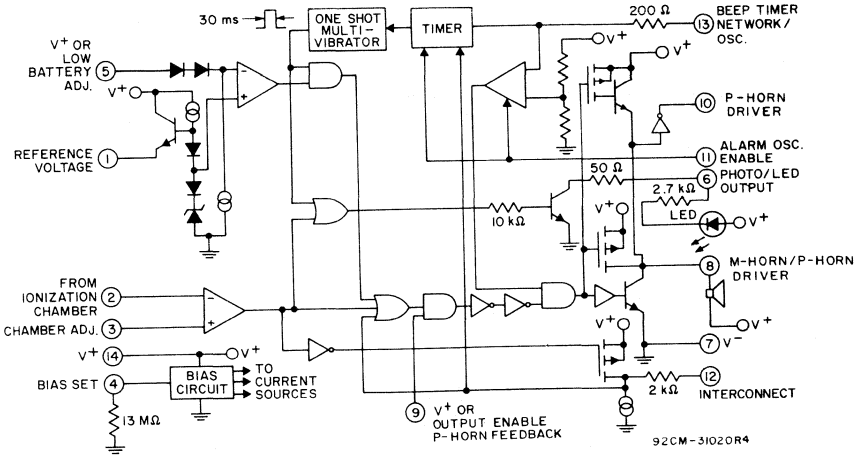


Fig. 1 - Simplified functional diagram for CA3164A.

File Number **1139**

CA3164A

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE, V+ ..... +11 V
DEVICE DISSIPATION, P_D:
Up to T_A = 25°C ..... 600 mW
Above T_A = 25°C derate linearly at ..... 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +50°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from
case for 10 seconds max. ..... +265°C

OPERATING MODE TRUTH TABLE

CONDITION	BATTERY	LED TERM. 6	ALARM HORN TERMS. 8, 9, 10	SYSTEM REMOTE OUTPUT TERM. 12	REMOTE UNIT ALARM STATUS
No Smoke in Chamber	NORMAL	BLINK[1]	OFF	LOW	OFF
No Smoke in Chamber	LOW	BLINK[1]	BEEP[1]	LOW	OFF
Smoke in Chamber	X	ON	ON[2]	HIGH	ON
Remote Alarm On, No Smoke in Local Chamber	X	BLINK[1]	ON[2]	HIGH[3]	ON

X = Don't Care

1. 30-ms pulse every 50 seconds (typ.).
2. Alarm horn may be programmed for continuous sound by connecting terminal 11 to V+.
   The alarm may be pulsed by connecting terminal 11 to ground through a resistor (from 3.9 to 10 MΩ.) The typical duty cycle is 95% ON, and is determined by the size of the resistor.
3. Signal received from activated remote alarm.

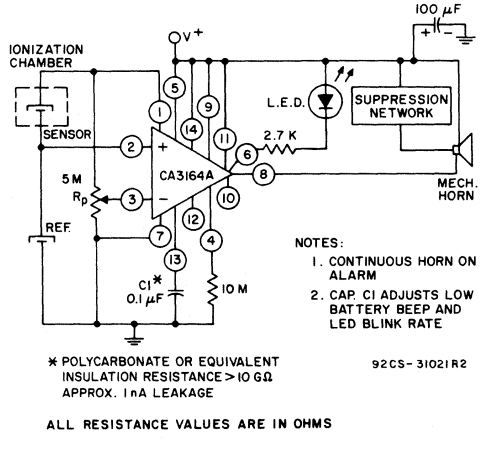


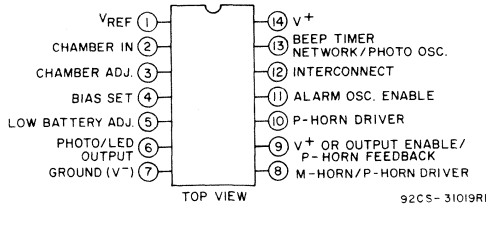
Fig. 2 - Basic ionization detector with electromechanical horn.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 9 V

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Operating Voltage			7	9	11	V
Common-Mode Input Voltage Range, V_{ICR}		(V+ -2 V) = 7 V	0	—	7	V
Low-Battery Trigger Voltage		External adjust (Increase only)	7	7.4	7.6	V
Horn Driver		Term. 8 = 100 mA	—	—	0.5	V
$V_{CE(sat)}$		Term. 8 = 300 mA	—	—	1.1	
Reference Voltage		Term. 1	6.1	6.5	6.9	V
Input Leakage Current, I_L		Term. 2	—	—	1	pA
		Term. 2 at 50°C	—	—	2.5	
		Term. 3	—	—	50	
Standby Current (10 MΩ from Term. 4 to ground)		No LED connected	—	8*	14	μA
		LED connected -20 mA for 30 ms every 60 s	—	18	—	
		Photoelectric operation - LED photocurrent = 0.6 A (5-second rate)	—	13	—	
Reference Source Current			5	—	—	μA
LED Driver Sink Current		Term. 6	20	50	—	mA
Output Sink Current	Term. 8	Term. 8 = 1.1 V	200	300	—	mA
	Term. 8	Term. 8 = 0.5 V	100	150	—	
	Term.10	Term. 10 = 2 V	20	25	—	
Output Source Current	Term. 8	Term. 8 = V+ -2V	20	25	—	mA
	Term. 10	Term. 10 = V+ -2V	20	25	—	
Interconnect Current	Source	VO = 0 V	1.5	3.5	6	mA
	Sink	VO = 9 V	—	45	65	μA
Remote Fan-out			20	—	—	
Low-Battery Adjust, Term. 5 Input Current			50	70	225	nA
Timing Current		Term. 13	10	—	62	nA
LED Blink Period		Adjustable	—	—	1	PPM
LED Pulse Width		Fixed	—	30	—	ms
Alarm Pulse Duty Cycle		On-time	—	95	—	%
(4.7 MΩ from Term. 11)		On-time = 95%	—	0.5	—	s
to ground)		Off-time = 5%	—	0.026	—	

*Adjustable to 5 μA.

TERMINAL ASSIGNMENT



CA3164A

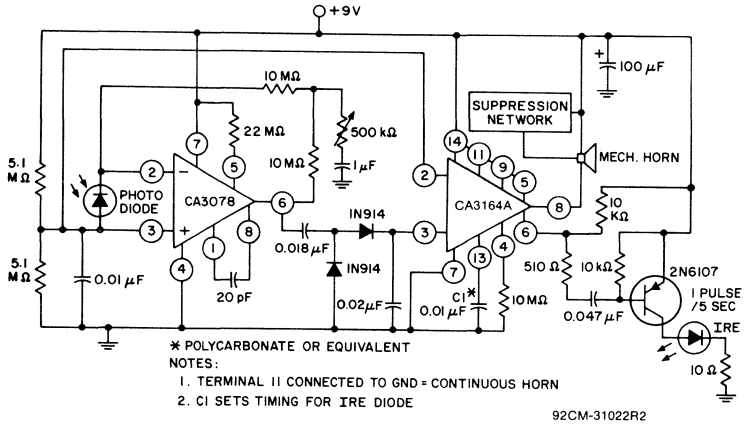


Fig. 3 - Typical photoelectric system using CA3164A.

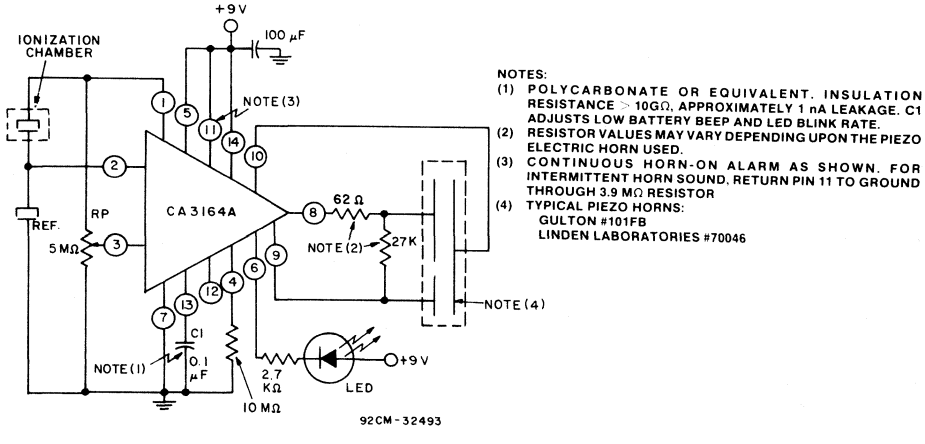
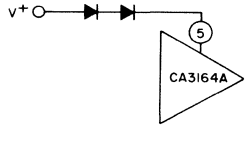


Fig. 4 - Basic ionization detector with piezoelectric horn.

Connections for Optional Functions

1. Low Battery Adjustment - Terminal 5

Add diodes as shown below to increase the low-battery trigger point.

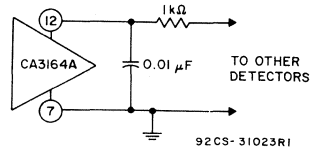


2. Sounder Operating Mode

Continuous sound on alarm - connect terminal 11 to V+.
Pulsed sound on alarm - connect a 3.9MΩ resistor between terminal 11 and ground.

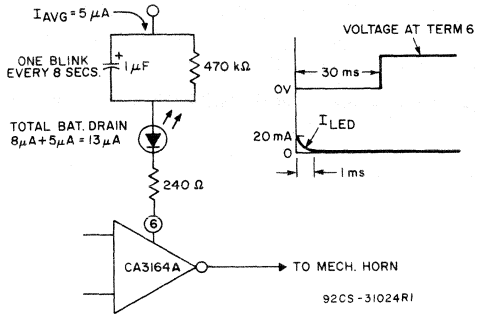
3. Remote (Interconnect)

Connect terminal 12 to same terminal on all other units (fan out = 20 units). When interconnecting units for the remote-alarm function, the extremely low currents involved make it extremely important that a provision be made for limiting externally induced transients into the remote terminal. For example, inadvertent contact with external power sources or electricial storm activity may cause triggering of the remote alarm function. The circuit below will reduce the possibility of such occurrences.



4. LED On-Time Adjustment

The CA3164A is designed to provide a fixed LED on-time of approximately 30 ms. For applications requiring a reduction in one-time, the following circuit is recommended:



This circuit reduces the LED on-time but does not affect the horn on-time of 30 ms. When using this configuration during the continuous-alarm mode (smoke in chamber), the LED will be off instead of on, as shown in the truth table. If the horn is pulsed during the alarm mode, the LED will blink at the pulse rate.

Cleaning Procedure

To insure leakage currents of less than 1 pA, the following procedure is recommended:

(a) degrease in trichlorethylene
(b) rinse in de-ionized water

Circuit Description

Basic Functions - The CA3164A is designed to interface directly with an ionization-chamber type of smoke detector. Upon being triggered by a decreasing voltage at the ionization-chamber output, the IC operates a mechanical transducer. In addition to this basic smoke-detector function, another circuit monitors and compares the battery voltage to an internal reference-voltage source. Once the battery voltage drops below a defined level, a short 30-ms beep sound is produced in synchronism with an LED indicator every 50 seconds. This rate is determined by a programming resistor connected between terminal 4 and ground and an external 0.1 μF capacitor connected between terminal 13 and ground.

A buffered output voltage is available from the reference supply that may be used to operate the ionization chamber. This voltage helps maintain constant sensitivity with decreasing supply voltage.

There are two alarm modes and two conditions that will sound the alarm. The first alarm condition is the normal smoke in the ionization chamber; the other condition is a high level to the remote input/output terminal of the IC.

The first alarm mode is the customary continuous sound. The second alarm mode is an interrupted or pulsed sound.

Operation - The CA3164A is current programmable by placing a resistor from terminal 4 to ground. This resistor establishes the operating current levels for all the current sources within the IC including the timing circuits.

An operational amplifier configuration is used for the ionization chamber input. P-channel MOS field-effect transistors are used on this input in the bootstrap configuration shown in Fig. 5 to drive the protection diodes and maintain the subpicoampere input current.

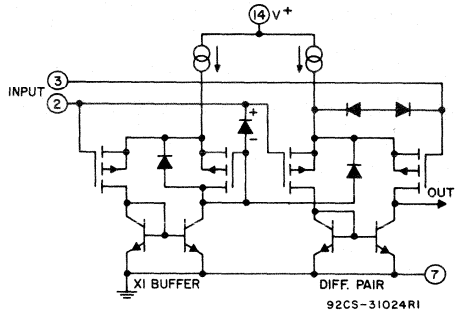


Fig. 5 - Schematic of ionization-chamber amplifier.

A conventional bipolar amplifier is used for the battery monitor circuit. The zener diode is biased at about 3 μA. This zener voltage is raised one V_{AK} and then applied to the base of an emitter-follower transistor to buffer and reflect the zener voltage to the outside reference terminal. By providing an additional input terminal (terminal 5), where three level-shifting diodes are available, an additional external means is provided to raise the voltage level at which the CA3164A goes into the low-voltage alarm mode.

An integrating type of timer is used to generate the one-minute LED power-monitor and battery-function indicator pulse. Fig. 6 shows the system. A constant-current source charges the external 0.1 μF timing capacitor C_T, which subsequently triggers the 30-ms one-shot multivibrator composed of n-channel MOS transistor N3 and n-p-n transistor Q1.

N_3 is then cut off and its drain climbs to the supply rail, linearly charging capacitor C_{PULSE}. When the drain of N_3 reaches the supply rail, the charging current ceases, cutting off the base current of Q1 and discharging the capacitor.

A open-collector n-p-n transistor is used to drive the optional external LED power monitor and battery-condition indicator (Fig. 1).

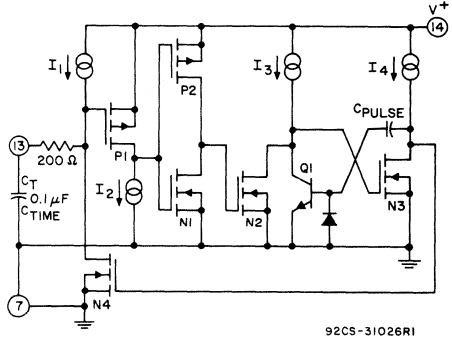


Fig. 6 - Schematic of timer and one-shot multivibrator.

CA3164A

The schematic diagram of the drive circuit for a mechanical horn (M-horn) and a piezoelectric horn (P-horn) is shown in Fig. 7. For M-horn operation, the output of the driver at terminal 8 is used. A large n-p-n transistor Q3 with an active pull-up transistor Q2 provide over 300 mA of drive current. In the M-horn mode, terminal 9 must be returned directly to V+. P-horn operation requires the output from a second inverting amplifier at terminal 10, as well as the output from terminal 8. For P-horn operation, terminal 9 is connected to the feedback terminal of the horn.

The output terminals 8 and 10 are capable of driving power FET's with input capacities greater than 1000 pF. With terminal 9 used as an input, an inverted output is available at terminal 8 while the output of terminal 10 is non-inverted.

Typical Switching Times in ns.
Conditions: V+ = 9V; Input to Term. 9 = 100 kHz, 8.5V Sq. Wave

	t_{PLH}	t_{TLH}	t_{PHL}	t_{THL}	Capacitive Load (pF)
Term. 8	340	155	180	80	0
Term. 10	200	25	360	70	0
Term. 8	385	220	205	100	1000
Term. 10	235	72	425	100	1000

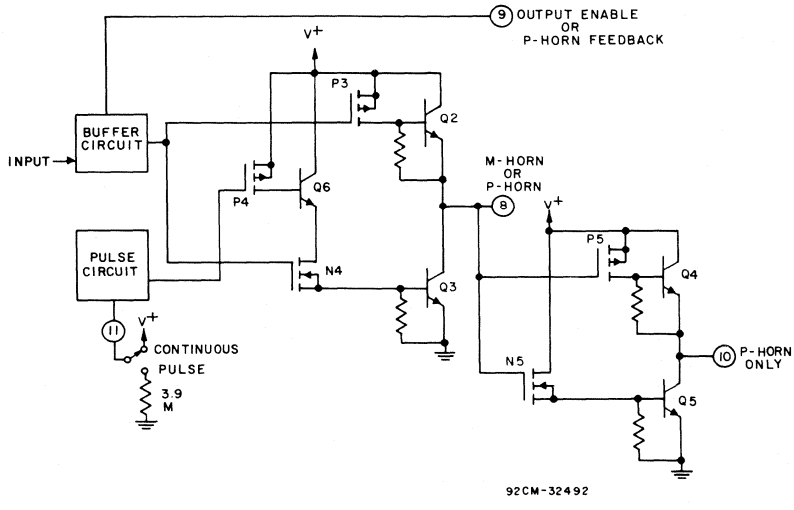


Fig. 7 - Schematic of mechanical and piezoelectric horn drivers.

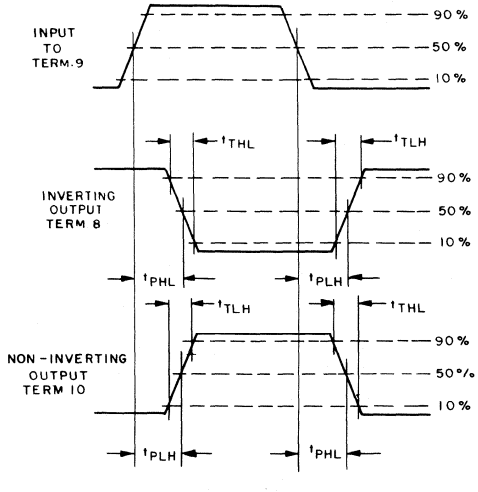


Fig. 8 - Transition times and propagation delay times.

The horn output, on alarm, can be continuous or pulsed. The mode is determined by the connection of terminal 11. When this terminal is connected to V+, the alarm sound is continuous, and when it is connected to ground through a programming resistor, as shown in Fig. 7, the alarm is pulsed. The pulse rate is determined by the sum of the current through the programming resistor connected to terminal 11 and the current from the basic timer-current source. Thus, when the detector goes into the alarm mode, the nominal 50-second time period is decreased to a nominal 0.5-second period. This 0.5-second period is set by the external 3.9 MΩ resistor. PMOS transistor P4 and bipolar transistor Q6 provide the on-off switching of NMOS transistor N4 in the driver circuit to provide the pulsed output from the horn.

Terminal 12, the interconnect terminal, is both an input and output for the circuit. When connected by two wires to other units, alarm in any one unit will activate the other units. A small sinking current of only 10 μA keeps the line impedance down while a sourcing current of over 2 mA is available in the alarm mode. This current is more than sufficient to trigger over 20 additional units.

Photoflash Circuit

Low standby current drain helps extend the battery life in portable consumer electronic products that must deliver only occasional bursts of power. The CA3164A control IC is a BiMOS chip that consumes less than 15 μA during standby; yet it can provide 100 mA of chopped current to the dc-to-dc converter in an electronic photoflash circuit during the energy-reservior charging cycle.

In the photoflash application, Fig 9, the CA3164A drives the primary of step-up transformer T1 with symmetrically chopped current at a 500 to 2000-Hz rate. The bridge-connected diodes. D1 through D4, rectify the output of T1 and charge the energy-reservior capacitor, C3, to approximately 280 V. The maximum charge of C3 is determined by the voltage-divider ratio R2:R3. A tap between these resistors provides a turn-off signal to pin 2 of the CA3164A. LED D6 is energized while C3 charges.

During the C3 charge cycle, capacitor C4 is also charged via D5. R4 and the primary of step-up transformer T2. When the manual triac-trigger switch (in the camera) is momentarily closed, the triac conducts and C4 is discharged through the primary of T2, generating a short 4-kV pulse across the secondary of T2. This pulse overcomes the ionization potential of the photoflash tube which, once fired, continues to draw current from reservoir-capacitor C3 until the charge is exhausted.

The CA3164A's chopper frequency, determined by R1, R5 and C5, is about 500 Hz with the components shown. The duty cycle is determined primarily by R7 and approximates 50% when R7 is 31.4 kΩ. Capacitor C3 recharges in about 20 seconds.

Other Applications of the CA3164A

Although the primary function of the CA3164A is smoke detection, it may also be used in many other circuits that require high front-end sensitivity and the very high input resistance of MOS transistors. The internal circuitry of the CA3164A requires a minimum of external components, and the low battery drain eliminates the need for ac power in most circuits.

A few of the possible uses are: humidity sensor, where two metal electrodes replace the ionization chamber; intrusion alarm; P-horn driver; controller for a dc-to-dc converter such as might be used in an electronic photoflash unit; or with a photodiode as an automatic switch for turning on night lights.

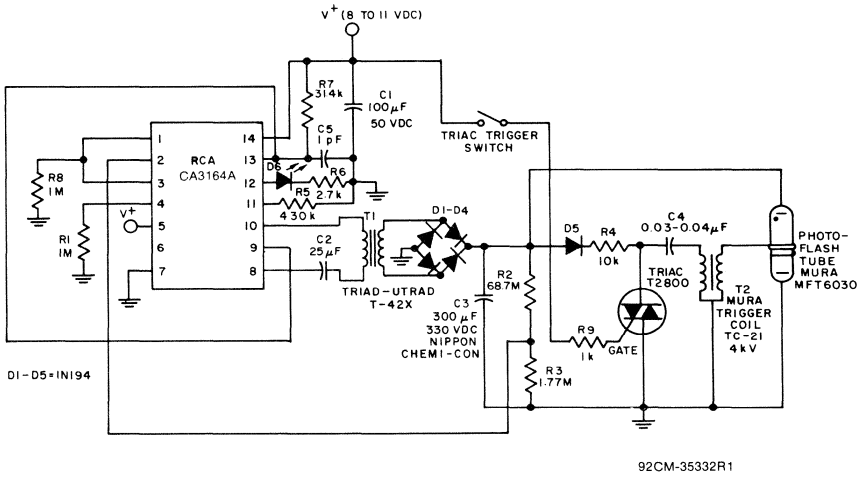


Fig. 9 - CA3164A in photoflash circuit.

Arrays — Technical Data

Type No.	Description	Page No.
Amplifier		
CA3026	Dual Differential Amplifier	501
CA3048	Four Independent AC Amplifiers	763
CA3049	Dual High Freq. Differential	526
CA3050	Dual Differential Amplifier with emitter follower inputs	531
CA3051	Same as CA3050, except in a plastic pkg.	531
CA3052	Same as CA3048, except RIAA noise Tests	770
CA3054	Same as CA3026, except in a plastic pkg.	501
CA3060	Triple Transconductance Amplifier	247
CA3102	Similar to CA3049 except in a plastic pkg.	526
Diode		
CA3019	One full wave bridge & two independent diodes	646
CA3039	Five independent diodes with cathode connected to substrate	648
CA3141	10 High Voltage Diodes, 3 pairs common cathode, 2 pairs common anode	703
Transistor		
CA1724	Four individual 80V, 1A transistor	637
CA1725	Four individual 70V, 1A transistor	637
CA3018	Four Monolithic transistors, 2 independent, emitter follower	640
CA3045	Five Monolithic transistors, 3 independent, 2 diff. connected	652
CA3046	Same as CA3045 except in a plastic pkg.	652
CA3050	Dual differential amp. with emitter follower	531
CA3051	Same as CA3050 except in a plastic pkg.	531
CA3081	Seven transistor common emitter array	151
CA3082	Seven transistor common collector array	151
CA3083	Five monolithic, independent, gen. purpose trans.	658
CA3086	Five mnolithic transistors, 3 independent, 2 diff. connected	662
CA3096	2 PNP, 3 NPN Monolithic transistors	667
CA3097	Thyristor - PUT, SCR, Zener PNP/NPN, and independent NPN transistor	677
CA3118	High voltage version of CA3018	688
CA3127	Five independent transistors	695
CA3138	Four individual high current transistors	700
CA3146	High voltage version of CA3046	688
CA3183	High voltage version of CA3083	688
CA3227	High freq. version of CA3127	706
CA3246	High freq. version of CA3146	706
CA3250	Common-emitter array	171
CA3251	Common-collector array	171
CA3600	CMOS array, 3 PMOS, 3NMOS Device	709
CD74HCU04	Hex Inverter (Unbuffered)	—

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

CA1724, CA1725

High-Current N-P-N Transistor Arrays

Four Individual Sealed-Junction
High-Current N-P-N Transistors

Features:

- **High Current — 1 A**
- **High Breakdown Voltage:**
  CA1725 = 80 V dc min. $V_{(BR)CES}$ @ I_C = 10 μA
  CA1724 = 70 V dc min. $V_{(VR)CES}$ @ I_C = 10 μA
- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**
- **Electrically similar and pin compatible with industry types MPQ3724, MPQ3725; FPQ3724, FPQ3725; DH3724, DH3725; SP3724, SP3725 in similar packages**

The RCA-CA1724 and -CA1725 are high-current n-p-n transistor arrays each containing 4 individual sealed-junction high-current n-p-n transistors. They are intended for high-current driver applications.

These devices are alike except for breakdown voltage ratings.

The CA1724 and CA1725 are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of −55°C to +125°C.

Applications

- **High-Current LED Driver**
- **High-Voltage Switching**
- **Relay and Solenoid Driver**
- **Lamp Driver**

Comparison of High Current N-P-N Arrays

CHARACTERISTIC	CA1725			CA3725			CA3138A		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
V_{CEO}(sus)	50	58	—	50	—	—	15	20	—
$V_{(BR)CBO}$	80	94	—	80	—	—	25	60	—
$V_{(BR)EBO}$	6	6.9	—	6	—	—	5	7.2	—
h_{FE} @ 1A	20	25	—	20	—	—	40	170	—
h_{FE} @ 500 mA	30	35	—	30	—	—	95	170	—
h_{FE} @ 100 mA	35	40	—	35	—	—	80	160	450
V_{CE}(SAT) @ 500 mA	—	0.38	0.5	—	—	0.5	—	0.26	0.4
t_{ON} @ 500 mA	—	38	—	—	—	40	—	31	—
t_{OFF} @ 500 mA	—	185	—	—	—	60	—	105	—
C_{EB}	—	100	—	—	95	—	—	77	—
C_{CB}	—	12.5	—	—	12	—	—	18	—

File Number **1228**

CA1724, CA1725

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	LIMITS						Units
		CA1724			CA1725			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO(sus)}$*	I_C = 10 mA, I_B = 0	40	45	—	50	58	—	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = 10 μA, I_B = 0	70	75	—	80	94	—	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	70	75	—	80	94	—	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	6.9	—	6	6.9	—	V
Base-to-Emitter Saturation Voltage, $V_{BE(sat)}$*	I_C = 500 mA, I_B = 50 mA	0.75	0.89	1.0	0.75	0.9	1.0	V
Collector-to-Emitter Saturation Voltage $V_{CE(sat)}$	I_C = 500 mA, I_B = 50 mA	—	0.36	0.5	—	0.38	0.5	V
Collector-Cutoff Current, I_{CBO}	V_{CB} = 40 V, I_E = 0	—	0.3	1.7	—	0.3	1.7	μA
Static Forward-Current Transfer Ratio (Beta), h_{FE}	I_C = 100 mA, V_{CE} = 1.0 V	35	40	—	35	40	—	
	I_C = 500 mA, V_{CE} = 1.0 V	30	35	—	30	35	—	
	I_C = A, V_{CE} = 1.0 V	20	25	—	20	25	—	
Turn-On Time (See Test Ckt.Fig.6), t_{on}	I_C = 500 mA, I_{B_1} = 50 mA	—	38	—	—	38	—	ns
Turn-Off Time (See Test Ckt.Fig.6), t_{off}	I_C = 500mA, I_{B_1} = I_{B_2} = 50 mA	—	185	—	—	185	—	ns
Emitter-to-Base Capacitance, C_{eb}	I_C = 0, V_{EB} = 0.5 V	—	102	—	—	100	—	pF
Collector-to-Base Capacitance, C_{cb}	I_E = 0, V_{CB} = 10 V	—	14	—	—	12.5	—	pF

* Pulse Conditions: width = 300 μs; duty cycle = 1%.

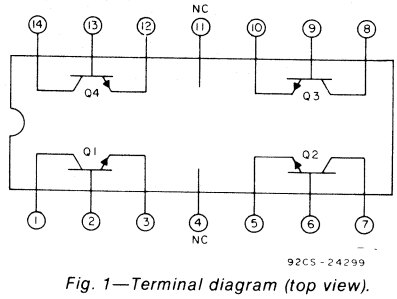


Fig. 1—Terminal diagram (top view).

CA1724, CA1725

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		CA1724	CA1725	
COLLECTOR-TO-EMITTER VOLTAGE With Base Open	V_{CEO}	40	50	V
COLLECTOR-TO-BASE VOLTAGE	V_{CBO}	70	80	V
EMITTER-TO-BASE VOLTAGE With Collector Open	V_{EBO}	6		V
COLLECTOR CURRENT	I_C	1.0		A
POWER DISSIPATION:	P_D			
For Each Transistor		1.0		W
Total Package		2.0		W
At T_A above 25°C derate linearly (Total Package)		20		mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating		−55 to +125		°C
Storage		−65 to +150		°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/32" (3.17 mm) from seating plane for 10 s max.		300		°C

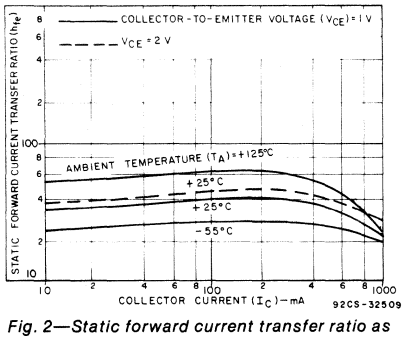


Fig. 2—Static forward current transfer ratio as a function of collector current.

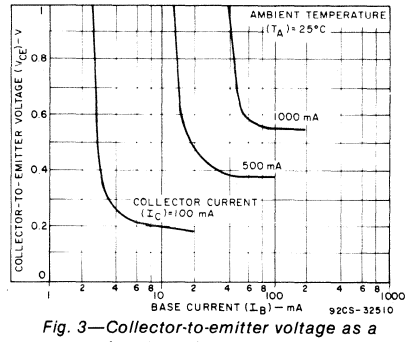


Fig. 3—Collector-to-emitter voltage as a function of base current.

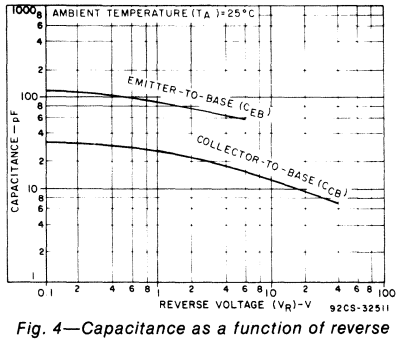


Fig. 4—Capacitance as a function of reverse voltage.

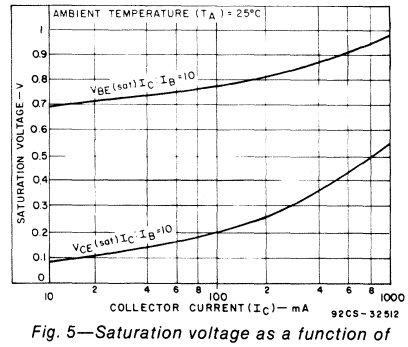


Fig. 5—Saturation voltage as a function of collector current.

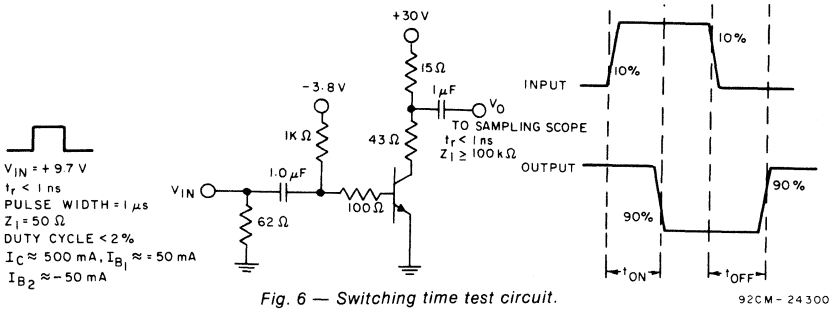


Fig. 6 — Switching time test circuit.

CA3018, CA3018A

General-Purpose Transistor Arrays

Two Isolated Transistors and
a Darlington-Connected Transistor Pair

For Low-Power Applications at Frequencies
from DC Through the VHF Range

Features:

- *Matched monolithic general purpose transistors*
- *H_{FE} matched ± 10%*
- *V_{BE} matched ± 2 mV CA3018A (± 5m V CA3018)*
- *Operation from DC to 120 MHz*
- *Wide operating current range*
- *CA3018A performance characteristics controlled from 10 μA to 10 mA*
- *Low noise figure - 3.2 dB typical at 1KHz*
- *Full military temperature range capability (-55 to +125° C)*

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Applications

- *General use in signal processing systems in DC through VHF range*
- *Custom designed differential amplifiers*
- *Temperature compensated amplifiers*
- *See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested applications.*

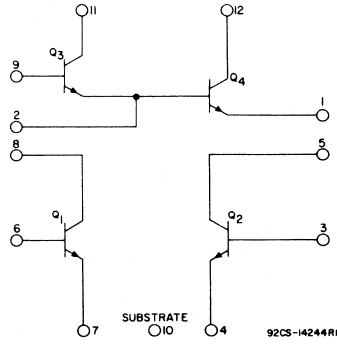


Fig. 1 — Schematic Diagram for CA3018 and CA3018A

File Number **338**

CA3018, CA3018A

aximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
wer Dissipation, P:			
ny one transistor	300	300	mW
otal package	450	450	mW
ate at 5 mW/°C for $T_A > 85°C$			
mperature Range:			
perating	-55 to + 125	-55 to + 125	°C
torage.	-65 to + 150	-65 to + 150	°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO} ·	15	15	V
Collector-to-Base Voltage, V_{CBO} · ·	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO} · · ·	5	5	V
Collector Current, I_C · · · · · · · · ·	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. . . . . +265°C

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	3
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA I_C=1mA I_C=10μA	– 30 –	100 100 54	– 200 –	50 60 30	100 100 54	– 200 –	– – –	4
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	4
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V I_C=1mA I_C=100μA	1500 –	5400 –	– –	2000 1000	5400 2800	– –	–	5
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V I_E=1mA I_E=10mA	– –	0.715 0.800	– –	0.600 –	0.715 0.800	0.800 0.900	V	6
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	6,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\lvert \frac{\Delta V_{BE}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	–	-1.9	–	–	-1.9	–	mV/°C	7
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V I_E=10mA I_E= 1mA	– –	1.46 1.32	– –	– 1.10	1.46 1.32	1.60 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\lvert \frac{\Delta V_{BED}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\lvert \frac{V_{BE_1} - V_{BE_2}}{\Delta T} \rvert$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

CA3018, CA3018A

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS										
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

STATIC CHARACTERISTICS

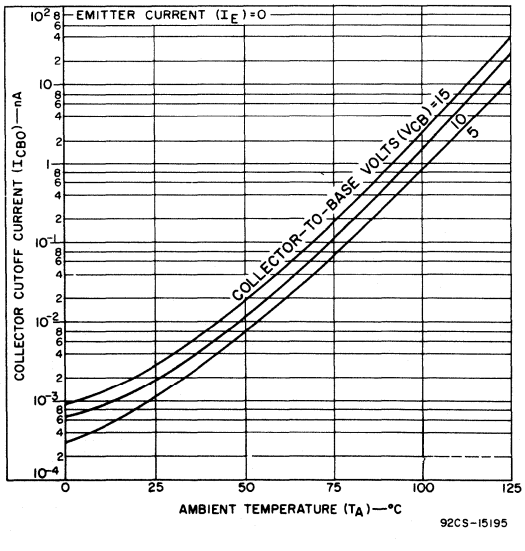


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

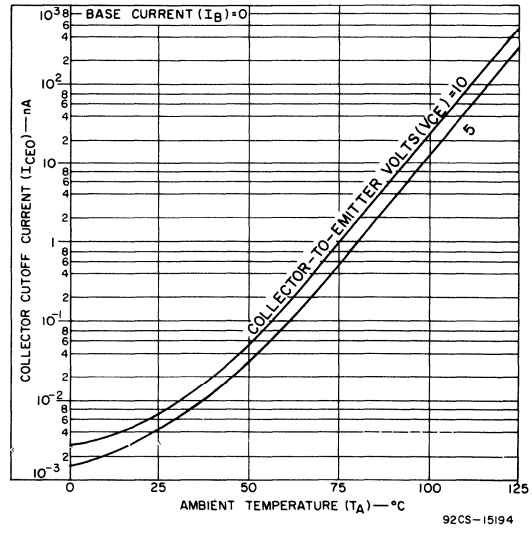


Fig.3 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

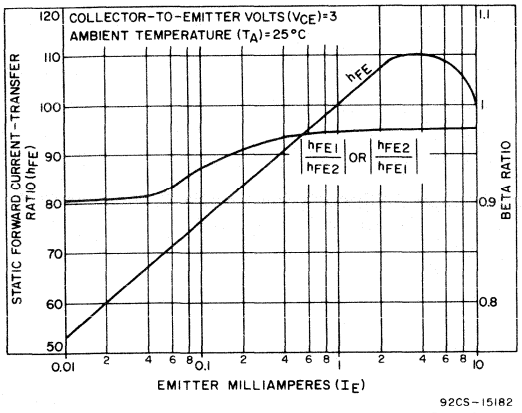


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current.

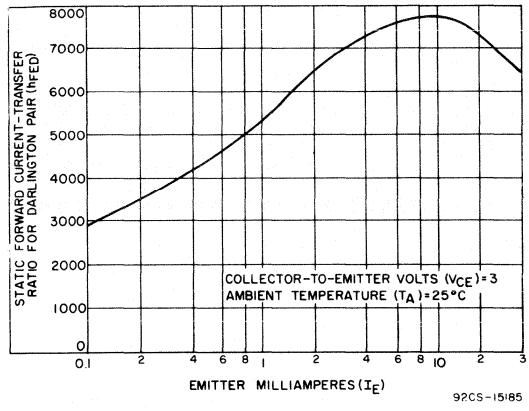


Fig.5 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

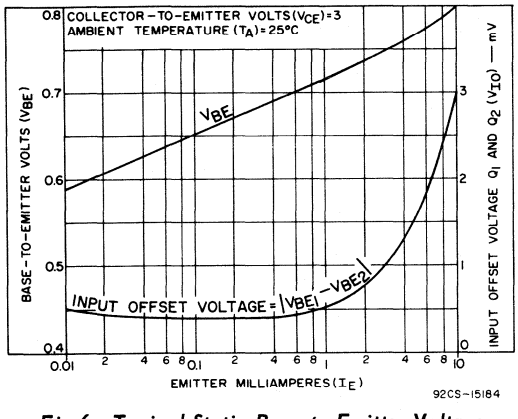


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

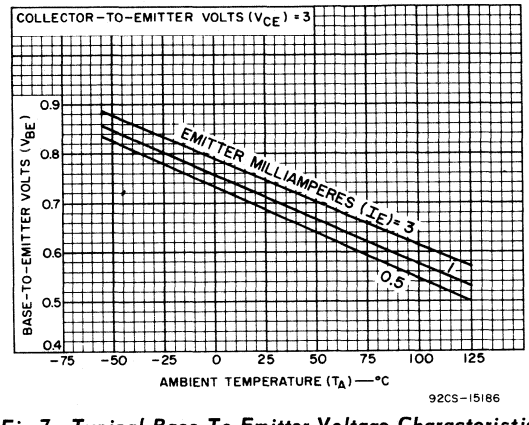


Fig.7 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

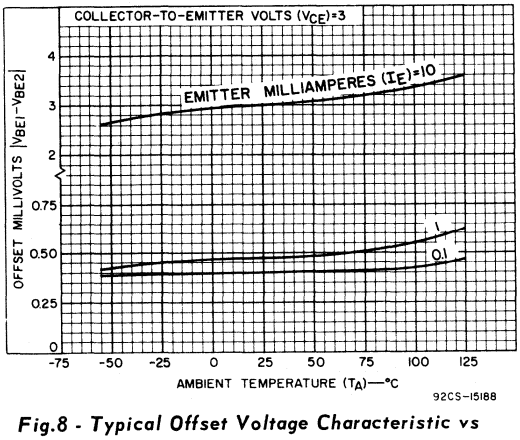


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

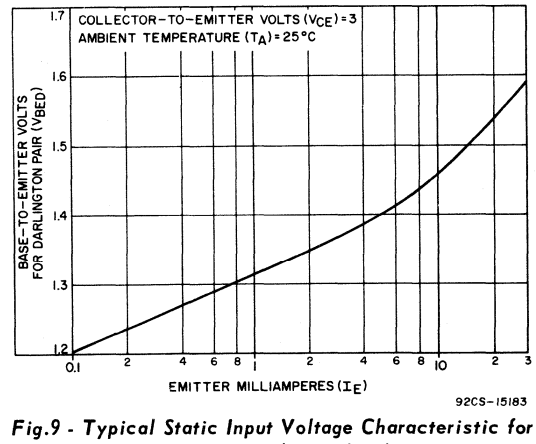


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

CA3018, CA3018A

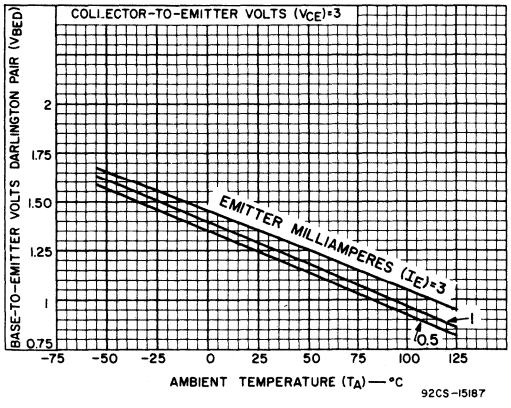


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

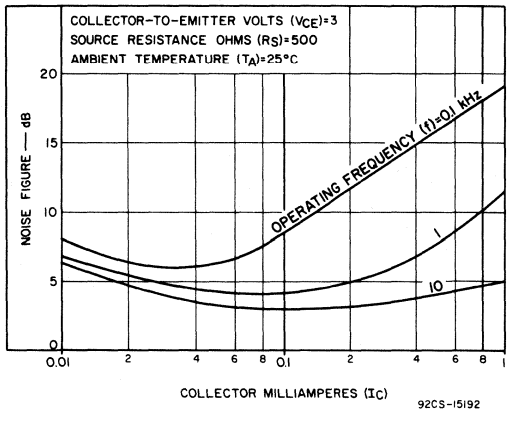


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

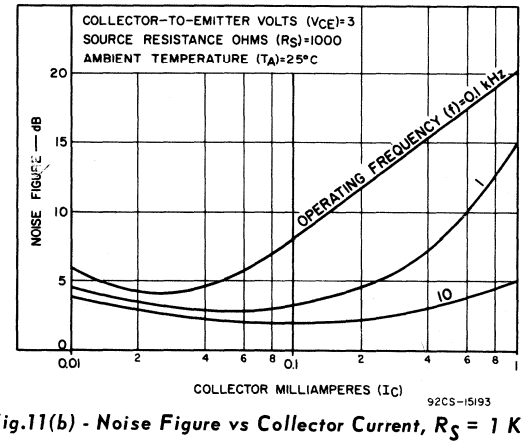


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

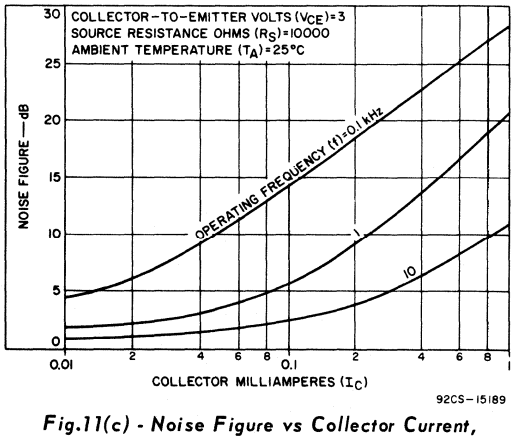


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

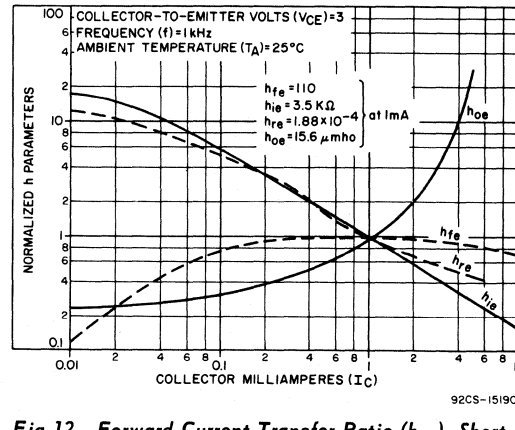


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

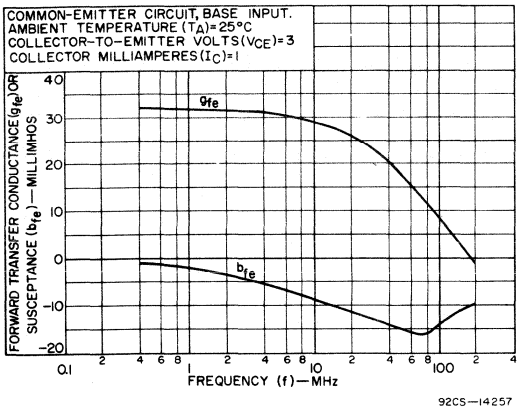


Fig. 13 - Forward Transfer Admittance (Y_{fe})

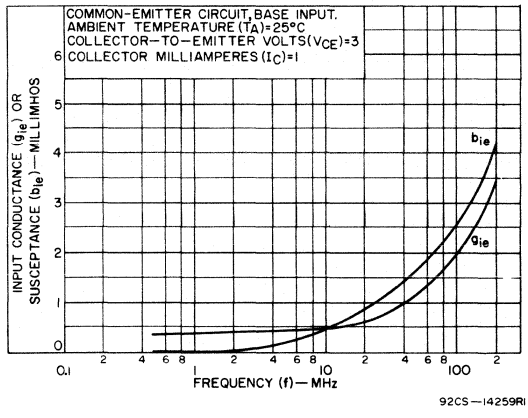


Fig. 14 - Input Admittance (Y_{ie})

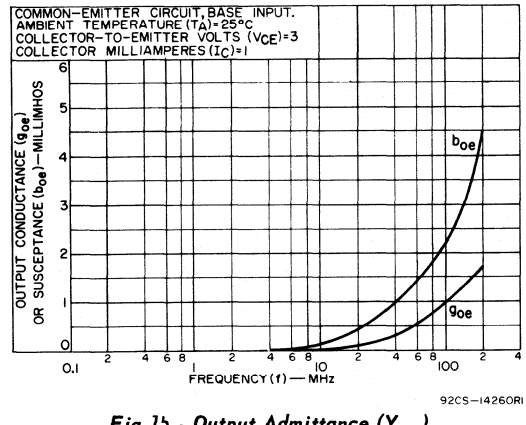


Fig. 15 - Output Admittance (Y_{oe})

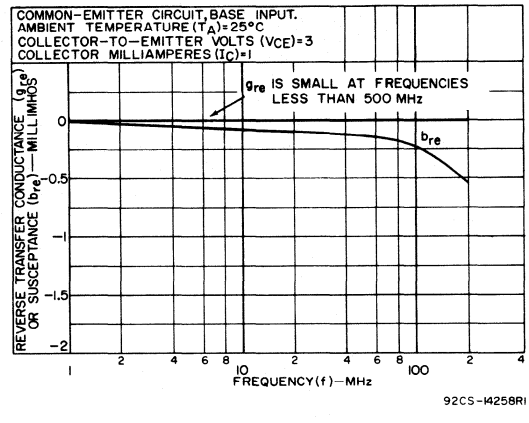


Fig. 16 - Reverse Transfer Admittance (Y_{re})

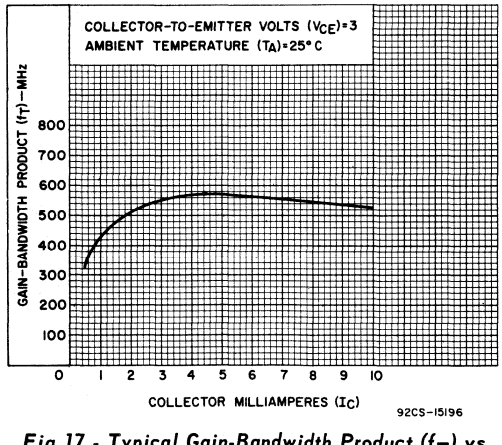


Fig. 17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

CA3019

Ultra-Fast Low-Capacitance Matched Diodes

For Applications in Communications and Switching Systems

Features:

- *Excellent diode match*
- *Low leakage current*
- *Low pedestal voltage when gating*
- *Companion Application Note, ICAN-5299: "Application of the RCA-CA3019 Integrated-Circuit Diode Array"*

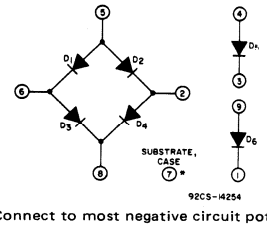
The RCA-CA3019 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Four of the diodes are internally connected as a "quad" and two are independently accessible. The substrate is internally connected to the 10-lead TO-5-style case.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

Applications:

- *Modulator*
- *Mixer*
- *Balanced modulator*
- *Analog switch*
- *Diode gate for chopper-modulator applications*



*Connect to most negative circuit potential.

Fig. 1 — Schematic Diagram.

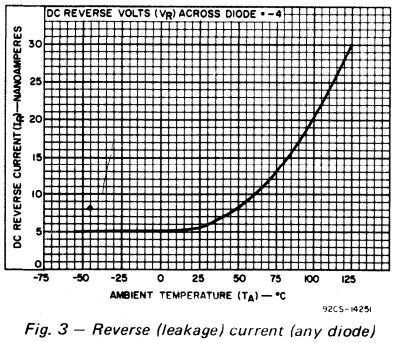


Fig. 3 — Reverse (leakage) current (any diode) as a function of temperature.

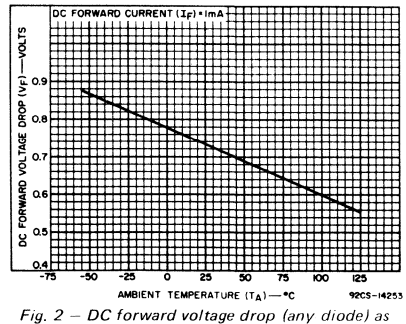


Fig. 2 — DC forward voltage drop (any diode) as a function of temperature.

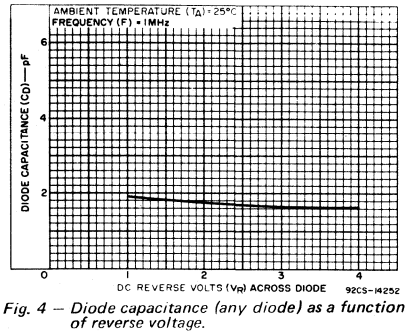


Fig. 4 — Diode capacitance (any diode) as a function of reverse voltage.

File Number **236**

Absolute-Maximum Ratings:

DISSIPATION:
- Any one diode unit . . . 20 max. mW
- Total for device . . . . 120 max. mW

TEMPERATURE RANGE:
- Storage . . . . . −65 to +200 °C
- Operating . . . . . −55 to +125 °C

DC Forward Current, I_F . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

VOLTAGE: See Table

Absolute-Maximum Voltage Limits:

TERM.	VOLTAGE LIMITS		CONDITIONS	
	NEG.	POS.	TERM.	VOLT.
1	−3	+12	7	−6
2	−3	+12	7	−6
3	−3	+12	7	−6
4	−3	+12	7	−6
5	−3	+12	7	−6
6	−3	+12	7	−6
7	−18	0	1,2, 3,6, 8	0
8	−3	+12	7	−6
9	−3	+12	7	−6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

Characteristics Apply for Each Diode Unit, Unless Otherwise Specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3019			Units
		Min.	Typ.	Max.	
DC Forward Voltage Drop	DC Forward Current (I_F) = 1 mA	–	0.73	0.78	V
DC Reverse Breakdown Voltage	DC Reverse Current (I_R) = −10 μA	4	6	–	V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	DC Reverse Current (I_R)= −10 μA	25	80	–	V
DC Reverse (Leakage) Current	DC Reverse Voltage (V_R) =−4 V	–	0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	DC Reverse Voltage (V_R) = −4 V	–	0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	DC Forward Current (I_F)= 1 mA	–	1	5	mV
Single Diode Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = −2V	–	1.8	–	pF
Diode Quad-to-Substrate Capacitance	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = −2 V				
	Terminal 2 or 6 to Terminal 7	–	4.4	–	pF
	Terminal 5 or 8 to Terminal 7	–	2.7	–	pF
Series Gate Switching Pedestal Voltage		–	10	–	mV

CA3039

Diode Array

Six Matched Diodes on a Common Substrate

Ultra-Fast Low-Capacitance Matched Diodes For Applications in Communications and Switching Systems

Features:

- *Excellent reverse recovery time - 1 ns typ.*
- *Matched monolithic construction - V_F matched within 5 mV*
- *Low diode capacitance - C_D = 0.65 pF typical at V_R = -2 V*

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

Applications

- *Balanced modulators or demodulators*
- *Ring modulators*
- *High speed diode gates*
- *Analog switches*

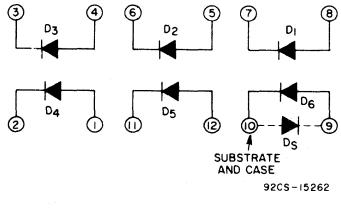


Fig. 1 — Schematic Diagram for CA3039.

File Number **343**

ABSOLUTE MAXIMUM RATINGS at T_A = 25 °C

Dissipation:

Any one diode unit . . . . . 100 mW

Total for device . . . . . 600 mW

For T_A > 55 °C . . . . . derate linearly 5.7 mW/°C

Temperature Range:

Operating . . . . . -55 to +125 °C

Storage . . . . . -65 to +150°C

Peak Inverse Voltage, PIV for: D_1-D_5 . . . 5 V

D_6 . . . . . 0.5 V

Peak Diode-to-Substrate Voltage, V_{DI}

for D_1-D_5 (term. 1,4,5,8 or 12 to term. 10) +20, -1 V

DC Forward Current, I_F . . . . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

LEAD TEMPERATURE (During Soldering)

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)

from case for 10 seconds max. . . . . + 265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARAC-TERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = -4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = -10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	-1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = -2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

CA3039

TYPICAL CHARACTERISTICS

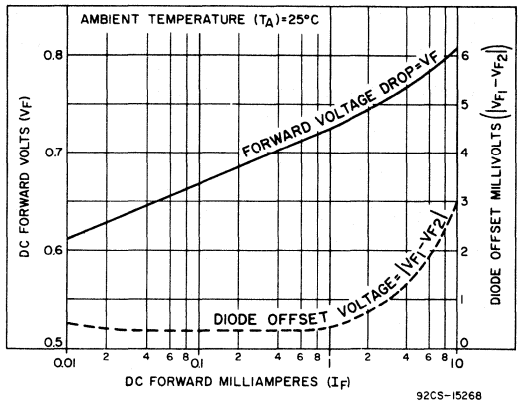


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

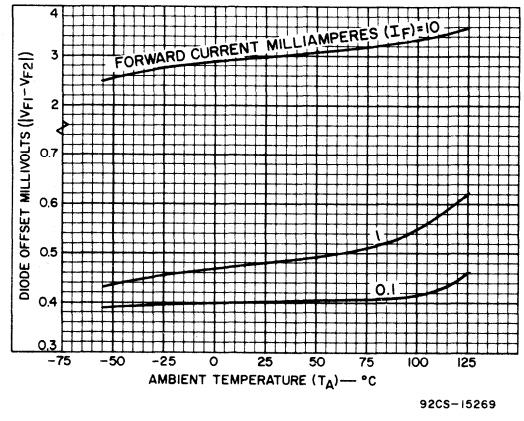


Fig. 5 - Diode offset voltage (any diode) vs temperature

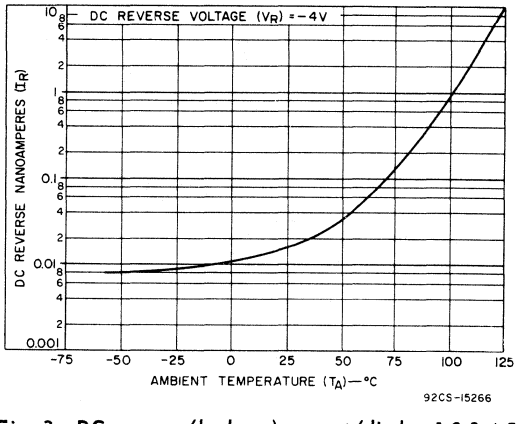


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

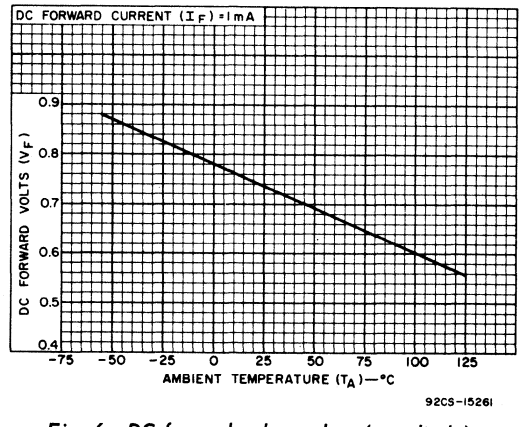


Fig. 6 - DC forward voltage drop (any diode) vs temperature

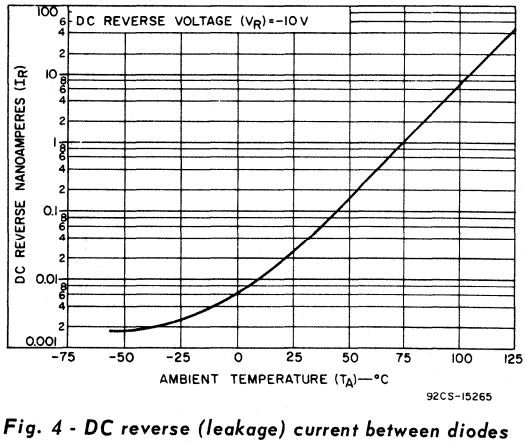


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

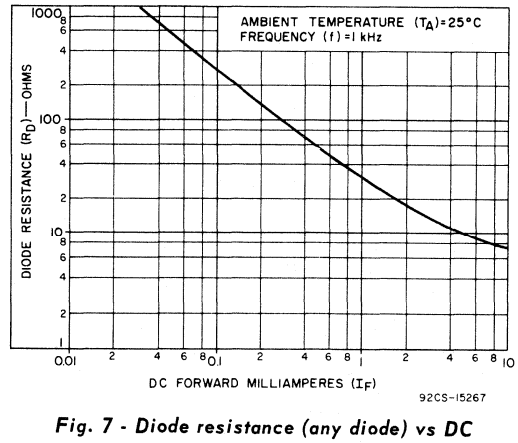


Fig. 7 - Diode resistance (any diode) vs DC forward current

TYPICAL CHARACTERISTICS

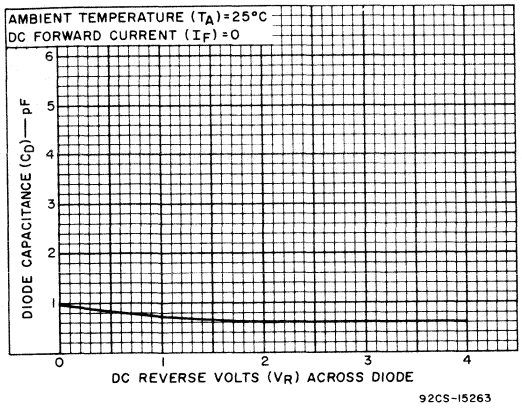


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

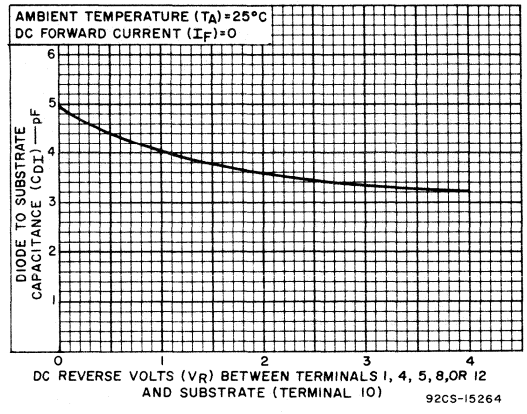


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

CA3045, CA3046

General-Purpose N-P-N Transistor Arrays

Three Isolated Transistors and One Differentially-Connected Transistor Pair

For Low-Power Applications at Frequencies from DC through the VHF Range

Features

- **Two matched pairs of transistors**
  V_{BE} matched ± 5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- **5 general purpose monolithic transistors**
- **Operation from DC to 120 MHz**
- **Wide operating current range**
- **Low noise figure - - 3.2 dB typ. at 1 kHz**
- **Full military temperature range for CA3045 -55 to +125°C**

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

Applications

- **General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

The CA3045 and CA3046 are available in the packages shown below

Package	Suffix Letter	CA3045	CA3046
14-Lead Dual-In-Line Plastic	E		√
14-Lead Dual-In-Line Ceramic	D	√	
14-Line Dual-In-Line Frit-Seal Ceramic	F	√	
Chip	H	√	

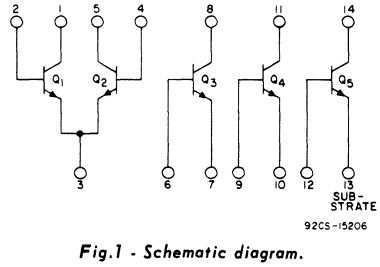


Fig.1 - Schematic diagram.

File Number **341**

CA3045, CA3046

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C	CA3045		CA3046, CA3045F		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Collector Current	50	–	50	–	mA
Temperature Range:					
Operating	−55 to +125		−55 to +125		°C
Storage	−65 to +150		−65 to +150		°C
Lead Temperature (During Soldering):					
At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max.	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V	-
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-	4
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-	
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-	
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA	5
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V	6
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	−1.9	-	mV/°C	7
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	1.1	-	μV/°C	8

CA3045, CA3046

ELECTRICAL CHARACTERISTICS (Cont'd.)

DYNAMIC CHARACTERISTICS							
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB	9(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-	10
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ	
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-	11
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-	12
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-	13
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-	14
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-	15
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF	-

STATIC CHARACTERISTICS

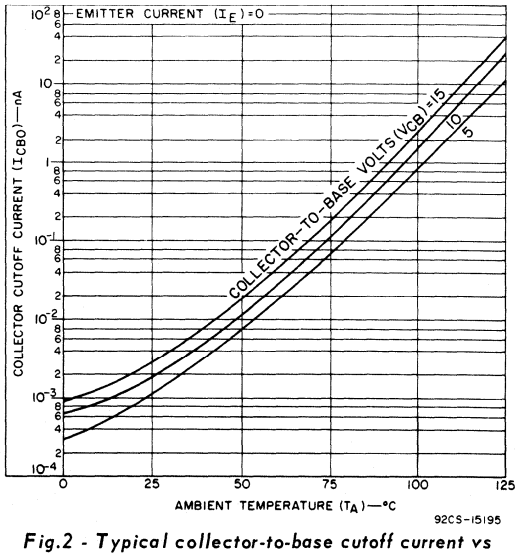


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

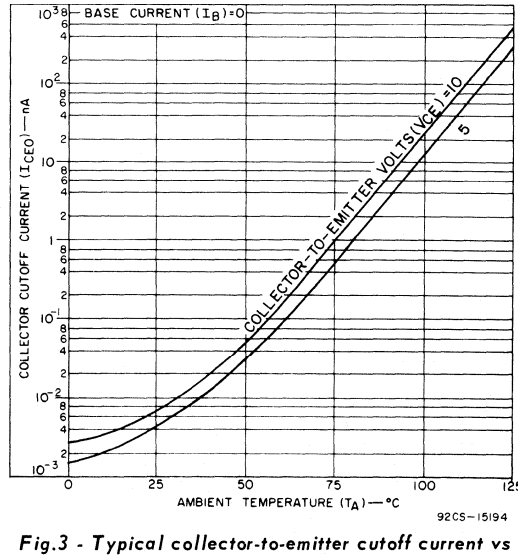


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC CHARACTERISTICS

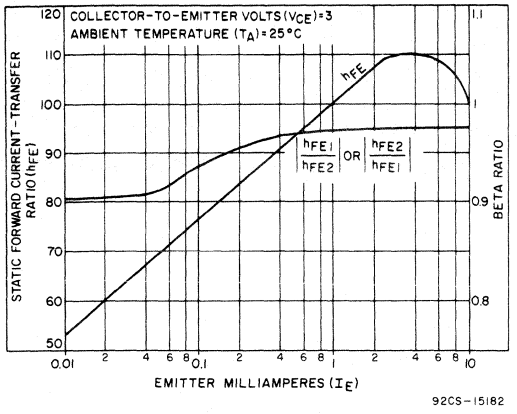


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

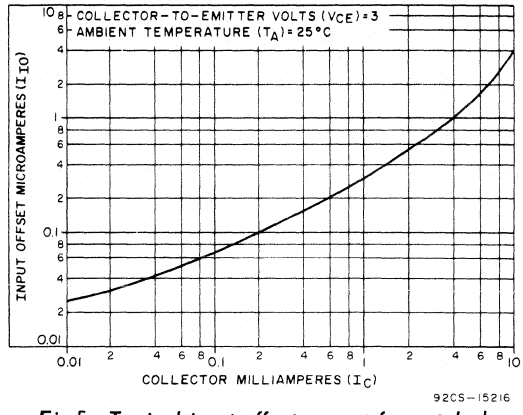


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

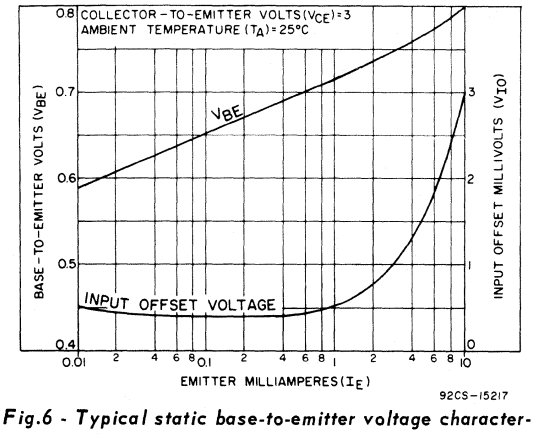


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

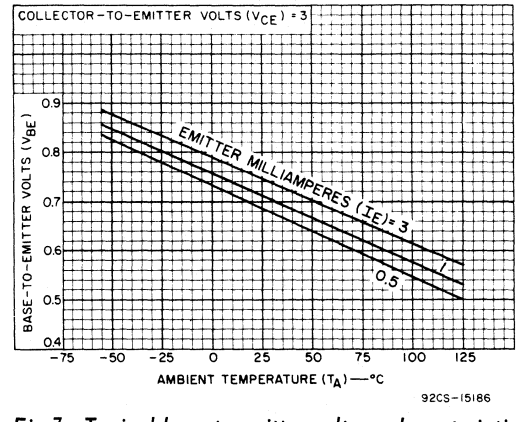


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

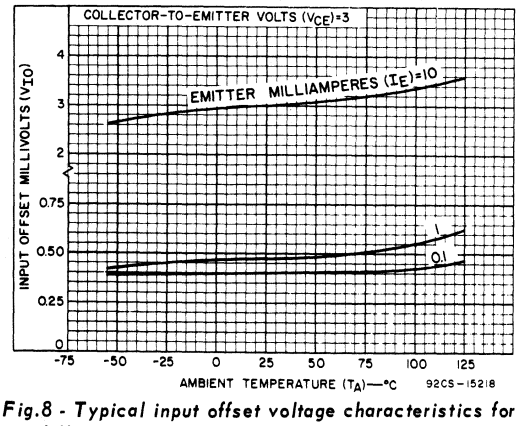


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

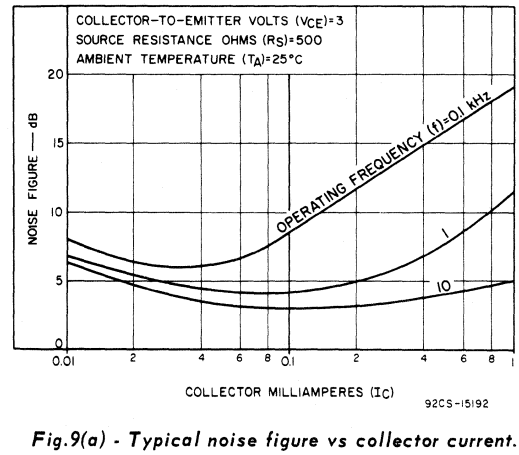


Fig.9(a) - Typical noise figure vs collector current.

CA3045, CA3046

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

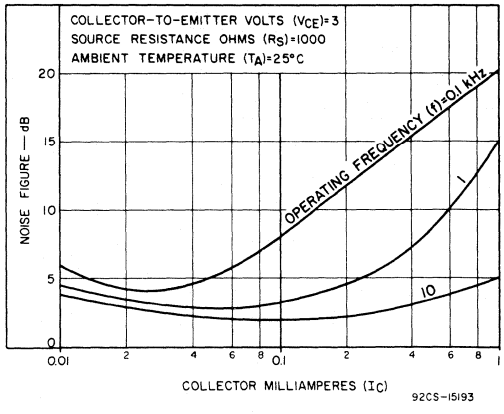


Fig.9(b) - Typical noise figure vs collector current.

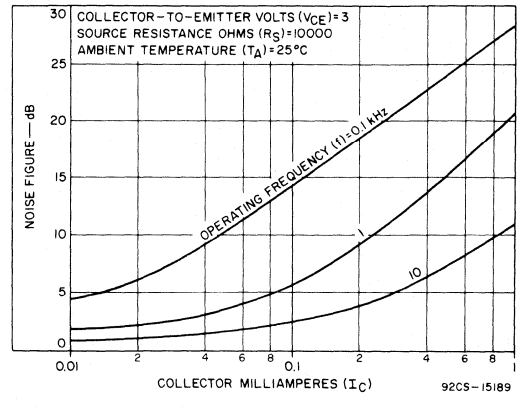


Fig.9(c) - Typical noise figure vs collector current.

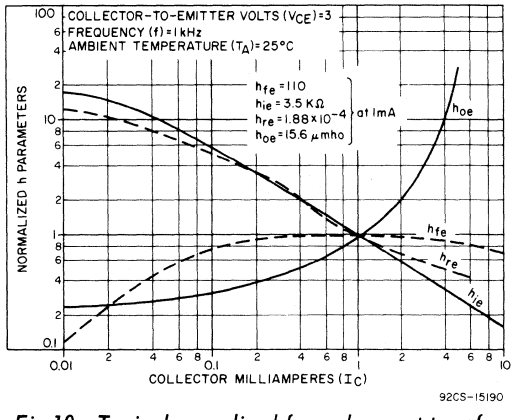


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

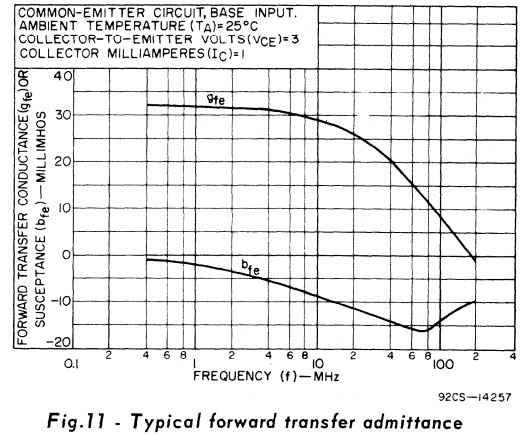


Fig.11 - Typical forward transfer admittance vs frequency.

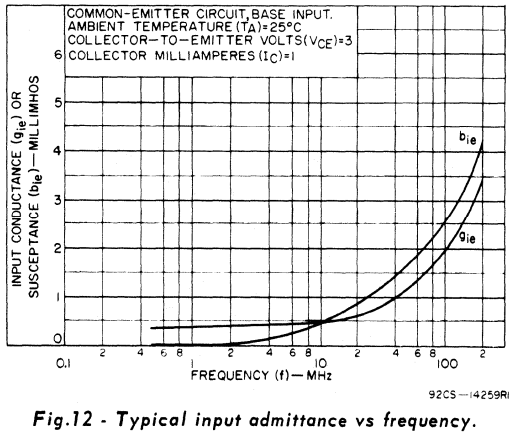


Fig.12 - Typical input admittance vs frequency.

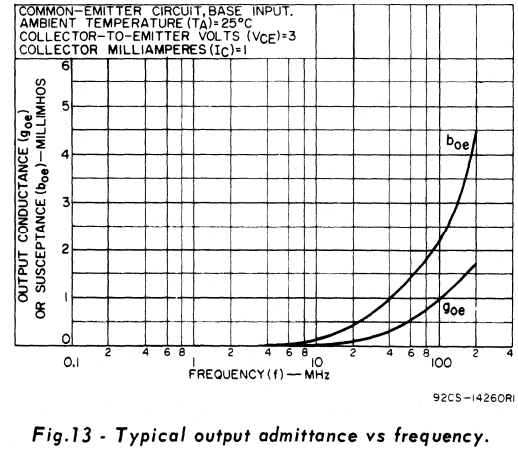


Fig.13 - Typical output admittance vs frequency.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

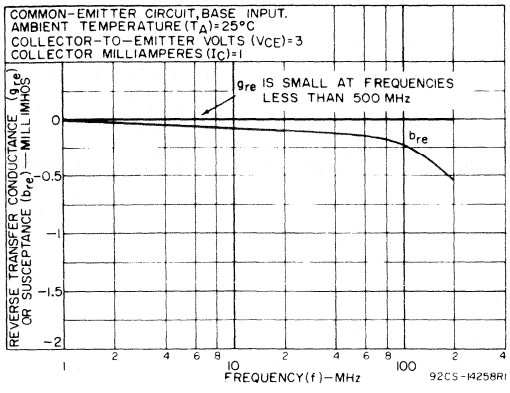


Fig.14 - Typical reverse transfer admittance vs frequency.

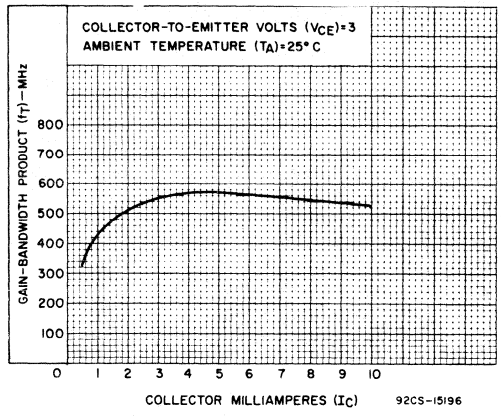


Fig.15 - Typical gain-bandwidth product vs collector current.

CA3083

General-Purpose High-Current N-P-N Transistor Array

Features:

- *High I_C: 100 mA max.*
- *Low V_{CEsat} (at 50 mA): 0.7V max.*
- *Matched pair (Q1 and Q2) -*
  V_{IO} (V_{BE} matched): ± 5 mV max.
  I_{IO} (at 1 mA): 2.5 μA max.
- *5 independent transistors plus separate substrate connection*

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line frit-seal ceramic package. The CA3083 is also available in chip form.

Applications:

- *Signal processing and switching systems operating from DC to VHF*
- *Lamp and relay driver*
- *Differential amplifier*
- *Temperature-compensated amplifier*
- *Thyristor firing*
- *See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications*

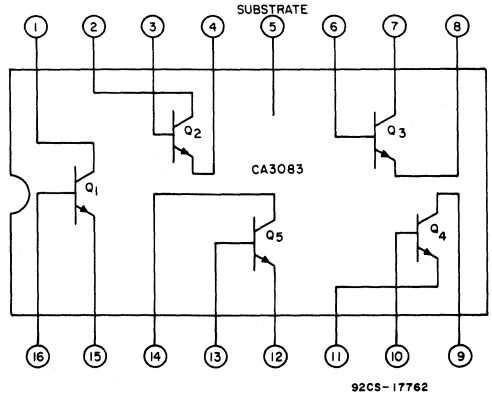


Fig. 1 — Functional diagram of the CA3083.

File Number **481**

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to +150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA I_C = 50mA	2	40 40	76 75	– –	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 10 mA		–	450	–	MHz
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	8	–	0.7	2.5	μA

CA3083

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

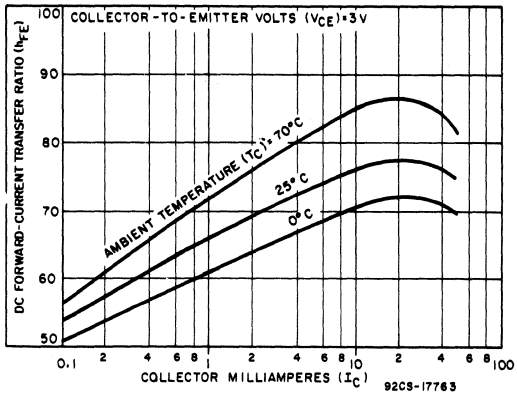


Fig.2 – h_{FE} vs I_C

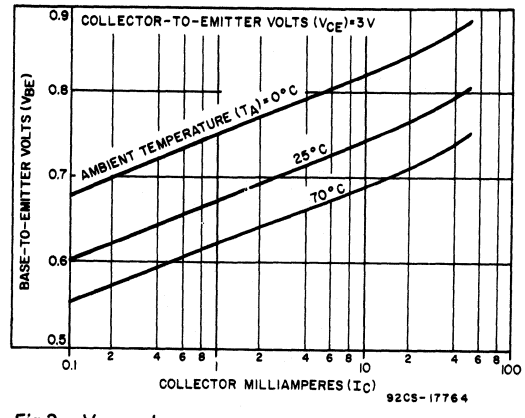


Fig.3 – V_{BE} vs I_C

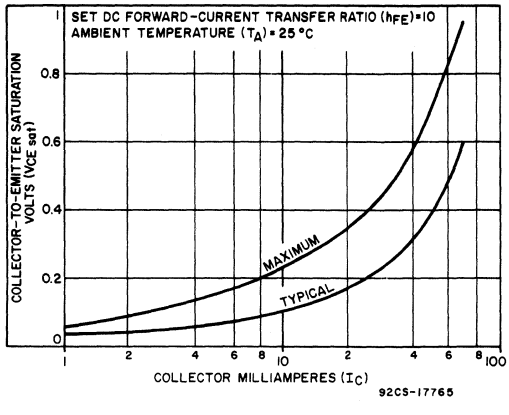


Fig.4 – V_{CEsat} vs I_C at 25°C

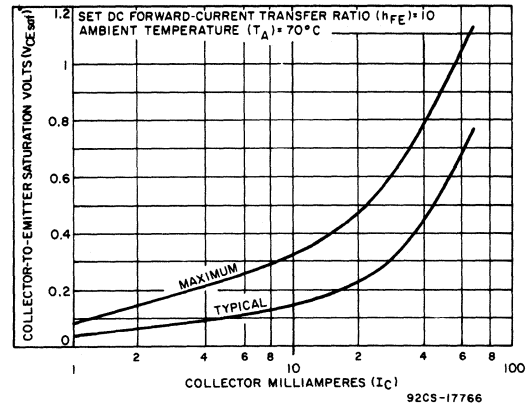


Fig.5 – V_{CEsat} vs I_C at 70°C

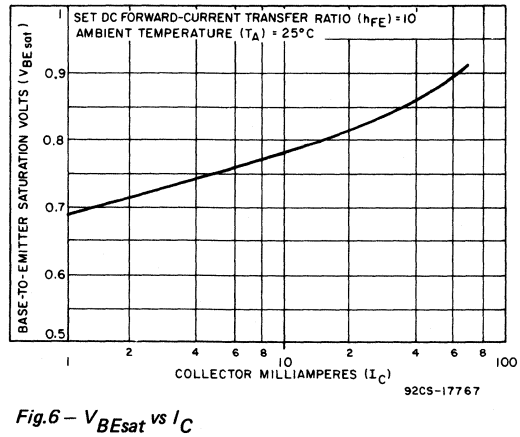


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

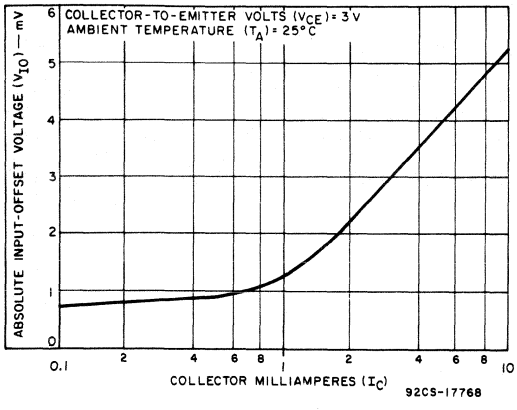


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

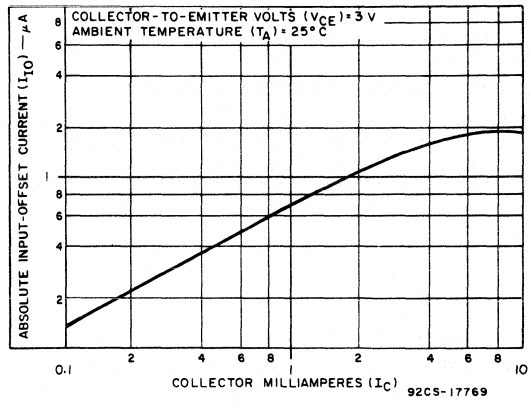


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

CA3086

General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially–Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

Applications

- **General-purpose use in signal processing systems operating in the DC to 120-MHz range**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

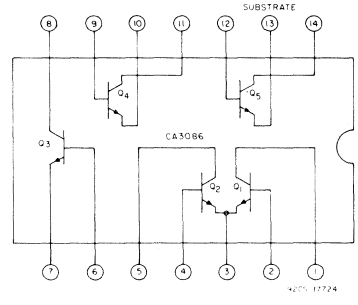


Fig.1 – Functional diagram of the CA3086.

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to + 125	°C
Storage	−65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

File Number **483**

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS
			Typ. Characteristic Curves Fig. No.	Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

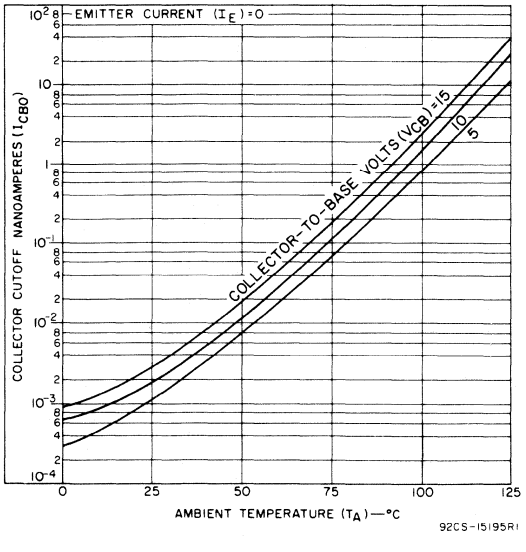


Fig.2– I_{CBO} vs T_A.

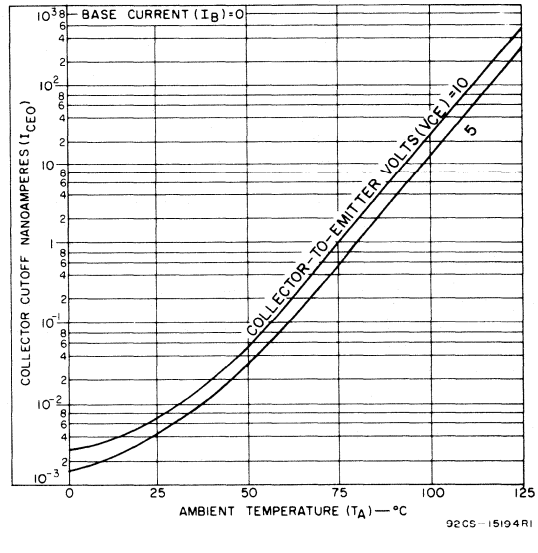


Fig.3– I_{CEO} vs T_A.

CA3086

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		—	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		—	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	—
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	—
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	Y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	Y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}			11	See Curve	—
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		—	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		—	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

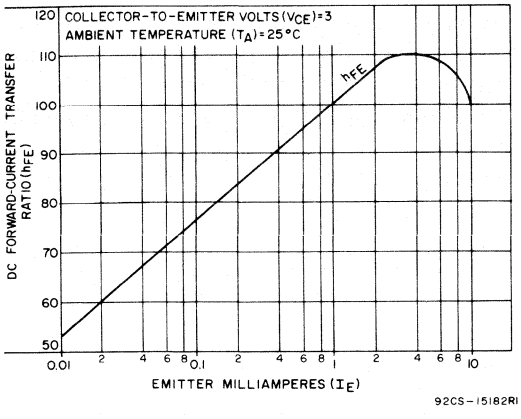


Fig.4– h_{FE} vs I_E.

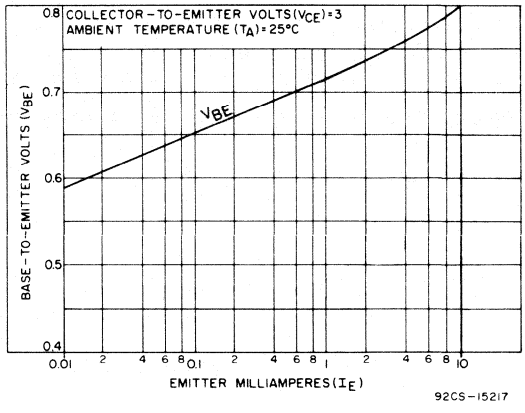


Fig.5– V_{BE} vs I_E.

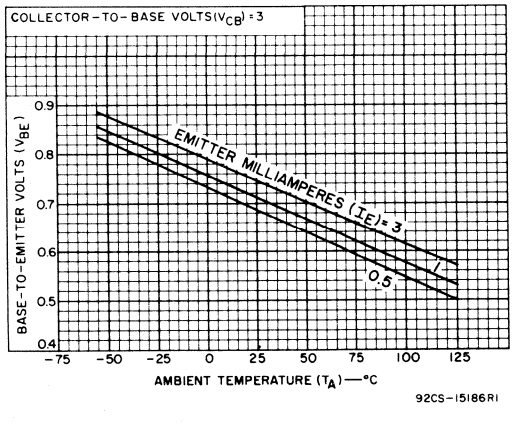


Fig.6– V_{BE} vs T_A

CA3086

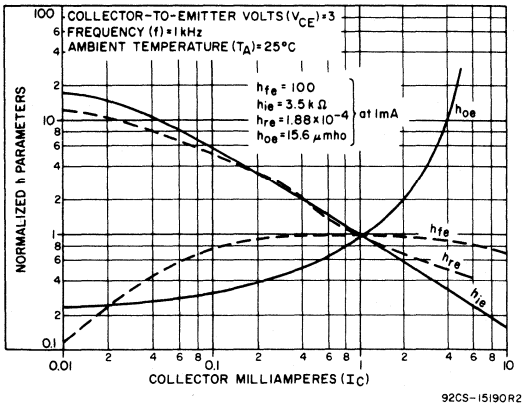


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

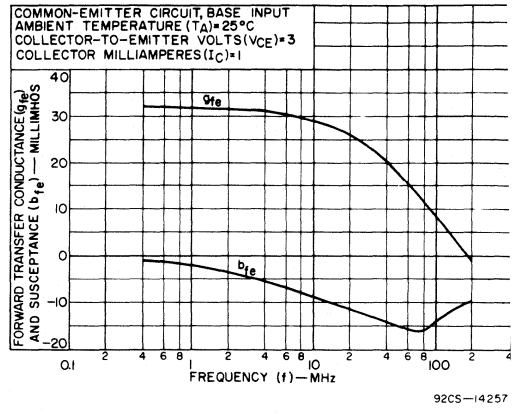


Fig.8 – y_{fe} vs f.

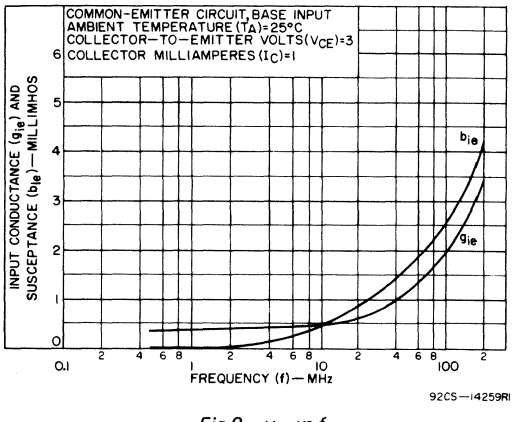


Fig.9 – y_{ie} vs f.

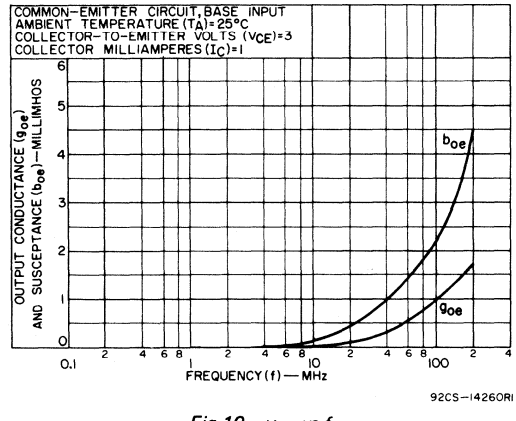


Fig.10 – y_{oe} vs f.

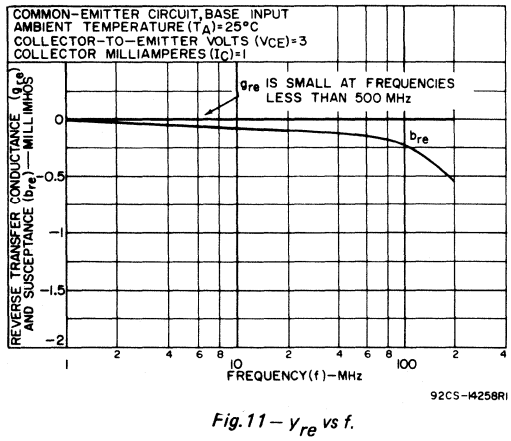


Fig.11 – y_{re} vs f.

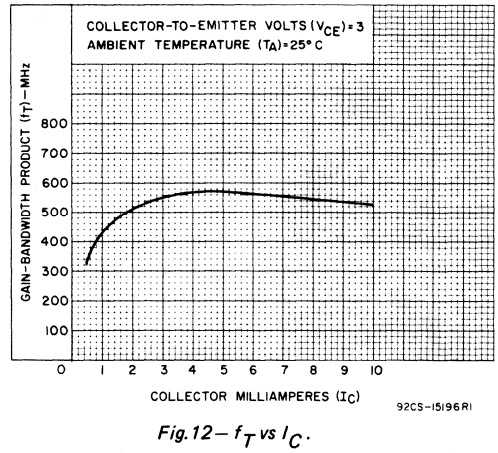


Fig.12 – f_T vs I_C.

CA3096, CA3096A, CA3096C

N-P-N/P-N-P Transistor Array

Five-Independent Transistors: Three n-p-n and Two p-n-p

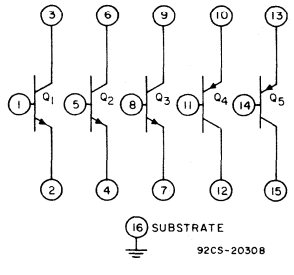
Applications:

- *Differential Amplifiers*
- *DC Amplifiers*
- *Sense Amplifiers*
- *Level Shifters*
- *Timers*
- *Lamp and Relay Drivers*
- *Thyristor Firing Circuits*
- *Temperature-Compensated Amplifiers*
- *Operational Amplifiers*

RCA-CA3096CE, CA3096E, and CA3096AE are general-purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE, CA3096E, and CA3096CE are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE}(SAT)$. The CA3096CE is a relaxed version of the CA3096E.

The CA3096CE, CA3096E, and CA3096AE are supplied in 16-lead dual-in-line plastic packages. (E-suffix). The CA3096 is also available in chip form. (H suffix).



Schematic Diagram

CA3096AE, CA3096E, CA3096CE
ESSENTIAL DIFFERENCES

CHARACTERISTIC		CA3096AE	CA3096E	CA3096CE
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	−40	−40	−24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	−40	−40	−24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-150	20-150	15-200
h_{FE} @ 100 μA	p-n-p	40-200	40-200	30-300
I_{CBO} (nA) Max.	n-p-n	40	100	100
	p-n-p	−40	−100	−100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	−100	−1000	−1000
$V_{CE}(SAT)$ (V) Max.	p-n-p	0.5	0.7	0.7
$\lvert V_{IO}\rvert$ (mV) Max.	n-p-n	5	–	–
	p-n-p	5	–	–
$\lvert I_{IO}\rvert$ (μA) Max.	n-p-n	0.6	–	–
	p-n-p	0.25	–	–

File Number **595**

CA3096, CA3096A, CA3096C

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}:			
CA3096AE, CA3096E	35	−40	V
CA3096CE	24	−24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}:			
CA3096AE, CA3096E	45	−40	V
CA3096CE	30	−24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}:			
CA3096AE, CA3096E	45	–	V
CA3096CE	30	–	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO}:			
CA3096AE, CA3096E	–	−40	V
CA3096CE	–	−24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}:			
CA3096E, CA3096E	6	−40	V
CA3096CE	6	−24	V
COLLECTOR CURRENT, I_C (All Types)	50	−10	mA
POWER DISSIPATION, P_D:			
Up to $T_A = 55°C$:			
Device (Total)	750		mW
Each Transistor	200		mW
Above $T_A = 55°C$ derate linearly at	6.67		mW/°C
AMBIENT-TEMPERATURE RANGE, T_A:			
Operating	−55 to +125°C		
Storage	−65 to +150°C		
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C		

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	–	0.001	40	–	0.001	100	–	0.001	100	nA
I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	–	0.006	100	–	0.006	1000	–	0.006	1000	nA
$V_{(BR)CEO}$	$I_C = 1$ mA, $I_B = 0$	35	50	–	35	50	–	24	35	–	V
$V_{(BR)CBO}$	$I_C = 10\,\mu$A, $I_E = 0$	45	100	–	45	100	–	30	80	–	V
$V_{(BR)CIO}$	$I_{CI} = 10\,\mu$A, $I_B = I_E = 0$	45	100	–	45	100	–	30	80	–	V
$V_{(BR)EBO}$	$I_E = 10\,\mu$A, $I_C = 0$	6	8	–	6	8	–	6	8	–	V
V_Z	$I_Z = 10\,\mu$A	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	$I_C = 10$ mA, $I_B = 1$ mA	–	0.24	0.5	–	0.24	0.7	–	0.24	0.7	V
V_{BE}	$I_C = 1$ mA, $V_{CE} = 5$ V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = 1$ mA, $V_{CE} = 5$ V	–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (Cont'd)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	$V_{CB} = -10$ V, $I_E = 0$	–	−0.006	−40	–	−0.06	−100	–	−0.06	−100	nA
I_{CEO}	$V_{CE} = -10$V, $I_B = 0$	–	−0.12	−100	–	−0.12	−1000	–	−0.12	−1000	nA
$V_{(BR)CEO}$	$I_C = -100\,\mu$A, $I_B = 0$	−40	−75	–	−40	−75	–	−24	−30	–	V
$V_{(BR)CBO}$	$I_C = -10\,\mu$A, $I_E = 0$	−40	−80	–	−40	−80	–	−24	−60	–	V
$V_{(BR)EBO}$	$I_E = -10\,\mu$A, $I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{(BR)EIO}$	$I_{EI} = 10\,\mu$A, $I_B = I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{CE(SAT)}$	$I_C = -1$ mA, $I_B = -100\,\mu$A	–	−0.16	−0.4	–	−0.16	−0.4	–	−0.16	−0.4	V
V_{BE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	V
h_{FE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	40	85	250	40	85	250	30	85	300	
	$I_C = -1$ mA, $V_{CE} = -5$ V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	–	2.2	–	–	2.2	–	–	2.2	–	mV/°C

I_{CBO} Collector-Cutoff Current

I_{CEO} Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage

$V_{CE(SAT)}$ Collector-to-Emitter Saturation Voltage

V_{BE} Base-to-Emitter Voltage

h_{FE} DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

CA3096, CA3096A, CA3096C

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (CA3096AE Only)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		CA3096AE			
		Min.	Typ.	Max.	
For Transistors Q1 and Q2 (as a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	V_{CE} = 5 V, I_C = 1 mA	–	0.3	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	1.1	–	μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	V_{CE} = −5 V, I_C = −100 μA, R_S = 0	–	0.15	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	0.54	–	μV/°C

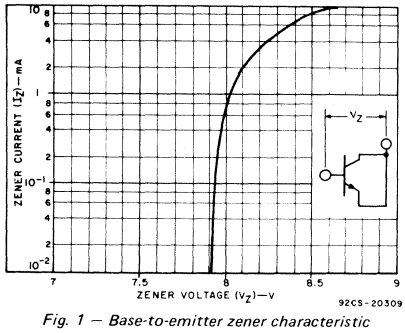


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

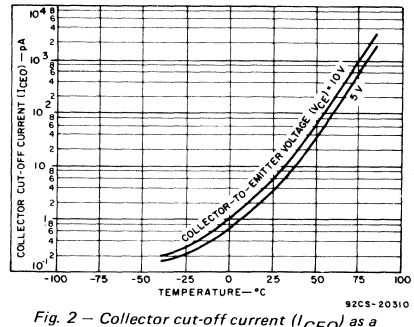


Fig. 2 – Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

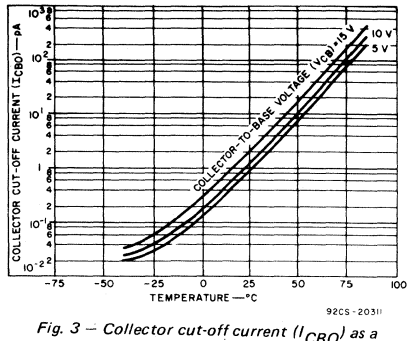


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

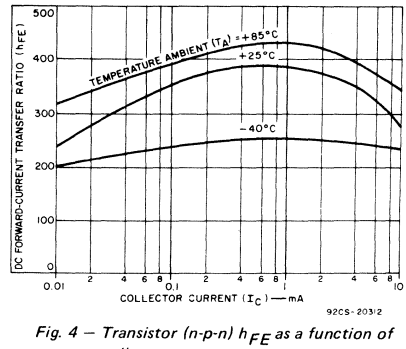


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance, R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance, R_o		80	kΩ
Admittance Characteristics:	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA		
Forward Transfer Admittance, $\frac{g_{fe}}{y_{fe}\ b_{fe}}$		7.5 −j13	mmho
Input Admittance, $\frac{g_{ie}}{y_{ie}\ b_{ie}}$		2.2 j3.1	mmho
Output Admittance, $\frac{g_{oe}}{y_{oe}\ b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
	V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance, R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance, R_o		680	kΩ
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance, C_{BI}	V_{BI} = 3 V	3.05	pF

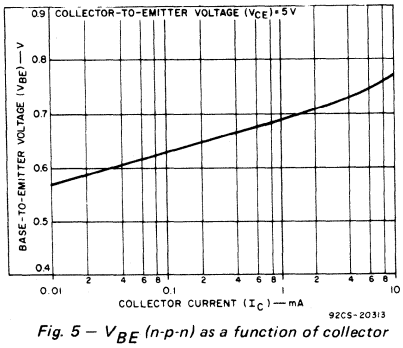


Fig. 5 — V_{BE} (n-p-n) as a function of collector current.

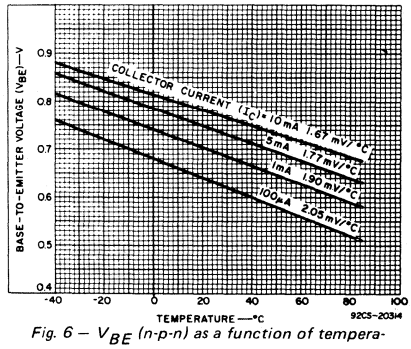


Fig. 6 — V_{BE} (n-p-n) as a function of temperature.

CA3096, CA3096A, CA3096C

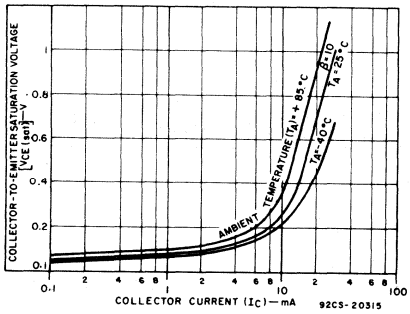


Fig. 7 – $V_{CE}(SAT)$ (n-p-n) as a function of collector current.

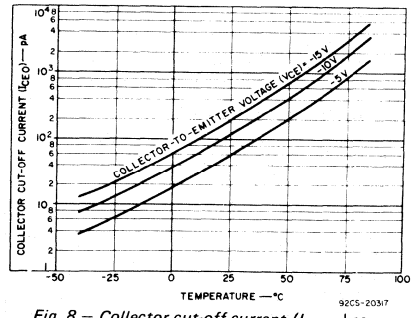


Fig. 8 – Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

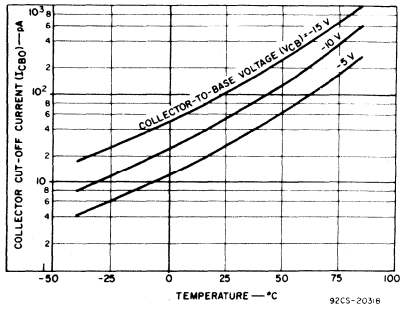


Fig. 9 – Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

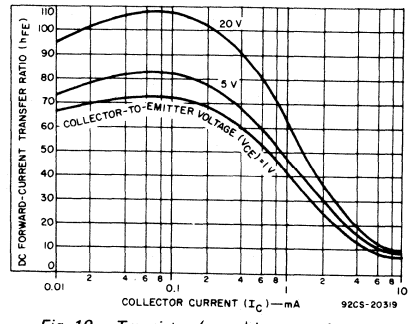


Fig. 10 – Transistor (p-n-p) h_{FE} as a function of collector current.

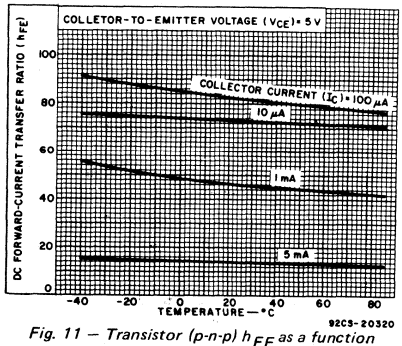


Fig. 11 – Transistor (p-n-p) h_{FE} as a function of temperature.

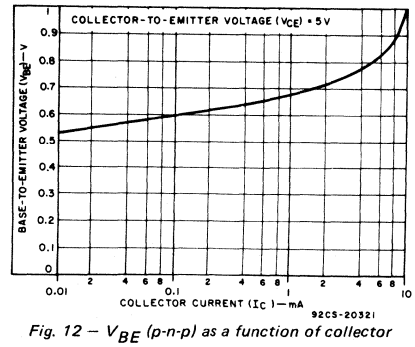


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

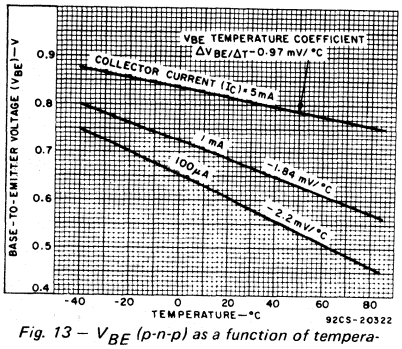


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

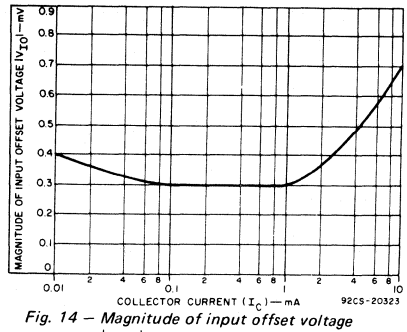


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

CA3096, CA3096A, CA3096C

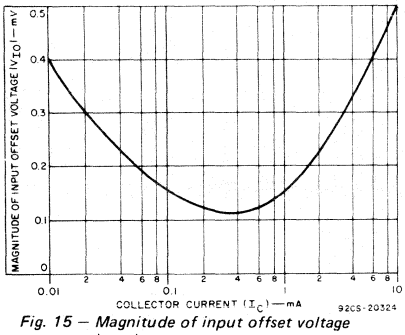


Fig. 15 — Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor Q_4–Q_5

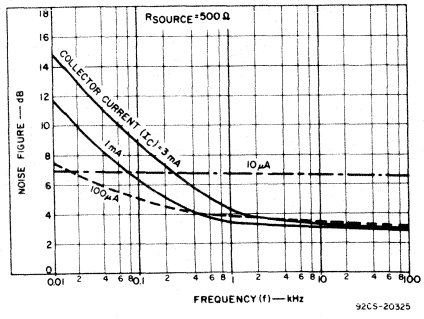


Fig. 16 — Noise figure as a function of frequency for n-p-n transistors.

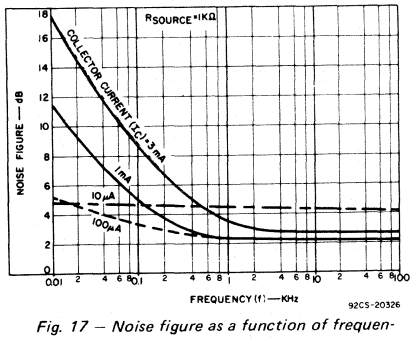


Fig. 17 — Noise figure as a function of frequency for n-p-n transistors.

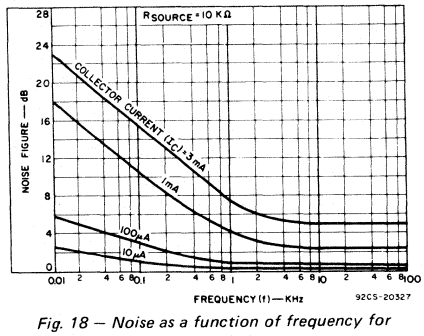


Fig. 18 — Noise as a function of frequency for n-p-n transistors.

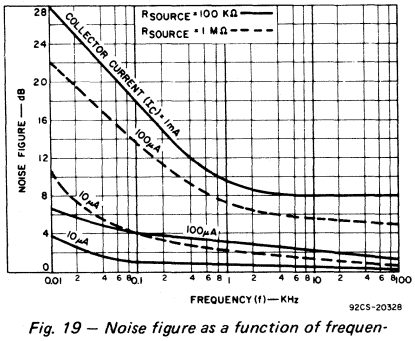


Fig. 19 — Noise figure as a function of frequency for n-p-n transistors.

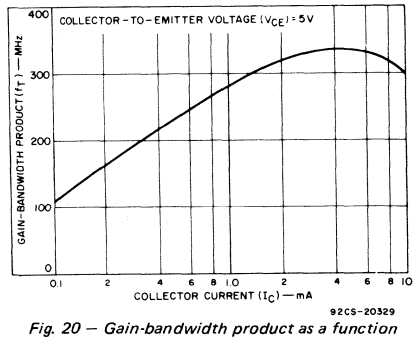


Fig. 20 — Gain-bandwidth product as a function of collector current (n-p-n).

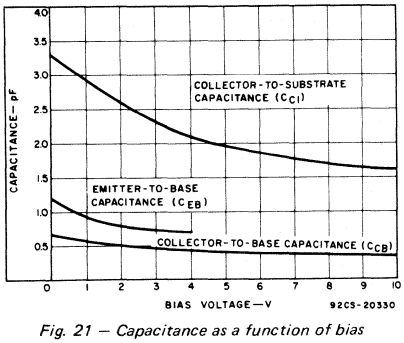


Fig. 21 — Capacitance as a function of bias voltage (n-p-n).

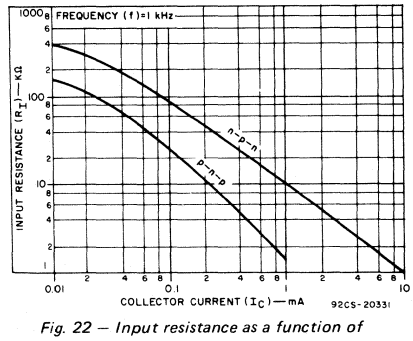


Fig. 22 — Input resistance as a function of collector current.

CA3096, CA3096A, CA3096C

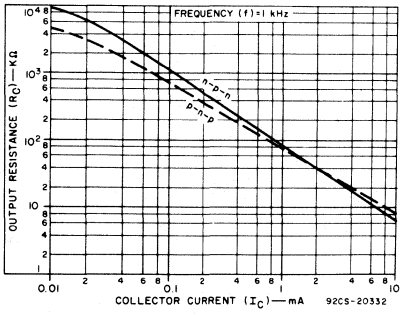


Fig. 23 – Output resistance as a function of collector current.

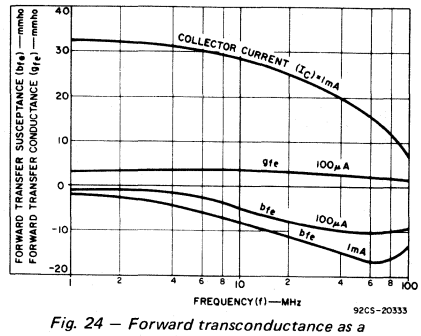


Fig. 24 – Forward transconductance as a function of frequency.

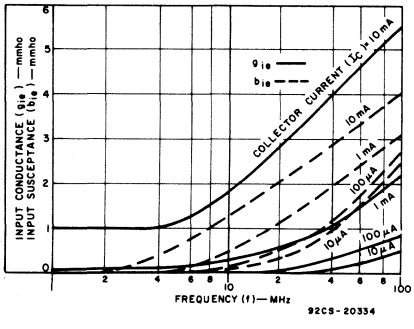


Fig. 25 – Input admittance as a function of frequency.

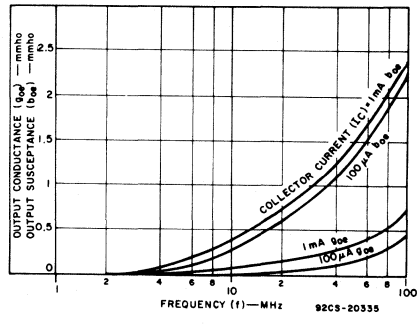


Fig. 26 – Output admittance as a function of frequency.

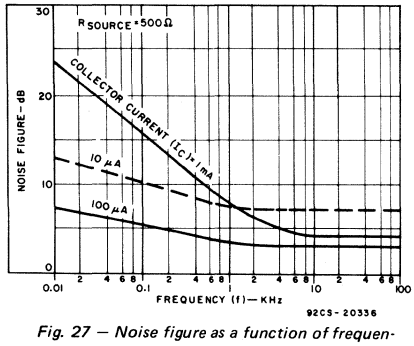


Fig. 27 – Noise figure as a function of frequency (p-n-p).

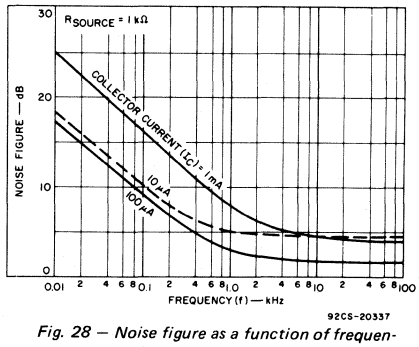


Fig. 28 – Noise figure as a function of frequency (p-n-p).

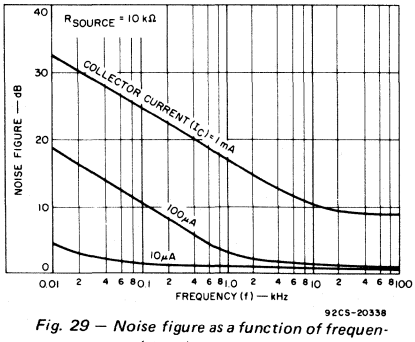


Fig. 29 – Noise figure as a function of frequency (p-n-p).

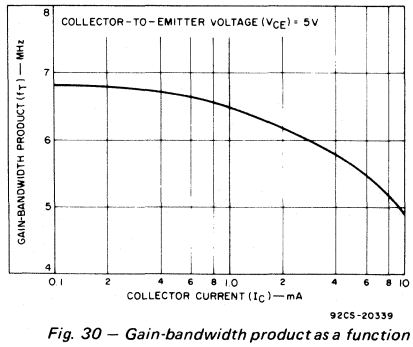


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

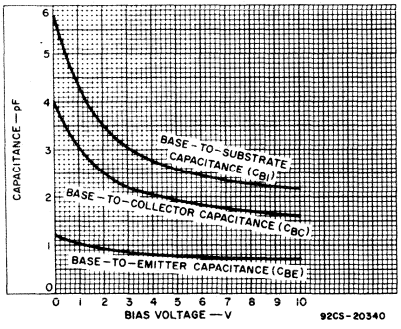


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

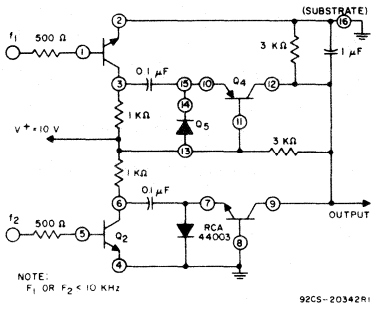


Fig. 32 – Frequency comparator using CA3096E.

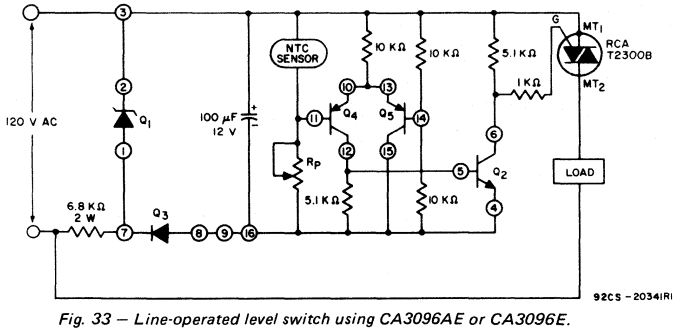


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

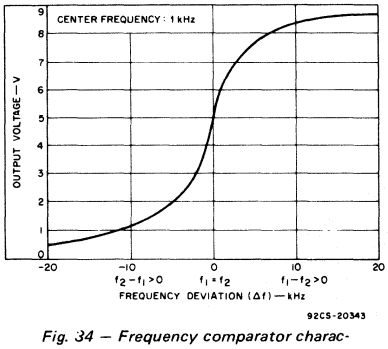


Fig. 34 – Frequency comparator characteristics.

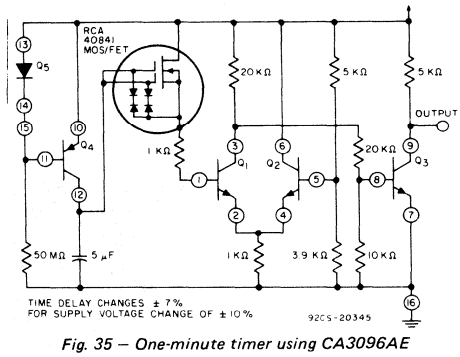


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

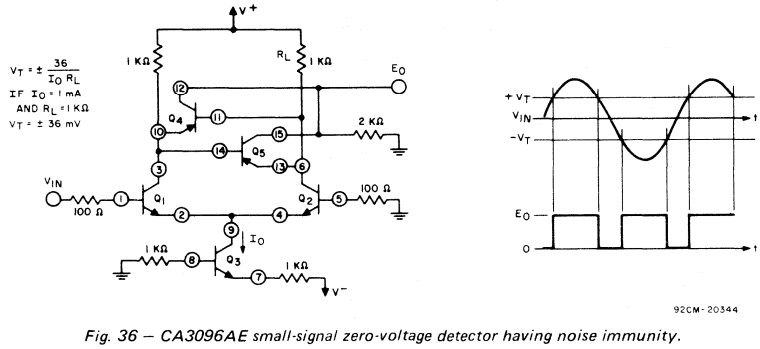


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

CA3096, CA3096A, CA3096C

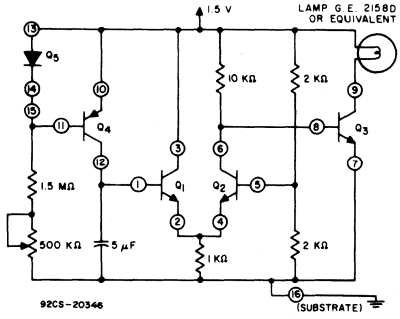


Fig. 37 – Ten-second timer operated form 1.5-volt supply using CA3096E.

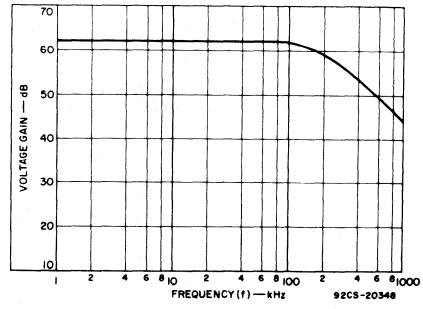
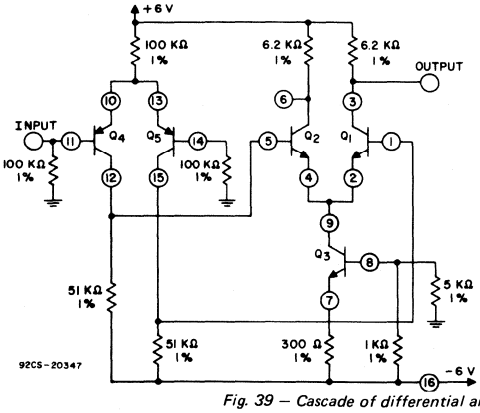


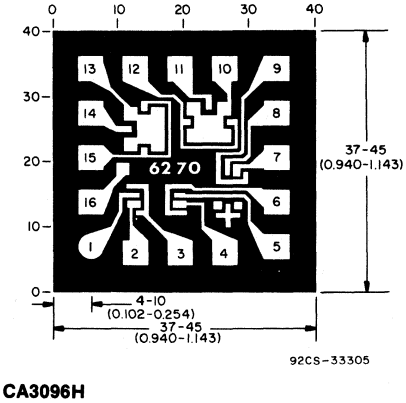
Fig. 38 – Gain-frequency characteristics.



Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V.
3. Low bias current: $<1\ \mu A$.

Fig. 39 – Cascade of differential amplifiers using CA3096AE.



CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

CA3097

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

Features:

- *Complete isolation between elements*
- *n-p-n transistor - V_{CEO} = 30 V (min.) I_C = 100 mA (max.)*
- *p-n-p/n-p-n transistor pair - beta ≥ 8000 (typ.) @ I_C = 10 mA, individual p-n-p, n-p-n, or transistor pair operation*
- *Programmable unijunction transistor [PUT] - peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ± 30 V*
- *(PUT) Extremely long RC time constants with low value of external capacitor*
- *Sensitive-gate silicon controlled rectifier (SCR) - 150 mA forward current (max.)*
- *Zener-diode impedance (Z_Z) = 15Ω (typ.) at 10 mA*

RCA-CA3097E* Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of −55 to +125° C.

*Formerly Dev. No. TA6281.

Applications:

- *Timers*
- *Light dimmers/motor controls*
- *Oscillators*
- *"One-shot" multivibrators*
- *Voltage regulators*
- *Comparators, Schmitt triggers*
- *Constant-current sources*
- *Amplifiers*
- *Logic circuits*
- *SCR triggering*
- *Pulse circuits*

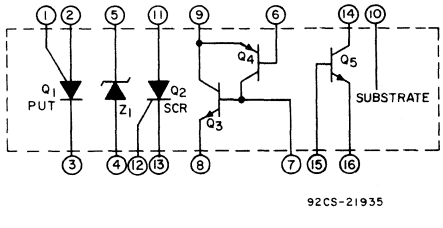


Fig. 1 — Schematic diagram of CA3097E.

File Number **633**

CA3097

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE(SAT)}$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE(SAT)}$	I_C = -1mA, I_B = –100μA	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

CA3097

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S, = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISE TIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	– –	V

* $V_T = V_P - V_S$ (Fig. 22)

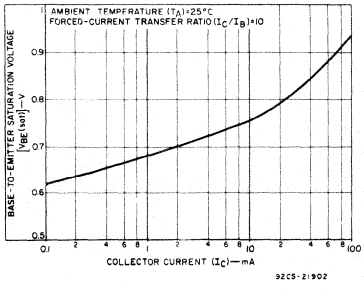


Fig. 2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

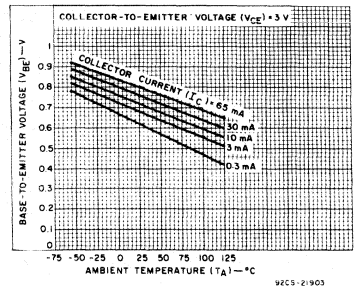


Fig. 3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

TYPICAL CHARACTERISTICS

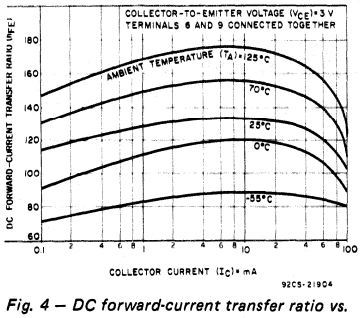


Fig. 4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

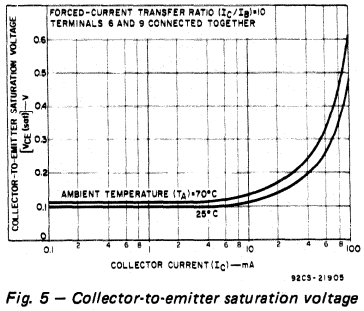


Fig. 5 – Collector-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

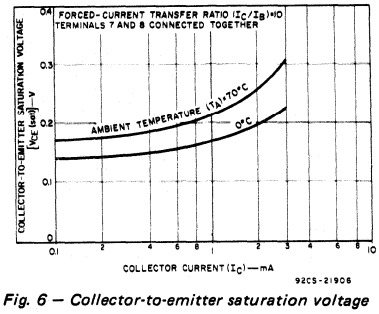


Fig. 6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

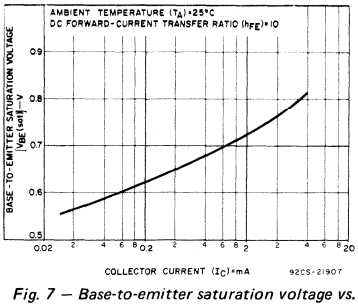


Fig. 7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

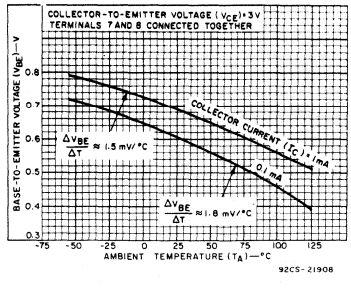


Fig. 8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

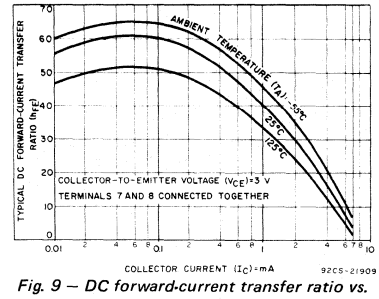


Fig. 9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

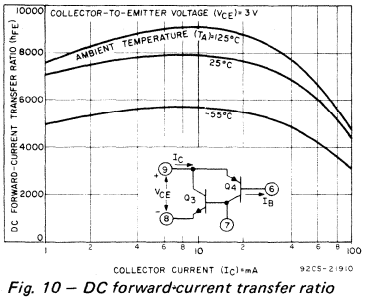


Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

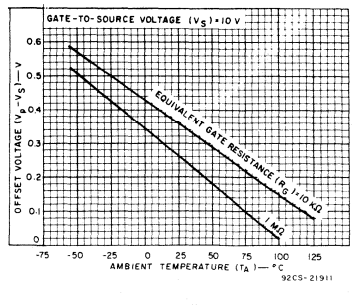


Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

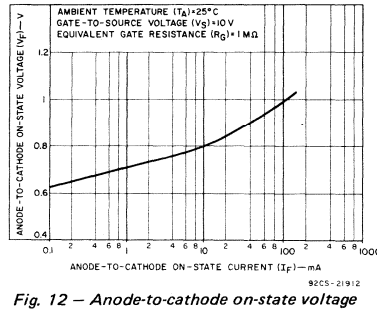


Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

CA3097

TYPICAL CHARACTERISTICS (CONT'D)

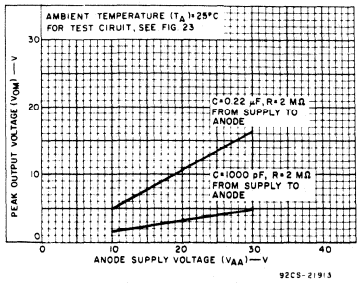


Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

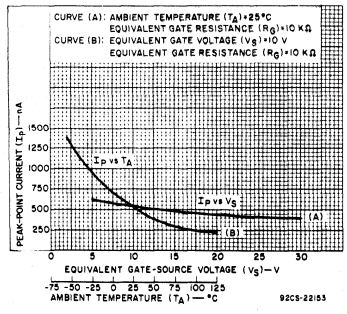


Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

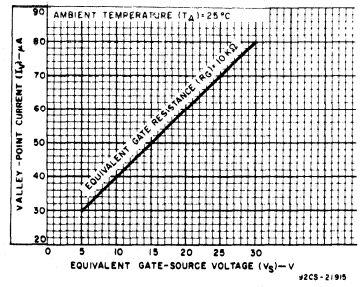


Fig.15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

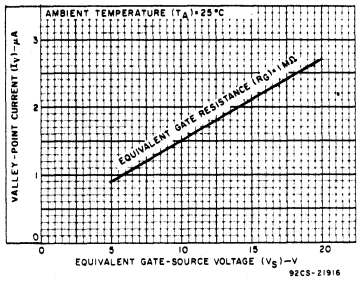


Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

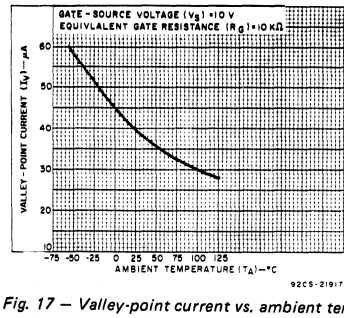


Fig. 17 – Valley-point current vs. ambient temperature for Q1 (PUT).

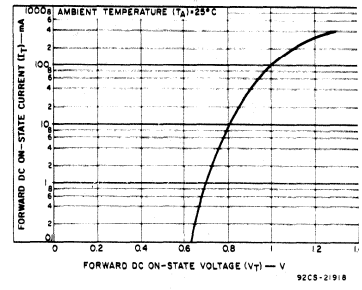


Fig. 18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

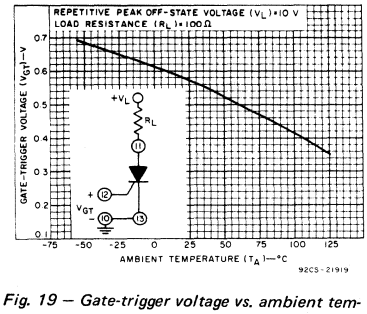


Fig. 19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

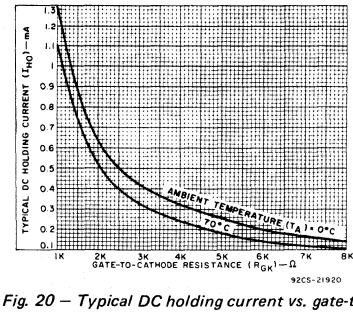


Fig. 20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

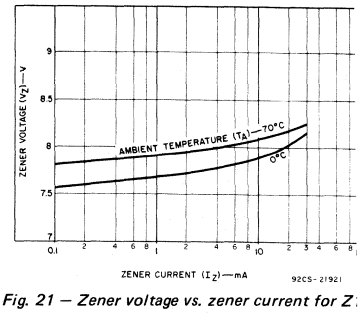


Fig. 21 – Zener voltage vs. zener current for Z

OPERATING CONSIDERATIONS FOR CA3097

. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector . . . . . terminal 9
Base . . . . . terminal 7
Emitter . . . . . terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector . . . . . terminal 7
Base . . . . . terminal 6
Emitter . . . . . terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal **is greater** than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low I_P.....I_P = 15 nA at V_S = 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external

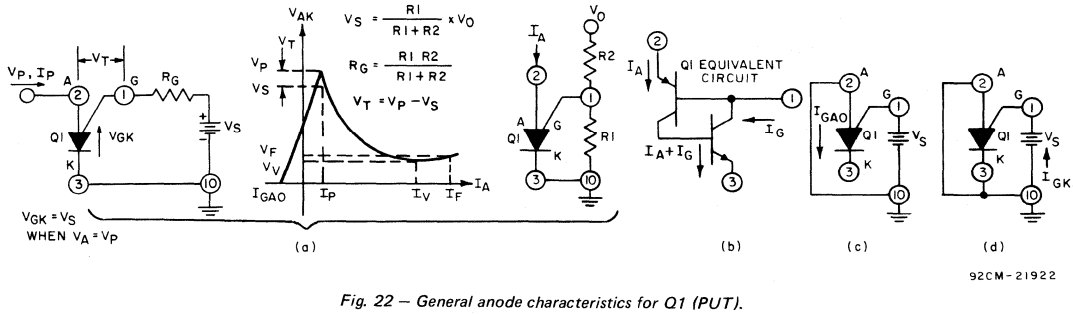


Fig. 22 – General anode characteristics for Q1 (PUT).

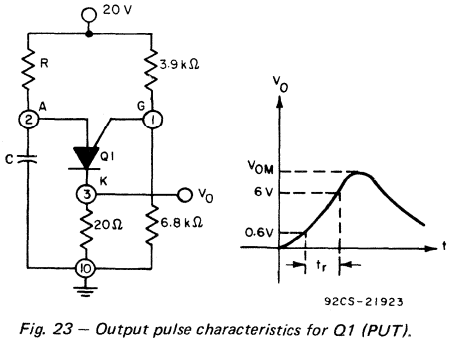


Fig. 23 – Output pulse characteristics for Q1 (PUT).

CA3097

OPERATING CONSIDERATIONS (CONT'D)

timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

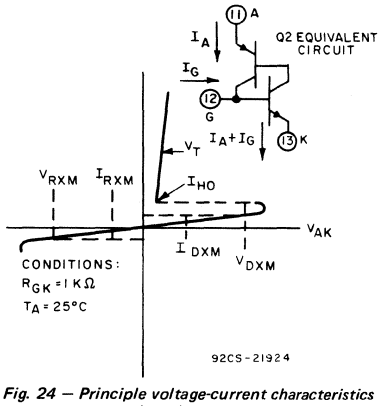


Fig. 24 — Principle voltage-current characteristics for Q2 (SCR).

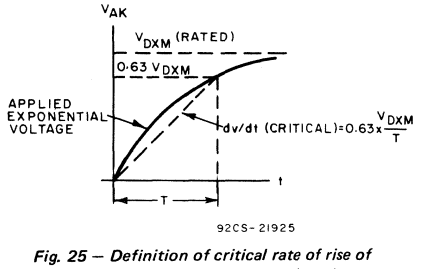
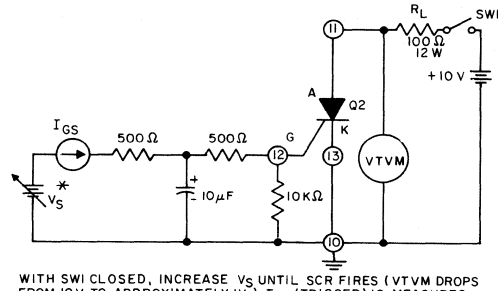


Fig. 25 — Definition of critical rate of rise of off-state voltage for Q2 (SCR).

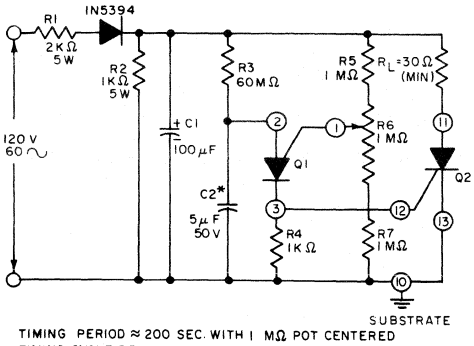


WITH SW1 CLOSED, INCREASE V_S UNTIL SCR FIRES (VTVM DROPS FROM 10V TO APPROXIMATELY 1V). I_{GS} (TRIGGER) IS MEASURED JUST PRIOR TO THIS TRIGGERING POINT. NOTE THAT I_{GS} MAY DECREASE AS V_S IS INCREASED DUE TO CURRENT DRAWN OUT OF THE GATE TERMINAL OF THE SCR AS IT TURNS ON. TO UNLATCH THE SCR OPEN SW1.

* V_S SHOULD BE CAPABLE OF SUPPLYING MILLIVOLT INCREMENTS NEAR THE TRIGGER POINT

Fig. 26 — Test circuit for determining I_{GS} in Q2 (SCR).

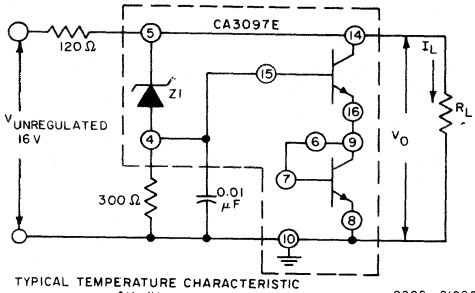
APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC. WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 4308, 5 μF AT 50 V
SPRAGUE TYPE 6308, 5 μF AT 50 V
OR EQUIVALENT

92CS-21927

Fig. 27 – AC line-operated one-shot timer.



TYPICAL TEMPERATURE CHARACTERISTIC

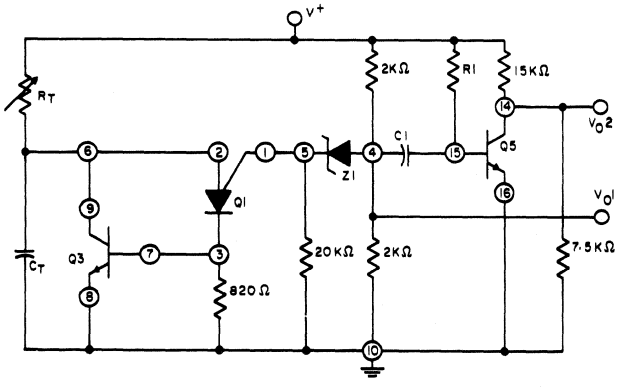
@ $R_L = 330\,\Omega$ $\frac{\Delta V_O / V_O}{\Delta T} \times 100 = \pm 0.01\ \%/°C$

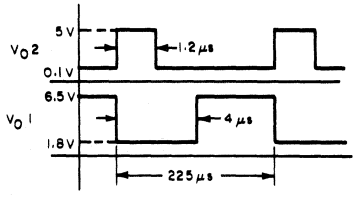
92CS-21928

TYP. LOAD REGULATION @ I_L = 0 TO 40 mA, $(\Delta V_O / V_O) \times 100$ = −3% (NO LOAD TO FULL LOAD)

TYP. LINE REGULATION @ $R_L = 330\,\Omega$, $\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.55\%/V$

Fig. 28 – Temperature-compensated shunt regulator.





PULSE RATE ADJUSTED BY VARYING R_T OR C_T.
OUTPUT PULSE WIDTH ADJUSTED BY $R_1 C_1$
DIFFERENTIATING TIME CONSTANT

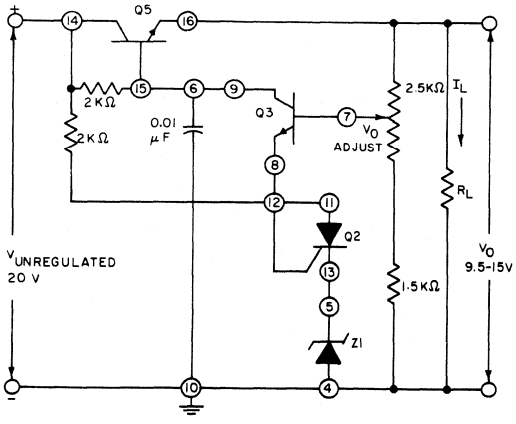
TYPICAL OPERATION FOR:
$V^+ = 15$ V, $C_T = 0.1\,\mu F$, $R_T = 4.3\,K\Omega$
$C_1 = 82$ pF, $R_1 = 60\,K\Omega$

92CM-21929

Fig. 29 – Pulse generator.

CA3097

APPLICATIONS CIRCUITS



TYPICAL LOAD REGULATION @ V_O=12 V, I_L=0 TO 40 mA

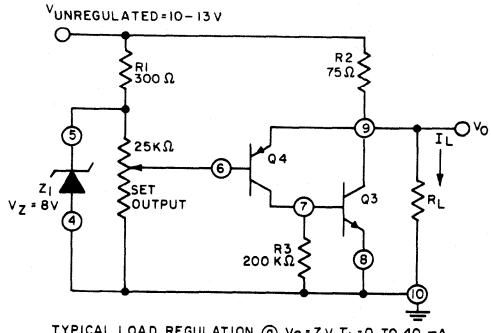
$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\%$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O=12 V

$\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.45\%/V$

92CS-21930

Fig. 30 — Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O=7 V, I_L=0 TO 40 mA

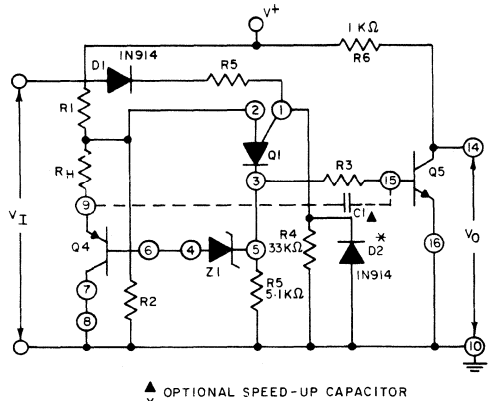
$\frac{\Delta V_O}{V_O} \times 100 = -1.1\%$

TYPICAL LINE REGULATION @ V_O=7 V, I_L=20 mA

$\frac{\Delta V_O}{V_O} \Big/ \Delta V_{UNREGULATED} = \pm 0.85\%/VOLT$

92CS-21931

Fig. 31 — 5 to 7.5 V shunt regulator.



▲ OPTIONAL SPEED-UP CAPACITOR

* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:

FREQUENCY IN = 0-10 KHz

SUPPLY VOLTAGE (V^+) = 15 V

R1, R2, R_H = 5.1 KΩ

R3 = 6.2 KΩ, R_S = 300Ω

C_1 = 820 pF

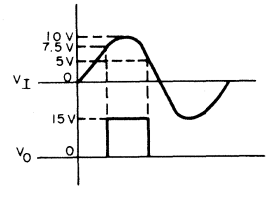
$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V

HYSTERESIS VOLTAGE = 2.5 V

UPPER THRESHOLD VOLTAGE ($V_{TH}U$) $\approx V^+ \frac{R2}{R1+R2}$

LOWER THRESHOLD VOLTAGE ($V_{TH}L$) $\approx \frac{(V^+)\left(\frac{R2\,R_H}{R2+R_H}\right)}{\frac{R2\,R_H}{R2+R_H}+R1}$

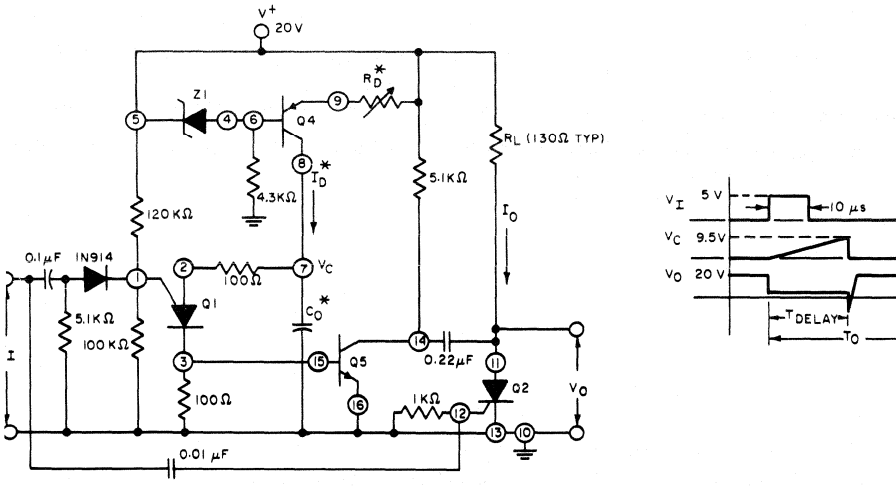
HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$



92CM-21932

Fig. 32 — Schmitt trigger.

APPLICATIONS CIRCUITS (CONT'D)

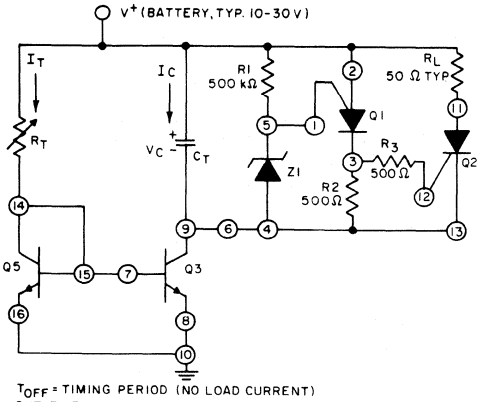


*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY C_D,I_D MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP)

92CM-21933

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V

$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$

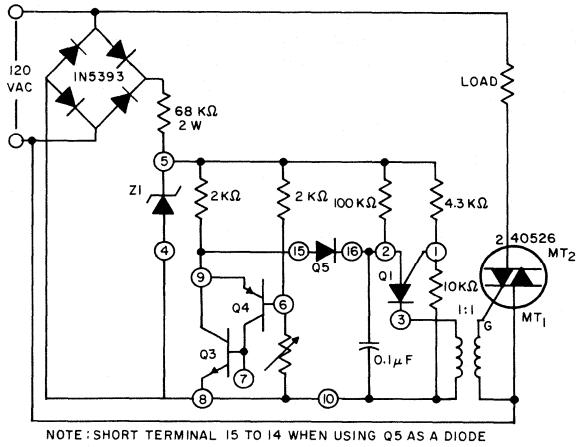
T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA

EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN
C_T = 1000 μF, I_T = 16 μA

$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx$ 1 MΩ)

92CS-21934

Fig.34 – Low-current-drain battery-operated long interval astable timer.



NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

92CS-22178

Fig.35 – Phase control circuit.

CA3118, CA3146, CA3183
High-Voltage Transistor Arrays

Features
- **Matched general-purpose transistors**
- **V_{BE} matched ±5mV max.**
- **Operation from DC to 120 MHz (CA3118AT, T; CA3146AE, E)**
- **Low-noise figure: 3.2dB typ. at 1kHz (CA3118AT, T; CA3146AE, E)**
- **High I_C: 75mA max. (CA3183AE, E)**

RCA-CA3118AT, CA3118T, CA3146AE, CA3146E, CA-3183AE, and CA3183E* are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3118AT and CA3118T consist of four transistors with two of the transistors connected in a Darlington configuration. These types are well suited for a wide variety of applications in low-power systems in the DC through VHF range. Both types are supplied in a hermetically sealed 12-lead TO-5 type package and operate over the full military temperature range. (CA3118AT and CA3118T are high-voltage versions of the popular predecessor type CA3018.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range. Both types are supplied in a 14-lead dual-in-line plastic package and operate over the ambient temperature range of −40°C to +85°C. (CA3146AE and CA3146E are high-voltage versions of the popular predecessor type CA3046.)

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. Both types are supplied in a 16-lead dual-in-line plastic package and operate over the ambient temperature range of −40°C to +85°C. (CA3183AE and CA3183E are high-voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

Applications
- **General use in signal processing systems in DC through VHF range**
- **Custom designed differential amplifiers**
- **Temperature compensated amplifiers**
- **Lamp and relay drivers (CA3183AE, E)**
- **Thyristor firing (CA3183AE, E)**

For detailed application information, see companion Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated Circuit Transistor Array."

*Formerly Developmental Types Nos.
CA3118AT – TA6091
CA3118T – TA6182
CA3146AE – TA6084
CA3146E – TA6181
CA3183AE – TA6094
CA3183E – TA6183

TYPE	P_T● max. mW	I_C max. mA	V_{CEO} max. V	V_{CBO} max. V	V_{CE} sat. at 10 mA typ. V	h_{FE} at 1mA, & V_{CE}=5V typ.	V_{IO} Diff. Pair at 1mA max. mV	I_{IO} Diff. Pair at 1mA max. μA	T_A Range (Operating) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3118AT	300	50	40	50	0.33	95	±5	2	−55 – +125
CA3118T	300	50	30	40	0.33	95	±5	2	−55 – +125
CA3146AE	300	50	40	50	0.33	95	±5	2	−40 – +85
CA3146E	300	50	30	40	0.33	95	±5	2	−40 – +85
CA3183AE	500	75	40	50	0.16	75	±5	2.5	−40 – +85
CA3183E	500	75	30	40	0.16	75	±5	2.5	−40 – +85

●Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3118 Series circuits is 450 mW at temperatures up to +85°C, then derate linearly at 5 mW°C. The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW°C.

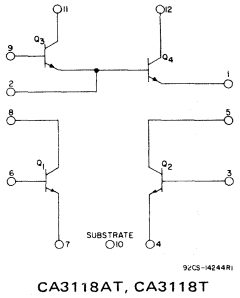
File Number **532**

CA3118, CA3146, CA3183

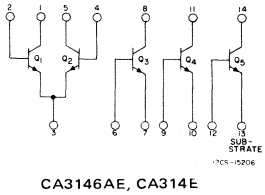
MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor –		
CA3118AT, CA3118T, CA3146AE, CA3146E	300	mW
CA3183AE, CA3183E	500	mW
Total package –		
Up to 85°C (CA3118AT, CA3118T)	450	mW
Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	750	mW
Above 85°C (CA3118AT, CA3118T)	derate linearly 5	mW/°C
Above 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E)	derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating –		
CA3118AT, CA3118T	–55 to +125	°C
CA3146AE, CA3146E, CA3183AE, CA3183E	–40 to +85	°C
Storage (all types)	–65 to +150	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO}):		
CA3118AT, CA3146AE, CA3183AE	40	V
CA3118T, CA3146E, CA3183E	30	V
Collector-to-Base Voltage (V_{CBO}):		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Collector-to-Substrate Voltage (V_{CIO}): ■		
CA3118AT, CA3146AE, CA3183AE	50	V
CA3118T, CA3146E, CA3183E	40	V
Emitter-to-Base Voltage (V_{EBO}) all types	5	V
Collector Current –		
CA3118AT, CA3118T, CA3146AE, CA3146E	50	mA
CA3183AE, CA3183E	75	mA
Base Current (I_B) – CA3183AE, CA3183E	20	mA

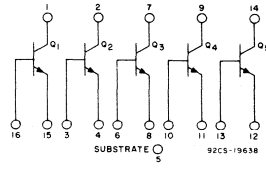
■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3118AT, CA3118T



CA3146AE, CA314E



CA3183AE, CA3183E

Fig. 1 – Schematic diagrams of high-voltage arrays.

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} min.	V_{CBO} min.	$V_{CE\ sat.}$ typ. V	V_{BE} typ. V	I_C max. mA	C_{CB} typ. pF	C_{CI} typ. pF	C_{EB} typ. pF
				I_C=10 mA	I_C=1 mA				
CA3018	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3018A	338	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3118AT		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3118T		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=10 mA	I_C=1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C=50 mA	I_C=10 mA				
CA3083	481	15	20	0.4	0.74	100	–	–	–
CA3183AE		40	50	1.7	0.75	75	–	–	–
CA3183E		30	40	1.7	0.75	75	–	–	–

NOTE: Related predecessor types are shown in shaded areas.

CA3118, CA3146, CA3183

STATIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char. Curve Fig. No.	LIMITS CA3118AT, CA3146AE Min.	CA3118AT, CA3146AE Typ.	CA3118AT, CA3146AE Max.	CA3118T, CA3146E Min.	CA3118T, CA3146E Typ.	CA3118T, CA3146E Max.	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = 0, I_E = 0	–	50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0	–	5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	2	–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	3	–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V, I_C=10mA	4	–	85	–	–	85	–	–
		V_{CE}=5V, I_C=1mA	4	30	100	–	30	100	–	
		V_{CE}=5V, I_C=10μA	4	–	90	–	–	90	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 1mA	5	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 10mA, I_B = 1mA	6	–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):										
Collector-Cutoff Current (CA3118AT and CA3118T only)	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	5	–	–	–	μA
DC Forward-Current Transfer Ratio (CA3118AT and CA3118T only)	h_{FE}	V_{CE} = 5V, I_C = 1mA	7	1500	9000	–	1500	9000	–	–
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V, I_E = 10mA	8	–	1.46	–	–	1.46	–	V
		V_{CE}=5V, I_E = 1mA	8,9	–	1.32	–	–	1.32	–	
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_E = 1mA	–	–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):										
Magnitude of Input Offset Voltage $\lvert V_{BE1} - V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	V_{CE} = 5V, I_E = 1mA	10,11	–	0.48	5	–	0.48	5	mV
Magnitude of h_{FE} Ratio (CA3118AT and CA3118T only)		V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA	–	0.9	1.0	1.1	0.9	1.0	1.1	–
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\Delta V_{BE}}{\Delta T}\right\rvert$	V_{CE} = 5V, I_E = 1mA	–	–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} ($V_{BE1} - V_{BE2}$) Temperature Coefficient	$\left\lvert\frac{\Delta V_{IO}}{\Delta T}\right\rvert$	V_{CE} = 5V, $I_{C1} = I_{C2}$ = 1mA	–	–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\lvert I_{IO_1} - I_{IO_2}\rvert$ (CA3146AE and CA3146E only)	I_{IO}	V_{CE} = 5V, $I_{C_1} = I_{C_2}$ = 1 mA	12	–	0.3	2	–	0.3	2	μA

DYNAMIC ELECTRICAL CHARACTERISTICS – CA3118 and CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char. Curve Fig.No.	CA3118AT CA3146AE			CA3118T CA3146E			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100μA, Source resistance = 1 kΩ	14	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		16	–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		16	–	15.6	–	–	15.6	–	μmho
Open-Circuit Reverse Voltage Transfer Ratio	h_{re}		16	–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–
Admittance Characteristics:										
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	17	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		18	–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		19	–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}		20		See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	21	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	22	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	22	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	22	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char Curve Fig. No.	LIMITS CA3183AE			CA3183E			UNITS
				Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	–	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	–	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100μA, I_B=0, I_E = 0	–	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	23	–	–	10	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	24	–	–	1	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}= 3 V, I_C = 10mA	25,26	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	–	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	27	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	28	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):										
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	29	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		30	–	0.78	2.5	–	0.78	2.5	μA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

CA3118, CA3146, CA3183

TYPICAL STATIC CHARACTERISTICS CURVES — CA3118 and CA3146 SERIES

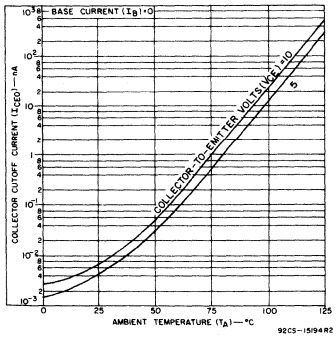


Fig. 2 – I_{CEO} vs. T_A for any transistor.

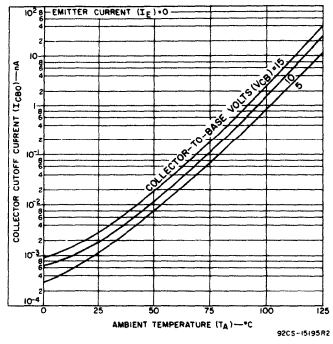


Fig. 3 – I_{CBO} vs. T_A for any transistor.

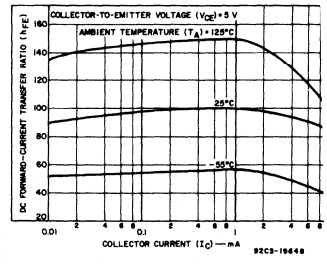


Fig. 4 – h_{FE} vs. I_C for any transistor.

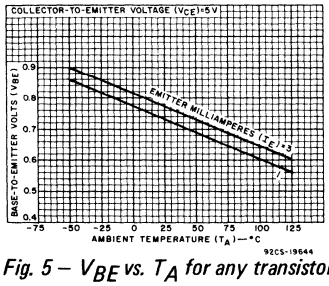


Fig. 5 – V_{BE} vs. T_A for any transistor.

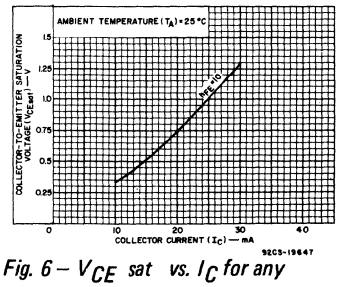


Fig. 6 – $V_{CE\ sat}$ vs. I_C for any transistor.

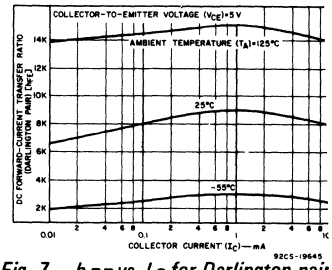


Fig. 7 – h_{FE} vs. I_C for Darlington pair (Q3 and Q4) for types CA3118AT and CA3118T.

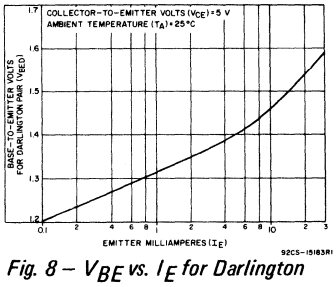


Fig. 8 – V_{BE} vs. I_E for Darlington pair (Q3 and Q4).

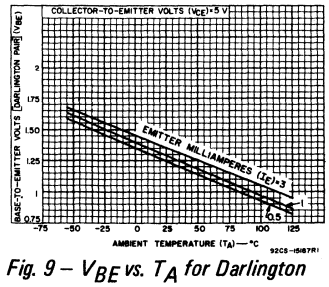


Fig. 9 – V_{BE} vs. T_A for Darlington pair (Q3 and Q4).

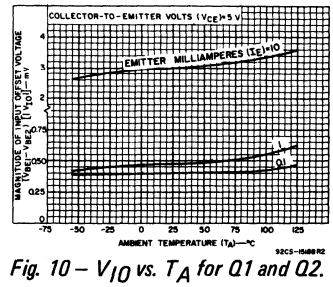


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

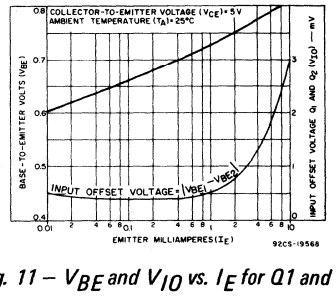


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

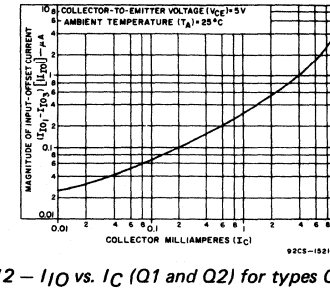


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) – CA3118, CA3146 SERIES

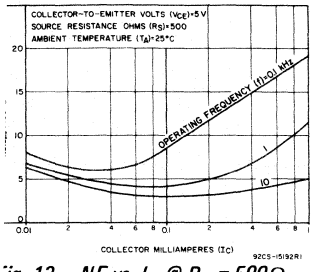


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

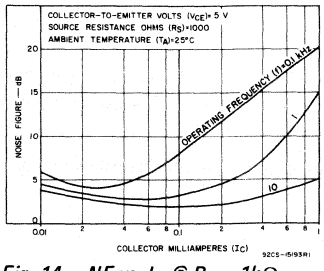


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

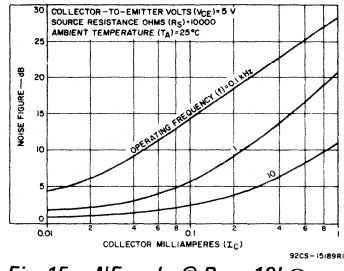


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

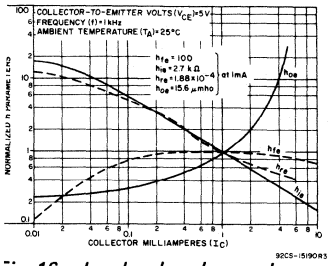


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

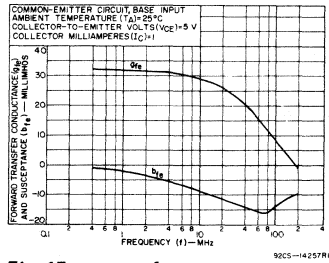


Fig. 17 – y_{fe} vs. f.

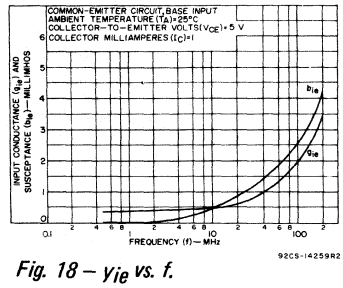


Fig. 18 – y_{ie} vs. f.

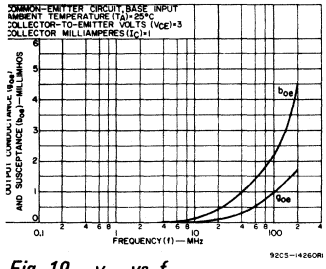


Fig. 19 – y_{oe} vs. f.

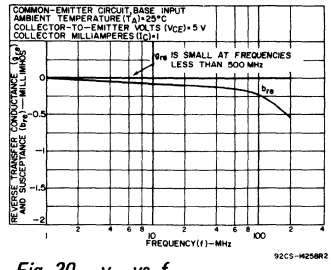


Fig. 20 – y_{re} vs. f.

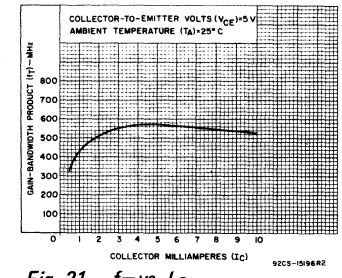


Fig. 21 – f_T vs. I_C.

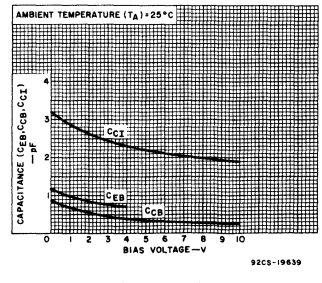


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

CA3118, CA3146, CA3183

TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

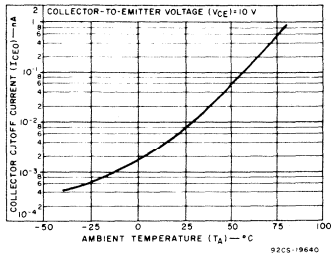


Fig. 23 – I_{CEO} vs. T_A for any transistor.

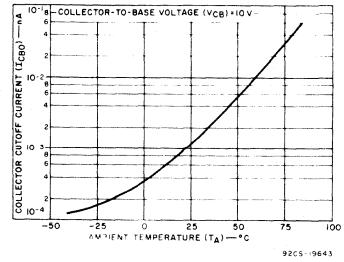


Fig. 24 – I_{CBO} vs. T_A for any transistor.

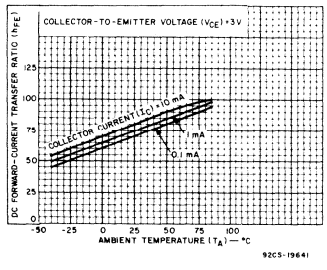


Fig. 25 – h_{FE} vs. T_A for any transistor.

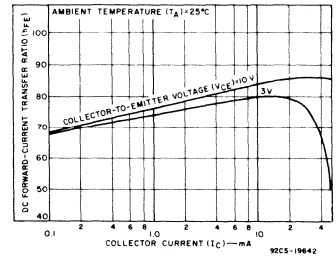


Fig. 26 – h_{FE} vs. I_C for any transistor.

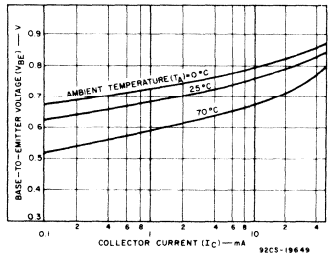


Fig. 27 – V_{BE} vs. I_C for any transistor.

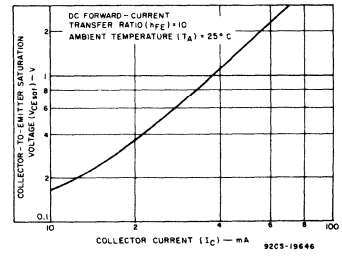


Fig. 28 – $V_{CE\ sat}$ vs. I_C for any transistor.

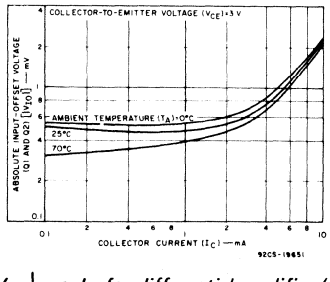


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

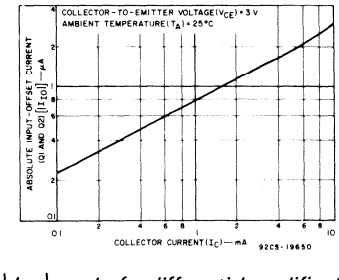


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

CA3127

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Gain-bandwidth product (f_T) > 1 GHz*
- *Power gain = 30 dB (typ.) at 100 MHz*
- *Noise figure = 3.5 dB (typ.)* at 100 MHz
- *Five independent transistors on a common substrate*

RCA-CA3127* consits of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127 useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

The CA3127 is supplied in the 16-lead dual-in-line plastic package (E suffix), 16-lead dual-in-line frit-seal ceramic package (F suffix), and is also available in clip form (H suffix). It operates over the full military temperature range of -55 to +125° C.

*Formerly RCA Dev. No. TA6206.

Applications:

- *VHF amplifiers*
- *Multifunction combinations - RF/mixer/oscillator*
- *Sense amplifiers*
- *Synchronous detectors*
- *VHF mixers*
- *IF converter*
- *IF amplifiers*
- *Synthesizers*
- *Cascade amplifiers*

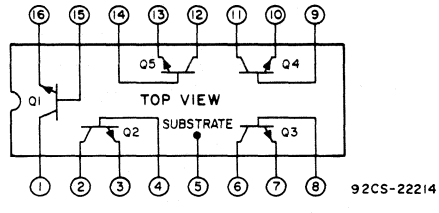


Fig. 1 — Schematic diagram of CA3127.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P_D:

Any one transistor ..... 85 mW

Total Package:

For T_A up to 75° C ..... 425 mW

For T_A > 75° C Derate Linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:

Operating ..... -55 to +125° C

Storage ..... -65 to +125° C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO} ..... 15 V

Collector-to-Base Voltage, V_{CBO} ..... 20 V

Collector-to-Substrate Voltage, V_{CIO}* ..... 20 V

Collector Current, I_C ..... 20 mA

*The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

File Number **662**

CA3127

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\ \mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\ \mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
I/F Noise Figure	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz, $R_L = 1\ k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration, f = 100 MHz, $V^+ = 12$ V	27	30	–	dB
Noise Figure	$I_C = 1$ mA	–	3.5	–	dB
Input Resistance	Common-Emitter	–	400	–	Ω
Output Resistance	Configuration	–	4.6	–	$k\Omega$
Input Capacitance	$V_{CE} = 6$ V	–	3.7	–	pF
Output Capacitance	$I_C = 1$ mA	–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

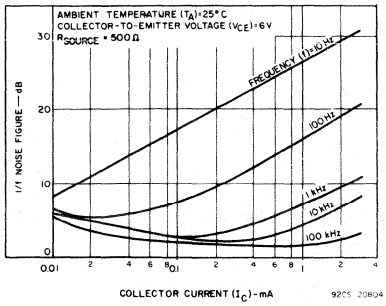


Fig. 2 — 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

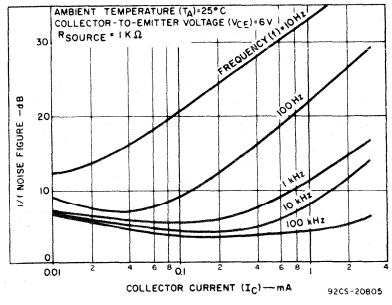


Fig. 3 — 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

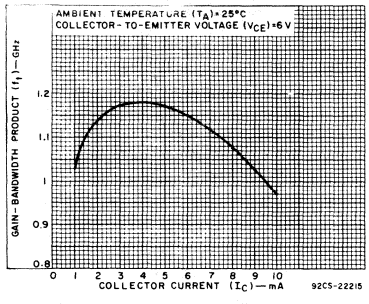


Fig. 4 — Gain-bandwidth product as a function of collector current.

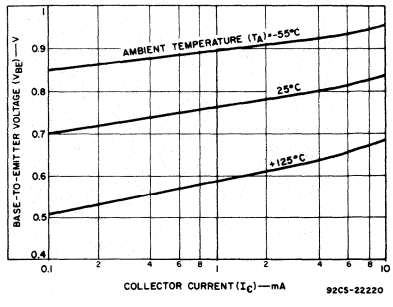


Fig. 5 — Base-to-emitter voltage as a function of collector current.

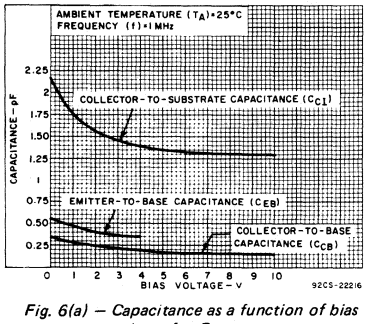


Fig. 6(a) — Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	—	6 V	—	6 V	—	4 V	—	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) — Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

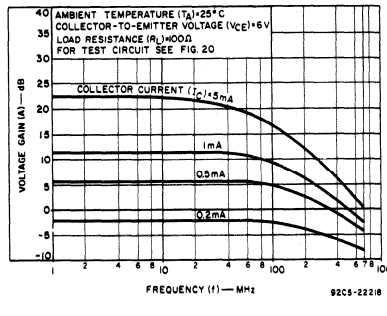


Fig. 7 — Voltage gain as a function of frequency at R_L = 100 Ω.

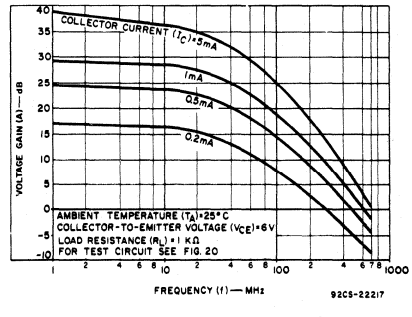


Fig. 8 — Voltage gain as a function of frequency at R_L = 1 kΩ.

CA3127

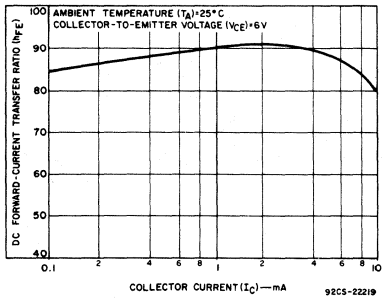


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

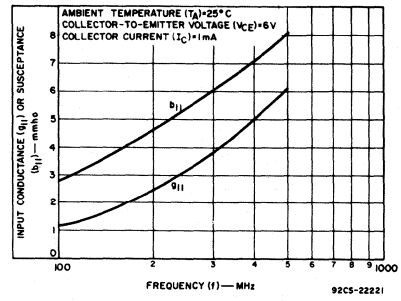


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

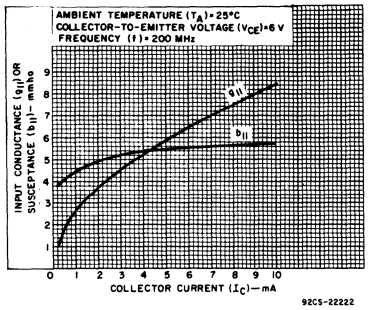


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

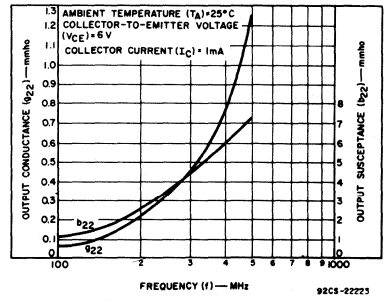


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

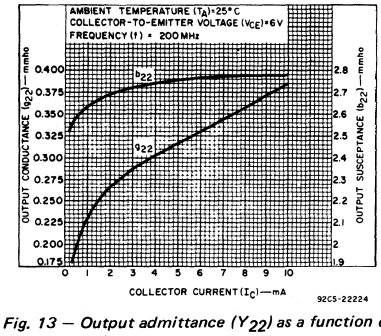


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

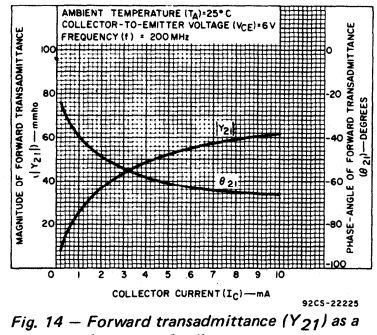


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

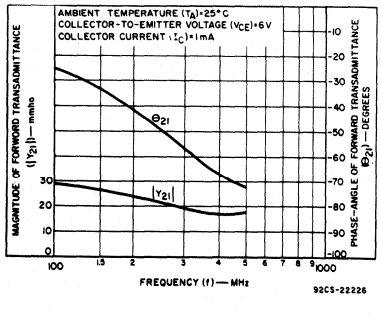


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

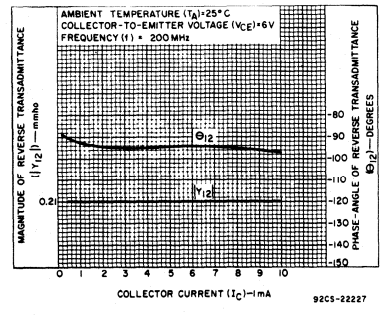


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

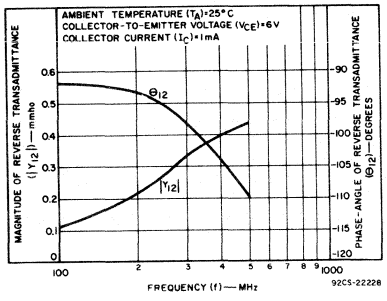


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

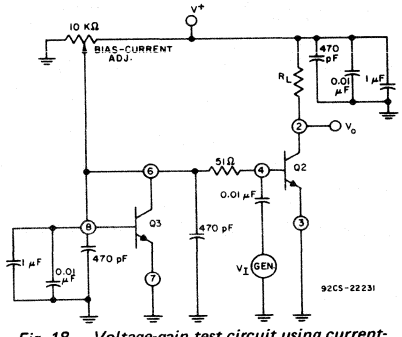
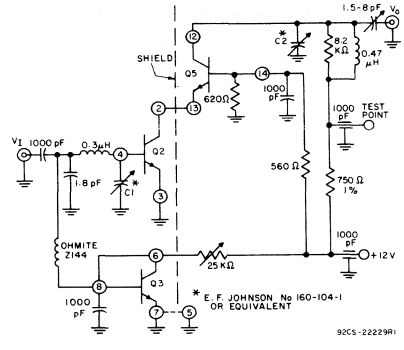


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

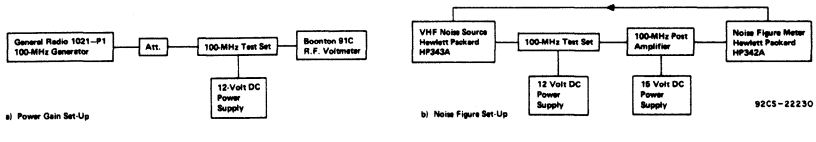


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

CA3138, CA3138A

High-Current, High-Beta N-P-N Transistor Arrays

For Industrial, Commercial, and Military Applications

Four Isolated Discrete Sealed-Junction High-Current N-P-N Transistors

Features:

- **High Current –1 A**
- **High Beta – 95 min. at I_C = 500 mA, V_{CE} = 5 V**
- **Low V_{CE}(SAT) –0.4 V max. at I_C = 500 mA, I_B = 12.5 mA**
- **Silicon Nitride Passivated**
- **Platinum Silicide Ohmic Contacts**

The RCA-CA3138 and CA3138A are high-current n-p-n transistor arrays containing four isolated (discrete) sealed-junction high-current n-p-n transistors. They are intended for high-current, high-speed switching and driver applications.

The CA3138A has all the features and characteristics of the CA3138 but is intended for applications requiring premium grade specifications –– higher rating for V_{CBO} of 25 volts and limits established for I_{CEO}, I_{EBO}, and h_{FE} at 10 mA.

The CA3138 and CA3138A are supplied in a 14-lead dual-in-line plastic package and operate over the full military temperature range of –55°C to +125°C.

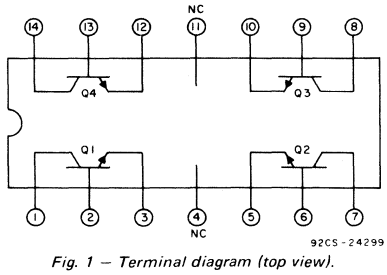


Fig. 1 – Terminal diagram (top view).

Applications:

- **High-Current LED Driver**
- **Relay and Solenoid Driver**
- **Lamp Driver**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

COLLECTOR-TO-EMITTER VOLTAGE ..... With Base Open (V_{CEO})	15	V
COLLECTOR-TO-BASE VOLTAGE With Emitter Open (V_{CBO})		
CA3138	20	V
CA3138A	25	V
EMITTER-TO-BASE VOLTAGE ..... With Collector Open (V_{EBO})	5	V
COLLECTOR CURRENT (I_C)	1	A
POWER DISSIPATION (P_D):		
At T_A up to 25°C:		
For Each Transistor	1	W
Total Package	2	W
At T_A above 25°C derate linearly	20	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

File Number **1131**

CA3138, CA3138A

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic		Test Conditions	LIMITS						Units
			CA3138			CA3138A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Collector-to-Emitter Sustaining Voltage, $V_{CEO}(sus)$*		I_C = 1 mA, I_B = 0	15	20	–	15	20	–	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$		I_C = 10 μA	20	55	–	25	60	–	V
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$		I_C = 10 μA, I_E = 0	20	55	–	25	60	–	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$		I_E = 10 μA, I_C = 0	5	7.2	–	5	7.2	–	V
Base-to-Emitter Saturation Voltage, $V_{BE}(sat)$*		I_C = 500 mA, I_B = 12.5 mA	0.7	0.81	1.1	0.7	0.81	1.1	V
Collector-to-Emitter Saturation Voltage, $V_{CE}(sat)$*		I_C=500 mA, I_B = 12.5 mA	–	0.26	0.4	–	0.26	0.4	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 15 V	–	0.03	1	–	0.02	0.1	μA
	I_{CEO}	V_{CE} = 10 V	–	0.5	–	–	0.3	1.0	
	I_{EBO}	V_{EB} = 4 V	–	0.01	–	–	0.01	0.1	
Static Forward-Current Transfer Ratio (Beta), h_{FE}*		I_C=10 mA, V_{CE} = 5 V	–	–	–	35	140	–	
		I_C = 100 mA, V_{CE} = 5 V	80	160	450	80	160	450	
		I_C = 500 mA, V_{CE} = 5 V	95	170	500	95	170	500	
		I_C = 1 A, V_{CE} = 5 V	40	170	–	40	170	–	
Small-Signal Forward Current Transfer Ratio, h_{fe}		I_C = 50 mA, V_{CE} = 10 V, f = 100 MHz	2	–	–	2	–	–	
Collector-to-Base Capacitance, C_{CB}		V_{CB} = 10 V, I_E = 0	–	18	–	–	18	–	pF
Emitter-to-Base Capacitance, C_{EB}		V_{EB} = 0.5 V, I_C = 0	–	77	–	–	77	–	pF
Rise Time (See Test Ckt. Fig. 6), t_r		I_C = 570 mA	–	6	–	–	6	–	ns
Fall Time (See Test Ckt. Fig. 6), t_f		I_{B1} = 30 mA	–	100	–	–	100	–	ns
Delay Time (See Test Ckt. Fig. 6), t_d		I_{B2} = 0	–	7.5	–	–	7.5	–	ns
Storage Time (See Test Ckt. Fig. 6), t_s			–	850	–	–	850	–	ns

*Pulse Conditions: width = 300 μs; duty cycle = 1%.

CA3138, CA3138A

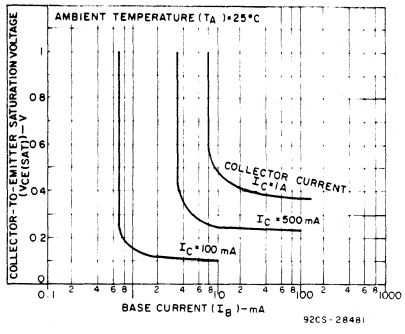


Fig. 2 – $V_{CE(sat)}$ vs I_B

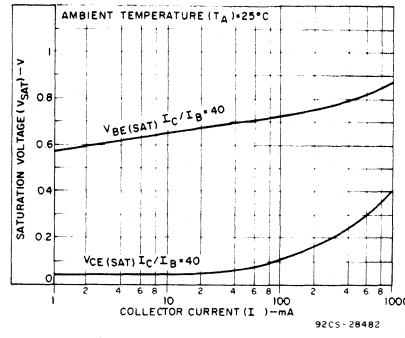


Fig. 3 – V_{sat} vs I_C

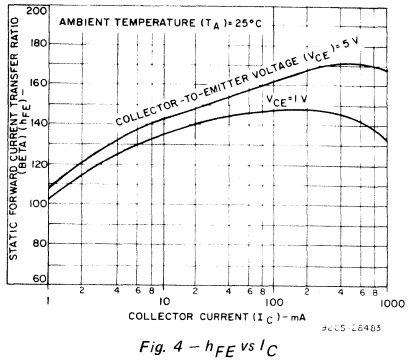


Fig. 4 – h_{FE} vs I_C

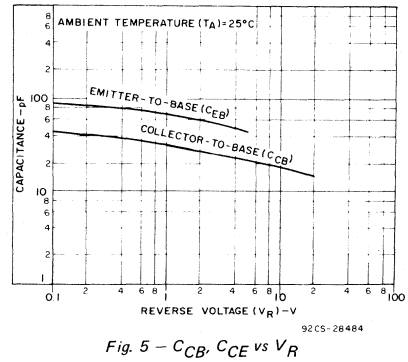


Fig. 5 – C_{CB}, C_{CE} vs V_R

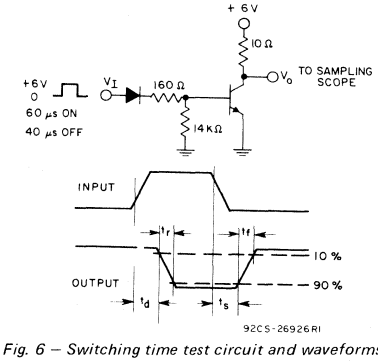


Fig. 6 – Switching time test circuit and waveforms.

CA3141

High-Voltage Diode Array

For Commercial, Industrial, and Military Applications

Features:

- *Matched monolithic construction - V_F for each diode pair matched to within 0.55 mV (typ.) at $I_F = 1$ mA*
- *Low diode capacitance - 0.3 pF (typ.) at $V_R = 2$ V*
- *High diode-to-substrate breakdown voltage - 30 V (min.)*
- *Low reverse (leakage) current - 100 nA (max.)*

The RCA-CA3141E High-Voltage Diode Array consists of ten general-purpose high-reverse-breakdown diodes. Six diodes are internally connected to form three common-cathode diode pairs, and the remaining four diodes are internally connected to form two common-anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141E extremely useful for a wide variety of applications in communications and switching systems.

The CA3141 is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

Applications:

- *Balanced modulators or demodulators*
- *Analog switches*
- *High-voltage diode gates*
- *Current ratio detectors*

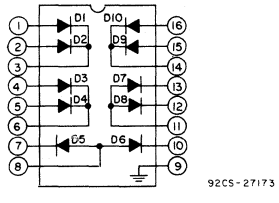


Fig. 1 — Terminal assignment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK INVERSE VOLTAGE (PIV) ..... 30 V

PEAK DIODE-TO-SUBSTRATE VOLTAGE ..... 30 V

PEAK FORWARD SURGE CURRENT [I_F (SURGE)] ..... 100 mA

DC FORWARD CURRENT (I_F) ..... 25 mA

DISSIPATION:

Any one diode unit ..... 50 mW

Total Package:

Up to 55°C ..... 650 mW

For $T_A > 55°C$ ..... Derate linearly at 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... −55 to +125°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. ..... +265°C

File Number **906**

CA3141

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNIT
DC Forward Voltage Drop, V_F	I_F (Anode)	100 μA	–	0.7	0.9	V
		1 mA	–	0.78	1	
		10 mA	–	0.93	1.2	
DC Reverse Breakdown Voltage, $V_{(BR)R}$	$I_F = -10$ μA		30	50	–	V
DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$	$I_{DI} = 10$ μA		30	50	–	V
DC Reverse (Leakage) Current, I_R	$V_F = -20$ V		–	–	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate, I_{DI}	$V_{DI} = 20$ V		–	–	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs	$V_{DI} = 20$ V, $I_{FA} = 1$ mA		–	0.55	–	mV
Temperature Coefficient of Forward Voltage Drop, $\Delta V_F/\Delta T$	$I_F = 1$ mA		–	−1.5	–	mV/°C
Reverse Recovery Time, t_{rr}	$I_F = 2$ mA, $I_R = 2$ mA		–	50	–	ns
Diode Capacitance, C_D			See Fig. 5			pF
Diode Anode-to-Substrate Capacitance, C_{DAI}			See Fig. 6			pF
Diode Cathode-to-Substrate Capacitance, C_{DCI}			See Fig. 7			pF
Magnitude of Cathode-to-Anode Current Ratio, $\lvert I_{FC}/I_{FA} \rvert$	$I_{FA} = 1$ mA, $V_{DS} = 10$ V		0.9	0.96	–	

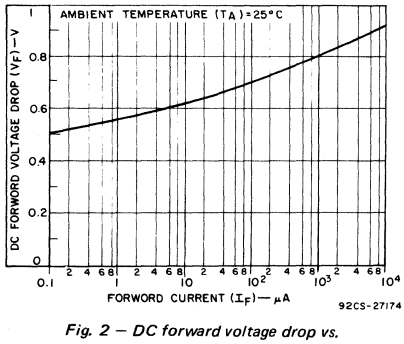


Fig. 2 – DC forward voltage drop vs. forward current.

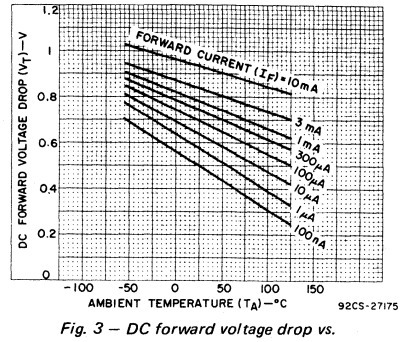


Fig. 3 – DC forward voltage drop vs. ambient temperature.

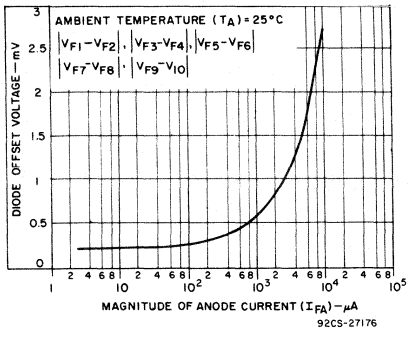


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

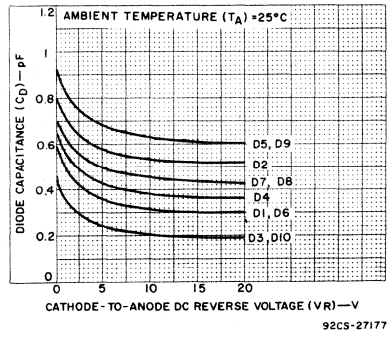


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

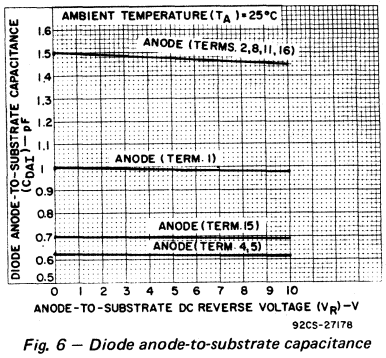


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

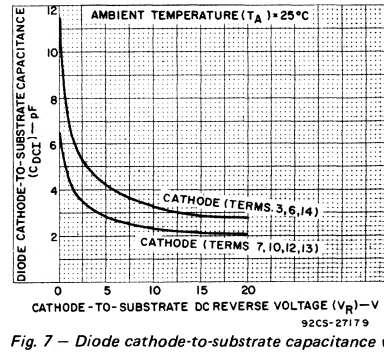


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

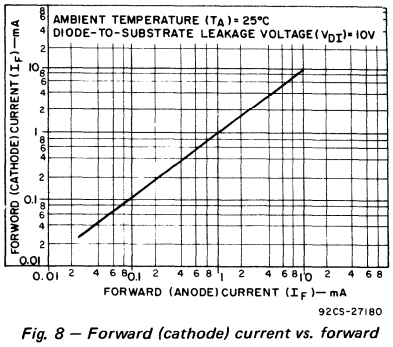


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

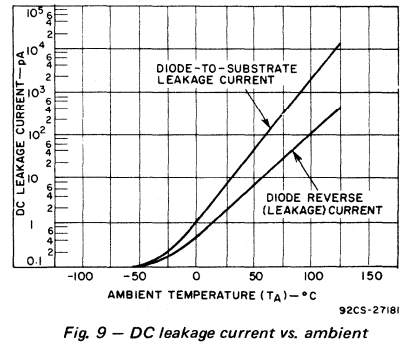


Fig. 9 — DC leakage current vs. ambient temperature.

CA3227, CA3246

High-Frequency N-P-N Transistor Arrays

For Low-Power Applications at Frequencies up to 1.5 GHz

Features:

- *Gain-bandwidth product (f_T) > 3 GHz*
- *Five transistors on a common substrate*

The RCA-CA3227E and CA3246E* consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3 GHz, making them useful from dc to 1.5 GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

The CA3227E is supplied in a 16-lead dual-in-line plastic package and the CA3246E is supplied in a 14-lead dual-in-line plastic package.

*Formerly RCA Developmental Nos. TA10854 and TA10855, respectively.

Applications:

- *VHF amplifiers*
- *VHF mixers*
- *Multifunction combinations - RF/mixer/oscillator*
- *IF converter*
- *IF amplifiers*
- *Sense amplifiers*
- *Synthesizers*
- *Synchronous detectors*
- *Cascade amplifiers*

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C:*

POWER DISSIPATION, P_D:

Any one transistor ..... 85 mW

Total Package:

For T_A up to 75°C ..... 425 mW

For T_A > 75°C Derate Linearly at ..... 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... −55 to +125°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

The following ratings apply for each transistor in the device.

Collector-to-Emitter Voltage, V_{CEO} ..... 8 V

Collector-to-Base Voltage, V_{CBO} ..... 12 V

Collector-to-Substrate Voltage, V_{CIO}§ ..... 20 V

Collector Current, I_C ..... 20 mA

§The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227E and terminal 13/CA3246E) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

File Number **1345**

CA3227, CA3246

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10 μA, I_E=0	12	20	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1 mA, I_B=0	8	10	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{C1}=10 μA, I_B=0, I_E=0	20	—	—	V
Emitter-Cutoff-Current*	I_{EBO}	V_{EB}=4.5 V, I_C=0	—	—	10	μA
Collector-Cutoff-Current	I_{CEO}	V_{CE}=5 V, I_B=0	—	—	1	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB}=8 V, I_E=0	—	—	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=6 V, I_C=10 mA	—	110	—	
		V_{CE}=6 V, I_C=1 mA	40	150	—	
		V_{CE}=6 V, I_C=0.1 mA	—	150	—	
Base-to-Emitter Voltage	V_{BE}	V_{CE}=6 V, I_C=1 mA	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=10 mA, I_B=1 mA	—	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=10 mA, I_B=1 mA	0.74	—	0.94	V

*On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

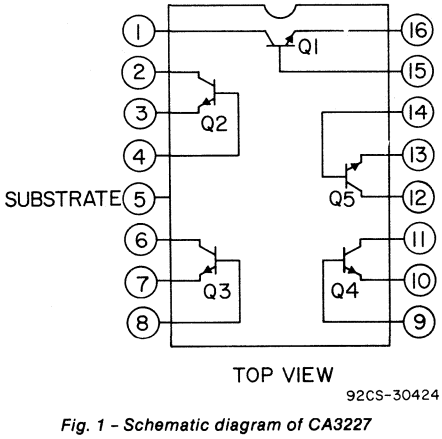


Fig. 1 - Schematic diagram of CA3227

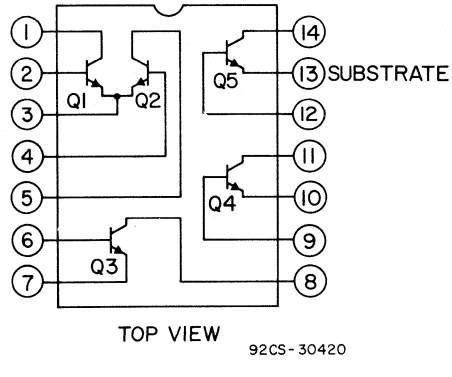


Fig. 2 - Schematic diagram of CA3246

CA3227, CA3246

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, 200 MHz, Common Emitter
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each Transistor			
Input Admittance, Y_{11} b_{11}	I_C=1 mA, V_{CE}=5 V	4	mmho
g_{11}		0.75	
Output Admittance, Y_{22} b_{22}		2.7	mmho
g_{22}		0.13	
Forward Transfer Admittance, Y_{21} Y_{21}		29.3	mmho
θ_{21}		−33	degrees
Reverse Transfer Admittance, Y_{12} Y_{12}		0.38	mmho
θ_{12}		−97	degrees
Input Admittance, Y_{11} b_{11}	I_C=10 mA, V_{CE}=5 V	4.8	mmho
g_{11}		2.85	
Output Admittance, Y_{22} b_{22}		2.75	
g_{22}		0.9	
Forward Transfer Admittance, Y_{21} Y_{21}		95	mmho
θ_{21}		−62	degrees
Reverse Transfer Admittance, Y_{12} Y_{12}		0.39	mmho
θ_{12}		−97	degrees
Small-Signal Forward Current Transfer Ratio h_{21}	I_C=1 mA, V_{CE}=5 V	7.1	
	I_C=10 mA, V_{CE}=5 V	17	
Typical Capacities @ 1 MHz, Three-Terminal Measurement			
Collector-to-Base Capacitance, C_{CB}	V_{CB}=6 V	0.3	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI}=6 V	1.6	pF
Collector-to-Emitter Capacitance, C_{CE}	V_{CE}=6 V	0.4	pF
Emitter-to-Base Capacitance, C_{EB}	V_{EB}=3 V	0.75	pF

CA3600

CMOS Transistor Array

For Linear Circuit Applications

Features:

- High input resistance . . . . . 100 GΩ (typ.)
- Low gate-terminal current . . . . 10 pA (typ.)
- Matched p-channel pair:
  Gate-voltage differential (I_D = -100 μA) ±20 mV (max.)
- No "Popcorn" (burst) noise
- Stable transfer characteristics over an operating temperature range of −55°C to +125°C when operated in complementary circuit configuration at supply voltages in the 5 to 15 volt range (see Fig. 14)
- Integrated integral gate-protection system (see Fig. 34)
- High voltage gain (see Fig. 11). . . up to 53 dB (typ.) per CMOS stage
- Individual MOS transistors have square-law characteristics, superior cross-modulation performance, and greater dynamic range than bipolar transistors

RCA-CA3600E is an array of COmplementary-Symmetry MOS Field-Effect Transistors* on a monolithic silicon substrate. It is comprised of three n-channel and three p-channel enhancement-type MOS transistors arrayed as shown in Fig. 1, and specified and tested for linear circuit operation. These transistors are uniquely suitable for service in complementary-symmetry circuits at supply voltages in the range of 3 to 15 volts and are useful at frequencies up to 5 MHz (untuned). Each transistor in the CA3600E can conduct currents up to 10 mA. This device is supplied in the 14-lead dual-in-line plastic package.

Formerly RCA Dev. No. TA6368.

* The theory and construction of COS/MOS transistors are described in the "RCA C MOS Integrated Circuits Manual," RCA Solid State Division Technical Series Publication No. CMS-272.

Applications:

- High input impedance, general-purpose amplifiers
- Pre-amplifiers
- Differential amplifiers
- Op-amps and comparators
- Constant-current sources and current mirrors
- Micropower amplifiers and oscillators
- Control of lamps, LED's, relays, and thyristors
- Timers
- Choppers
- Mixers

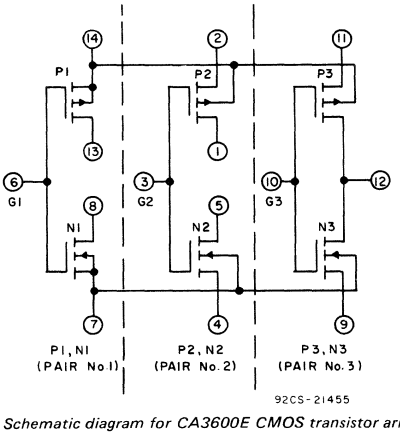


Fig.1 – Schematic diagram for CA3600E CMOS transistor array. (See Fig.34 for internal gate-and-channel-protection circuits)

1. Drain terminal, p-channel of pair no. 2
2. Source terminal, p-channel of pair no. 2
3. Common gate terminal of pair no. 2
4. Source terminal, n-channel of pair no. 2
5. Drain terminal, n-channel of pair no. 2
6. Common gate terminal of pair no. 1
7. Source terminal, n-channel of pair no. 1 and substrate connection for all n-channel transistors - - - V_{SS} terminal
8. Drain terminal, n-channel of pair no. 1
9. Source terminal, n-channel of pair no. 3
10. Common gate terminal of pair no. 3
11. Source terminal, p-channel of pair no. 3
12. Common drain terminal of pair no. 3
13. Drain terminal, p-channel of pair no. 1
14. Source terminal, p-channel of pair no. 1 and substrate connection for all p-channel transistors - - - V_{DD} terminal

Terminal Identification for Fig. 1.

File Number **619**

CA3600

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

DISSIPATION:	
Any one transistor at T_A up to 55°C	150 mW
Total package at T_A up to 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering)	
At distance not less than 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

The Following Ratings Apply for Each Transistor in the Device:

DRAIN-TO-SOURCE VOLTAGE, V_{DS}:	
n-channel	+15 V
p-channel	−15 V
DRAIN-TO-GATE VOLTAGE, V_{DG}:	
n-channel	+15 V
p-channel	−15 V
SOURCE-TO-SUBSTRATE VOLTAGE, V_{SB}:	
n-channel	+15 V
p-channel	−15 V
GATE-TO-SOURCE VOLTAGE, V_{GS}:	
p-channel transistors (p_1, p_2, p_3)	0 V(min.),$-V_D$(max.)
n-channel transistors (n_1, n_2, n_3)	0 V(min.),$+V_D$(max.)
CMOS transistor-pairs (p_1-n_1, p_2-n_2, p_3-n_3)	0 V(min.),$+V_{DD}$(max.)
DRAIN CURRENT, $\|I_D\|$	10 mA
GATE CURRENT, $\|I_G\|$	100 μA

The Following Rating Applies for Each CMOS Transistor-Pair in the Device:

DC SUPPLY VOLTAGE ($V_{DD} - V_{SS}$)	+15 V

Rules for Maintaining Electrical Isolation Between Transistors and Monolithic Substrate

Terminal No. 14 must be maintained at the most positive potential (or equally positive potential) with respect to any other terminal in the CA3600E.

Terminal No. 7 must be maintained at the most negative potential (or equally negative potential) with respect to any other terminal in the CA3600E.

Violation of these rules will result in improper transistor operation, circuit "latching," and/or possible permanent damage to the CA3600E.

Note: Users should observe the "Considerations in Handling CA3600E Devices", discussed on page 13.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	TYPICAL CURVE OR CIRCUIT FIG. NO.	LIMITS			UNIT
				Min.	Typ.	Max.	
For Each p-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=−10 V,V_{GS}=−3.6 V	2,3,4	−0.5	−1.1	−2.0	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=−10 μA	–	–	−1.75	–	V
Gate-to-Source Voltage Differential (p_1 vs. p_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=−100 μA,V_{DS}=−10 V	5	–	±4	±20	mV
Forward Transconductance	g_{fs}	I_D=−1 mA,f=1 kHz	6	–	920	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=−1 mA,f=1 kHz,R_s=0 Ω	7	–	0.03	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=−1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.2	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (p_1/p_2)	I_{MTR}	I_1=−100 μA,V_{DS}=−10 V	30	0.7	1.1	1.5	–
Gate-Terminal Current	I_{GT}	V_{DS}=−10 V,V_{GS}=−3.5 V	–	–	±0.015	−40	nA
Input Capacitance	C_I	–	–	–	6.3	–	pF
Output Capacitance	C_O	–	–	–	3	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.75	–	pF
For Each n-Channel MOS Transistor							
Drain Current	I_D	V_{DS}=+10 V,V_{GS}=+3.6 V	2,3,4	0.4	0.9	1.6	mA
Gate-to-Source Threshold Voltage	$V_{GS(th)}$	I_D=10 μA	–	–	1.5	–	V
Gate-to-Source Voltage Differential (n_1 vs n_2)	$\lvert V_{GS1}-V_{GS2}\rvert$	I_D=100 μA,V_{DS}=+10 V	5	–	±30	–	mV
Forward Transconductance	g_{fs}	I_D=1 mA,f=1 kHz	6	–	860	–	μmho
Low-Frequency Noise Voltage	e_N	I_D=1 mA,f=1 kHz,R_s=0 Ω	7	–	0.2	–	μV $\sqrt{Hz}$
Low-Frequency Noise Current	i_N	I_D=1 mA,f=1 kHz,R_s=1 MΩ	7	–	0.3	–	pA $\sqrt{Hz}$
Current-Mirror Transfer Ratio (n_1/n_2)	I_{MTR}	I_1=100 μA,V_{DS}=+10 V	29	0.7	1.3	2.0	–
Gate-Terminal Current	I_{GT}	V_{DS}=+10 V,V_{GS}=+3.7 V	–	–	±0.01	+40	nA
Input Capacitance	C_I	–	–	–	5.5	–	pF
Output Capacitance	C_O	–	–	–	2.0	–	pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	0.35	–	pF
For Each CMOS Transistor Pair							
Drain Current	I_{DD}	V_{DD}=+10 V	9,10	1.0	2.2	4.0	mA
Drain-to-Source Cutoff Current	$I_{DD(off)}$	V_{DD}=+10 V,V_{SS}=0 V Gate Voltage(V_G)=+10 V or 0 V	8	–	0.5	100	nA
DC Output Voltage	V_O	V_{DD}=+10 V	10	4.2	5.0	5.8	V
Forward Transconductance	g_{fs}	V_{DD}=+10 V, f = 1 kHz	6	–	2300	–	μmho
Slew Rate (Open-Loop)	SR	V_{DD}=+15 V	10	–	95	–	V/μs
Amplifier Voltage Gain	A_{OL}	V_{DD}=+10 V,f=1 kHz,R_b=22 MΩ R_s=50 Ω	10,11	–	32	–	dB
Gate-Terminal Current	I_{GT}	V_{DD}=+10 V	10	–	±0.005	±20	nA
Broadband Output Noise Voltage	E_{ON}	V_{DD}=+10 V,R_b=22 MΩ,R_s=10 kΩ	10,11	–	500		μV
Input Capacitance	C_I	–	–	–	11.8		pF
Output Capacitance	C_O	–	–	–	5.0		pF
Input-to-Output Capacitance	C_{I-O}	–	–	–	1.1		pF

CA3600

TYPICAL CHARACTERISTICS CURVES

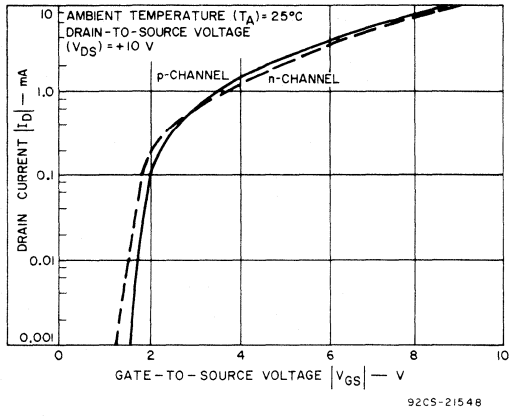


Fig. 2—Drain current vs. gate-to-source voltage.

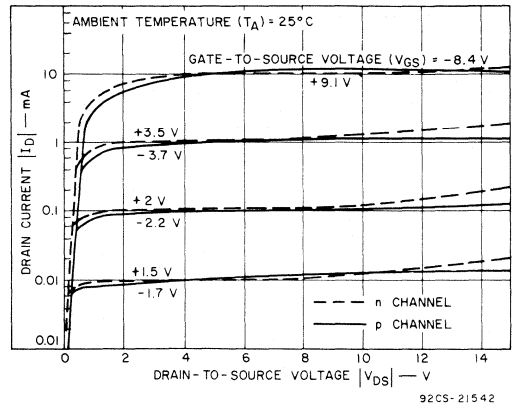


Fig. 3— Drain current vs. drain-to-source voltage.

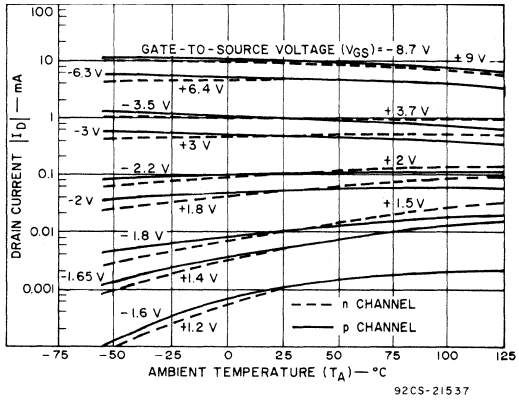


Fig. 4— Drain current vs. ambient temperature.

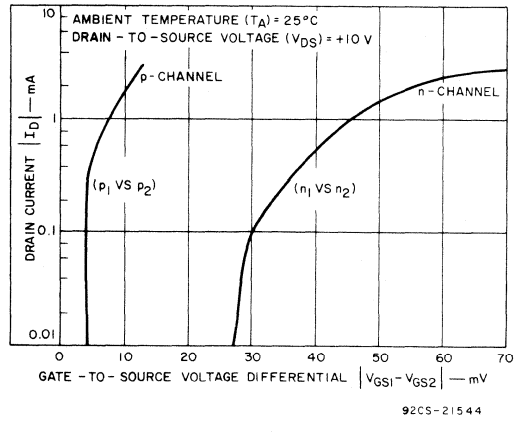


Fig. 5— Gate-to-source voltage differential vs. drain current.

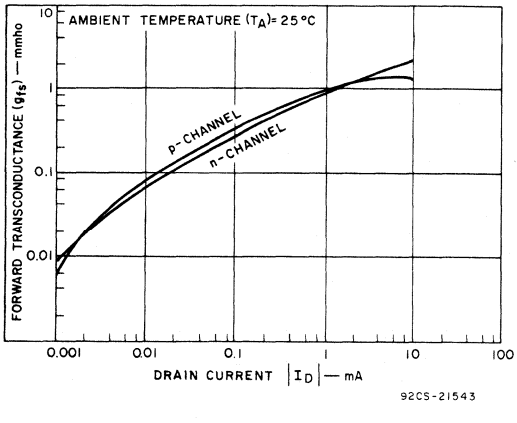


Fig. 6— Forward transconductance vs. drain current.

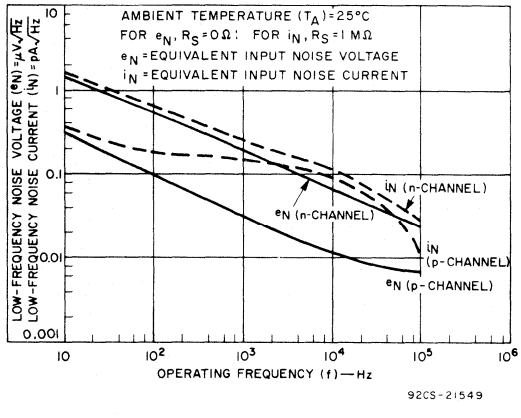


Fig. 7— Noise voltage and noise current vs. operating frequency.

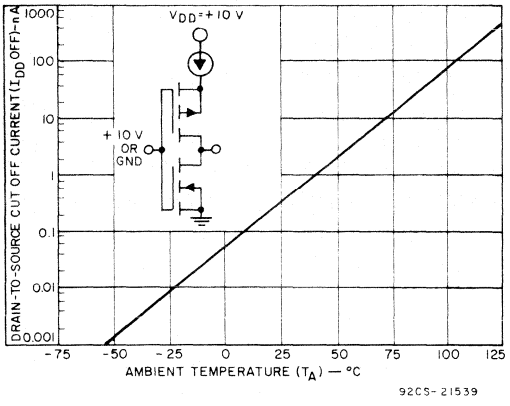


Fig. 8– Drain-to-source cutoff current vs. ambient temperature.

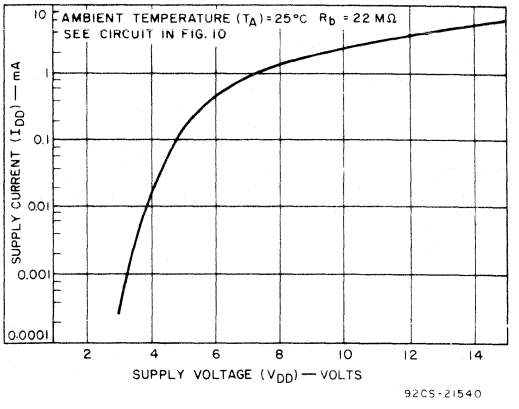


Fig.9 – Typical V_{DD} vs. I_{DD} characteristics for amplifier circuits of Fig.10 and Fig.15.

APPLICATIONS

The Basic CMOS Linear Amplifier

P-n-p and n-p-n bipolar transistors have been used for many years in the design of so-called "true-complementary" linear amplifier circuits[1]. Since mutually compatible p-channel and n-channel MOS FET devices were not generally available, "true-complementary" amplifier circuits using MOS transistors were seldom used. Now, CMOS transistor technology[5] has made it possible to supply compatible p-channel/n-channel transistors in monolithic IC form such as the CA3600E CMOS transistor array shown in Fig. 1.

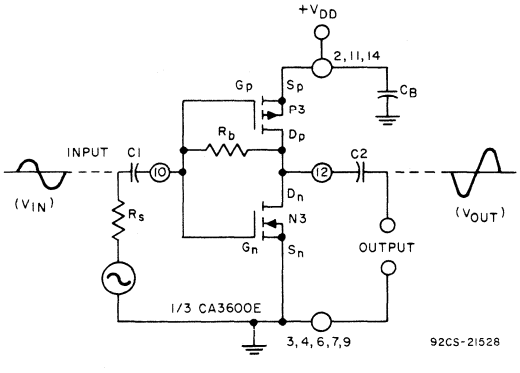


Fig. 10– CMOS transistor-pair biased for linear-mode operation.

A "True-Complementary" Linear Amplifier Using CMOS Transistors

Fig. 10 shows the schematic diagram of a single-stage "true-complementary" linear amplifier using one pair of the complementary MOS transistors in the CA3600E, connected in a common-source circuit. Resistor R_b is used to bias the complementary pair for Class A operation, as described subsequently, and R_s represents the source resistance of the signal source. This generic amplifier is suitable for operation with a single or split voltage supply in the range of 3 to 15 volts. Fig. 11 shows voltage gain as a function of operating frequency at various supply voltages for the single-stage amplifier. This amplifier is capable of producing very high output-swing voltages (V_{out}); for example, its output voltages can be swung to within several millivolts of either supply-voltage "rail". Fig. 9 shows typical supply voltage (V_{DD}) vs. supply current (I_{DD}) characteristics for the single-stage amplifier. The curves in Fig. 12 show the normalized amplifier supply current as a function of ambient temperature at various supply voltages. When the amplifier is operating at V_{DD} = 3 V, the supply current changes rapidly as a function of temperature because the MOS transistors are operating in the proximity of their individual gate-source threshold voltages.

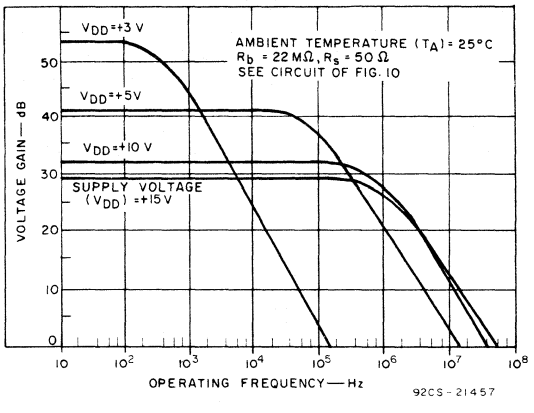


Fig. 11– Typical voltage gain vs. frequency characteristics for amplifier circuit of Fig. 10.

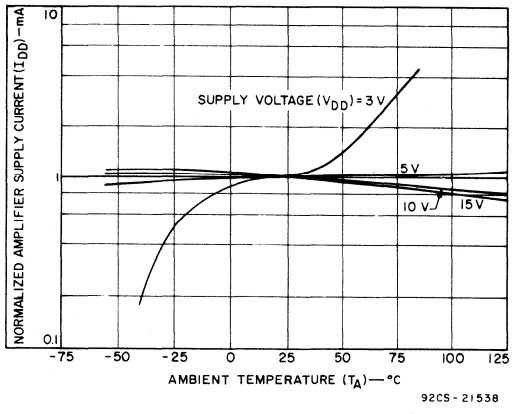


Fig. 12– Normalized amplifier supply current vs. ambient temperature characteristics for amplifier circuit of Fig. 10.

Voltage-Transfer Characteristics

Fig. 13 illustrates a voltage-transfer characteristic curve of a CMOS transistor pair connected in the amplifier circuit of Fig. 10, with a biasing resistor (R_b) connected between the drain and gate terminals (10,12). If the p- and n-channel transistors have identical characteristics, their channel resistances are equal, and the biasing method shown establishes a steady-

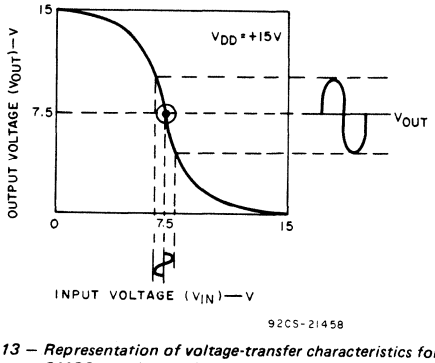


Fig. 13 – Representation of voltage-transfer characteristics for CMOS transistor pair.

state condition such that terminal 12 is at mid-potential between V_{DD} and ground. Thus, with negligibly small gate-source leakage resistances, under zero-signal conditions, the biasing resistor (R_b) establishes gate potential at the mid-point between V_{DD} and ground, i.e., $V_{in} = V_{out}$. Under these conditions the amplifier is biased for operation about the mid-point ("0") in the linear segment on the steep transition of the voltage-transfer characteristic as shown in Fig. 13. When the input signal (V_{in}) swings in the positive direction, there is a reduction in the instantaneous output voltage (V_{out}) with respect to ground. Negative-going input signals have inverse effects. Thus, phase-inversion occurs in the CMOS-pair amplifier. Power-supply current is constant during dynamic linear operation, i.e., Class A amplifier service. When t signal input-voltage level (V_{in}) becomes very large, the outp signal (V_{out}) waveforms become distorted because the tra sistors are driven into the non-linear portions of their volta transfer characteristics. If the positive-going input-signal sufficiently large, for example, the p-channel transistor can driven to cutoff and the amplifier supply current (I_{DD}) reduced to essentially zero.

Fig. 14 shows typical voltage-transfer characteristics of eac CMOS pair in the CA3600E at several values of V_{DD}. Th shape of these transfer characteristics is comparatively consta despite temperature changes from –55 to +125°C.

The biasing arrangement used in the circuit of Fig. 10 provide an easy method of establishing feedback for ac signals i accordance with the R_b/R_s ratio. When the feedback of a signals is not desirable, the circuit of Fig. 15 may be usec The ac bypass capacitor (C_3) minimizes ac signal feedback

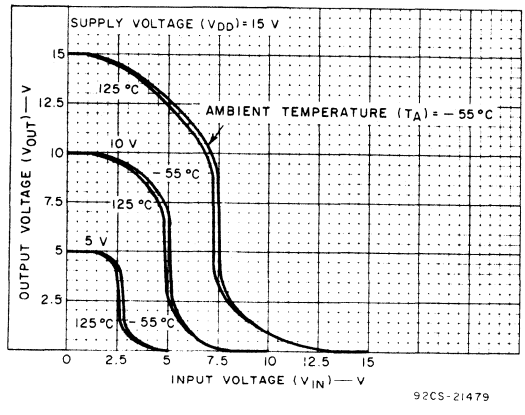


Fig. 14– Voltage transfer characteristics for CMOS transistor-pair amplifier in Fig. 10.

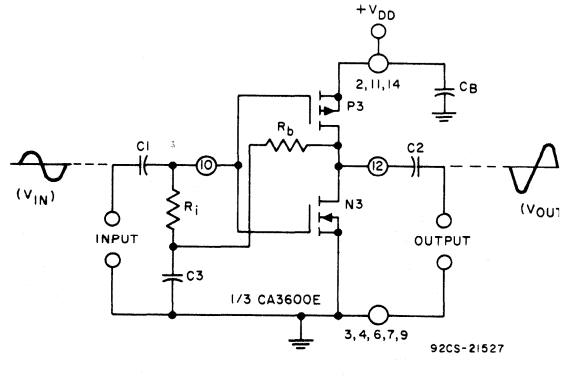


Fig. 15– Alternate method of biasing CMOS transistor-pair for linear-mode operation.

Cascading Amplifier Stages of CMOS Transistor Pairs

Ultra-high-gain amplifiers can be designed by cascading stages of CMOS transistor pairs as shown in Fig. 16. The biasing system used is similar to that described above in connection with Fig. 10. The supply current for the three-stage amplifier shown in Fig. 16 is typically three times the values shown in Fig. 9. Gain and frequency-response characteristics of the amplifier are shown in Fig. 17.

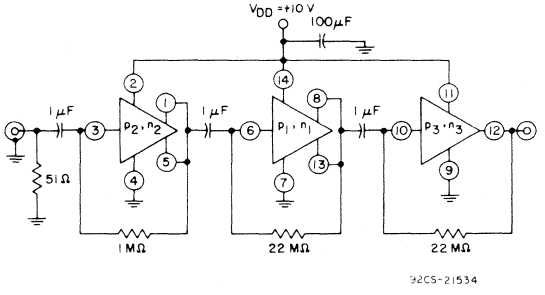


Fig. 16– High-gain amplifier uses cascaded CMOS transistor-pair in CA3600E.

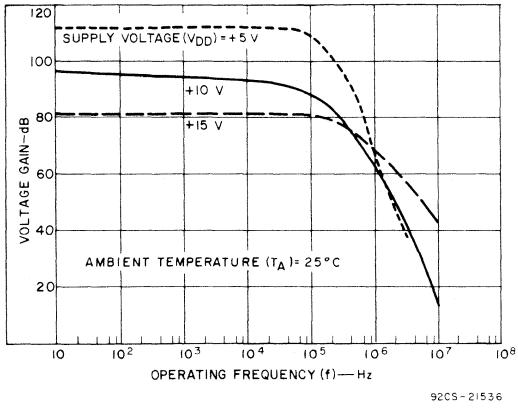


Fig. 17– Typical voltage gain vs. operating frequency characteristics for three-stage CMOS transistor-pair amplifier in Fig. 16.

Post-Amplifiers For Op-Amps

CMOS transistor-pairs can be advantageously applied as post-amplifiers for op-amps. Because the input impedance of the CMOS pair is comparatively high, the op-amp operates under essentially unloaded conditions. Each CMOS pair can sink and source output current up to about 10 mA. Additionally, the op-amp output can be directly coupled to bias the CMOS pair. A detailed description of the subject has been published previously.[2]

The schematic diagram in Fig. 18 shows a CMOS transistor-pair serving as a post-amplifier to an RCA-CA3080 Operational Transconductance Amplifier.[3] The approximate 30-dB gain in a single CMOS transistor-pair is an added increment to the 100-dB gain in the CA3080, yielding a total forward gain of about 130 dB. The open-loop slew rate of the circuit in Fig. 19 is approximately 65 V/μs. When compensated for the unity-gain voltage-follower mode shown in Fig. 19, the slew rate is about 1 V/μs. For greater current output, the two remaining transistor pairs of the CA3600E may be connected in parallel with the single stages shown in Figs. 18 and 19.

The use of the two-stage CMOS post-amplifier shown in Fig. 20 increases the total open-loop gain of the system to about 160 dB (100,000,000X). Open-loop slew rate remains at about 65 V/μs. A slew rate of about 1 V/μs is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 21. These circuits operate in concert with stability.

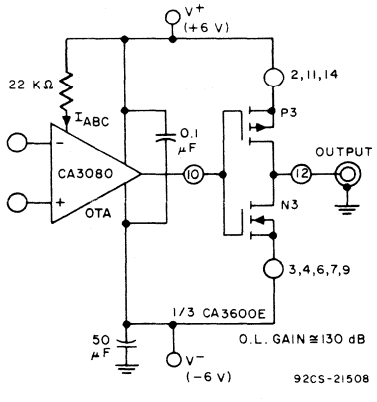


Fig. 18– CMOS transistor-pair used as post-amplifier to op-amp in open-loop circuit.

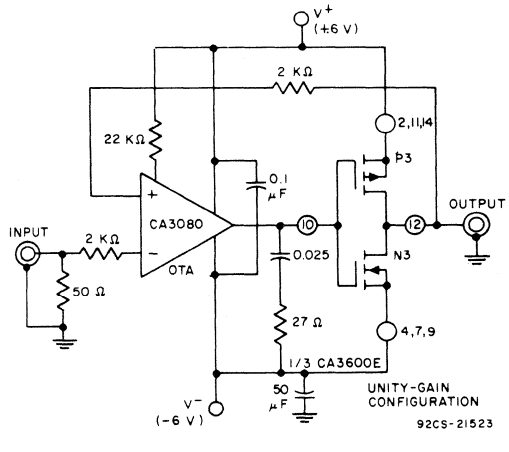


Fig. 19– CMOS transistor-pair used as post-amplifier to op-amp in unity-gain circuit.

CA3600

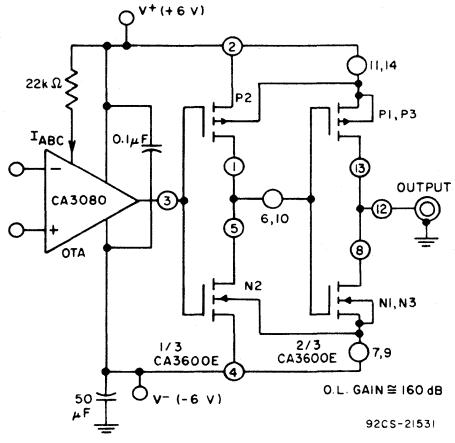


Fig. 20– CMOS transistor-pairs used as two-stage post-amplifier to op-amp in open-loop circuit.

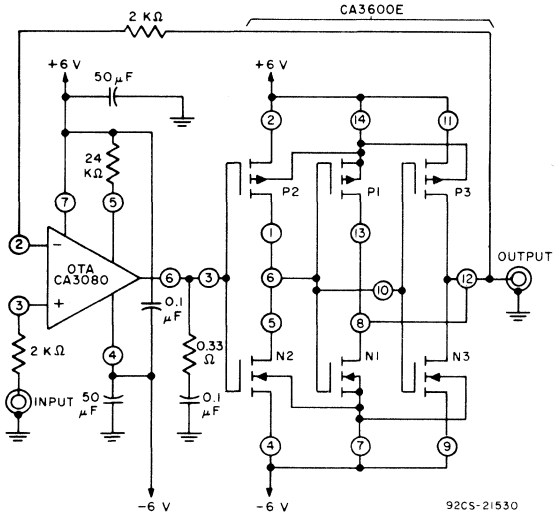


Fig. 21– Unity-gain amplifier uses CMOS transistor-pairs as two-stage post-amplifier to op-amp.

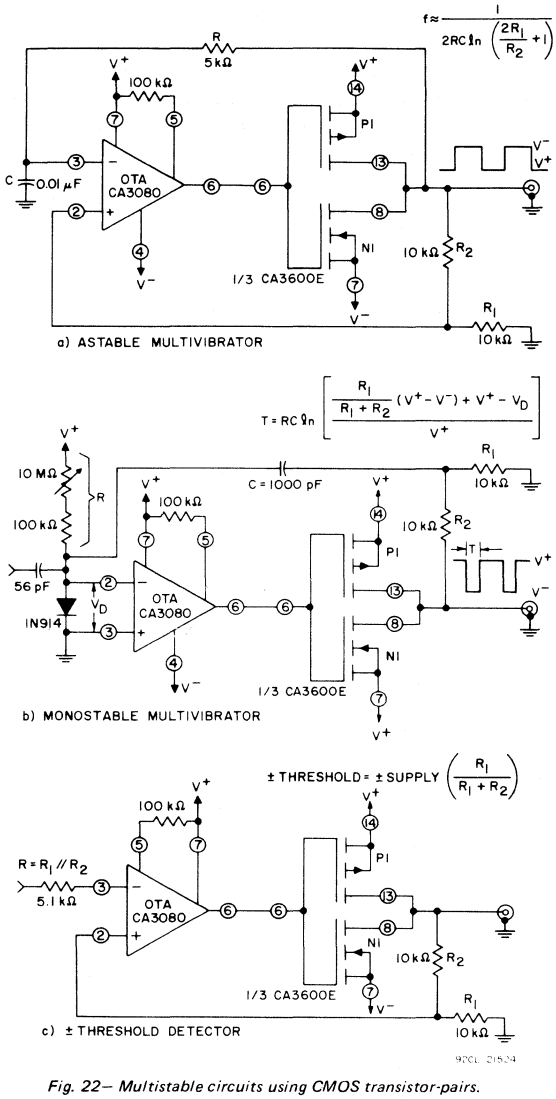


Fig. 22– Multistable circuits using CMOS transistor-pairs.

Multivibrators, Threshold Detectors, and Comparators

Descriptions of several circuits using CMOS transistor-pairs in both monostable and astable multivibrators have been published.[4,5] The characteristics of CMOS pairs are also ideal for mating with micropower op-amps in circuits such as the precision multistable circuits shown in Fig. 22. In these circuits precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080 Operational Transconductance Amplifier.[2,3] Moreover, speed vs. power consumption tradeoffs can be made by adjustment of the Amplifier-Bias-Current (I_{ABC}) supplied to terminal 5 of the CA3080. The quiescent power consumption of the circuits shown in Fig. 22 is typically 6 mW, but can be made to operate in the micropower region by suitable modifications.

The schematic diagram of a programmable micropower comparator, shown in Fig. 23 employs the combination of an op-amp (CA3080A) and COS/MOS transistor-pairs in the CA3600E. Quiescent power consumption of the circuit is about 10 μW(typ.). When the comparator is strobed "ON", transistor P1 is driven into conduction and the OTA becomes active. Under these conditions, the circuit consumes 420 μW and responds to a differential-input signal in about 8 μs. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 ns but the power consumption is increased to 21 mW. The differential amplifier input common-mode range for this circuit is −1 V to +10.5 V. Voltage gain of this micropower comparator is typically 130 dB

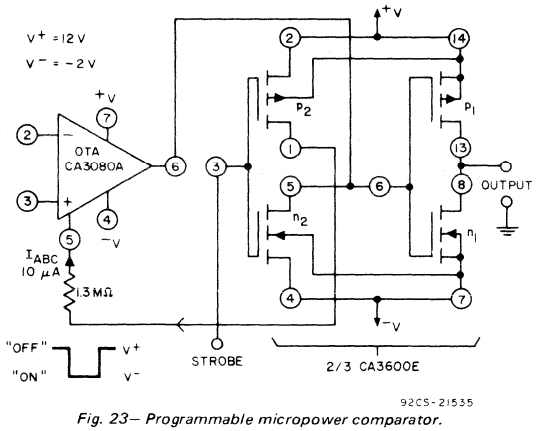


Fig. 23— Programmable micropower comparator.

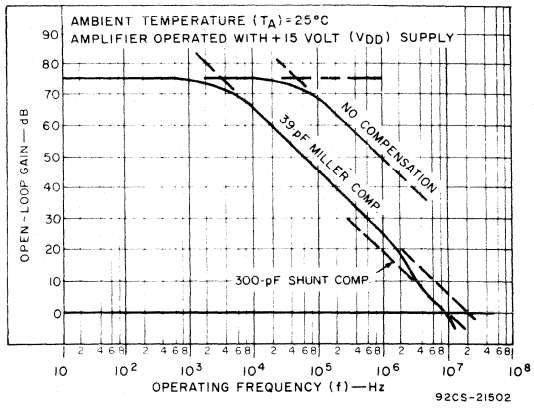


Fig. 25— Open-loop gain characteristic for op-amp in Fig. 24.

Operational Amplifiers

CMOS transistor-pairs can be used in conjunction with a bipolar transistor-array IC to build an op-amp as shown in Fig. 24. It is particularly suited for single-supply operation (e.g., mobile and aircraft service). The op-amp is unique in that it is responsive to small-signal ground-referenced inputs and the output stage can easily be driven within 1 mV of ground potential. Its open-loop gain characteristics are shown in Fig. 25; the open-loop slew rate is approximately 30 V/μs.

This circuit is ideal for use as a unity-gain voltage-follower and has been described for operation in connection with a 9-Bit Single-Supply Digital-to-Analog Converter (DAC) using **CMOS transistors in the resistor-network switches.**[6]

The op-amp in Fig. 24 has three stages; its first stage is a differential input circuit using two p-channel transistors (P_4,P_5) in a CA3600E. The second stage is an n-p-n

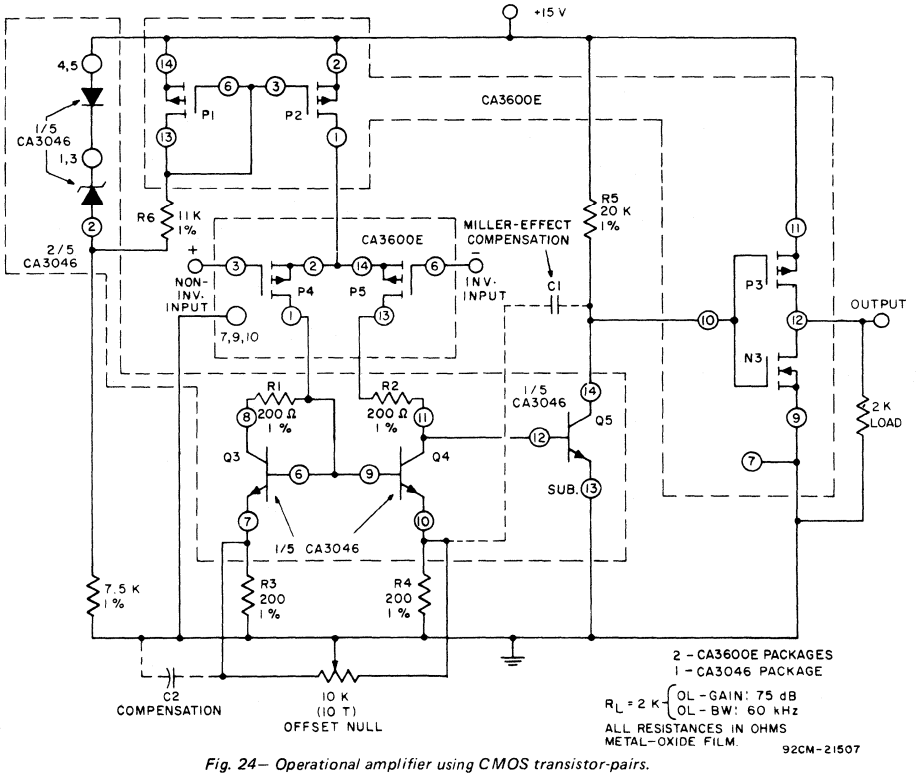


Fig. 24— Operational amplifier using CMOS transistor-pairs.

transistor (Q_5) and the output stage is a CMOS transistor-pair (P_3,N_3) operating in the manner described above. A constant current of about 400 μA is established in the differential input stage by the zener network in the upper-left portion of Fig. 24. The zener network energizes a current mirror comprised of two p-channel transistors (P_1,P_2) to establish constant-current flow in the differential amplifier stage (P_4,P_5). The drain load for the differential amplifier consists of resistors R_1,R_4 and a current mirror (Q_3,Q_4) to optimize conditions for balanced operation of the differential amplifier. The operating theory of current-mirror circuits has been described in reference.[2] Amplifier voltage-offset is nulled with the 10-kilohm balance potentiometer. The second-stage current is established by R_5, and is selected to approximate the first-stage current level (400 μA), to assure similar positive and negative slew rates. The amplifier is shown driving a 2-kilohm load, a typical value used with monolithic op-amps. Voltage gain varies inversely with the choice of load resistance.

The amplifier can be compensated with a single capacitor (C_1), connected as shown by the dotted lines. However, optimum compensation for the unity-gain non-inverting mode is provided by two capacitors: Miller Effect feedback through a 39-pF capacitor C_1 (connected as shown), and a 300-pF capacitor connected between terminals 7 and 13 of the CA3046 transistor array to shunt one-half the driving current. Fig. 25 shows the open-loop gain characteristics with compensation for unity-gain operation. When the amplifier is operated as a voltage-follower, it is recommended that a 1-kilohm resistor, shunted with a 150-pF capacitor, be connected between the amplifier output terminal and terminal 6 of P_5 to avoid a potential latch situation involving the integral gate-protection network. The circuit can also be latched if either input terminal is driven more than about 0.7 volt below ground potential. This latch situation can be avoided by connecting a 1N914 diode from each input terminal to ground, with the diode anode grounded.

Analog Timer

The CA3600E is useful in the design of analog timer circuits. A typical circuit is shown in Fig. 26. For purposes of explanation, let it be assumed that capacitor C_1 initially is in a completely discharged condition; terminal 10, therefore, is initially at ground potential and transistor N_3 is non-conductive. The circuitry at the left of terminal 10 provides a source of constant-current flow through P_1 to charge capacitor C_1 increasingly positive with respect to ground. After the passage of time (T), capacitor C_1 is charged sufficiently in the positive direction so that transistor N_3 is driven into conduction by its gate and the lamp is lighted to signify the end of the time-delay period. The circuit is reset by momentarily closing switch S_1 to discharge capacitor C_1 through R_4.

Resistor-divider network R_1,R_2 establishes the supply voltage to a constant-current network comprised of resistor R_3 and the series-connected COS/MOS pair N_2,P_2, biased for linear operation by resistor R_b as previously described. This combination is connected to the gate terminal (No. 6) of transistor P_1 to form a current mirror, i.e., the current flowing through P_1 to charge C_1 will be essentially equal to the constant-current flow established through R_3, N_2, and P_2. A description of current-mirror operation with MOS transistors is given subsequently.

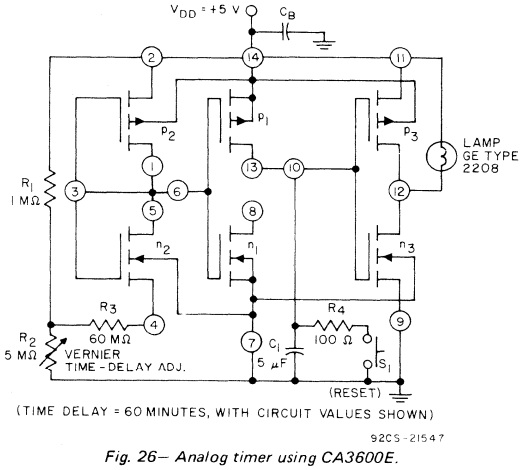


Fig. 26– Analog timer using CA3600E.

Oscillator Circuits

Oscillator circuits using CMOS transistor-pairs have been widely used for several years in clock and watch circuits because of their low power consumption and good frequency stability. Details of their operating theory and characteristics have been published.[5,7]

The design of CMOS oscillator circuits, like the design of any oscillator circuit, involves the provision of an amplifying section to operate compatibly with an appropriate feedback network. A single-stage amplifier using a CMOS transistor-pair has already been described. A suitable feedback network to insure stable oscillator performance is easily added, as illustrated in connection with the crystal oscillator circuit shown in Fig. 27. The familiar pi-network has been connected between the input and output terminals, points "D" and "G", to provide the required 180° phase shift for stable oscillator performance. The frequency-determining crystal is an integral part of the pi-network feedback circuit. The resistors R_1 and R_2 decrease the total power consumption of the oscillator at a particular supply voltage and enhance the frequency stability. Variable frequency oscillators can be built by replacing the crystal with an appropriate inductance and tuning the pi-network by conventional means.

Current Mirrors Using MOS Transistors

Monolithic linear IC's using bipolar transistors frequently employ so-called "current-mirror" circuits. The theory and practical applications of current mirrors using bipolar transistors have been described in the literature.[2] As shown in

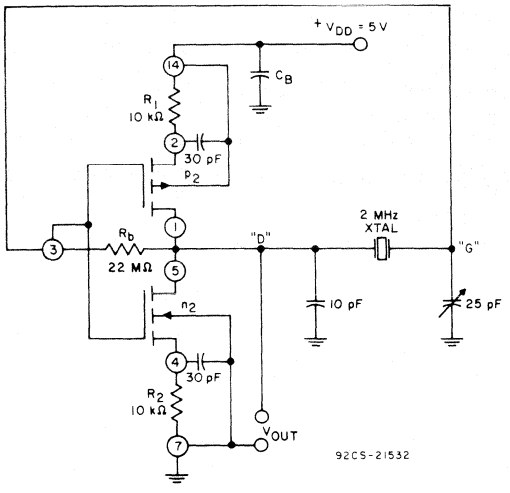


Fig. 27– Typical crystal-oscillator circuit using CMOS transistor-pair (1/3 CA3600E).

Fig. 28, a rudimentary form of "current-mirror" consists of a transistor Q_1 with a second transistor Q_2 connected as a diode. When both transistors have identical characteristics, a current I_1 forced to flow through Q_2 produces a current (I_2) of equal magnitude to flow in the collector of Q_1 (provided there is sufficient collector potential for Q_1). In a common form of application, a source of potential is used to force

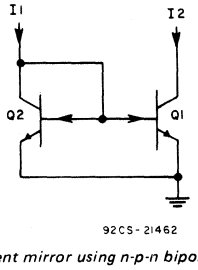


Fig. 28– Current mirror using n-p-n bipolar transistors.

constant-current flow I_1, and thus to establish the flow of constant current I_2 through Q_1. Arrangements of this generic current-mirror type are frequently used when Q_1 acts as the common-emitter impedance in a differential-amplifier circuit.

MOS transistors are also applicable as current mirrors, as shown in Fig. 29. The diode-connected MOS transistor N_2 functions as a transistor with 100 per-cent feedback. Therefore, the gate-to-source voltage (V_{GS}) in N_2 retains control of the drain current as in normal transistor action, i.e., $I_D \cong g_{fs}V_{GS}$, where g_{fs} is the forward transconductance of the device. If a current I_1 is forced into the diode-connected transistor (N_2), the gate-to-source voltage will rise until equilibrium is reached. Thus, a gate-to-source voltage is established in N_2 such that N_2 "sinks" the applied current I_1.

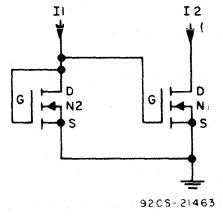


Fig. 29– Current mirror using n-channel MOS transistors.

If the gate and source terminals of another transistor (N_1) are connected in shunt with the gate and source terminals of N_2, as shown in Fig. 29, N_1 is also able to "sink" a mirror current approximately equal to that flowing in the drain lead of the diode-connected transistor N_2. It is assumed that both MOS transistors have identical characteristics, a prerequisite that is essentially established by the monolithic IC fabrication technology used in manufacturing the CA3600E CMOS transistor array.

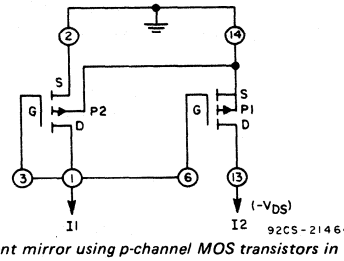


Fig. 30– Current mirror using p-channel MOS transistors in CA3600E.

Current mirrors can also be designed with p-channel MOS transistors as illustrated by the arrangement in Fig. 30 using transistors in the CA3600E. The characteristics of a current mirror using the p-channel transistors in the CA3600E are superior to those which can be achieved with a current mirror using the n-channel transistors because the characteristics of the p-channel transistors are more nearly matched. The data

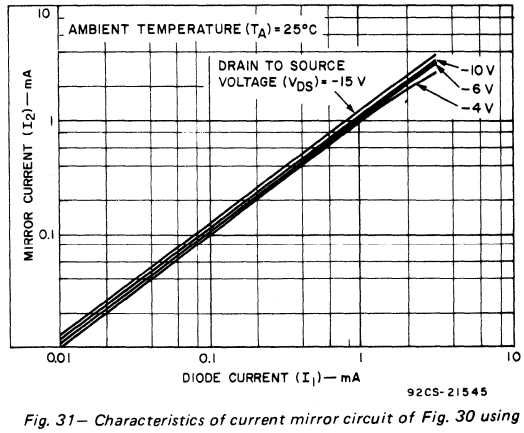


Fig. 31– Characteristics of current mirror circuit of Fig. 30 using p-channel transistors.

contained in Fig. 31 show the high degree of tracking between I_1 and I_2 for several values of drain voltage V_D. Fig. 32 also illustrates the fact that this high degree of tracking between I_1 and I_2 can be maintained to within about one per-cent despite wide variations in ambient temperature.

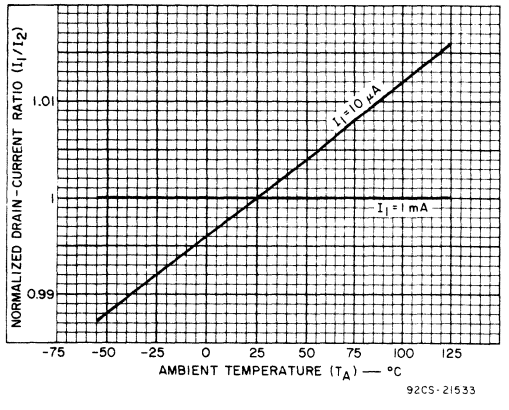


Fig. 32— Normalized drain current ratio vs. ambient temperature for typical current mirror using p-channel transistors (Fig. 30).

The op-amp circuit in Fig. 24 contains an illustrative example of a current-mirror circuit using two p-channel transistors in the CA3600E. Transistor P_2 serves as a constant-current source (≅ 400 μA) for the differential amplifier, consisting of transistors P_4 and P_5 and their drain-load network. Transistor P_2 is in a "mirrored" connection with transistor P_1. A stabilized source of supply potential is developed across the zener diode (terminals 11 and 12 of the CA3083) and drives about 400 μA of current through R_6 and P_1.

Complementary Current Mirrors Using CMOS Transistor-Pairs

CMOS transistor-pairs can be applied advantageously in the design of Complementary Current-Mirrors, as shown in Fig. 33. Transistors P_1 and N_1 are series-connected and biased for linear operation as previously described, so that there is a current flow I_{D1} through P_1 and N_1. The potential developed between terminals 13 and 14 is applied as gate-source (2,3) voltage for P_2, forcing "mirror" operation of P_2 to produce a current source $I_{D2\text{-}P}$ equal to I_{D1}. Likewise, the potential developed between terminals 7 and 8 is applied as gate-source (3,4) voltage for N_2 forcing "mirror" operation of N_2 to produce a current-sink $I_{D2\text{-}N}$ equal to I_{D1}.

A variant of this complementary current mirror is used in the analog timer circuit shown in Fig. 26. Transistors P_2 and N_2 are series-connected together with a 60-megohm resistor to establish their drain current at 5 nA. The potential developed across terminals 1 and 2 also appears as the gate-source voltage for transistor P_1, thereby establishing a mirror-current source of 5 nA at terminal 13 to charge capacitor C_1 linearily. In this circuit, the "mirrored" current-sink available at terminal 8 (transistor N_1) is unused. This type of current-mirror configuration is exceptionally stable with temperature variations.

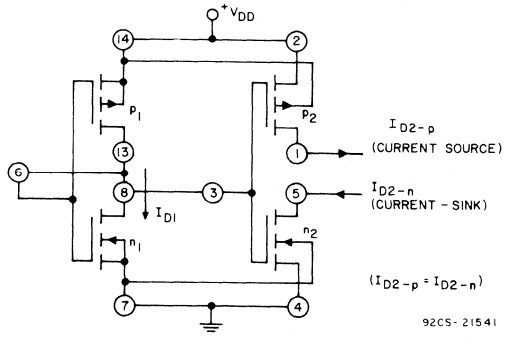


Fig. 33— Complementary current mirrors using CMOS transistor-pairs in CA3600E.

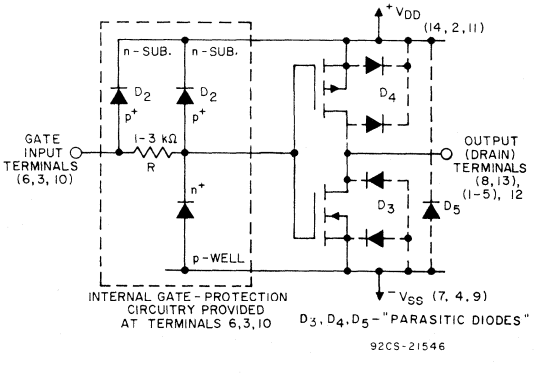


Fig. 34— Integral protection circuits used in CA3600E.

Considerations in Handling CA3600E Devices

Failure of the gate-channel oxide was a persistent problem in early MOS devices. The breakdown of the oxide is generally in the order of 100 volts, and the dc resistance is in the order of 10^{12} ohms. Because of this extremely high resistance, even a very-low-energy source (such as static charge) is capable of developing sufficient voltage to cause damage. Furthermore, the oxide can be punctured and damaged by a single voltage excursion beyond the breakdown limit.

Fig. 34 shows a protection circuit[5,8] which is incorporated at each gate-lead of the CA3600E. A typical value of 1 to 3 kilohms is used for the input resistor R, which functions in combination with the capacitance of the gate and the associated protective diode to integrate and clamp input voltages to a safe level. This circuit also shows the "substrate diodes" (D_3, D_4, and D_5) which provide protection to the MOS channels at the output terminals.

Although the gate-protection system is very effective in guarding against damage due to static charges, it is prudent to observe the following precautions:[5,9]

1. The leads of devices should be in contact with a conductive material, except when being tested or in actual operation. A conductive material such as "ECCOSORB LD26"* or equivalent is suggested for use during storage and/or handling. Devices should not be inserted in non-conductive containers such as conventional plastic "snow" or trays.
2. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
3. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
4. Signals from low-impedance sources should not be applied to the gate terminals while the power supply is off. As a corollary, it follows that the power supply should not be turned off while a signal from a low-impedance source is being applied to any gate terminal. When the V_{DD} supply is off, the positive "back-bias" voltage is removed from the cathode of diode D_2 (see Fig. 34). Consequently, an input signal with positive-going polarity can drive D_2 into conduction. Under these conditions a low-impedance signal source can provide sufficient current to permanently damage D_2 and/or melt aluminum interconnection paths. Therefore, if, in any system design using the CA3600E, any gate input excursion is expected to exceed $+V_{DD}$ or fall below $-V_{SS}$, the current through the input diodes should be limited to 100 μA.
5. All unused gate-input terminals should be connected to V_{SS} (ground). When source terminals (e.g., Nos. 2 and 11) of p-channel transistors are unused in circuitry, they should be connected to terminal No. 14. Likewise, when source terminals (e.g., Nos. 4 and 9) of n-channel transistors are unused, they should be connected to terminal No. 7.
6. After CA3600E units have been mounted on circuit boards, proper handling precautions should still be observed. Until these subassemblies are inserted into a complete system, the board is no more than an extension of the device leads mounted on the board. It is a good practice to place conductive tape or jumpers on circuit-board terminals to "ground" gate terminals.
7. In some applications of the CA3600E separate positive and negative power supplies may be employed (e.g., see Fig.22). In such applications provisions must be made so that the positive supply voltage is applied prior to the application of negative supply voltage and vice versa on shutdown. This precaution is necessary to avoid possible damage due to "latching" involving the substrate and protective diode circuits.

* Trade Mark: Emerson and Cumming, Inc.

Automotive Circuits — Technical Data

Type No.	Description	Page No.
Engine and Drive Train Controls		
CA324	Quad operational amplifier	204
CA339	Quad voltage comparator	437
CA358	Dual operational amplifier	210
CA3165	Electronic switching circuit	727
CA3169	Solenoid and Motor Driver	595
CA3219A	Quad-Power NAND Driver	603
CA3242	Quad-Gated Inverting Power Driver	606
CA3252	Quad-Gated Non-Inverting Power Driver	610
CD4538B	CMOS Dual Precision Monostable Multivibrator	—
CDP1802A	8-Bit Microprocessor	—
CDP1804A	8-Bit Microcomputer	—
CDP1805A	8-Bit Microprocessor	—
CDP6805E2	8-Bit Microprocessor	—
CDP6805E3	8-Bit Microprocessor	—
CDP6805F2	8-Bit Microcomputer	—
CDP6805G2	8-Bit Microcomputer	—
CDP6823	Parallel Interface	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05C4	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68A1	SPI A/D Converter	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—
Features (Optional Equipment)		
CA3169	Solenoid and Motor Driver	595
CA3219A	Quad-Power NAND Driver	603
CA3228	Speed Control System	733
CA3232	÷20 Prescaler	828
CA3242	Quad-Gated Inverting Power Driver	606
CA3252	Quad-Gated Non-Inverting Power Driver	610
CA3259	Stereo Sound Volume/Tone Control	832
CD4517B	CMOS Dual 64-Stage Static Shift Register	—
CD40106B	CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC05F2	8-Bit Microcomputer	—
Multiplex Communications		
CD4016B	CMOS Quad Bilateral Switch	—
CD4006B	CMOS 18-stage Static Shift Register	—
CD4512B	CMOS 8-Channel Data Selector	—
CD54/74HC/HCT157	Quad 2-Input Multiplexer	—
CD54/74HC/HCT257	Quad 2-Input Multiplexer, 3-State	—
CDP1802A	8-Bit Microprocessor	—
CDP1804A	8-Bit Microcomputer	—
CDP1805A	8-Bit Microprocessor	—
CDP1863	8-Bit Programmable Counter	—
CDP6402	Programmable UART	—
CDP6823	Parallel Interface	—
CDP6853	Asynchronous Communications Interface Adapter	—
CDP6805E2	8-Bit Microprocessor	—
CDP6805E3	8-Bit Microprocessor	—
CDP6805F2	8-Bit Microcomputer	—
CDP6805G2	8-Bit Microcomputer	—
CDP65C51E1	Asynchronous Communications Interface Adapter	—
CDP65C51E2	Asynchronous Communications Interface Adapter	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC04P2	8-Bit Microcomputer	—

Automotive Circuits (Cont'd)

Type No.	Description	Page No.
Multiplex Communications (Cont'd)		
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC68A1	SPI A/D Converter	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—
Body Computer		
CD54/74HC/HCT00	Quad 2-Input NAND Gate	—
CD54/74HC/HCT244	Octal Buffer/Line Driver; 3-State	—
CD54/74HC/HCT245	Octal Bus Transceiver; 3-State	—
CD54/74HC/HCT373	Octal Transparent Latch; 3-State	—
CD54/74HC/HCT374	Octal D-Type Flip-Flop; Positive-Edge Trigger; 3-State	—
CDM5364	8K x 8 ROM	—
CDM5365	8K x 8 ROM	—
CDM6116	2K x 8 RAM	—
CDM6264	8K x 8 RAM	—
CDM53128	16K x 8 ROM	—
CDM53256	32K x 8 ROM	—
CDP1851	Programmable I/O Interface	—
CDP1852	Byte-Wide I/O Port	—
CDP1855	8-Bit Programmable Multiply/Divide Unit	—
CDP1863	8-Bit Programmable Counter	—
CDP6818	Real Time Clock, MOTEL Bus	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05C4	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—
CDP68HC68T1	SPI Real-Time Clock	—
Entertainment		
CA3088	AM Receiver Subsystem and general purpose amplifier array	781
CA3089	FM IF System	785
CA3130	BiMOS OpAmp	292
CA3189	FM IF System	804
CA3195	RC Phase-Lock-Loop Stereo Decoder	810
CA3202	TV Horiz./Vert. Countdown Digital Sync System	1020
CA3209	FM IF System	820
CD4052	CMOS Analog Multiplexer/Demultiplexer	—
CDP6818	Real Time Clock, MOTEL Bus	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68R2	SPI RAM 256 Bytes	—
CDP68HC68T1	SPI Real Time Clock	—
Driver Information/Display		
LCD		
CD4054B	4-Segment Display Driver	—
CD4055B	BCD-to-7 Segment Decoder/Driver with Display freq. output	—
CD4056B	BCD-to-7 Segment Decoder/Driver with Strobed-latch function	—
CD4543B	BCD-to-7 Segment Decoder/Driver with Strobed-latch function	—
CD7211	Four-Digit LCD Decoder/Driver	174
CD7211A	Four-Digit LCD Decoder/Driver	174
CD7211M	Four-Digit LCD Decoder/Driver	179
CD7211AM	Four-Digit LCD Decoder/Driver	179
CD54/74HC/HC74543	BCD-to-7 Segment Latch/Decoder/Driver	—
LED		
CA3081	Common-emitter transistor array	151
CA3082	Common-collector transistor array	151
CA3083	High-Current NPN Transistor Array	658
CA3161	BCD-to-7-Segment Decoder/Driver, Current Output Driver, common anode	154

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Type No.	Description	Page No.
LED (Cont'd)		
CA3168	Dual BCD-to-7-Segment Decoder/Driver, common anode	158
CA3250	Common-emitter array	171
CA3251	Common-collector array	171
CD4026B	Decade counter/divider with 7-segment display outputs and display enable	—
CD4033B	Decade counter/divider with 7-segment display outputs and ripple blanking	—
CD4511B	BCD-to-7-Segment Latch Decoder Driver	—
CD54/74HC/HCT4511	High-Speed version of the CD4511B	—
CD40110B	Decade Up-Down Counter/Latch/Display Driver	—
Incandescent		
CA3081	Common-emitter transistor array	151
CA3082	Common-collector transistor array	151
CD4026B	Decade Counter/Divider with 7-segment display outputs and display enable	—
CD4033B	Decade counter/divider with 7-segment display outputs and ripple blanking	—
CD4511B	BCD-to-7 Segment Latch Decoder Driver	—
CD54/74HC/HCT4511	High-Speed Version of the CD4511B	—
CD4041UB	Quad true/complement buffer	—
CD4049UB	Hex buffer/converter (inverting)	—
CD54/74HC/HCT4049	High Speed Version of the CD4049UB	—
CD4050B	Hex buffer/converter (non-inverting)	—
CD54/74HC/HCT4050	High Speed Version of the CD4050B	—
CD40107B	Dual 2-Input NAND buffer/driver	—
Vacuum Fluorescent		
CA3207	Divide-by-14 counter, 1 of 14 Decoder/Driver for vacuum fluorescent anode drive	162
CA3208	14-Bit shift register with output latch/driver	162
CD4026B	Decade counter/divider with 7-segment display outputs and display enable	—
CD4033B	Decade counter/divider with 7-segment display outputs and ripple blanking	—
CD4511B	BCD-to-7-Segment latch decoder driver	—
CD54/74HC/HCT4511	High speed version of the CD4511B	—
General Purposes		
CD4094B	8-Stage Shift-and-Store Bus Register	—
CDM5364	8K x 8 ROM	—
CDM5365	8K x 8 ROM	—
CDM53128	16K x 8 ROM	—
CDM53256	32K x 8 ROM	—
CDP1863	8-Bit Programmable Counter	—
CDP6818	Real Time Clock, MOTEL Bus	—
CDP68HC04P2	8-Bit Microcomputer	—
CDP68HC04P3	8-Bit Microcomputer	—
CDP68HC05D2	8-Bit Microcomputer	—
CDP68HC68R1	SPI RAM 128 Bytes	—
CDP68HC68R2	SPI RAM 256 Bytes	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices.*

For data on CDPXXXX types, refer to *DATABOOK SSD-260*, CMOS Microprocessors, Memories, and Peripherals, or the specific data bulletin for that type shown in the *Index to Devices.*

CA3165

Electronic Switching Circuit

Features:

- *Switching initiated by damping of internal oscillator*
- *Proximity sensing of rotational motion*
- *Repeatable timing of switching states*
- *Five outputs - two complementary pairs and one non-inverting output (CA3165E1)*
- *Two outputs - one complementary pair (CA3165E)*

The RCA CA3165 is a single-chip electronic switching circuit intended primarily for ignition applications. It includes an oscillator that is amplitude-modulated by the rotor teeth of a distributor, a detector that develops the positive-going modulation envelope, a Schmitt trigger that eliminates switching uncertainties. Both types, CA3165E and CA3165E1, include two complementary high-current switched outputs for driving power transistors requiring up to 120 milliamperes. The CA3165E also includes two complementary low-current outputs that incorporate internal current limiting and a non-inverting output amplifier with uncommitted input capable of switching 27 milliamperes.

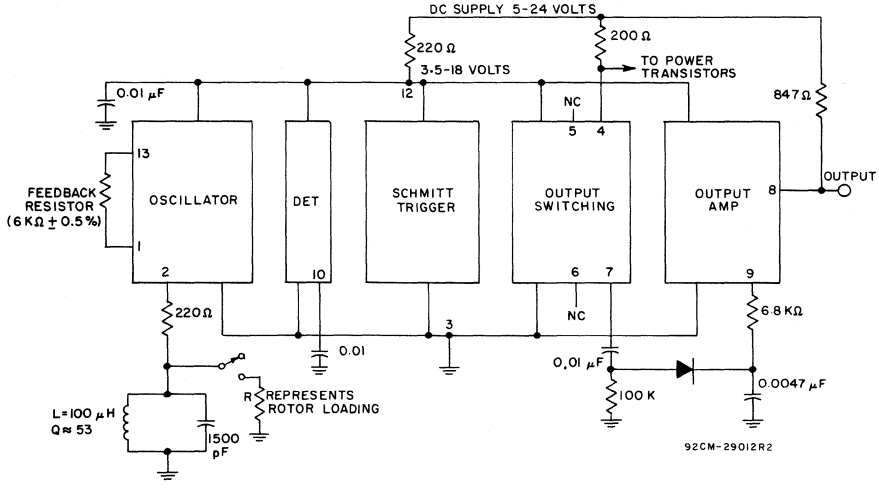
The CA3165 is supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix) and in the 14-lead dual-in-line plastic package (E1 suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3165E1	CA3165E		
DC Voltage (With reference to terminal 3):				
Terminal	4, 6, 8	4, 5	24	V
Terminal	5, 7, 12	7	18	V
Terminal	9	—	1.5	V
CURRENT (At terminals indicated):				
Terminal	4, 6	4, 5	120	mA
Terminal	5, 7	—	-0.1 to 0.1	mA
Terminal	8	—	30	mA
DEVICE DISSIPATION:				
Up to T_A = 55°C				600 mW
Above T_A = 55°C				Derate Linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:				
Operating				-40 to +85°C
Storage				-65 to +150°C
LEAD TEMPERATURE (During soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.				265°C

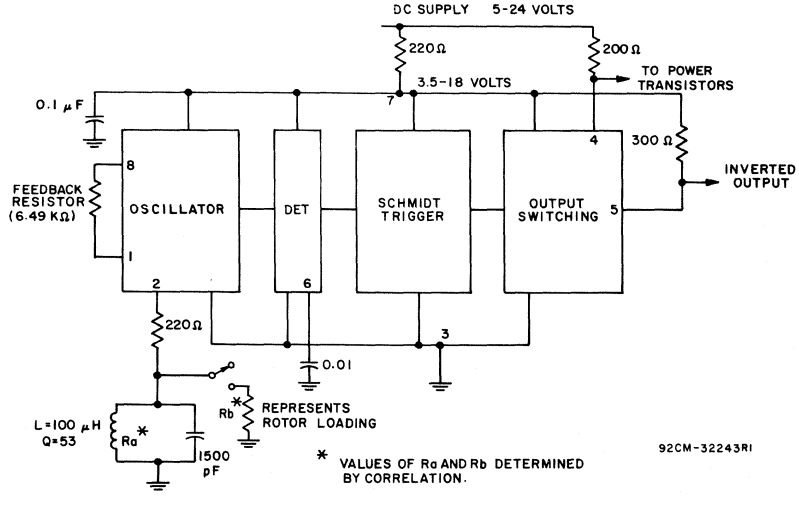
File Number **1278**

CA3165



Oscillator Condition	Terminal 10	Terminal 4	Terminal 5	Terminal 6	Terminal 7	Terminal 8
Unloaded	Low	High	High	Low	Low	Low
Loaded	High	Low	Low	High	High	High

Fig. 1 - Functional block diagram and application circuit for CA3165E1.



Oscillator Condition	Terminal 4	Terminal 5	Terminal 6
Unloaded	High	High	Low
Loaded	Low	Low	High

Fig. 2 - Functional block diagram and application circuit for CA3165E.

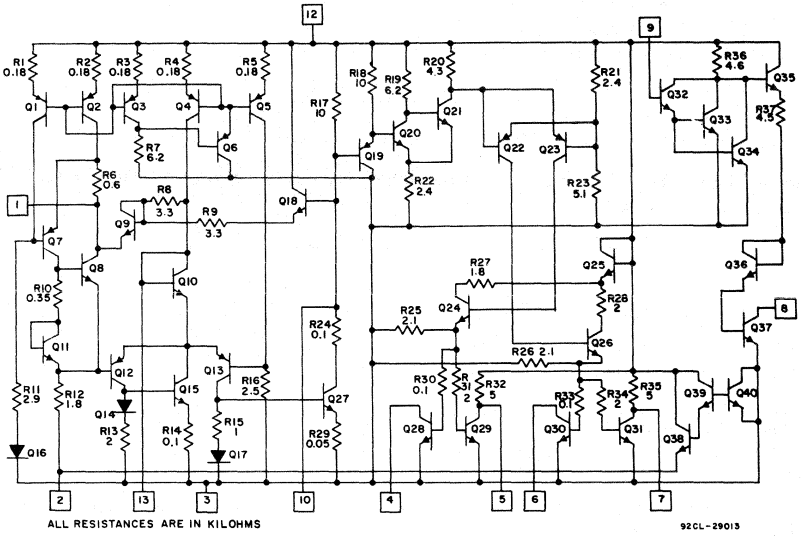


Fig. 3 - Schematic diagram for CA3165E1.

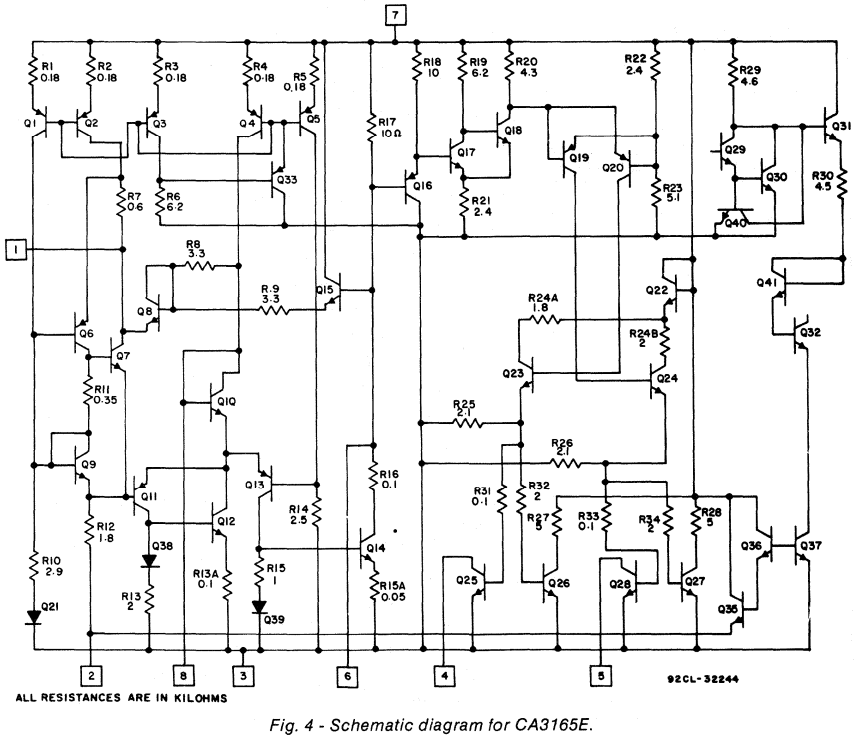


Fig. 4 - Schematic diagram for CA3165E.

CA3165

ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V^+ = 13$ V, Measured in the circuit of Fig. 5 (CA3165E1) or Fig. 6 (CA3165E)

CHARACTERISTIC		TEST PERIOD	LIMITS CA3165E1 Min.	CA3165E1 Typ.	CA3165E1 Max.	CA3165E Min.	CA3165E Typ.	CA3165E Max.	UNITS
Input Current at Term.*	Δ	Dwell	—	18.4	—	—	18.4	—	mA
		Spark	—	17.5	—	—	17.5	—	
Output Voltage at Term. 4	V_4	Dwell	12.8	—	—	12.8	—	—	V
		Spark	—	—	0.5	—	—	0.5	
Output Voltage at Term. 7	V_7	Dwell	—	—	1	—	—	—	V
Output Voltage at Term. 8	V_8	Dwell Portion of Spark	—	—	0.9	—	—	—	V
			1.2	—	—				
Oscillator Voltage at Term. 2	V_2	Dwell	—	4.4	—	—	4.4	—	V_{p-p}
		Spark	—	0.6	—	—	0.6	—	

	*	Δ
CA3165E	7	I_7
CA3165E1	12	I_{12}

APPLICATION INFORMATION

Figs. 5 and 6 shows the application of the CA3165 in a typical ignition system.

TERMINAL DESCRIPTIONS		
Terminal		
CA3165E1	CA3165E	Function
1	1	Oscillator feedback resistor, R_f
2	2	220Ω protective resistor to tank circuit
3	3	Ground
4	4	Direct output — R_7 load resistor 200 ohms ± 5%, and R_8 to power Darlington 15 ohms ± 10%
5	—	Direct output — low current — not connected
6	5	Inverted high current output
7	—	Inverted low current output through C_1 (0.01 μF) to D_3 and R_3 (100 K ohm)
8	—	Output amplifier output — through R_6 and R_5 (27 ohms and 820 ohms to supply)
9	—	Output amplifier input — through R_4 (6800 ohms) to D_3 and C_5 (0.0047 μF)
10	6	Detector output — C_2 to ground (0.0022 μF)
11	—	No connection
12	7	Circuit supply voltage through R_1 (220 ohms protective resistor) to automotive supply
13	8	Oscillator feedback resistor R_f to terminal 1
14	—	No connection

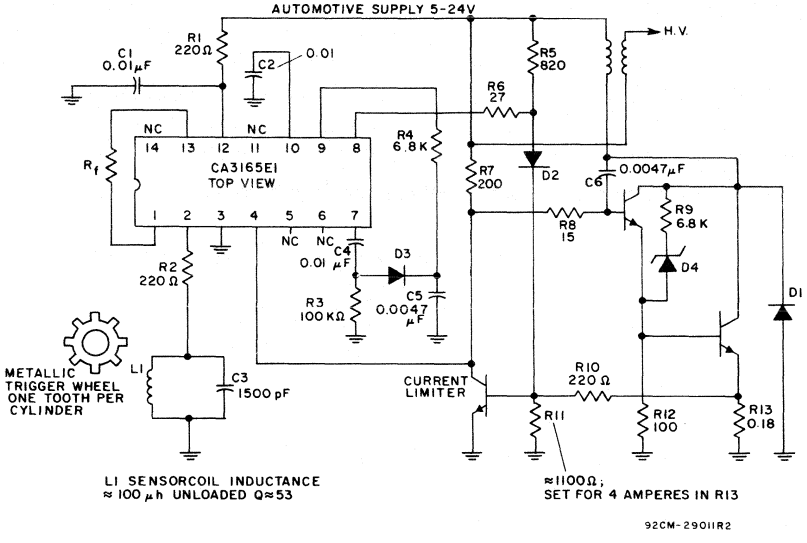


Fig. 5 - Typical ignition system using the CA3165E1.

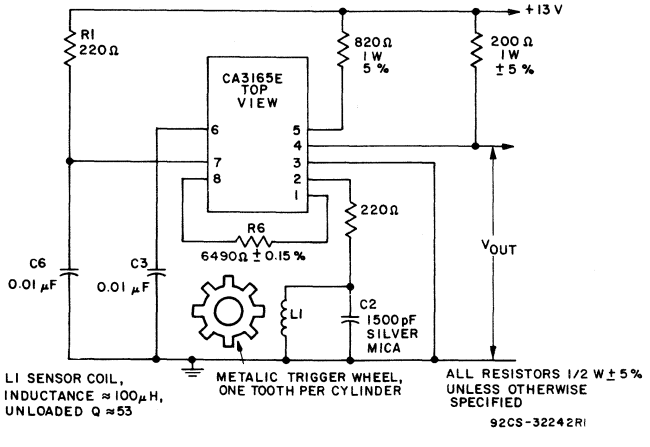


Fig. 6 - Typical ignition system using the CA3165E.

APPLICATION INFORMATION

Figs. 5 and 6 shows the application of the CA3165 in a typical ignition system. The oscillator on the chip operates at about 400 kHz as determined by the tuned circuit L1, C3. The amplitude of the oscillation is detected on the chip and applied to a Schmitt trigger which sets the terminal voltage as shown in the chart in Figs. 1 and 2 for the unloaded condition of the oscillator. As a metallic tooth in the rotor passes the coil L1 eddy-current losses occur which reduce the Q of the resonant circuit and decrease the amplitude of the oscillations to a level below that of a reference in the detector circuit. The output terminals are then switched to states as shown in the chart in Figs. 1 and 2 for the loaded condition of the oscillator. The oscillation is maintained at this lower amplitude by switching in additional feedback in the oscillator circuit. The fact that the oscillator continues to operate at some minimum level during this dwell period eliminates timing variations which would occur if the oscillator had to be restarted by random noise.

CA3165

APPLICATION INFORMATION (Continued)

Spark occurs as terminal 4 is switched from high to low. The output amplifier clamps terminal 4 low through the regulator during the duration of the spark.

The Dwell period represents the time that terminal 10 (CA3165E1) or terminal 6 (CA3165E) is high, terminal 4 is low, and the coil is charged.

The value of the oscillator feedback, resistor, R_f, is selected to set the dwell period. With a sintered-iron 8 f-tooth rotor, a typical value of R_f is 6500 ohms for 28.5 degrees of dwell out of a 45 degree cycle. For a star-type rotor and a particular coil in a typical distributor, the feedback resistor would be larger (typically 8800 ohms) depending on clearances, coil geometry and tooth shape.

Timing waveforms are shown in Fig. 7.

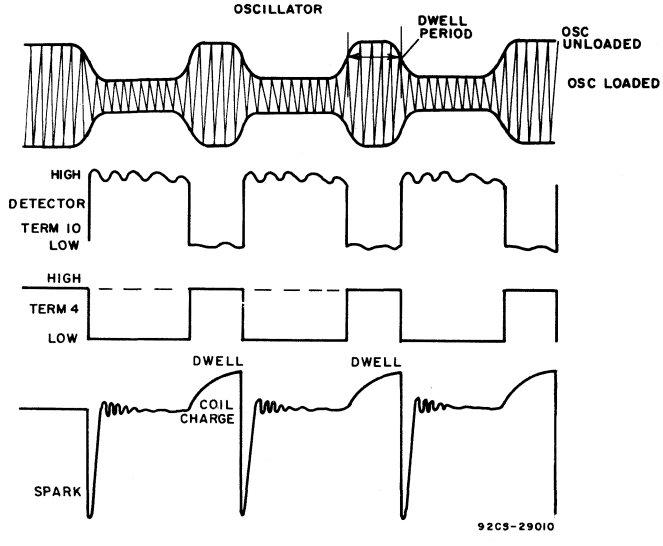
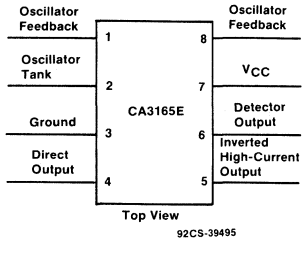
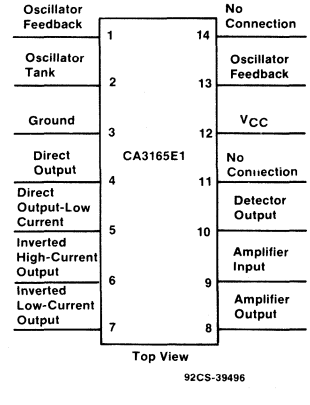


Fig. 7 - Timing sequence.

TERMINAL ASSIGNMENTS





CA3228

Speed-Control System

Features

- *Low power dissipation*
- *I^2L control logic*
- *Power-ON reset*
- *On-chip oscillator for system time reference*
- *Single input line for operator commands*
- *Amplitude encoded control signals*
- *Transient compensated input commands*
- *Controlled acceleration mode*
- *Internal redundant brake and low-speed disable*
- *Braking disable*

The RCA-CA3228• is a monolithic integrated circuit designed as an automotive speed-control system.

The system monitors vehicle speed and compares it to a stored reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed, set by the driver, is stored in a 9-bit counter.

The reference speed can be altered by the ACCEL and COAST driver commands. The ACCEL command causes the vehicle to accelerate at a controlled rate; the COAST command disables the servo, thereby forcing the vehicle to slow down. Application of the brake disables the servo and places the system in the standby mode while the RESUME command returns the vehicle to the last stored speed.

Vehicle speed and driver commands are inputs to the integrated circuit via external sensors. Actuators are needed to convert the output signals into the mechanical action necessary to control vehicle speed.

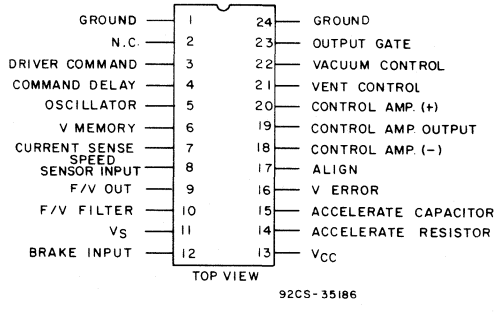
The CA3228 is supplied in a 24-lead dual-in-line plastic package (E suffix).

Refer to ICAN-7326 for application information.

• Formerly RCA Developmental Type No. TA10768.

Applications

- *Automotive speed control*
- *Residential and industrial heating and cooling controls*
- *Industrial ac and dc motor speed control*
- *Applications requiring acceleration and deceleration control*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25° C*

DC SUPPLY VOLTAGE (V_{CC}) ..... 9 V
DC SUPPLY CURRENT (I_{CC}) ..... 30 mA
DRIVER COMMAND INPUT (I_{CMD}), PIN 3 AND BRAKE INPUT (I_{BRAKE}), PIN 12 ..... 2 mA
POWER DISSIPATION PER PACKAGE:
For T_A=−40° C to 70° C ..... 695 mW
For T_A ABOVE 70° C ..... Derate linearly at 8.7 mW/° C
TEMPERATURE RANGE:
OPERATING ..... −40 to +85° C
STORAGE ..... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

File Number **1436**

CA3228

TYPICAL SWITCHING CHARACTERISTICS

DRIVER COMMAND INPUT HOLD TIMES
(Based on 0.68 μF on Pin 4)

ACCEL	50 ms
COAST	50 ms
RESUME	330 ms
ON	50 ms
OFF	50 ms
INTERNAL OSCILLATOR FREQUENCY, F_{osc}; (Based on 0.001 μF at Pin 5)	10 kHz

SYSTEM PERFORMANCE, F_{osc} = 50 kHz, f_s/Speed Ratio=2.22 Hz/mph

SPEED SENSOR INPUT FREQUENCY RANGE; f_s AT PIN 8	62 to 222 Hz
SPEED RESOLUTION	0.45 mph
MINIMUM OPERATING SPEED	25 mph
MAXIMUM STORED SPEED	100 mph
REDUNDANT BRAKE SPEED	11 mph

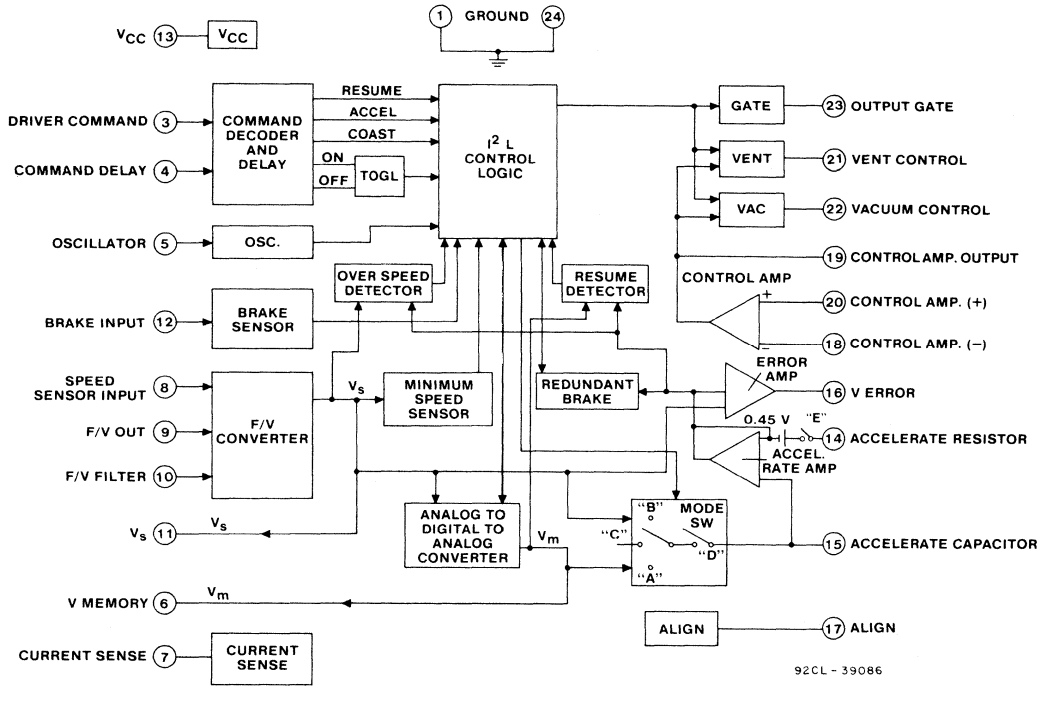


Fig. 1 - Block diagram for the CA3228.

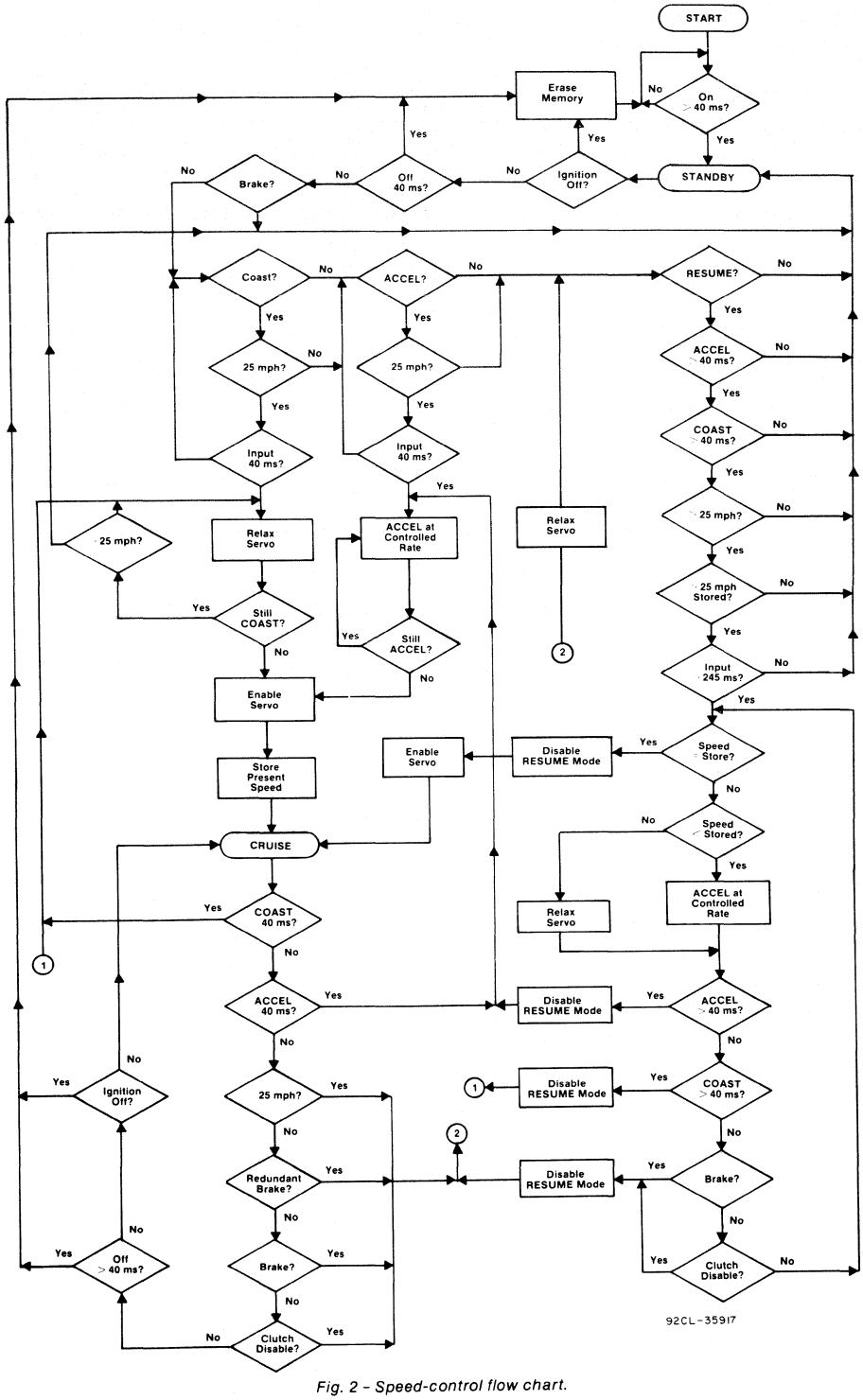


Fig. 2 - Speed-control flow chart.

CA3228

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{CC} = 8.20 V unless otherwise specified (Refer to Figs. 3 and 4.)

CHARACTERISTIC	TEST PIN	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
V_{CC} Operating Voltage	13		7.4	9	V
Speed Sensor Input Voltage Amplitude	T.P.B	$62 \leq f_s \leq 222$ Hz	3.5	15	Vpp
V_{CC} Supply Current, I_{CC}	13		7.50	30	mA
Current Sense Voltage, V_7	7	43 KΩ to ground	4.85	5.95	V
Align Voltage, V_{17}	17	41 KΩ to ground	4	4.20	V
Command Idle Voltage, V_{3IDLE}	3	S1,S2,S3,S4,S5 Open	7.6	7.9	V
RESUME Command Voltage, V_{3RES}	3	S2 Closed	5.95	6.56	V
ACCEL Command Voltage, V_{3ACCEL}	3	S3 Closed	3.95	4.91	V
COAST Command Voltage, V_{3COAST}	3	S4 Closed	1.22	2.23	V
OFF Voltage, V_{3OFF}	3	S5 Closed	0	0.77	V
ON Voltage, V_{3ON}	T.P.A	S1 Closed	9.2	28	V
Brake Input Voltage, V_{BRAKE}	12	S6 Closed	5.4	28	V
Output Voltage					
Gate V_{OL}	23	4.7 KΩ to V_{CC}	—	300	mV
Gate V_{OH}	23	4.7 KΩ to V_{CC}	8	—	V
VAC V_{OL}	22	1.2 KΩ to V_{CC}	—	400	mV
VAC V_{OH}	22	1.2 KΩ to V_{CC}	8	—	V
VENT V_{OL}	21	1.2 KΩ to V_{CC}	—	400	mV
VENT V_{OH}	21	1.2 KΩ to V_{CC}	8	—	V
Memory Set Error, V_6-V_{10}	6, 10		-77	67	mV
Deadband Range, V_{DB} (VAC and VENT Outputs off)	21, 22	Sweep Pin 19 Volt.@1 V/sec	0.96	1.43	V
Control Amplifier Gain, A_{CNTL}	16. 19	ACNTL = V_{19}/V_{16}	74	—	Ratio
D/A Voltage Range, V_M	6	Set Mode	6	7.50	V

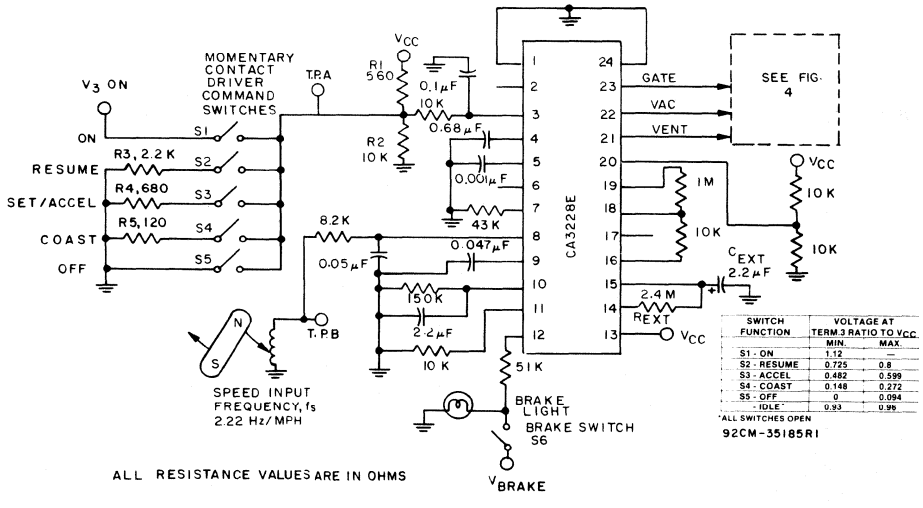
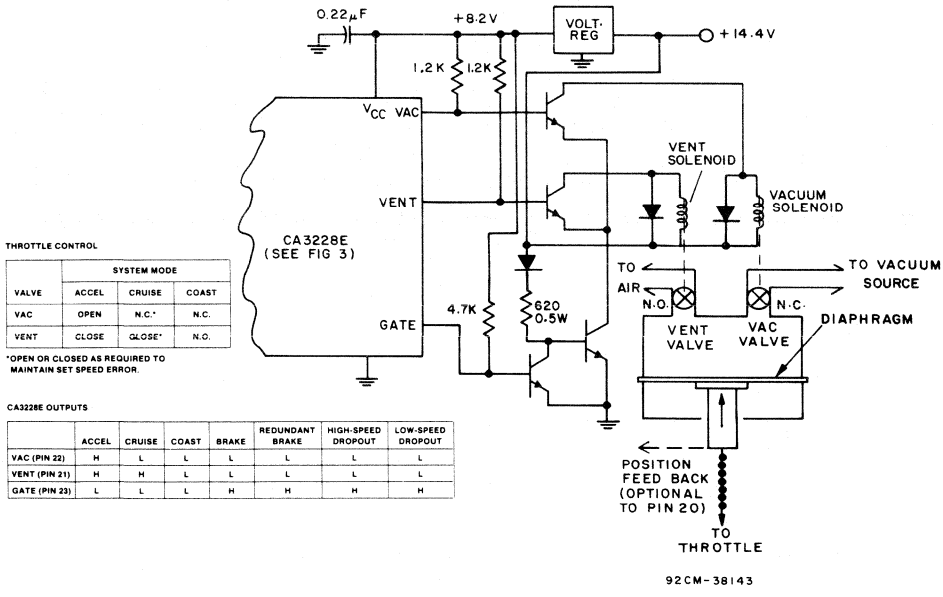


Fig. 3 - Typical automotive speed-control application.



THROTTLE CONTROL

VALVE	SYSTEM MODE		
	ACCEL	CRUISE	COAST
VAC	OPEN	N.C.*	N.C.
VENT	CLOSE	CLOSE*	N.O.

*OPEN OR CLOSED AS REQUIRED TO MAINTAIN SET SPEED ERROR.

CA3228E OUTPUTS

	ACCEL	CRUISE	COAST	BRAKE	REDUNDANT BRAKE	HIGH-SPEED DROPOUT	LOW-SPEED DROPOUT
VAC (PIN 22)	H	L	L	L	L	L	L
VENT (PIN 21)	H	H	L	L	L	L	L
GATE (PIN 23)	L	L	L	H	H	H	H

Fig. 4 - Solenoid drivers and servo vacuum control mechanism typical application.

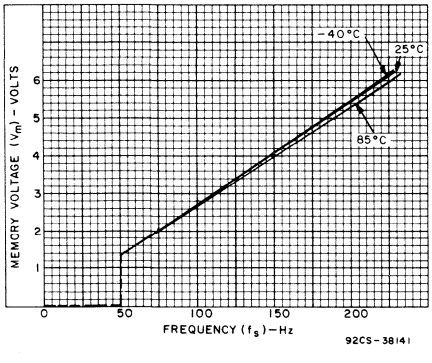


Fig. 5 - Typical D/A memory voltage, V_M versus frequency.

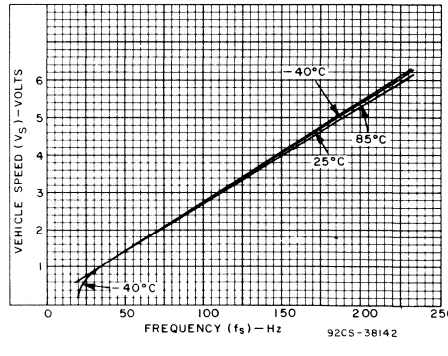


Fig. 6 - Typical characteristic F/V converter output, V_S versus frequency.

DEVICE DESCRIPTION AND OPERATION

Figs. 1, 2, and 3 show the functional block diagram, speed-control flow chart, and a typical automotive speed-control application, respectively.

Command Decoder and Delay Logics (Pins 3, 4)

Driver commands are input to pin 3 through the Driver Command Line. These signals are encoded on a single line as voltage levels selected by switches which adjust a resistor divider network.

The voltage level established is compared to a reference level which decodes the command. A command level greater than V_{CC} + 0.8 V turns the system On, enabling dynamic control. Once the system is enabled, a voltage level of 0.88 V_{CC}, 0.66 V_{CC}, and 0.38 V_{CC} decodes the RESUME, ACCEL, and COAST command, respectively. A driver command of 0.12 V_{CC} or less turns the system Off.

The Driver Command Delay established by the current sources and a capacitor at pin 4 assures that ON, OFF, ACCEL, and COAST commands are considered valid only if longer than 50 ms. The time for RESUME is 330 ms.

CA3228

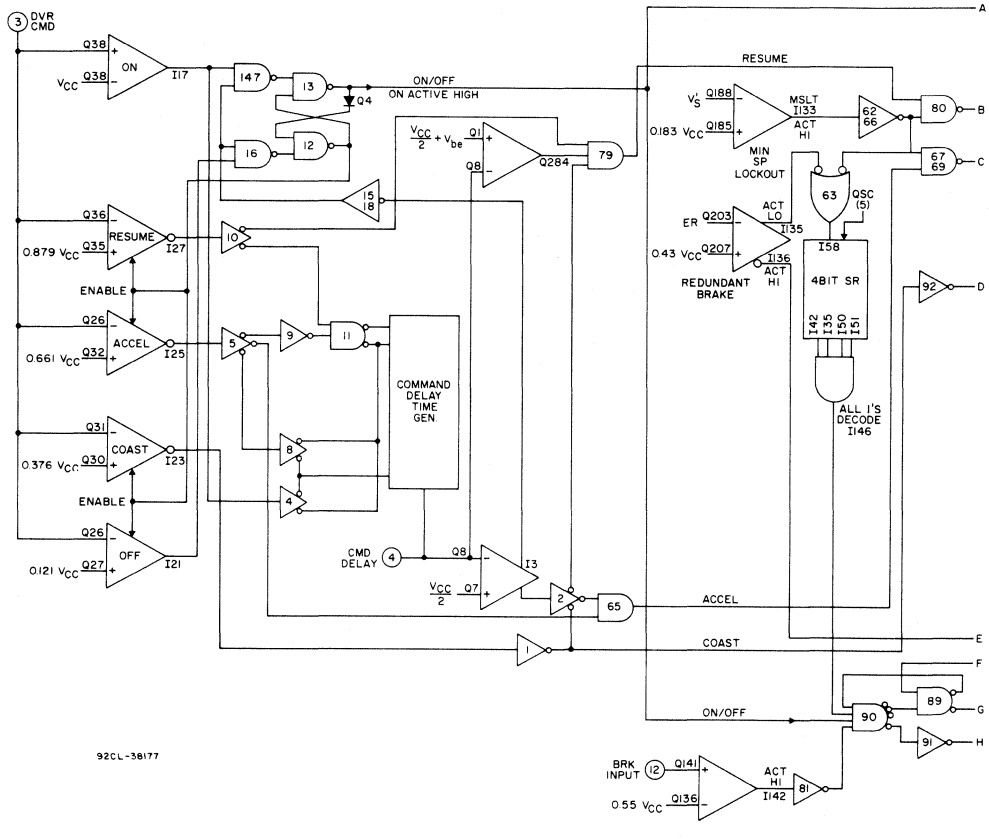


Fig. 7 - Functional block diagram for speed control (continued on next page).

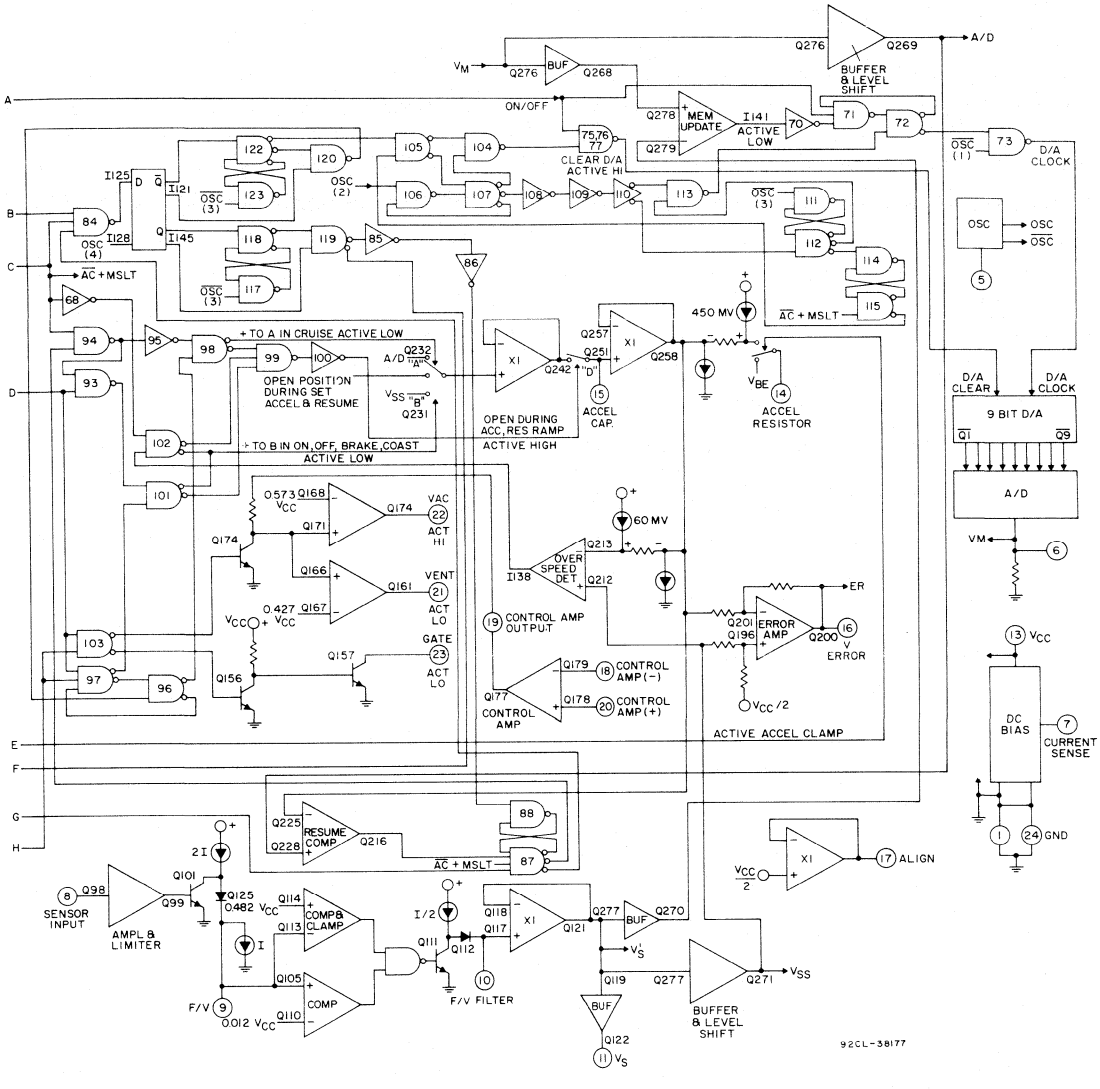


Fig. 7 - Functional block diagram for speed control (continued from previous page).

CA3228

DEVICE DESCRIPTION AND OPERATION (Cont'd)

Control Logic

The Control Logic accepts signals from the command decoder and other sensors. It causes the memory to be updated when operating in ACCEL and COAST modes. It will put the system in Standby mode if brakes are applied, if the speed error exceeds 11 mph, or if the vehicle speed drops below the minimum Speed Lockout (25 mph). It will return the vehicle to the previous set memory speed when a RESUME command is given.

Frequency to Voltage Converter (Pins 8-11)

The speed sensor input f_s at pin 8 is an ac signal whose frequency is directly proportional to the vehicle speed at approximately 2.22 Hz/mph. The current sources, capacitor and comparators at pin 9 cause equal rise and fall times to occur at pin 9 on the positive- and negative-going slopes of the sensor input. Pulse currents of time duration equal to the rise and fall times are used to charge the parallel resistor capacitor combination at pin 10 to give a voltage (V_S) at pin 10 proportional to frequency at approximately 27 mV/Hz. The f_s frequency range may be altered by changing the values of the filter capacitors at pins 8 and 9. However, the maximum-to-minimum frequency ratio will remain fixed.

Memory Voltage, V_M (Pin 6)

Upon release of the ACCEL or COAST switches the voltage, representing vehicle speed V_S determined by the output from the frequency-to-voltage converter, is stored as a binary number in a 9-bit counter. A memory update comparator allows clocking of the counter until memory voltage V_M equals V_S. The output of the counter controls a ladder network which provides memory voltage V_M at pin 6.

Analog Accelerate and Resume Generator (Pins 14, 15)

Numerous functions are combined in what is called the Analog Accelerate and Resume Generator. The circuit switches the signal output at pin 15 depending on the mode of operation. In the Accelerate and Resume mode the capacitor at pin 15 is charged at a fixed rate[450 mV/(R_{EXT}) (C_{EXT})]. In the Cruise mode pin 15 follows the memory voltage (V_M) and in the On, Off, Brake, Redundant Brake, Minimum Speed Lockout, and Coast modes, pin 15 follows the voltage representing vehicle speed (V_S).

Error Amplifier (Pin 16)

In the Cruise mode the Error Amplifier determines the difference between the set memory speed (V_M) and the actual speed (V_S). This error signal is fed to the control amplifier where it defines whether VAC or VENT is required. The error signal represents deviation in vehicle speed from the memory or set speed condition. The Error signal is also used to control the Redundant Brake feature.

Redundant Brake Comparator

When the error output drops below approximately 0.42 V_{CC}, the Redundant Brake output is activated. Redundant Brake causes the chip to go into the Standby mode.

Control Amplifier (Pins 18, 20)

The Control Amplifier is an op amp using external components to set the gain. Inputs to the Control Amplifier are from the Error Amplifier output, servo position sensor and align output. The output of the Control Amplifier controls the VAC and VENT outputs.

VAC, VENT and Gate-Driver Outputs (Pins 21, 22, 23)

The VAC, VENT and Gate Outputs are open collector devices used to control the throttle position. For the system to be able to supply vacuum, the gate output must be low. If the output from the Control Amplifier exceeds 0.573 V_{CC}, vacuum is supplied to the servo unit. If the output of the Control Amplifier is between 0.573 V_{CC} and 0.427 V_{CC} the vacuum is held in the servo unit and vehicle speed is maintained. If the output from the Control Amplifier drops below 0.427 V_{CC} or if the gate output is high, the servo unit vacuum is vented.

Overspeed Detector Comparator

The Overspeed Detector circuit is used when the following sequence of events occur: A speed is set in memory, the vehicle is manually accelerated (foot pedal) to a higher speed and then the ACCEL switch is activated.

During vehicle acceleration V_S voltage is greater than the V_M voltage into the memory update comparator. When the ACCEL command is given, the capacitor at pin 15 rapidly charges to within 60 mV of V_S before switching the comparator output low and starting the fixed acceleration rate from the present vehicle speed. The 60 mV of offset is required to insure that the output of the overspeed detector is low under normal operating conditions. Hysteresis is also designed into the comparator to eliminate noise problems which may prevent the chip from going into the Acceleration mode.

End of Resume Comparator

The Resume Comparator is used when the following sequence of events occurs: A speed is set in memory, the brake applied, causing the vehicle to go to a lower speed, and the RESUME switch is activated.

Activation of the RESUME switch causes a fixed acceleration rate from the lower speed until the capacitor voltage at pin 15 is equal to the V_M voltage. A filter circuit contained in the output of the resume comparator insures that noise doesn't reset the comparator until V_{pin} actually equals V_M.

Align Voltage Source (Pin 17)

The Align Voltage Source is a X1 buffer with an output of 0.5 V_{CC}.

Brake Input Comparator (Pin 12)

When the Brake Input exceeds 0.55 V_{CC}, the chip will go into the Standby mode from Cruise.

Minimum Speed Lockout

Assures that the system remains in a Standby mode if vehicle speed V_S is below 0.183 V_{CC}. It causes the system to revert to the Standby mode if V_S drops below 0.183 V_{CC} in the Cruise mode.

Digital Filter for Redundant Brake and Minimum Speed Lockout

A 4-bit shift register with an all '1's output decode is used to filter transients and electromagnetic interference. The filter prevents false signals from putting the system into Standby from Cruise.

Ramp Oscillator (Pin 5)

The Ramp Oscillator at pin 5 nominally varies between amplitudes of 4.1 and 6.1 V. The discharge rate is approximately 4X the charge rate. With a capacitor of 0.001 μF on pin 5, the nominal oscillator frequency is 50 kHz.

Radio/Communication Circuits

Radio/Communication Circuits — Technical Data

CA2111A

FM IF Amplifier-Limiter and Quadrature Detector

For FM IF and TV Sound IF Applications

Features:

- **Direct replacement for ULN2111A and MC1357**
- **Good sensitivity: Input limiting voltage (knee) (400 μV typ. at 10.7 MHz; 250 μV typ. at 4.5 MHz and 5.5 MHz)**
- **Excellent AM rejection (45 dB typ. at 10.7 MHz)**
- **Provision for output from 3-stage IF amplifier section**
- **Low harmonic distortion**
- **Quadrature detection permits simplified single-coil tuning**
- **Extremely low AFC voltage drift over full operating-temperature range**
- **Minimum number of external parts required**

The CA2111A, on a single monolithic chip, provides a multi-stage wideband amplifier-limiter, a quadrature detector, and an emitter-follower output stage. This device is designed for use in FM receivers and in the sound IF sections of TV receivers. In addition, an output terminal is provided which allows the use of the amplifier-limiter as a straight 60-dB wideband amplifier.

The amplifier-limiter features the excellent limiting characteristics of 3 cascaded differential amplifiers.

The quadrature detector requires only one coil in the associated outboard circuit and therefore, tuning is a simple procedure.

A unique feature of the CA2111A is its exceptionally low AFC voltage drift over the full operating-temperature range.

This device can be supplied in either dual-in-line or quad-in-line 14-lead plastic packages (CA2111AE and CA2111AQ, respectively).

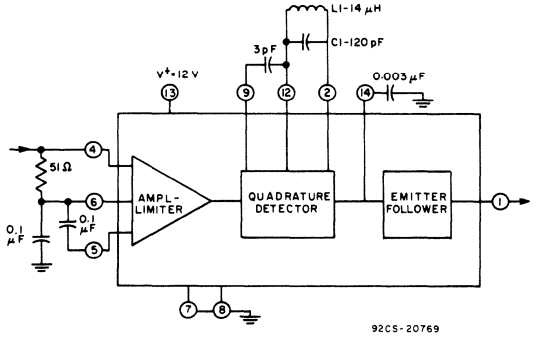


Fig. 1—Block diagram of CA2111A and associated outboard components.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC Supply Voltage [between terminals 5 (V^+) and 3 (V^-)]	16	V
Device Dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+265	°C

File Number **612**

CA2111A

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
DC Voltage:		$V^+ = 12V$	–	5.4	–	V
At Terminal 1	V_1	$= 8V$	–	3.7	–	
At Terminals 4, 5, 6, 10	$V_{4,5,6,10}$	$V^+ = 8V$	–	1.35	–	
At Terminals 2, 12	$V_{2,12}$		–	3.5	–	
DC Current (into Terminal 13)						mA
At $V^+ = 8V$			–	14	–	
At $V^+ = 12V$	I_{13}		–	16	–	
Amplifier Input Resistance	R_4	$f_o = 10.7$ MHz	–	7	–	kΩ
Amplifier Input Capacitance	C_4		–	11	–	pF
Detector Input Resistance	R_{12}		–	70	–	kΩ
Detector Input Capacitance	C_{12}		–	2.7	–	pF
Amplifier Output Resistance	R_{10}		–	60	–	Ω
Detector Output Resistance	R_1		–	200	–	Ω
De-Emphasis Resistance	R_{14}		–	8.8	–	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
FM Modulation Frequency = 400 Hz, Source Resistance = 50Ω

CHARACTERISTIC	SYMBOL	TEST CONDITIONS						UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		$f_o = 10.7$ MHz, $\Delta f = \pm 75$ KHz				$f_o = 4.5$ MHz, $\Delta f = \pm 25$ KHz	$f_o = 5.5$ MHz, $\Delta f = \pm 50$ KHz		
		$V^+ = 12V$		$V^+ = 8V$		$V^+ = 12V$	$V^+ = 12V$		
		LIMITS							
		TYP.	MAX.	TYP.	MAX.	TYP. MAX.	TYP. MAX.		
AMPL-LIMITER									
Input Limiting Threshold Voltage	V_i(lim) (4)	400	600	400	600	250 400	250 400	V (RMS)	3, 7, 8, 9
AM Rejection‡ *	AMR(1)	45	–	37	–	36 –	40 –	dB	3, 4, 5, 6
Ampl. Voltage Gain▲	A_V(10)	55	–	55	–	60 –	60 –	dB	3
DETECTOR									
Recovered Audio‡ Output Voltage	V_o(AF) (1)	0.48	–	0.3	–	0.72 –	1.2 –	V (RMS)	3, 7, 8, 9
Total Harmonic‡ Distortion	THD(1)	1	–	1	–	1.5 –	3 –	%	3

‡V_i = 10 mV (RMS) ▲$V_i \leq 50\ \mu V$ (rms) *100% FM, 30% AM

CA2111A

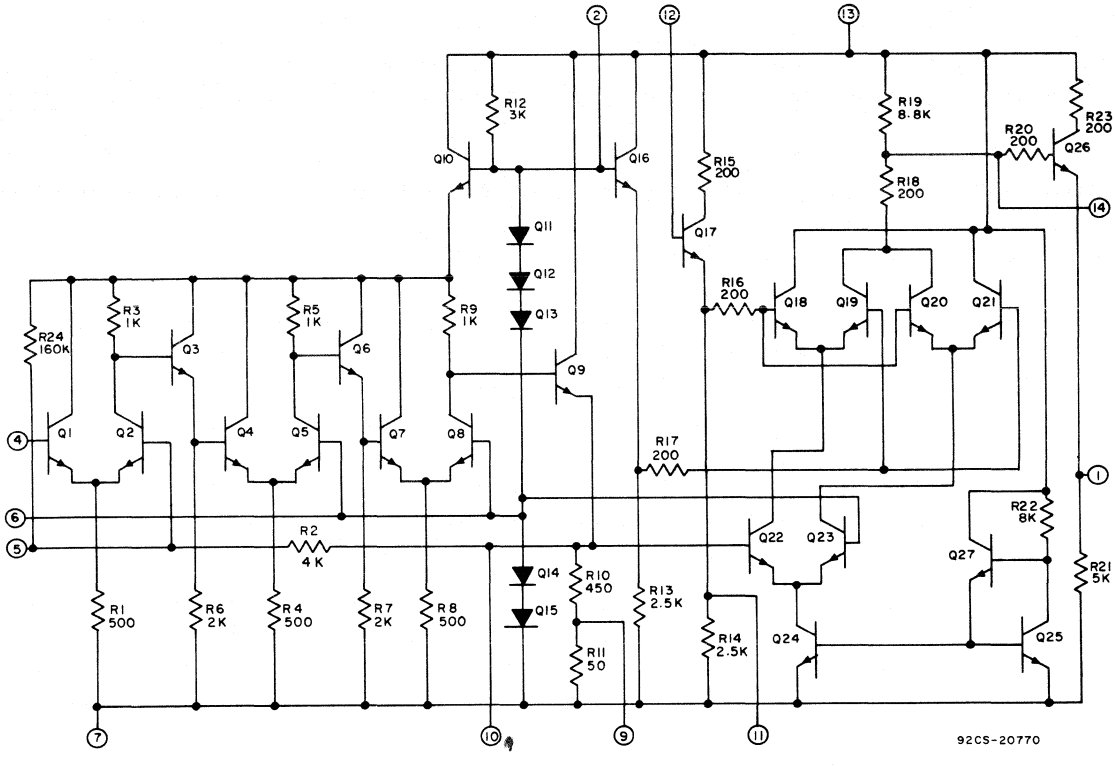
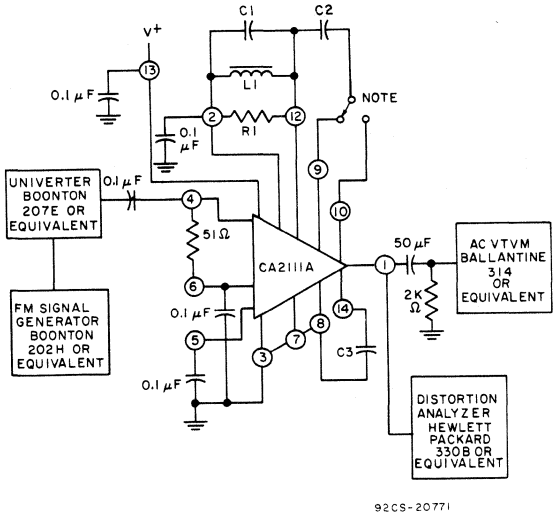


Fig. 2—Circuit schematic—CA2111A

NOTE:

Input to the quadrature coil can be from either terminal 9 or terminal 10. Terminal 9 is normally used because it lessens the possibility of overloads during tuning. The use of terminal 10 increases the limiting sensitivity significantly and has been used successfully in these tests.



COMPONENT VALUES							DETECTOR TRANSFER CHARACTERISTICS	
f	L_1	C_1	R_1	Q	C_2	C_3	UPPER PEAK	LOWER PEAK
MHz	μH	pF	KΩ	–	pF	μF	MHz	MHz
4.5	14	120	20	30	3	0.003	4.58	4.42
5.5	8	100	20	30	3	0.003	5.63	5.37
10.7	2	120	3.9	20	4.7	0.01	10.9	10.5

Fig. 3—Test circuit.

CA2111A

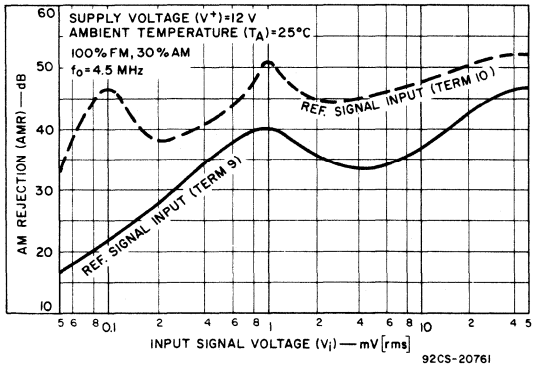


Fig. 4—AM rejection vs input voltage (4.5 MHz).

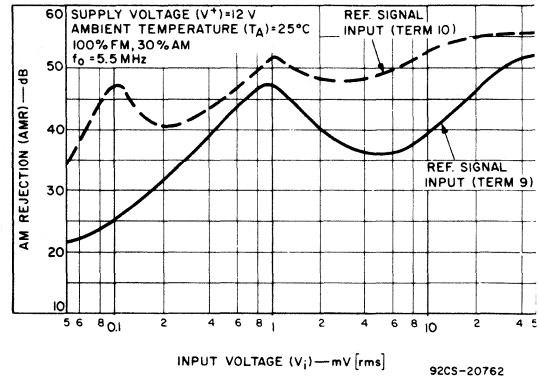


Fig. 5—AM rejection vs input voltage (5.5 MHz).

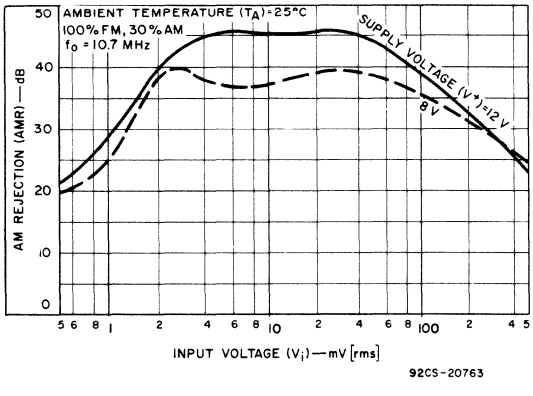


Fig. 6—AM rejection vs input voltage (10.7 MHz).

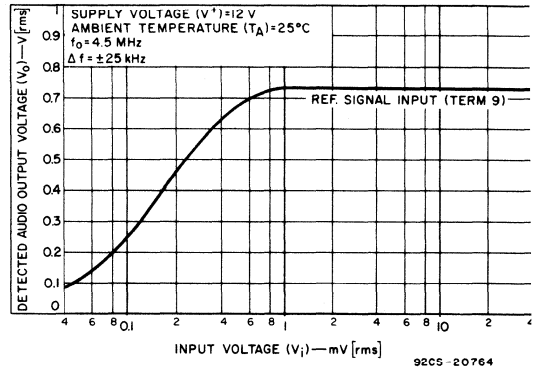


Fig. 7—Detected audio output vs input voltage (4.5 MHz).

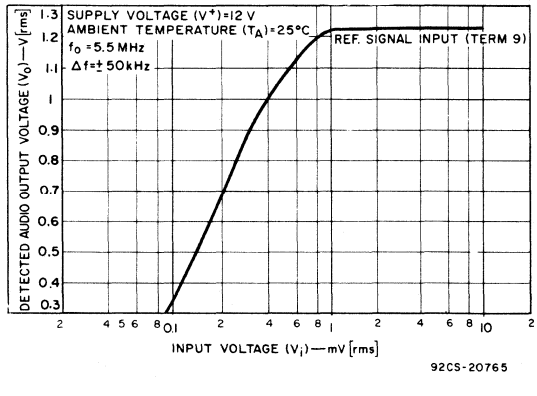


Fig. 8—Detected audio output vs input voltage (5.5 MHz).

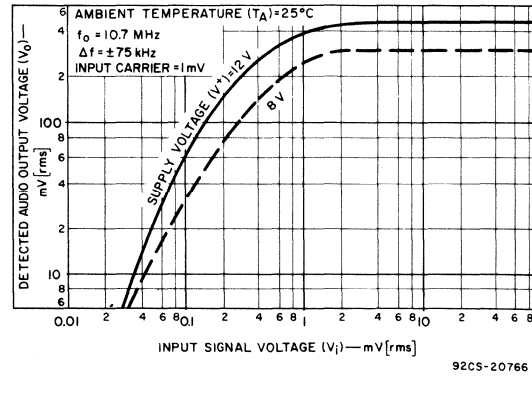


Fig. 9—Detected audio output voltage vs input voltage (10.7 MHz).

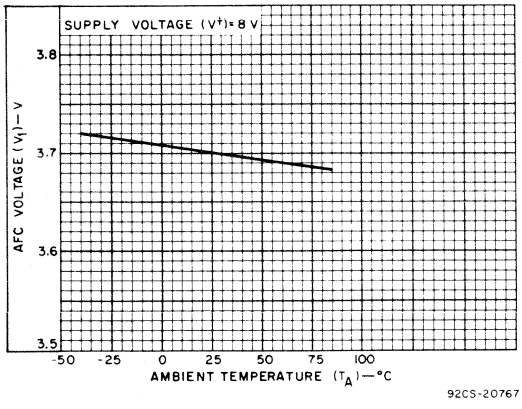


Fig. 10—AFC voltage vs ambient temp.

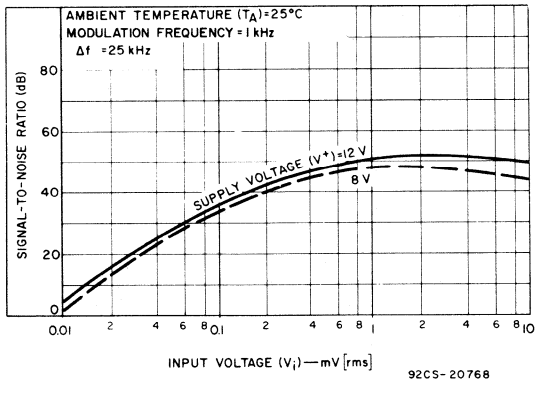


Fig. 11—Signal-to-noise ratio vs input voltage.

CA2136A

FM IF Amplifier-Limiter and Quadrature Detector

For FM IF and TV Sound IF Applications

Features:

- *Direct replacement for ULN2136A and LM1841*
- *Good sensitivity: Input limiting voltage (knee) (400 μV typ. at 10.7 MHz; 250 μV typ. at 4.5 MHz and 5.5 MHz)*
- *Excellent AM rejection (45 dB typ. at 10.7 MHz)*
- *Provision for output from 3-stage IF amplifier section*
- *Low harmonic distortion*
- *Quadrature detection permits simplified single-coil tuning*
- *Extremely low AFC voltage drift over full operating-temperature range*
- *Excellent line and load regulation*
- *Minimum number of external parts required*
- *Pin-compatible with the CA2111A*

The CA2136A integrated circuit includes a multistage wideband amplifier-limiter, a quadrature detector, an emitter-follower output stage, and a voltage regulator on a single monolithic chip. This device provides a regulated supply voltage for the tuner stages in FM receivers. It can be used in any amplifier-limiter or FM demodulator application.

The amplifier-limiter features the excellent limiting characteristics of three cascaded differential amplifiers. The quadrature detector requires only one coil in the associated outboard circuit; tuning, therefore, is a simple procedure.

A unique feature of the CA2136A is its exceptionally low AFC voltage drift over the full operating-temperature range.

This device can be supplied in either dual-in-line or quad-in-line 14-lead plastic packages.

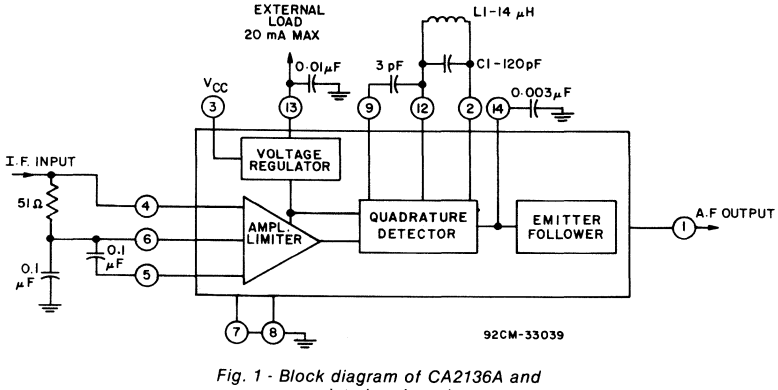


Fig. 1 - Block diagram of CA2136A and associated outboard components

File Number **1262**

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25°C$

DC SUPPLY VOLTAGE
[Between Terminals 3 (V+) and 7 (V−)] ..... 20 V
DEVICE DISSIPATION:
Up to $T_A = 60°C$ ..... 600 mW
Above $T_A = 60°C$ ..... Derate Linearly 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... −55 to +125 °C
Storage ..... −65 to +150 °C
EXTERNAL LOAD CURRENT ..... 20 mA
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265 °C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
DC Voltage:						
At Terminal 1	V_1	V+ = 12 V	3.5	4.3	5.0	
At Terminals 4, 5, 6, 10	$V_{4, 5, 6, 10}$	V+ = 12 V	—	1.35	—	V
At Terminals 2, 12	$V_{2, 12}$		—	3.8	—	
At Terminal 13	V_{13}		—	7.8	—	
DC Current (into Terminal 3)						
At V+ = 12 V	I_3		—	21	—	mA
Amplifier Input Resistance	R_4	f_O = 10.7 MHz	—	7	—	kΩ
Amplifier Input Capacitance	C_4		—	11	—	pF
Detector Input Resistance	R_{12}		—	70	—	kΩ
Detector Input Capacitance	C_{12}		—	2.7	—	pF
Amplifier Output Resistance	R_{10}		—	60	—	Ω
Detector Output Resistance	R_1		—	200	—	Ω
De-Emphasis Resistance	R_{14}		—	10.5	—	kΩ

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$
FM Modulation Frequency = 400 Hz, Source Resistance = 50 Ω

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		UNITS	TEST CIRCUIT OR CHARACTERISTIC CURVES FIG. NO.
		f_O = 10.7 MHz, Δf = ±75 kHz, V+ = 12 V			
		LIMITS			
		Typ.	Max.		
AMPLIFIER-LIMITER					
Input Limiting Threshold Voltage	V_i (lim) (4)	400	600	μV (rms)	3
AM Rejection‡ *	AMR (1)	40	—	dB	3
Ampl. Voltage Gain▲	A_V (10)	53	—	dB	3
DETECTOR					
Recovered Audio‡ Output Voltage	V_O (AF) (1)	0.4	—	V (rms)	3
Total Harmonic‡ Distortion	THD (1)	1	3	%	3
Line Regulator	V_{reg}	5	10	mV/V	

‡V_i = 10 mV (rms) ▲$V_i \leq 50$ μV (rms) *100% FM, 30% AM

CA3011, CA3012

Wide-Band Amplifiers

Features:

- *Exceptionally high amplifier gain: power gain at 4.5 MHz/s - 75 dB typ.*
- *Excellent limiting characteristics - Input limiting voltage (knee) = 600 μV typ. at 10.7 MHz/s*
- *Wide frequency capability - 100 kHz/s to > 20 MHz/s*

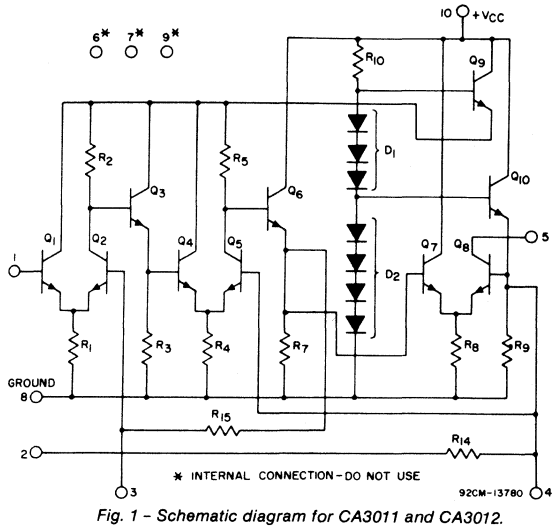


Fig. 1 - Schematic diagram for CA3011 and CA3012.

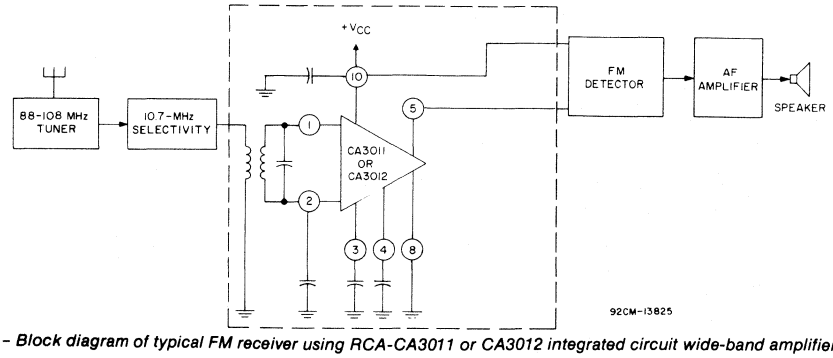


Fig. 2 - Block diagram of typical FM receiver using RCA-CA3011 or CA3012 integrated circuit wide-band amplifier.

File Number **128**

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

NOTE: TERMINALS 6, 7, AND 9 OF RCA-CA3011 AND CA3012 ARE USED FOR INTERNAL CONNECTIONS. DO NOT APPLY VOLTAGES OR MAKE EXTERNAL CONNECTIONS TO THESE TERMINALS.

CA3011

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Ground	+7.5
2	-3	+3	Same as 2	–		+2.5 to +7.5	+7.5	Ground	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		–	+7.5	Ground	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	–	Ground	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

CA3012

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Ground	+10
2	-3	+3	Same as 2	–		+2.5 to +10	+10	Ground	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
4	+2.5	+10	-3 to +3	Same as 1		–	+10	Ground	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	–	Ground	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

OPERATING-TEMPERATURE RANGE ..... -55 to +125° C
STORAGE-TEMPERATURE RANGE ..... -65 to +150° C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 2 ..... ±3 V
MAXIMUM DEVICE DISSIPATION ..... 300 mW
RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC}) .. 5.5 V

Example of Use of LIMITS TABLE:

For RCA-3012, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +10 volts
Terminal 5 is at a dc potential of +10 volts
Terminals 6, 7, and 9 are at 0 dc potential (NOT USED)
Terminal 8 is at dc ground potential
Terminal 10 is at a dc potential of +10 volts

CA3011, CA3012

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3011			RCA CA3012				
		Fig.	Mc/s	Volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	66	80	135	mW	4
					+25	60	90	133	66	90	121	mW	
					+125	–	70	–	65	70	121	mW	
			–	7.5	-55	–	130	–	97	130	190	mW	4
					+25	95	120	187	97	120	167	mW	
					+125	–	100	–	95	100	167	mW	
			–	10	-55	–	–	–	150	210	275	mW	4
					+25	–	–	–	150	190	255	mW	
					+125	–	–	–	150	160	255	mW	
Voltage Gain**	A	5	1	6	-55	–	55	–	50	55	–	dB	6
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		5	1	7.5	-55	–	59	–	55	59	–	dB	6
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		5	1	10	-55	–	–	–	55	61	–	dB	6
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		5	4.5	7.5	+25	60	67	–	60	67	–	dB	7
			10.7	7.5	+25	55	61	–	55	61	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	8	4.5	7.5	+25	–	3	–	–	3	–	kΩ	9
Parallel Input Capacitance	C_{IN}	8	4.5	7.5	+25	–	7	–	–	7	–	pF	9
Output Impedance Components: Parallel Output Resistance	R_{OUT}	10	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	11
Parallel Output Capacitance	C_{OUT}	10	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	11
Noise Figure	NF	12	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	13
Input Limiting Voltage (Knee)	$V_{i(lim)}$	5	4.5	7.5	+25	–	300	450	–	300	400	μV	6

* The total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

TYPICAL CHARACTERISTICS AND TEST SETUPS

DISSIPATION TEST SETUP

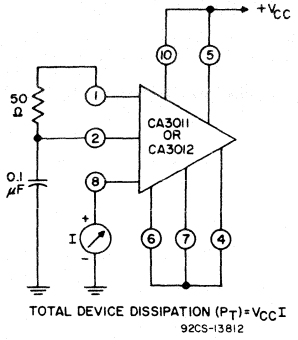


Fig.3

DISSIPATION VS TEMPERATURE

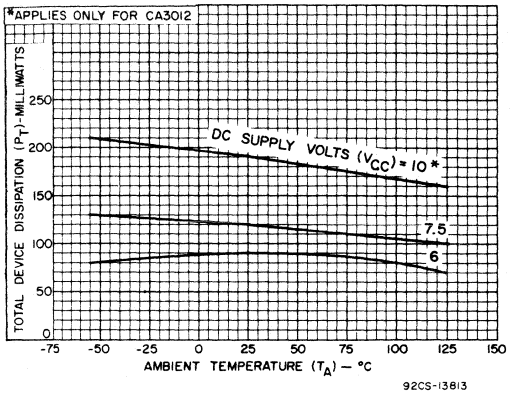
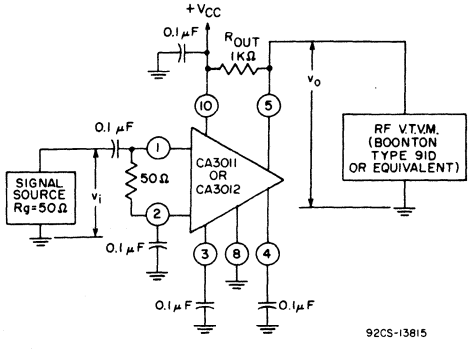


Fig.4

VOLTAGE-GAIN TEST SETUP



PROCEDURES

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

B - Input Limiting Voltage (Knee):

1) Repeat Steps A1 and A2, using v_i = 100 mV
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

Fig.5

VOLTAGE GAIN & INPUT LIMITING VOLTAGE VS TEMPERATURE

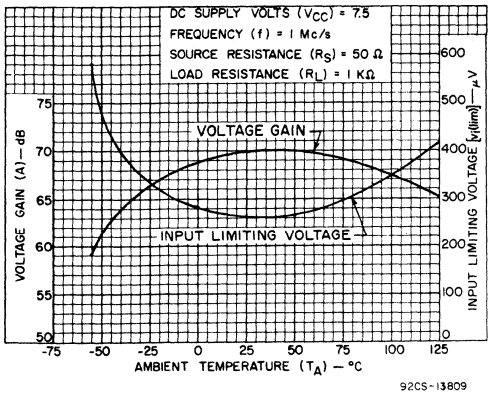


Fig.6

VOLTAGE GAIN AND INPUT LIMITING VOLTAGE VS FREQUENCY

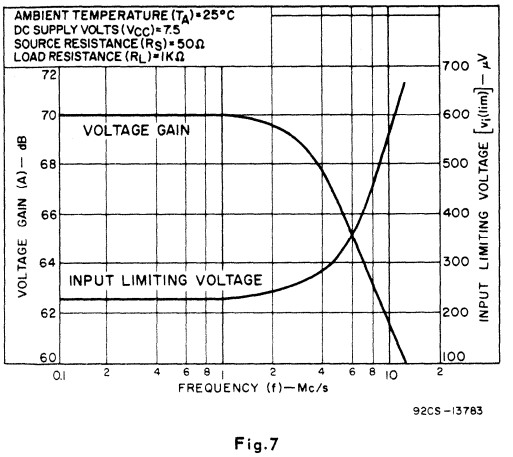


Fig.7

CA3011, CA3012

TYPICAL CHARACTERISTICS AND TEST SETUPS

INPUT-IMPEDANCE COMPONENTS
TEST SETUP

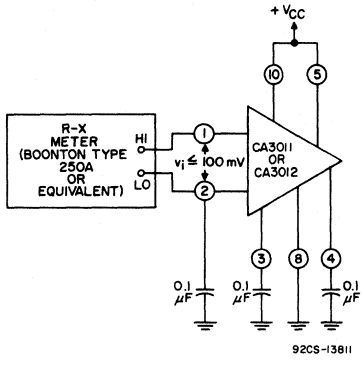


Fig.8

INPUT-IMPEDANCE COMPONENTS
VS FREQUENCY

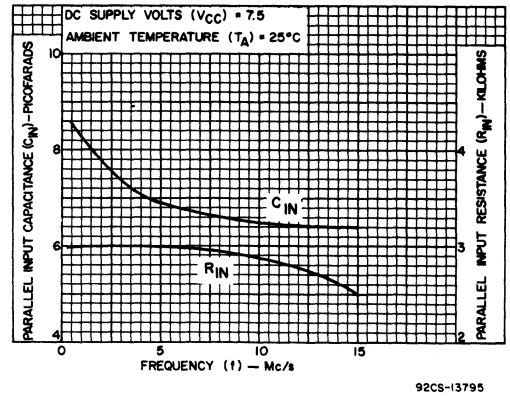


Fig.9

OUTPUT-IMPEDANCE COMPONENTS
TEST SETUP

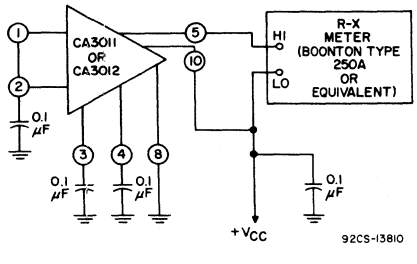


Fig. 10

OUTPUT-IMPEDANCE COMPONENTS
VS FREQUENCY

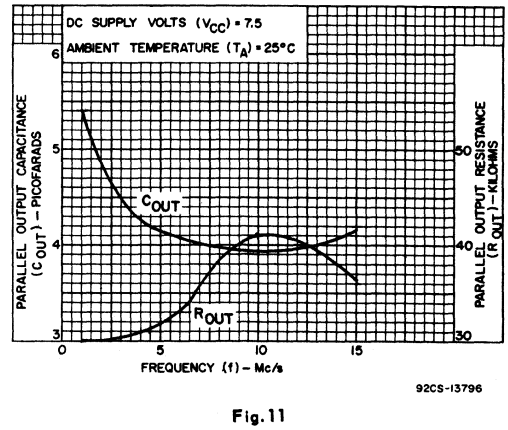
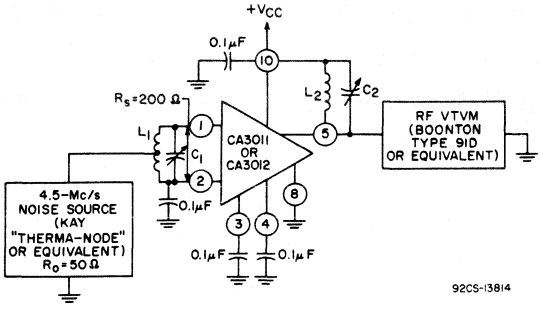


Fig. 11

TYPICAL CHARACTERISTICS AND TEST SETUPS

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1,C_2 = Arco Type 423 padder, or equivalent

Fig. 12

NOISE FIGURE VS DC SUPPLY VOLTAGE

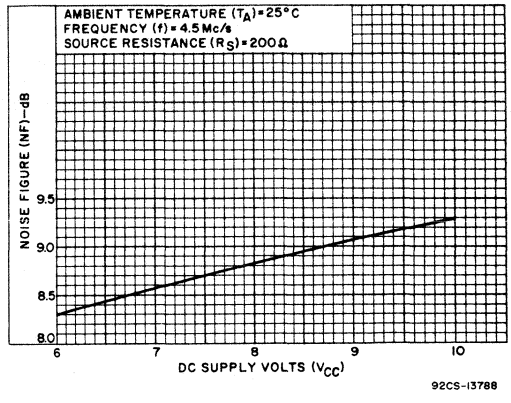


Fig. 13

CA3013, CA3014

Wide-Band Amplifier Discriminators

Features & Applications:

- *Exceptionally high gain: power gain at 4.5 MHz - 75 dB typ.*
- *Excellent limiting characteristics - input limiting voltage (knee) = 300 μV typ. at 4.5 MHz*
- *Excellent AM rejection: > 50 dB at 4.5 MHz*
- *High audio-voltage recovery - 220 mV typ at 4.5 MHz, 25 kHz deviation*
- *Wide frequency capability - 100 kHz to > 20 MHz*
- *Comprehensive circuit functions: if amplifier, AM and noise limiter, FM detector, audio preamplifier*

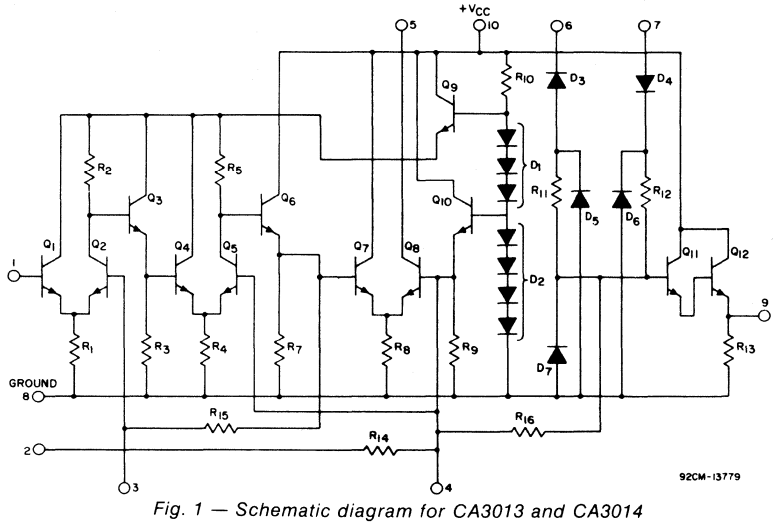


Fig. 1 — Schematic diagram for CA3013 and CA3014

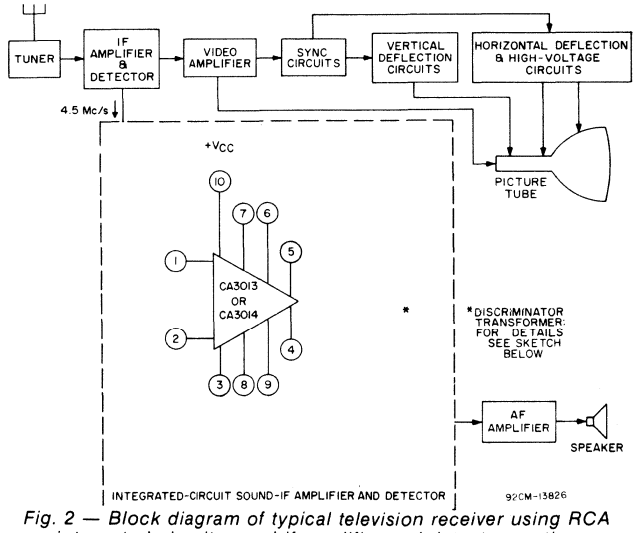


Fig. 2 — Block diagram of typical television receiver using RCA integrated-circuit sound-if amplifier and detector section

File Number **129**

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

CA3013

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
2	-3	+3	Same as 2	-		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		-	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	-	Same as 4	Same as 4	Ground	AF Output	+7.5
6	+2.5	+7.5	-3 to +3	Same as 1		Same as 6	+7.5	-	Same as 4	Ground	AF Output	+7.5
7	+2.5	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	-	Ground	AF Output	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
9	0	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	-	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

CA3014

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
2	-3	+3	Same as 2	-		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
4	+2.5	+10	-3 to +3	Same as 1		-	+10	Same as 4	Same as 4	Ground	AF Output	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	-	Same as 4	Same as 4	Ground	AF Output	+10
6	+2.5	+10	-3 to +3	Same as 1		Same as 6	+10	-	Same as 4	Ground	AF Output	+10
7	+2.5	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	-	Ground	AF Output	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
9	0	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	-	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

OPERATING-TEMPERATURE RANGE . . . . . -55 to +125 °C

STORAGE-TEMPERATURE RANGE. . . . . -65 to +150 °C

MAXIMUM INPUT-SIGNAL VOLTAGE:

Between Terminals 1 and 2. . . . . ±3 V

MAXIMUM DEVICE DISSIPATION. . . . . 300 mW

RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC}). . . . . 5.5 V

Example of use of LIMITS TABLE:

For RCA-CA3013, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +7.5 volts
Terminal 5 is at a dc potential of +7.5 volts
Terminals 6 and 7 are at the same dc potential as Terminal 4
Terminal 8 is at dc ground potential
Terminal 9 is used as the af output terminal
Terminal 10 is at a dc potential of +7.5 volts

CA3013, CA3014

ELECTRICAL CHARACTERISTICS (See Page 8 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTIC CURVES
		SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	RCA CA3013			RCA CA3014				
		Fig.	Mc/s	volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	73	80	120	mW	4
					+25	60	90	133	73	90	110	mW	
					+125	–	70	–	60	70	110	mW	
		3	–	7.5	-55	–	130	–	106	130	170	mW	4
					+25	87	120	187	106	120	150	mW	
					+125	–	100	–	90	100	150	mW	
		3	–	10	-55	–	–	–	165	210	250	mW	4
					+25	–	–	–	165	190	230	mW	
					+125	–	–	–	150	160	230	mW	
Voltage Gain**	A	5	1	6	-55	–	55	–	50	55	–	dB	6
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		5	1	7.5	-55	–	59	–	55	59	–	dB	6
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		5	1	10	-55	–	–	–	55	61	–	dB	6
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		5	4.5	7.5	+25	60	67	–	60	67	–	dB	7
			10.7	7.5	+25	55	60	–	55	60	–	dB	
Input-Impedance Components:													
Parallel Input Resistance	R_{IN}	8	4.5	7.5	+25	–	3	–	–	3	–	kΩ	9
Parallel Input Capacitance	C_{IN}	8	4.5	7.5	+25	–	7	–	–	7	–	pF	9
Output-Impedance Components:													
Parallel Output Resistance	R_{OUT}	10	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	11
Parallel Output Capacitance	C_{OUT}	10	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	11
Noise Figure	NF	12	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	13
Input Limiting Voltage (Knee)	v_i(lim)	14	4.5	7.5	+25	–	300	450	–	300	400	μV	15
Recovered AF Voltage	v_o(af)	14	4.5	6	+25	–	155	–	–	155	–	mV	15
				7.5	+25	128	188	–	135	188	–	mV	
				10	+25	–	–	–	–	220	–	mV	
Amplitude-Modulation Rejection	AMR	16	4.5	7.5	+25	–	50	–	–	50	–	dB	–
Discriminator Output Resistance	R_O(disc)	–	4.5	7.5	+25	–	60	–	–	60	–	Ω	–
Total Harmonic Distortion	THD	14	4.5	7.5	+25	–	1.8	–	–	1.8	–	%	17

* Total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

TYPICAL CHARACTERISTICS AND TEST SETUPS

DISSIPATION TEST SETUP

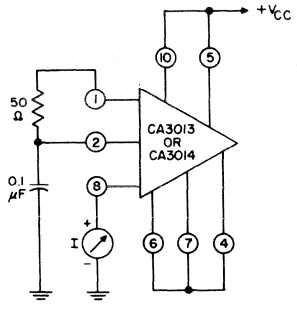


Fig.3

DISSIPATION vs. TEMPERATURE

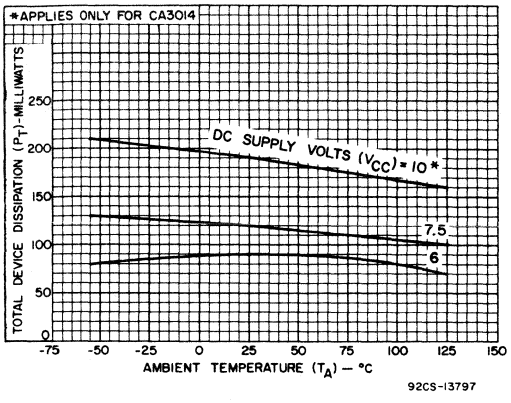
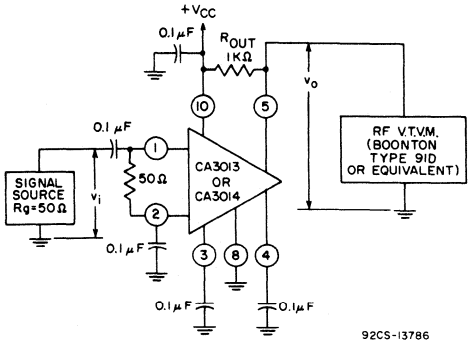


Fig.4

VOLTAGE-GAIN TEST SETUP



PROCEDURE:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$.
4) Repeat Steps 1, 2, and 3 for each frequency and/or temperature desired.

Fig.5

1-Mc/s VOLTAGE GAIN vs. TEMPERATURE

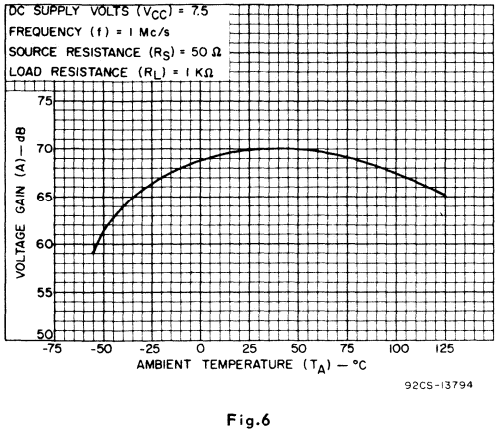


Fig.6

VOLTAGE GAIN vs. FREQUENCY

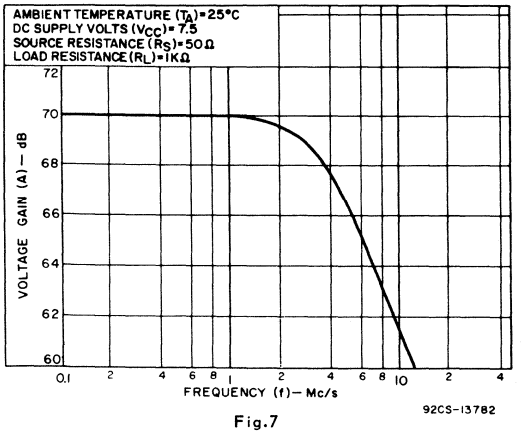


Fig.7

CA3013, CA3014

TYPICAL CHARACTERISTICS AND TEST SETUPS

INPUT-IMPEDANCE COMPONENTS TEST SETUP

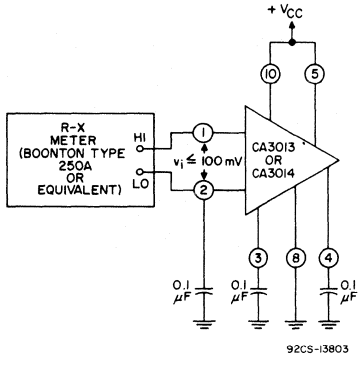


Fig.8

INPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

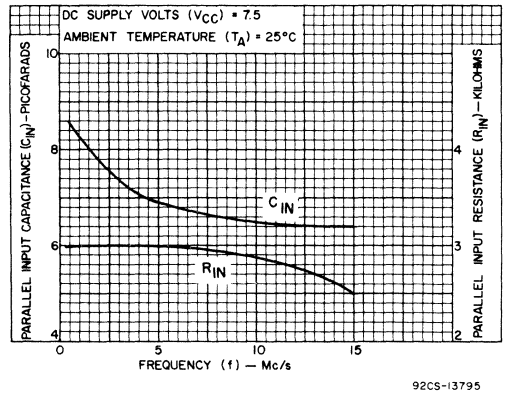


Fig.9

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

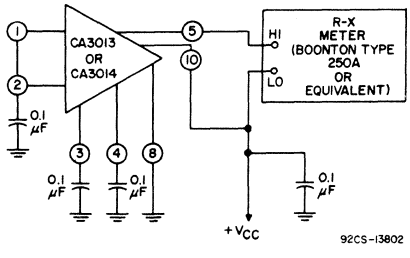


Fig.10

OUTPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

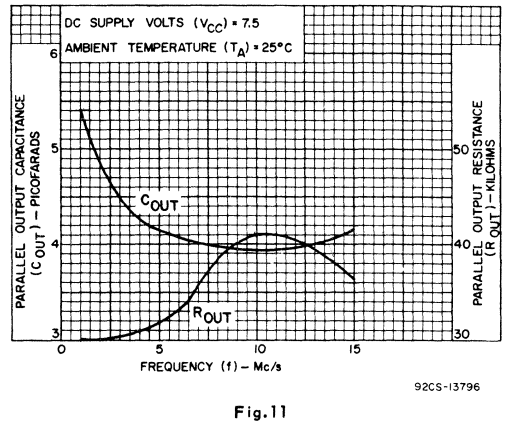
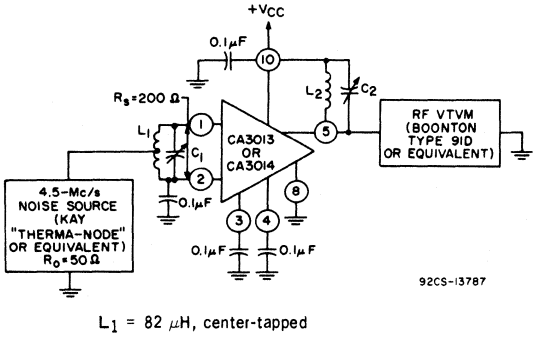


Fig.11

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1, C_2 = Arco Type 423 padder, or equivalent

Fig.12

NOISE FIGURE vs. DC SUPPLY VOLTAGE

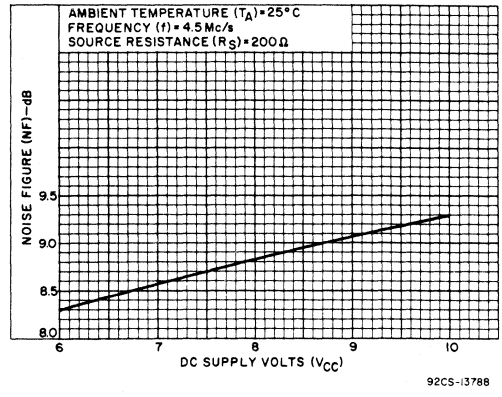
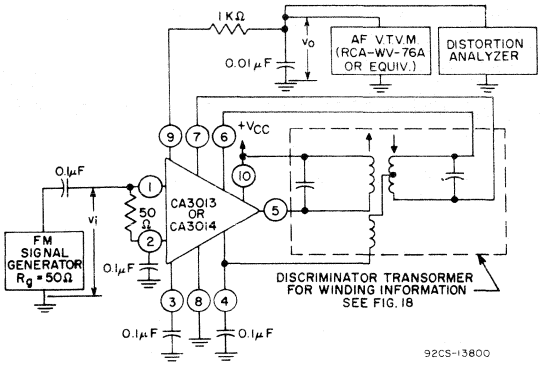


Fig.13

TYPICAL CHARACTERISTICS AND TEST SETUPS

INPUT LIMITING VOLTAGE, RECOVERED AF VOLTAGE, AND TOTAL HARMONIC DISTORTION TEST SETUP



PROCEDURE:

A - Recovered-AF Voltage Output:

1) Set input frequency = 4.5 Mc/s, v_i = 100 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.
2) Record v_o as Recovered-AF Voltage Output.

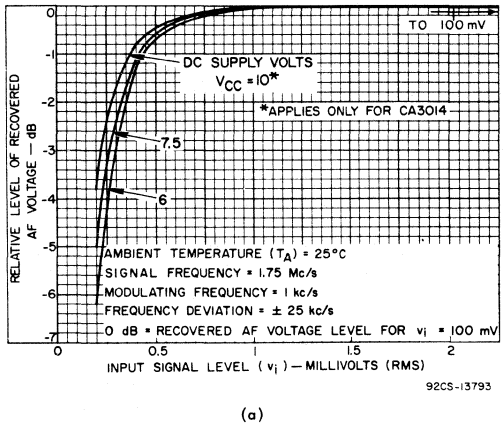
B - Input Limiting Voltage (Knee):

1) Repeat Steps A1 and A2, using v_i = 100 mV rms.
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

Fig. 14

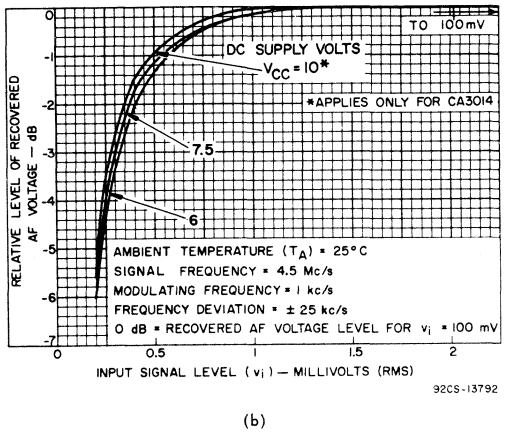
INPUT LIMITING VOLTAGE (KNEE) AND RECOVERED AF VOLTAGE

at 1.75 Mc/s



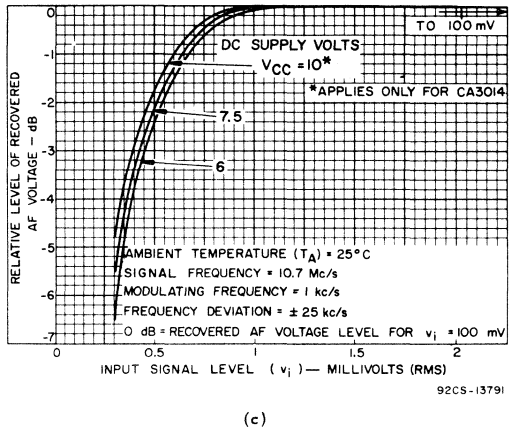
(a)

at 4.5 Mc/s



(b)

at 10.7 Mc/s



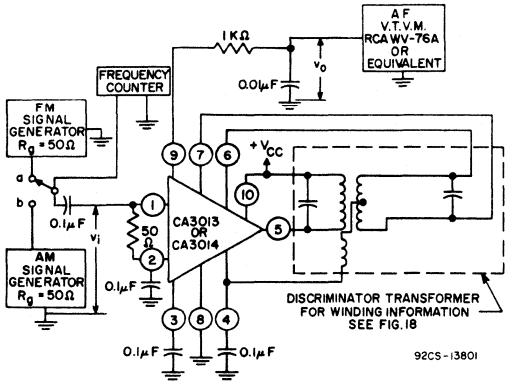
(c)

Fig. 15

CA3013, CA3014

TYPICAL CHARACTERISTICS AND TEST SETUPS

AM-REJECTION TEST SETUP



PROCEDURE:

1) With Switch S in position "a", set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.
2) Record v_o.
3) Place Switch S in position "b", and set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, % modulation = 50.
4) Measure v_o, and record value in dB below value in Step 2 as AM Rejection.

Fig. 16

TOTAL HARMONIC DISTORTION vs. DC SUPPLY VOLTAGE

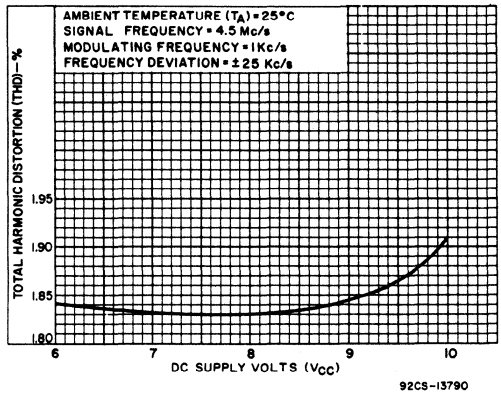
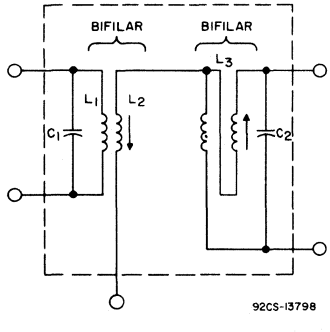


Fig. 17

DISCRIMINATOR TRANSFORMER SCHEMATIC



(a)

CONSTRUCTION DETAILS OF DISCRIMINATOR TRANSFORMERS SHOWN IN FIGS. 2, 14 AND 16

Coil-Form Outside Diameter = 7/32 inch

Slugs: Radio Industries, Inc. Type "E" Material, or equivalent

Wire Type: "GRIPEZE"*, or equivalent

Operating Frequency Mc/s	Wire Size (AWG #)	Turns L_1▲	Turns L_2▲	Turns L_3	C_1 pF	C_2 pF
1.75	40	44	20	44 total (22 bifilar wound)	820	820
4.5	36	18	7	22 total (11 bifilar wound)	560	330
10.7	36	18	18	18 total (9 bifilar wound)	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products.

▲ wound bifilar.

NOTE: The mutual coupling between L_1 and L_3 is adjusted for the desired degree of linearity.

(b)

Fig. 18

CA3048

Four Independent AC Amplifiers

For Low-Noise and General AC Applications
In Industrial Service

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- Noise figure at 1kHz..... 2 dB typ.
- High voltage gain..... 53 dB min.
- High input resistance..... 90 kΩ typ.
- Undistorted output voltage 2 V rms min.
- Output Impedance..... 1 kΩ typ.
- Open-loop bandwidth..... 300 kHz typ.

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply.

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

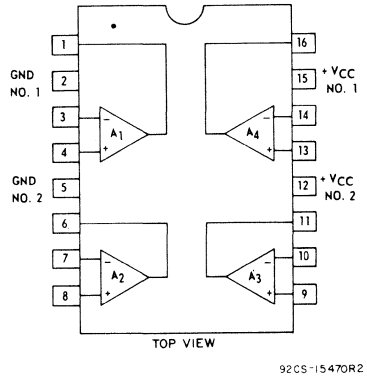


Fig. 1 - Block diagram for CA3048.

File Number **377**

CA3048

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A = 55°C . . . . . 750 mW
- Above T_A = 55°C . . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . -40°C to +85°C
- Storage . . . . . -65°C to +150°C

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

.ECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3048			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
TATIC								
:urrent drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V	3	9.5	13.5	17.5	mA	4,5
)C Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12V	3	6.1	6.9	8.1	V	-
)C Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12V	3	1.7	2.0	2.3	V	-
)C Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12V	3	2.2	2.5	2.8	V	-
)YNAMIC (Characteristics given are for each amplifier with no AC feedback)								
)pen-Loop Gain	A_{OL}	V_{CC} = +12V, E_{IN} = 2mV, f = 10kHz	6	53	58	-	dB	7,8
)utput Voltage Swing	V_O(rms)	V_{CC} = +12V, f = 1kHz, THD = 5%	6	2.0	2.4	-	V	-
)pen-Loop -3dB Bandwidth	BW	V_{CC} = +12V, E_{IN} = 2mV	6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz, E_{OUT} = 2V rms	6	-	0.65	-	%	10
nput Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground, f = 1kHz	-	-	90	-	kΩ	-
nput Capacitance	C_{IN}	f = 1MHz	-	-	9	-	pF	-
)utput Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground	-	-	1	-	kΩ	-
)utput Capacitance	C_{OUT}	f = 1MHz	-	-	18	-	pF	-
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12V, f = 1MHz	-	-	<0.1	-	pF	-
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V, R_S = 10kΩ, A = 40dB, Equivalent Noise BW = 50kHz	11	-	0.3	1	mV	-
Output Noise Voltage "Weighted"	E_N(WT)		12	-	0.5	2.2	mV	-
Noise Figure	NF (R_S = 5kΩ)	f = 10Hz	-	-	10	-	dB	-
		f = 100Hz	-	-	5.8	-	dB	
		f = 1kHz	-	-	2	-	dB	
		f = 10kHz	-	-	1.1	-	dB	
		f = 100kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V, f = 1kHz, 0dB = 0.78V	13	-	<-45	-	dB	-
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V, f = 1MHz	-	-	<0.02	-	pF	-

CA3048

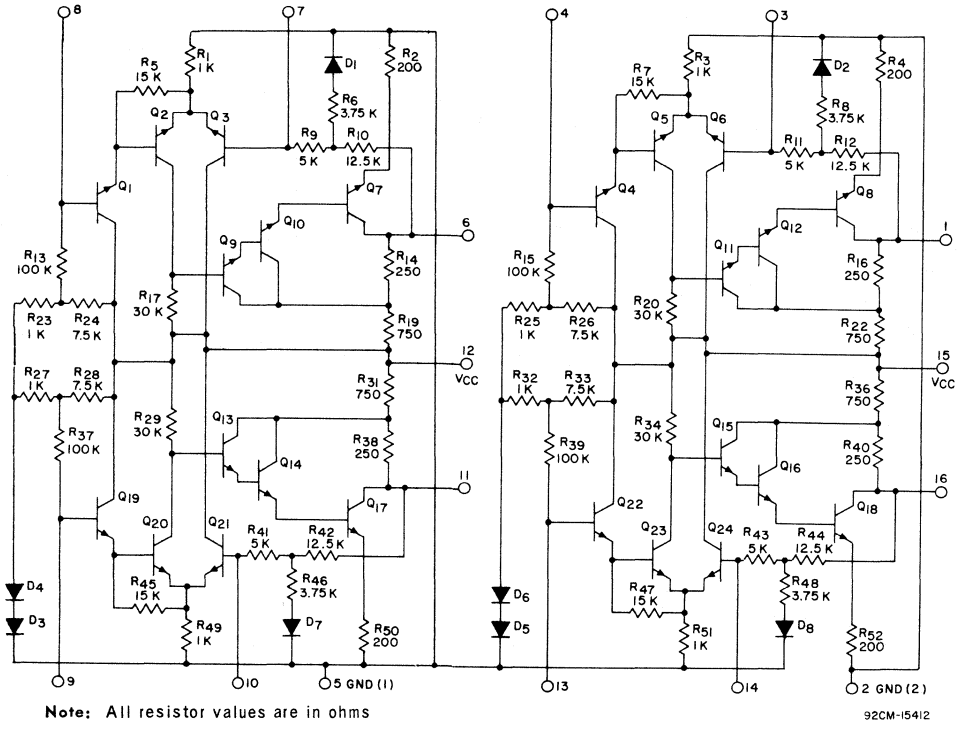


Fig.2 - Schematic diagram for CA3048.

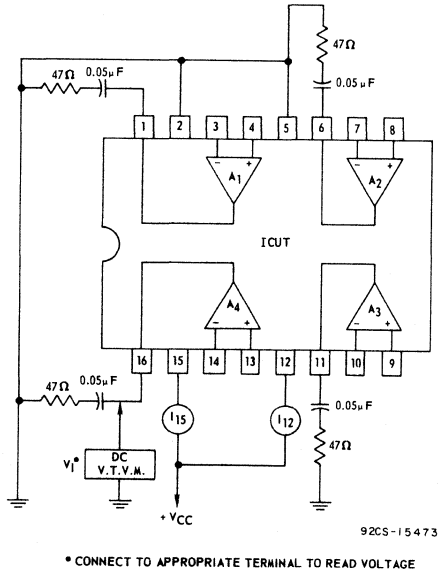


Fig.3 - Test circuit for measurement of collector supply voltage and currents.

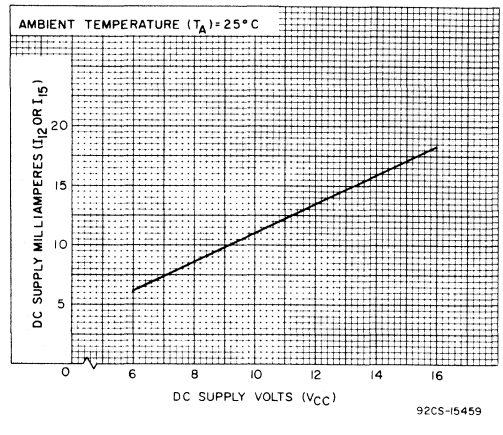


Fig.4 - Typical DC supply current vs supply voltage.

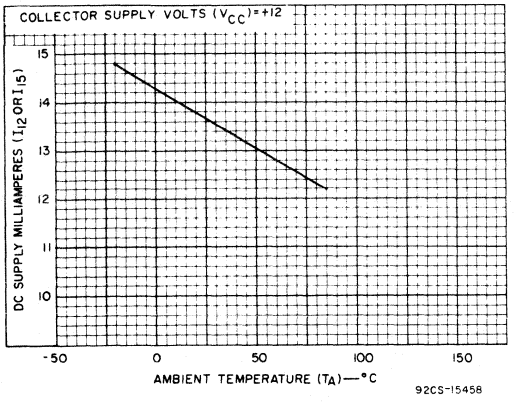


Fig.5 - Typical DC supply current vs ambient temperature.

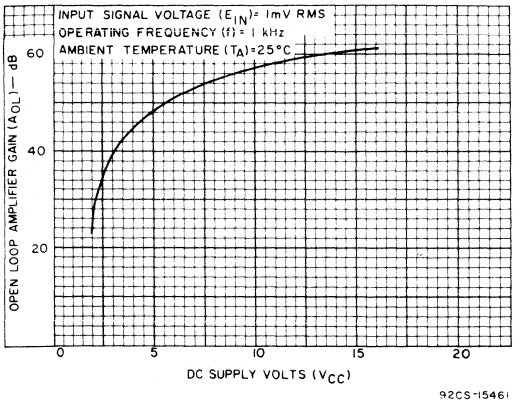
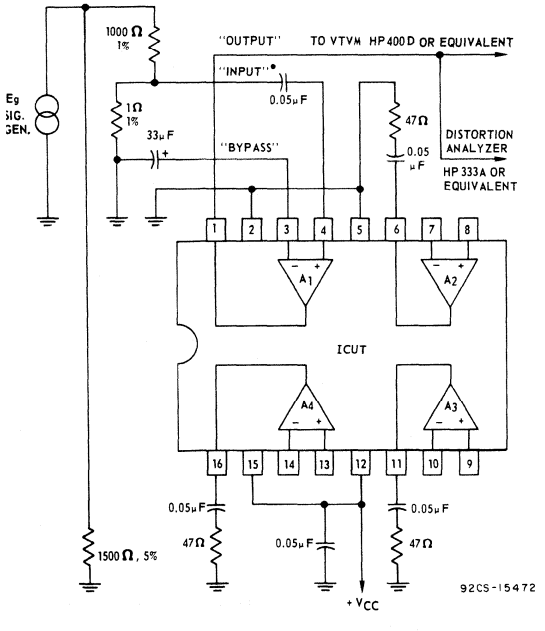


Fig.7 - Typical amplifier gain vs DC supply voltage.



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_S = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

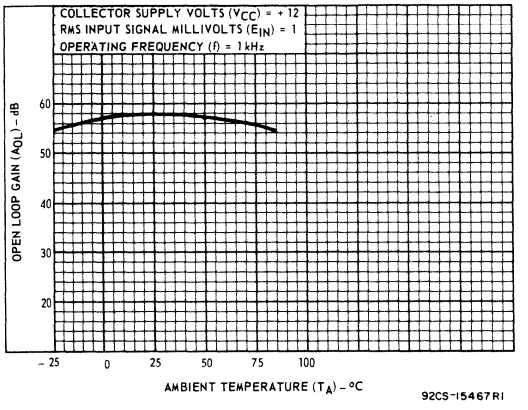


Fig.8 - Typical open-loop gain vs ambient temperature.

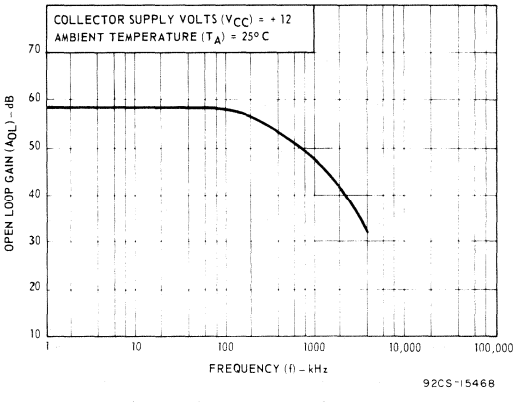


Fig.9 - Typical open-loop gain vs frequency.

CA3048

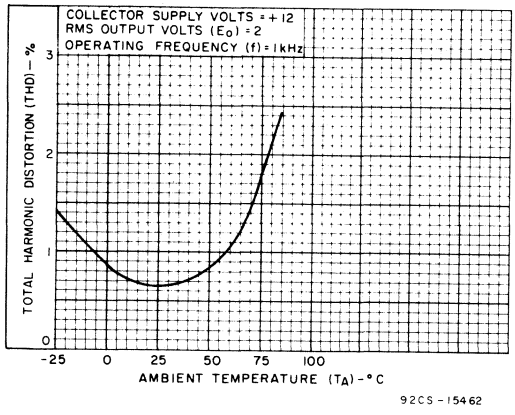
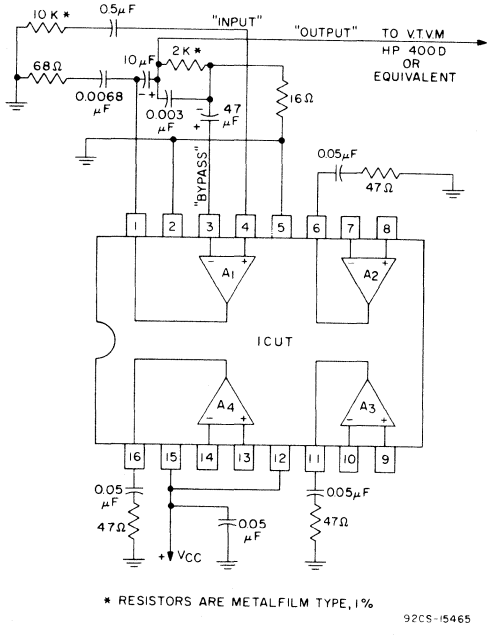


Fig.10 - Typical total harmonic distortion vs ambient temperature.

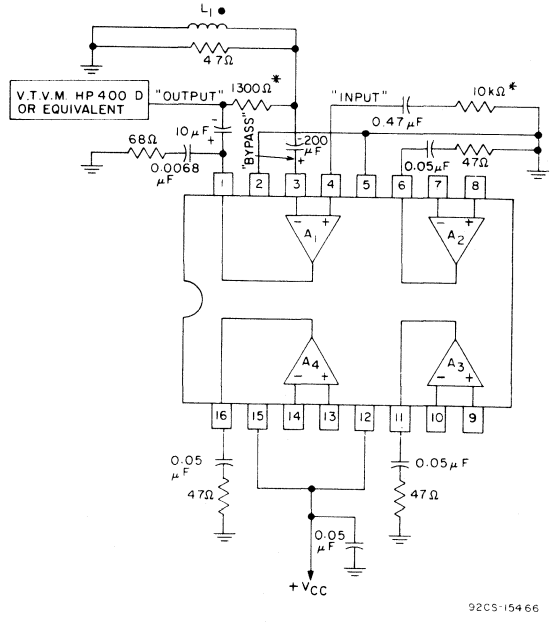


* RESISTORS ARE METALFILM TYPE, 1%

To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

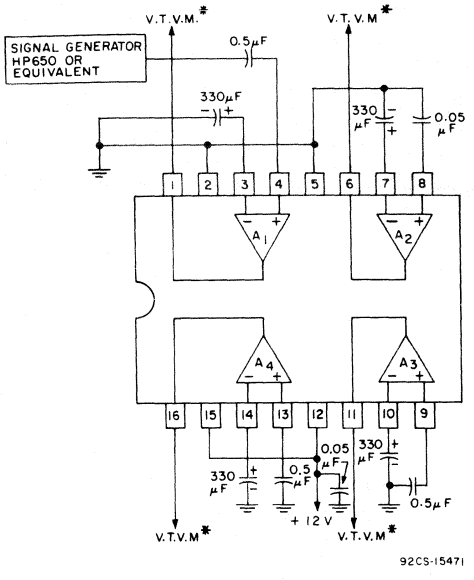


● L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

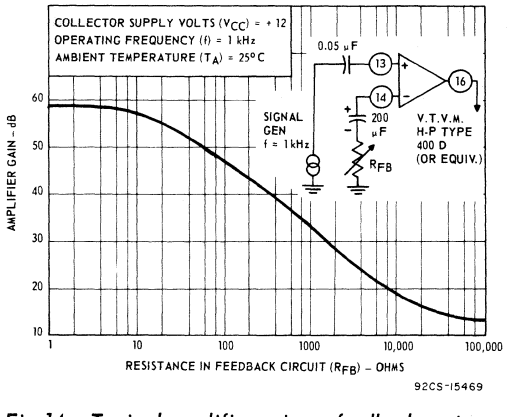


Fig.14 - Typical amplifier gain vs feedback resistance.

CA3052

Four Independent AC Amplifiers

Special-Function Sub-System for Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

Features:

- *Four AC amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Operates from single-ended supply*

EACH AMPLIFIER

- *High voltage gain - 53 dB min.*
- *High input resistance - 90 kΩ typ.*
- *Undistorted output voltage - 2 V rms min.*
- *Output impedance - 1 kΩ typ.*
- *Open-loop bandwidth - 300 kHz typ.*

The RCA-CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent ac amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. It can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

Applications:

- *Full-function stereo preamplifiers*
- *Tape recorder and playback preamplifiers*
- *Tone generators*

RCA-CA3052 is schematically identical with the CA3048 Amplifier Array (File No. 377). Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

ABSOLUTE-MAXIMUM RATING *at* $T_A = 25°C$:

DISSIPATION:

Up to $T_A = 55°C$ ..... 750 m

Above $T_A = 55°C$ ..... Derate linearly at 7.7 mW/°

TEMPERATURE RANGE:

Operating ..... −40° C to +85°

Storage ..... −65° C to +150°

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)

from case for 10 seconds max. ..... +265°

POWER SUPPLY VOLTAGE ..... +16

AC INPUT VOLTAGE ..... 0.5 V rm

File Number **387**

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	+2 -3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

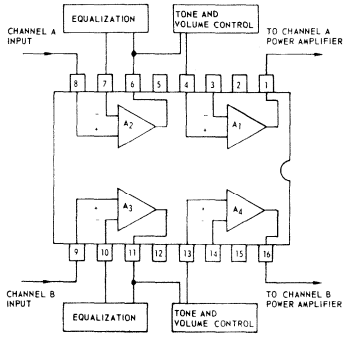


Fig. 1 – Block diagram of stereo preamplifier using CA3052.

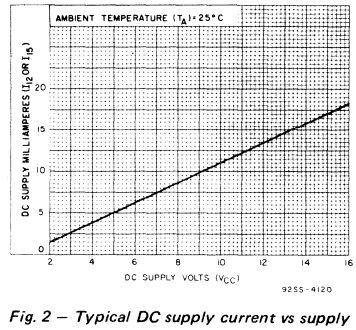


Fig. 2 – Typical DC supply current vs supply voltage.

CA3052

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS CA3052			UNITS
			MIN.	TYP.	MAX.	
STATIC						
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12 V	9.5	13.5	17.5	mA
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12 V	6.1	6.9	8.1	V
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12 V	1.7	2.0	2.3	V
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12 V	2.2	2.5	2.8	V
DYNAMIC each amplifier with no AC feedback unless otherwise noted–terminals 3, 7, 10, & 14 bypassed to ground						
Open-Loop Gain	A_{OL}	V_{CC} = +12 V E_{IN} = 2 mV f = 10 kHz	53	58	–	dB
Open-Loop Output Voltage Swing	$V_{O(rms)}$	V_{CC} = +12 V f = 1 kHz THD = 5%	2.0	2.4	–	V
Open-Loop -3 dB Bandwidth	BW	V_{CC} = +12 V E_{IN} = 2 mV	–	300	–	kHz
Open-Loop Total Harmonic Distortion	THD	V_{CC} = +12 V, f = 1 kHz E_{OUT} = 2 V rms	–	0.65	–	%
Input Resistance	R_I	V_{CC} = +12 V, f = 1 kHz	–	90	–	kΩ
Input Capacitance	C_I	V_{CC} = +12 V, f = 1 MHz	–	9	–	pF
Output Resistance	R_O	V_{CC} = +12 V, f = 1 kHz	–	1	–	kΩ
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12 V f = 1 MHz	–	< 0.1	–	pF
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{NI}‡	V_{CC} = +10 V R_S = 5 kΩ A = 45 dB	–	1.7	6.4	μV
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	V_{CC} = +10 V R_S = 5 kΩ A = 64 dB (1 kHz)	–	4	15.0	μV
Inter-Amplifier Audio Separation "Cross Talk"[11]		V_{CC} = +12 V f = 1 kHz 0 dB = 0.78 V	–	< -45	–	dB
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12 V f = 1 MHz	–	< 0.02	–	pF

*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit

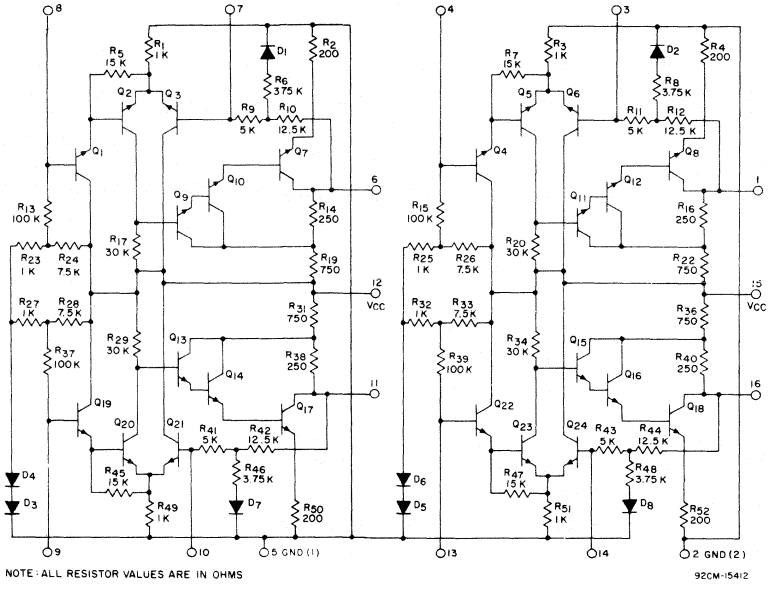


Fig. 3 – Schematic diagram for CA3052.

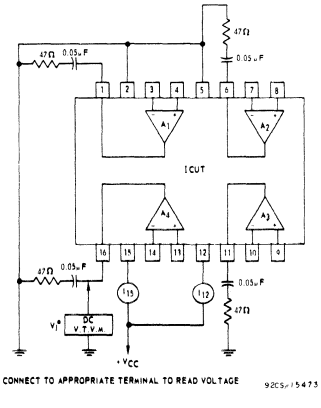


Fig. 4 – Test circuit for measurement of collector supply voltage and currents.

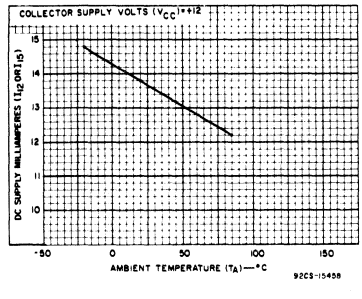
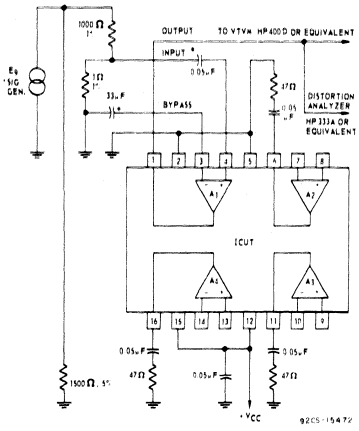


Fig. 5 – Typical DC supply current vs ambient temperature.

CA3052



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_S to 2 volts will make E_S = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 – Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

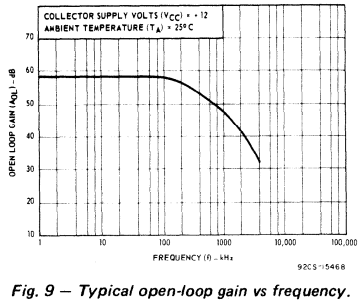


Fig. 9 – Typical open-loop gain vs frequency.

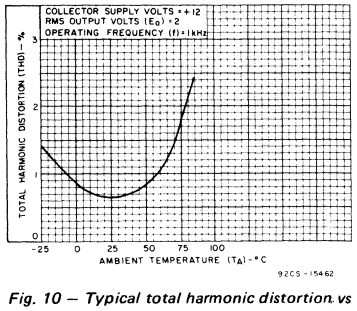


Fig. 10 – Typical total harmonic distortion vs ambient temperature.

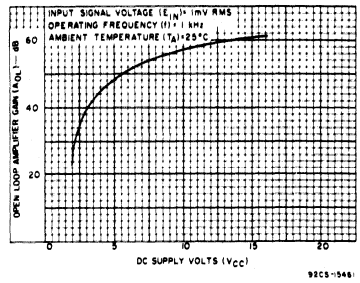


Fig. 7 – Typical amplifier gain vs DC supply voltage.

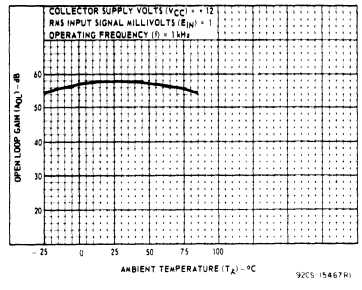
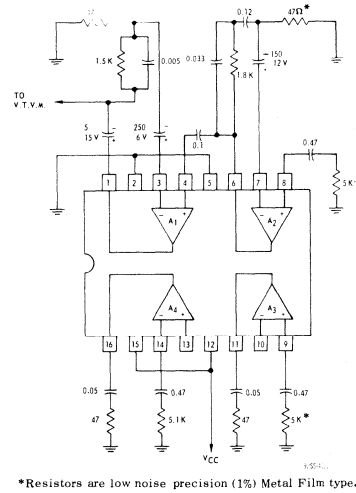
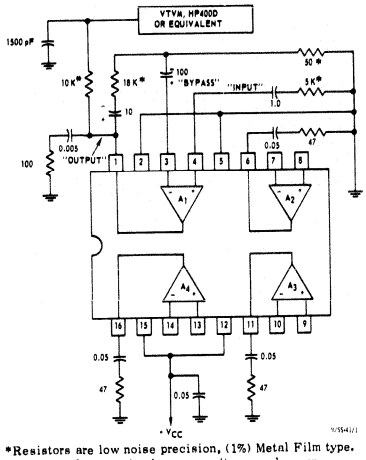


Fig. 8 – Typical open-loop gain vs ambient temperature.



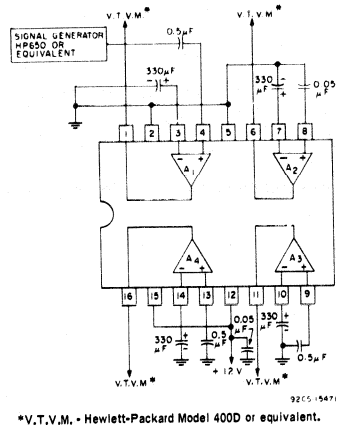
*Resistors are low noise precision (1%) Metal Film type.

Fig. 11 – Test circuit for equivalent input noise voltage measurement, RIAA compensated.



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 12– Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.

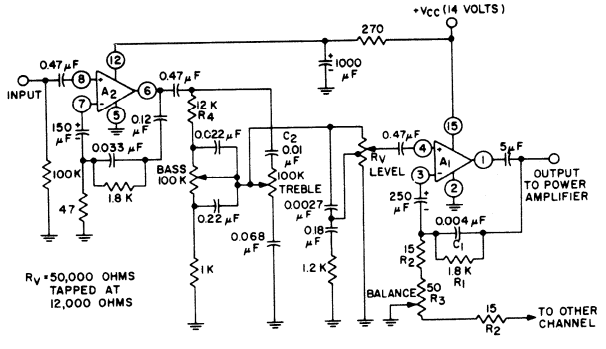


*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 13 – Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.



Performance Data

Gain at 1-kHz reference	47 dB
Boost at 100 Hz	11.5 dB
Boost at 10 kHz	11.5 dB
Cut at 100 Hz	10 dB
Cut at 10 kHz	9 dB
Noise:	
At maximum volume (input shorted)	> 70 dB below 1 volt
At minimum volume	> 80 dB below 1 volt
Total harmonic distortion (at 1-kHz reference and an output of 1 volt)	< 0.3 per cent

92CM-29305

Fig. 14 - Schematic of one channel of a complete stereo preamplifier.

CA3052

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3052 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig. 15 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3052, as in other devices having high gain-band-width product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3052 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

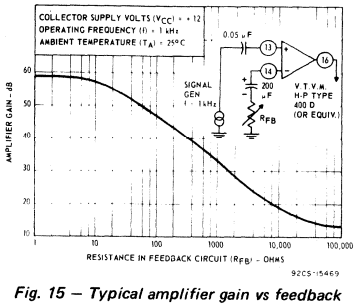


Fig. 15 – Typical amplifier gain vs feedback resistance.

CA3075

FM IF Amplifier-Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

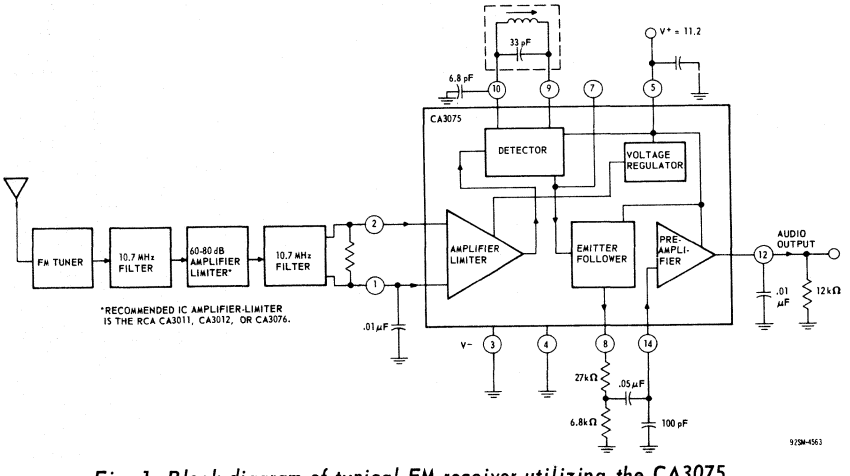


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

File Number **429**

CA3075

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

DC Supply Voltage [between Terminals 5 (V^+) and 3 (V^-)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During soldering for 10 s max.)	+260	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5	–	8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER Input Limiting Voltage (knee, − 3 dB point)	V_I(lim)	f_O = 10.7 MHz f(Modulation) = 400 Hz Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_O = 10.7 MHz f(Modulation) − 400 Hz FM: Deviation = ±75 kHz AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							–
Parallel Resistance	R_I	f_O = 10.7 MHz	–	4.5	–	kΩ	
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR							
Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_O = 10.7 MHz f(Modulation) = 400 Hz	–	1.5	–	V	3
Total Harmonic Distortion	THD	Deviation = ± 75 kHz	–	1	2	%	
AUDIO PREAMPLIFIER							
Voltage Gain	A(AF)	V_{IN} = 100 mV, f_O = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_O = 400 Hz	–	1.5	5	%	4

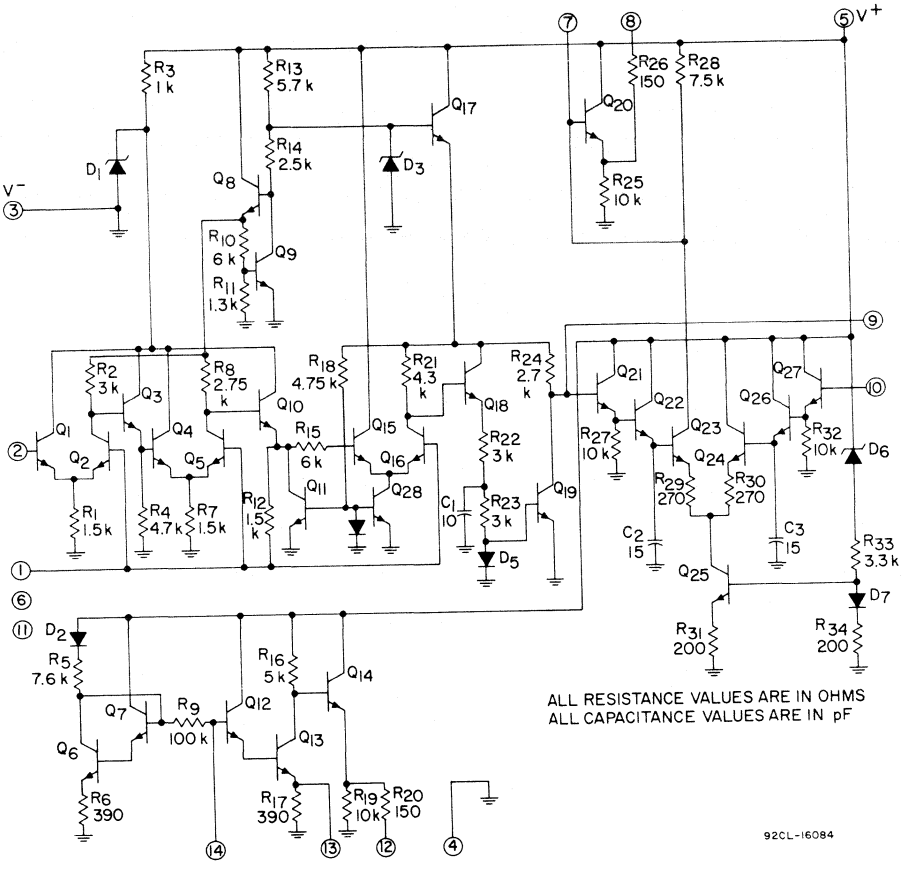


Fig. 2 - Schematic diagram of CA3075

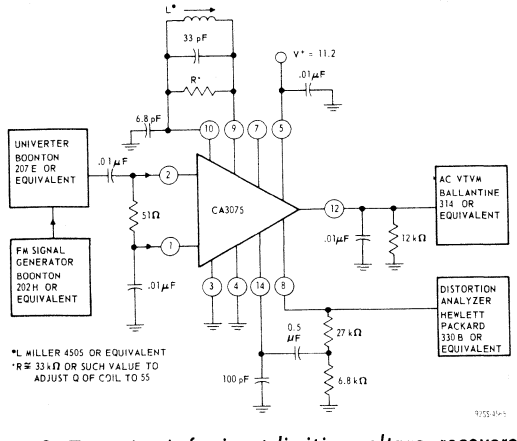


Fig. 3 - Test circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion

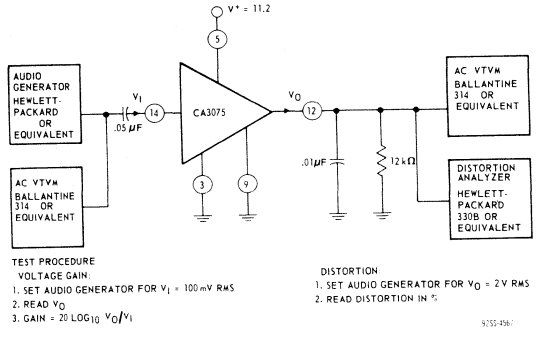


Fig. 4 - Test circuit for audio preamplifier voltage gain and total harmonic distortion

CA3075

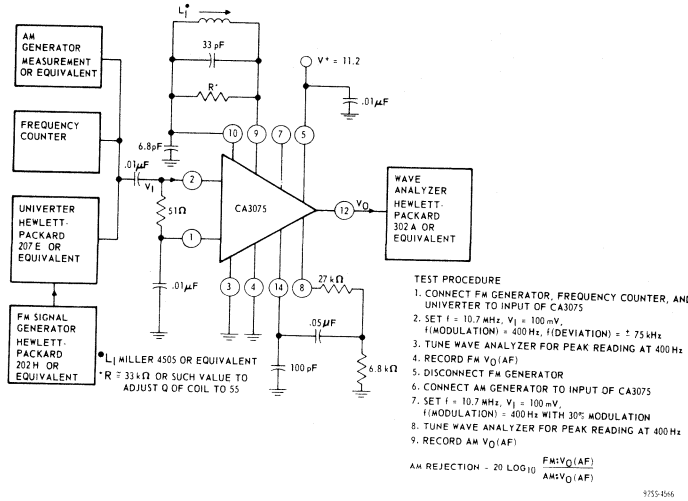


Fig. 5 - Test circuit for AM rejection

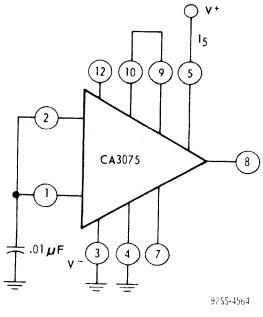
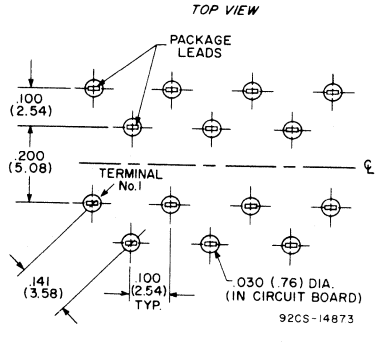


Fig. 6 - Test circuit for static characteristics

Recommended Mounting-Hole Dimensions and Spacings.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.

CA3088

AM Receiver Subsystem and General-Purpose Amplifier Array

Includes: AM Converter, IF Amplifiers, Detector and Audio Preamplifier

For Applications in a Variety of AM Broadcast and Communications Receivers and Applications Requiring an Array of Amplifiers

Features:

- **Excellent overload characteristics**
- **AGC for IF amplifier**
- **Buffered output signal for tuning meter**
- **Internal Zener diode provides voltage regulation**
- **Two IF amplifier stages**
- **Low-noise converter and first IF amplifier**
- **Low harmonic distortion (THD)**
- **Delayed AGC for RF amplifier**
- **Terminals for optional inclusion of tone control**
- **Operates from wide range of power supplies: V^+ = 6 to 16 volts**
- **Optional AC and/or DC feedback on wide-band amplifier**
- **Array of amplifiers for general-purpose applications**
- **Suitable for use with optional external RF stage, either MOS or bipolar**

RCA-CA3088E*, a monolithic integrated circuit, is an AM subsystem that provides the converter, IF amplifier, detector, and audio preamplifier stages for an AM receiver.

The CA3088E also provides internal AGC for the first IF amplifier stage, delayed AGC for an optional external RF amplifier, a buffer stage to drive a tuning meter, and terminals facilitating the optional use of a tone control.

Fig. 2 is a functional diagram of the CA3088E. The signal from the low-noise converter is applied to the first IF amplifier and is then coupled to the second IF amplifier. This IF signal is then detected and externally filtered. The resultant audio signal is applied to an audio preamplifier. Optionally, a tone control circuit may be connected at the junction of the detector circuit and the audio preamplifier. The gain of the first IF amplifier stage is controlled by an internal AGC circuit. The CA3088E supplies a delayed AGC signal output for use with an external RF amplifier. A buffered output signal is also available for driving a tuning meter. A DC voltage, internally regulated by a Zener diode, supplies the second IF amplifier, the AGC and tuning meter circuits and may also be used with any other stage.

The CA3088E features four independent transistor amplifiers, each incorporating internal biasing for temperature tracking. These amplifiers are particularly useful in general-purpose amplifier, oscillator, and detector applications in a wide variety of equipment designs.

The CA3088E utilizes a 16-lead dual-in-line plastic package and operates over an ambient temperature range of −40°C to +85°C.

*Formerly Developmental Type TA5842.

MAXIMUM RATINGS, *Absolute Maximum Values, at T_A = 25°C*

DC SUPPLY VOLTAGE:		
Across Term. 5 and Terms. 3, 6, 13, 16, respectively	16	V
DC CURRENT:		
At Terms. 3, 6, 13, 16, respectively	10	mA
At Term. 10	30	mA
DEVICE DISSIPATION:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
LEAD TEMPERATURE (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

File Number **560**

CA3088

ELECTRICAL CHARACTERISTICS, at $T_A = 25^oC$, $V^+ = 12$ V.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		TYPICAL VALUES	UNITS
			TEST CIRCUIT FIG. NO.		
Static (DC) Characteristics					
DC Voltages:					
Terms. 1, 4, 9, 11	$V_{1, 4, 9, 11}$		1	0.7	V
Terms. 2, 7, 8	$V_{2, 7, 8}$			1.4	V
Term. 10	V_{10}			5.6	V
Term. 12	V_{12}			0	V
Term. 15	V_{15}			3.5	V
DC Current:					
Term. 3	I_3		1	0.35	mA
Term. 6	I_6			1.0	mA
Term. 10	I_{10}			20	mA
Term. 13	I_{13}			0	mA
Term. 16	I_{16}			1.2	mA
Dynamic Characteristics					
Detector Output		30% Modulation	4	75	mV RMS
Audio Amplifier Gain	A_{AF}	f = 1 kHz	4	30	dB
Audio Distortion		V_{OUT} = 100 mV	4	0.2	%
Sensitivity:		f_{IN} = 1 MHz			
At Converter Stage Input		Signal-to-Noise Ratio (S/N) = 20 dB	2	200	μV/m
At RF Stage Input			4	100	μV/m
Total Harmonic Distortion	THD	30% Modulation	4	1.0	%
Input Resistance:	R_{IN}				
At Transistor Q1				3500	Ω
At Transistor Q5		No AGC,		2000	Ω
Input Capacitance:	C_{IN}				
At Transistor Q1		Input signal frequency		17	pF
At Transistor Q5		(f_{IN}) = 1 MHz		12	pF
Feedback Capacitance:	C_{FB}				
At Transistor Q1				1.5	pF
At Transistor Q5				1.5	pF

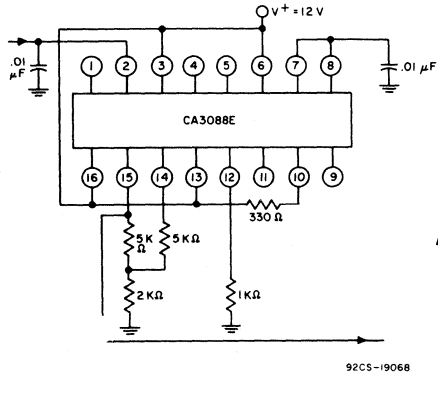


Fig.1—Test circuit for DC characteristics.

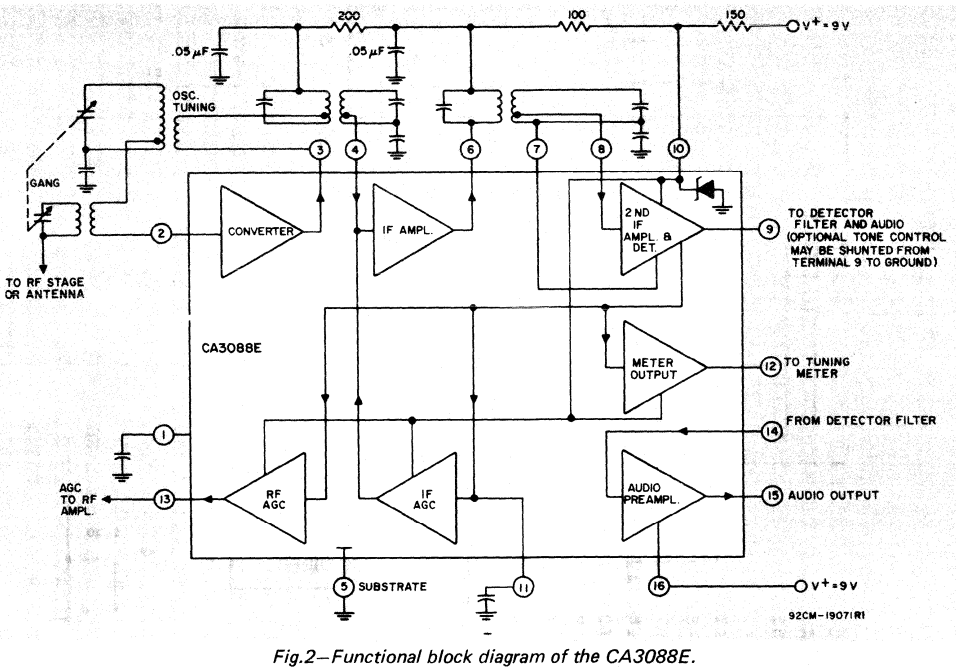


Fig.2—Functional block diagram of the CA3088E.

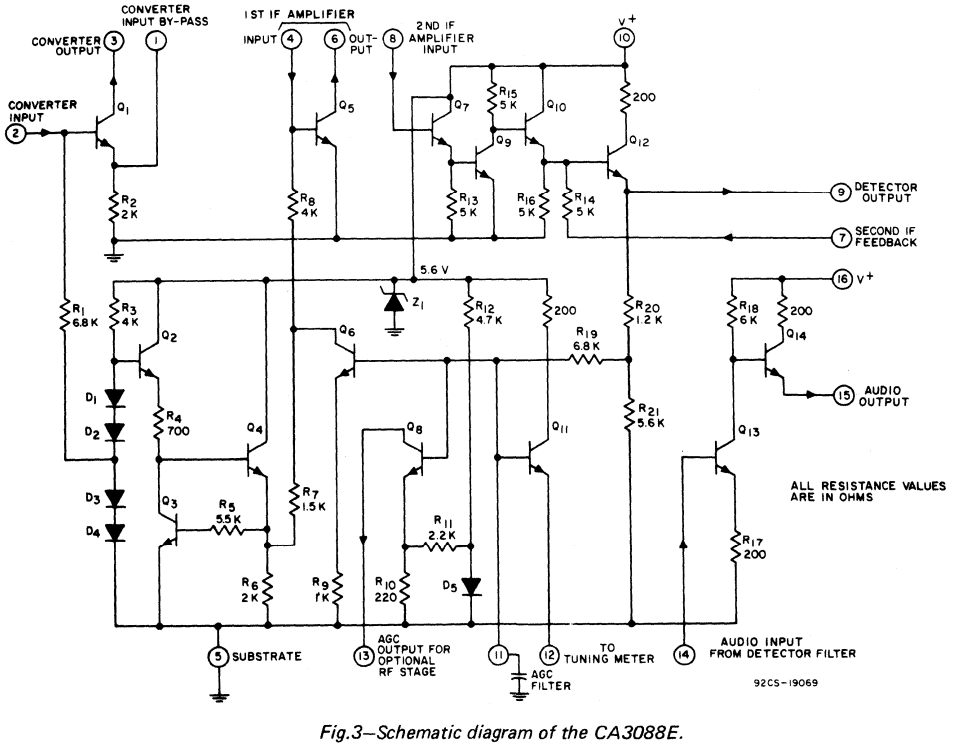


Fig.3—Schematic diagram of the CA3088E.

CA3088

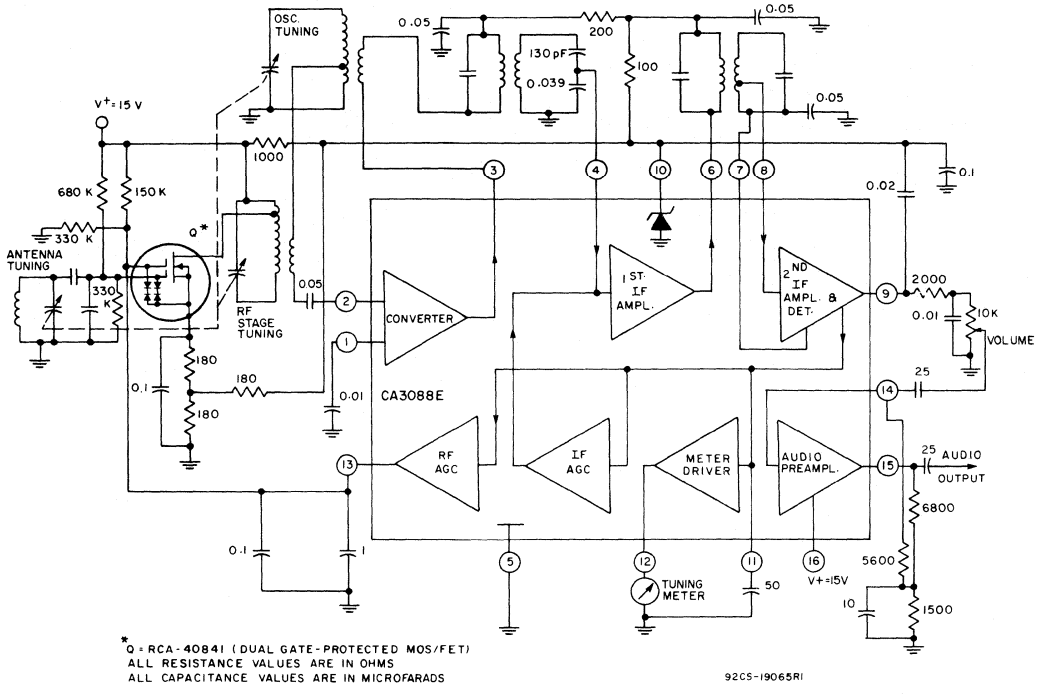


Fig.4—Typical AM broadcast receiver using the CA3088E with optional RF amplifier stage.

CA3089

FM IF System

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Includes———IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter

Features:

- **Exceptional limiting sensitivity: 12 μV typ. at −3 dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400 mV typ.**
- **Provides specific signal for control of inter-channel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply-voltage regulators**

RCA-CA3089E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

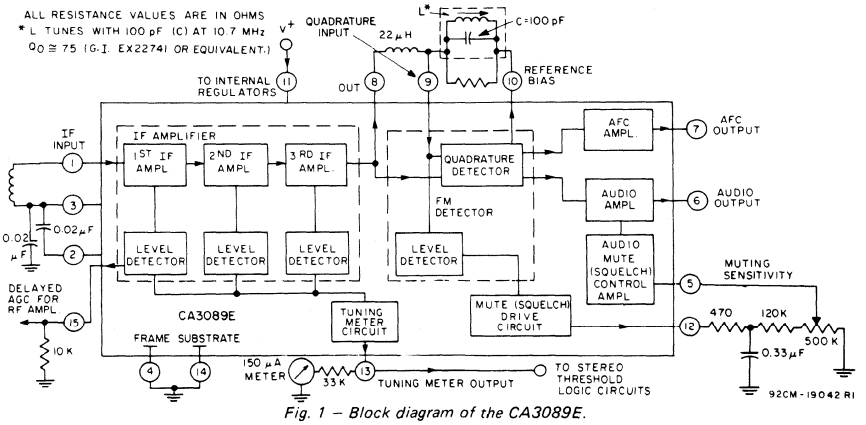


Fig. 1 – Block diagram of the CA3089E.

File Number **561**

CA3089

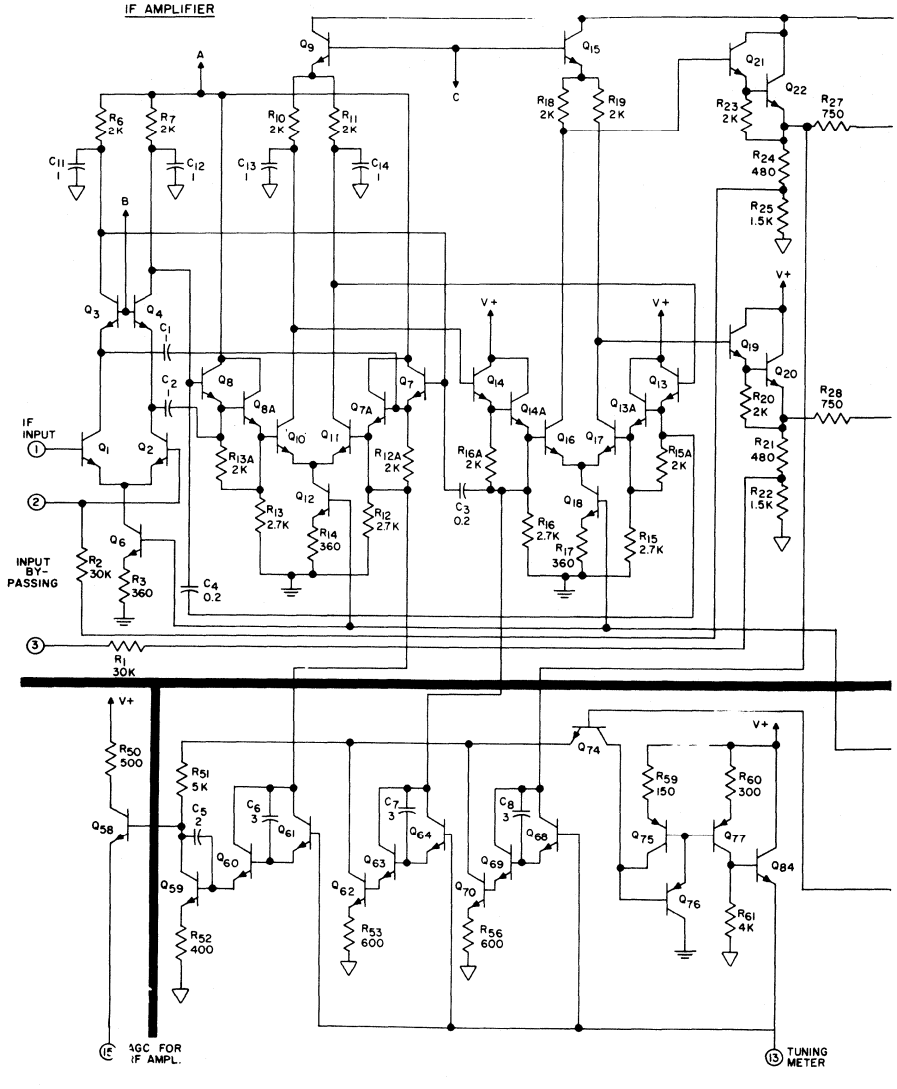


Fig. 2 - Schematic diagram of the CA3089E (cont'd on next page).

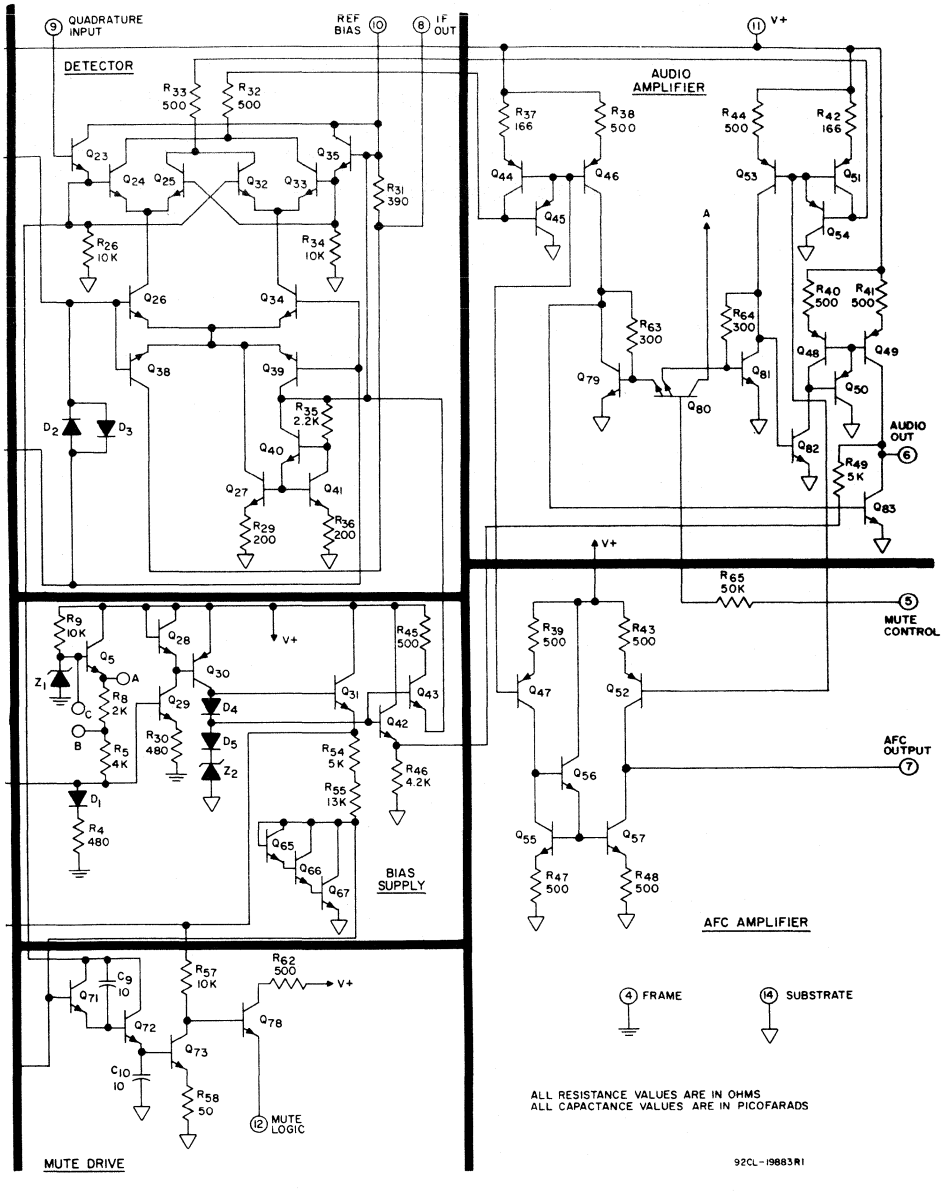


Fig. 2 - Schematic diagram of the CA3089E (cont'd from previous page).

CA3089

MAXIMUM RATINGS, *Absolute Maximum Values*

DC Supply Voltage:			
Between Terminals 11 and 4		16	V
Between Terminals 11 and 14		16	V
DC Current (out of Terminal 15)		2	mA
Device Dissipation:			
Up to $T_A = 60^\circ C$		600	mW
Above $T_A = 60^\circ C$	derate linearly	6.7	mW/°C
Ambient Temperature Range:			
Operating		−40 to + 85	°C
Storage		−65 to +150	°C
Lead Temperature (During Soldering):			
At distance not less than 1/32" (0.79mm) from case for 10 seconds max.		+265	°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ C$, V+ = 12 Volts (See Figs. 5 and 6)

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
Static (DC) Characteristics						
Quiescent Circuit Current	No signal input, Non muted		16	23	30	mA
DC Voltages: Terminal 1 (IF Input)			1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)			1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)			1.2	1.9	2.4	V
Terminal 6 (Audio Output)			5.0	5.6	6.0	V
Terminal 10 (DC Reference)			5.0	5.6	6.0	V
Dynamic Characteristics						
Input Limiting Voltage (−3 dB point), V_1 (lim)	–		–	12	25	μV
AM Rejection (Term. 6), AMR	V_{IN} = 0.1V, AM Mod. = 30%	f_O = 10.7 MHz, f_{mod} 400 Hz, Deviation = ±75 kHz	45	55	–	dB
Recovered AF Voltage (Term. 6) V_O (AF)	V_{IN} = 0.1 V		300	400	500	mV
Total Harmonic Distortion, THD:* Single Tuned (Term. 6)			–	0.5	1.0	%
Double Tuned (Term. 6)			–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)			60	67	–	dB

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8,9, and 10.

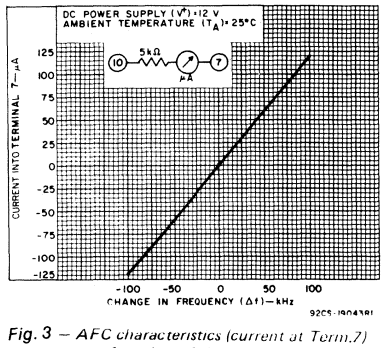


Fig. 3 – AFC characteristics (current at Term.7) as a function of change in frequency. (See test circuit Fig. 5.)

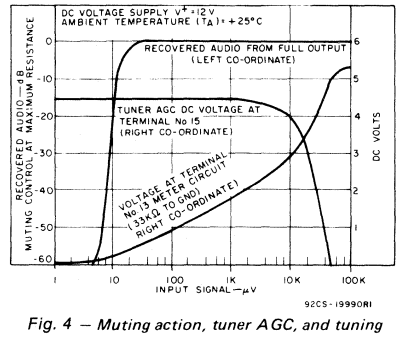


Fig. 4 – Muting action, tuner AGC, and tuning meter output as a function of input signal voltage. (See test circuit Fig.5.)

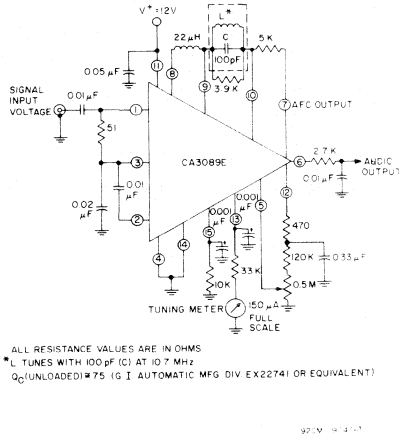


Fig. 5 – Test circuit for CA3089E using a single-tuned detector coil.

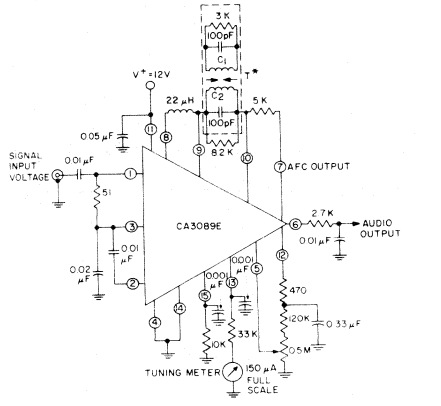
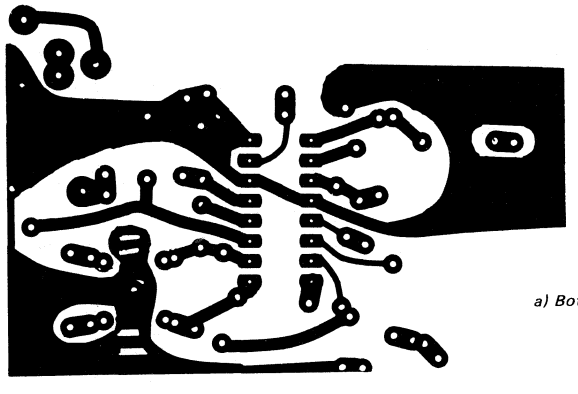
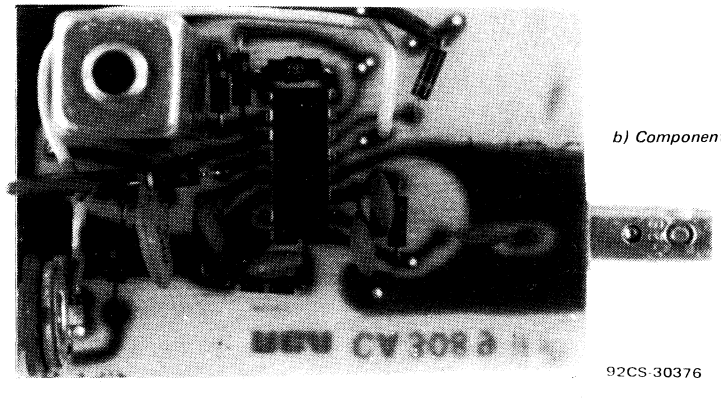


Fig. 6 – Test circuit for CA3089E using a double-tuned detector coil.



a) Bottom view of printed-circuit board.

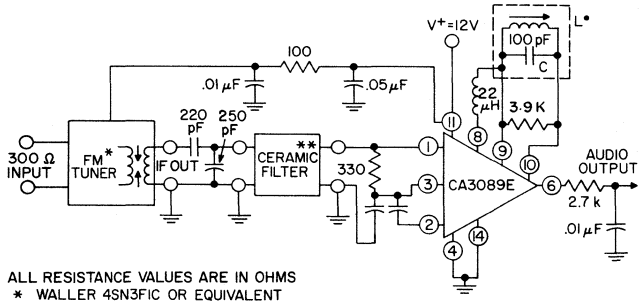


b) Component side – top view.

92CS-30376

Fig. 7 – Actual size photographs of the CA3089E and outboard components mounted on a printed-circuit board.

CA3089



ALL RESISTANCE VALUES ARE IN OHMS
* WALLER 4SN3FIC OR EQUIVALENT
** MURATA SFG 10.7 MA OR EQUIVALENT
• L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O UNLOADED ≅ 75 (G.I EX22741 OR EQUIVALENT)

Performance data at f_o = 98 MHz, f_{MOD} = 400 Hz, Deviation = ±75 kHz:

-3dB Limiting Sensitivity	2μV (Antenna Level)
20dB Quieting Sensitivity	1μV (Antenna Level)
30dB Quieting Sensitivity	1.5μV (Antenna Level)

Fig. 8 - Typical FM tuner using the CA3089E with a single-tuned detector coil.

CA3163

VHF/UHF Prescaler

Features:

- *Broadband operation - 90 to 1000 MHz*
- *High sensitivity*
- *Standard 5 V power supply*
- *Dual mode operation - VHF/UHF*
- *Complementary ECL outputs*
- *Independent VHF & UHF input terminals*

The RCA-CA3163E* is an integrated-circuit prescaler intended for use in TV frequency synthesis tuning systems over an input frequency range of 90 to 1000 MHz. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation can be selected by means of the bandswitch and the separate uhf and vhf input terminals provided. The output is a complementary emitter-coupled stage with controlled slew rate for harmonic suppression.

All input terminals should be ac coupled to the appropriate input signal source. Because of high sensitivity, unbuffered coupling from the local oscillator is possible in most cases. In the uhf mode, which is activated by applying a high level to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. As a result, approximately the same range of output frequencies are generated for both the uhf and vhf TV bands. An internal amplifier/multiplexer provides this control while isolating both inputs and amplifying the vhf signal. In addition, harmonic output is reduced above 40 MHz by limiting output signal rise and fall times and maintaining a balanced load.

The CA3163E is supplied in the 14-lead Dual-in-Line Plastic Package.

*Formerly RCA Developmental No. TA10535.

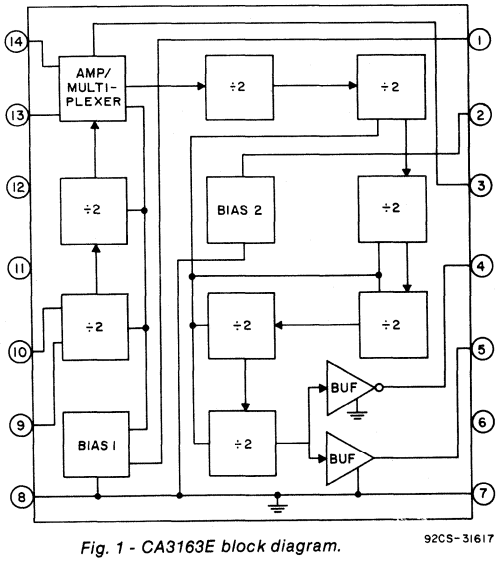
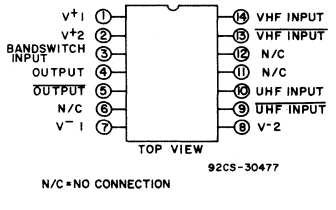


Fig. 1 - CA3163E block diagram. 92CS-31617

TERMINAL DIAGRAM



92CS-30477

N/C = NO CONNECTION

File Number **1092**

CA3163

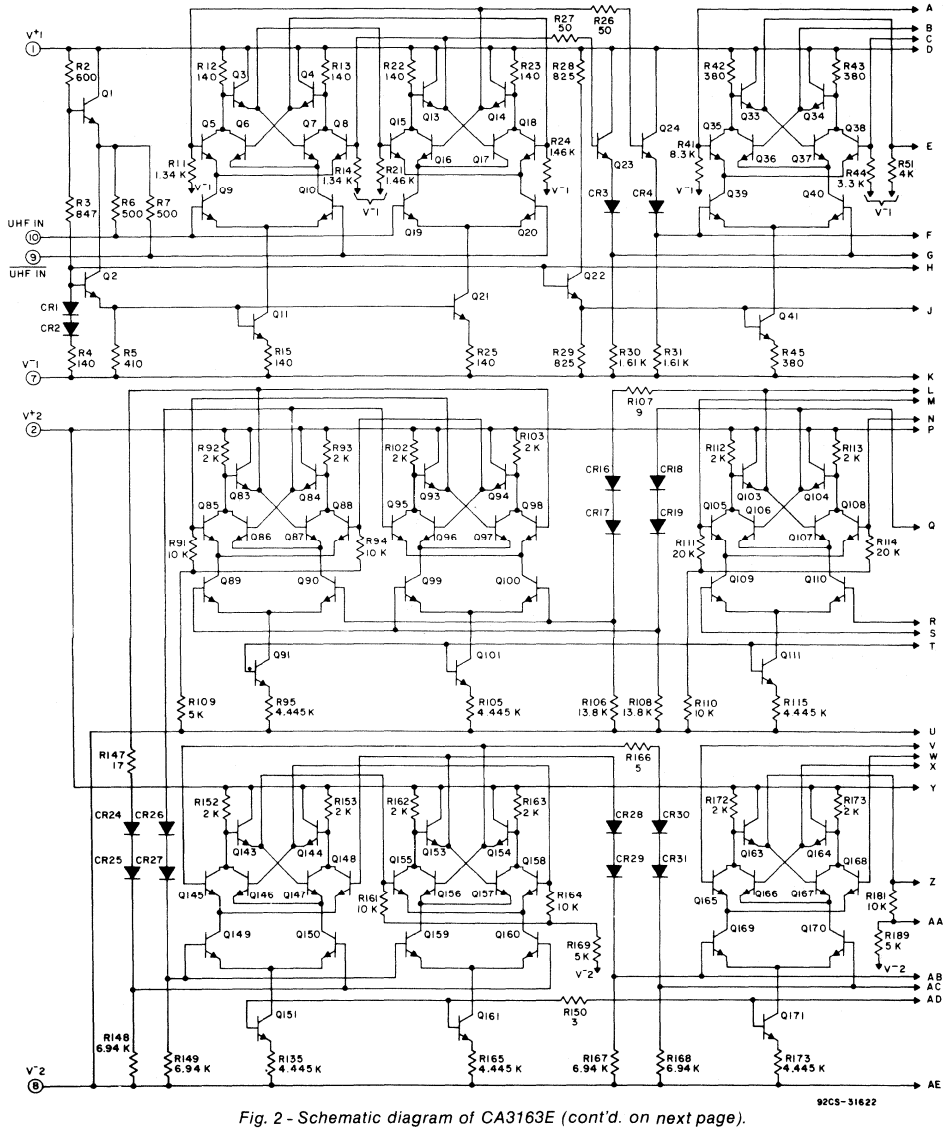


Fig. 2 - Schematic diagram of CA3163E (cont'd. on next page).

CA3163

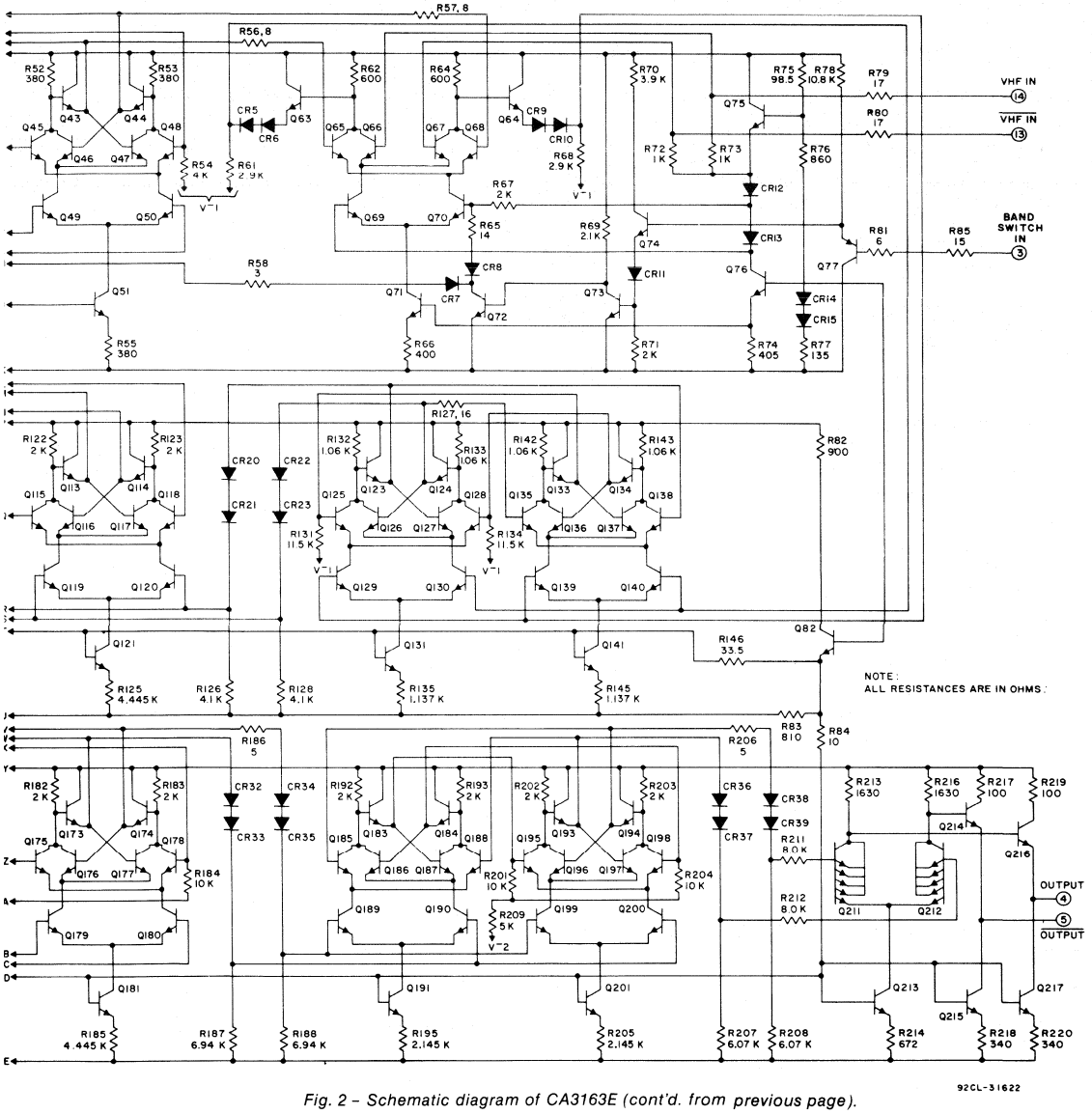


Fig. 2 - Schematic diagram of CA3163E (cont'd. from previous page).

CA3163

ELECTRICAL CHARACTERISTICS At T_A = 25°C, V^+ = 5VDC, V^- = 0 VDC; see Figs. 1 & 3

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current, I^+	Terms. (1+2), Fig. 1	30	60	90	mA
UHF Bandswitch Input Voltage, V_{BH}	High Level	2.4	—	—	V
VHF Bandswitch Input Voltage, V_{BL}	Low Level	—	—	0.8	V
UHF Bandswitch Input Current, I_{BH}	V_{BH} = 20 VDC, Fig. 1	—	—	0.5	mA
VHF Bandswitch Input Current, I_{BL}	V_{BL} = 0 VDC, Fig. 1	—	—	-1	mA
UHF Sensitivity Level Input Voltage, $V_{IN}(U)$	f_{IN} = 450 to 950 MHz, $f_{OUT} = f_{IN}/256$, Fig. 3	—	—	80	mVRMS
VHF Sensitivity Level Input Voltage, $V_{IN}(V)$	f_{IN} = 90 to 275 MHz, $f_{OUT} = f_{IN}/64$, Fig. 3	—	—	40	mVRMS
Output Voltage, V_O	Terms, 4 or 5, Fig. 3	0.65	1	—	V_{p-p}
Output Voltage Rise of Fall Time, t_r, t_f		—	70	—	ns

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	5.5	V
DC BANDSWITCH VOLTAGE	20	V
RMS INPUT VOLTAGE	0.5V	
DEVICE DISSIPATION:		
UP TO T_A = 70°C	600	mW
ABOVE T_A = 70°C	derate linearly at 7.5	mW/°C
AMBIENT TEMPERATURE RANGE:		
OPERATING	0 to 70	°C
STORAGE	-55 to +150	°C
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)		
FROM CASE FOR 10 SECONDS MAX.	+265	°C

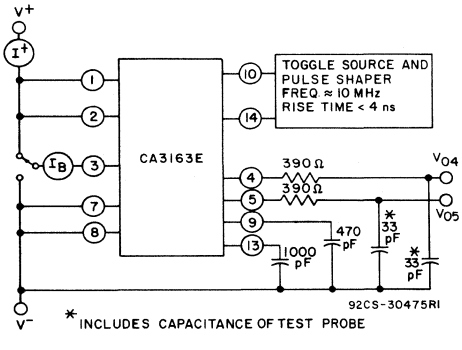


Fig. 3 - DC characteristics test circuit.

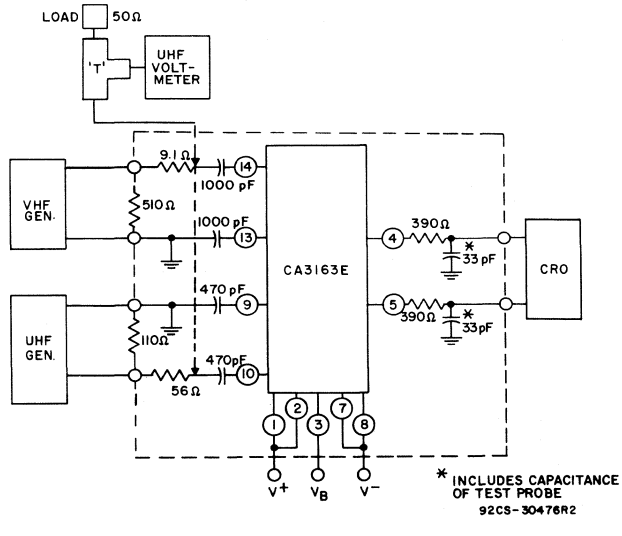


Fig. 4 - AC characteristics test circuit.

CA3179

1.25 GHz Prescaler

For Industrial Applications

FEATURES:
- *Broadband operation - DC to 1.25 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply*
- *Dual mode operation - VHF/UHF (÷ 64/ ÷ 256)*
- *Complementary ECL outputs*
- *Independent VHF and UHF input terminals*

The RCA-CA3179E is an integrated-circuit prescaler intended for use in communications and instrumentation systems. It performs division by 256 in the uhf mode and division by 64 in the vhf mode.

The mode of operation is selected by means of the bandswitch and the separate uhf and vhf input terminals provided. Either single- or double-ended inputs can be applied. These inputs are normally ac coupled, but dc coupling can be used if the specified bias levels are maintained. The output is a complementary emitter-coupled stage capable of driving a 33-pF or equivalent load. The harmonic output is reduced above 40 MHz by limiting output-signal rise and fall times and by maintaining a balanced load.

In the uhf mode, which is activated by applying a high level (logical 1) to the bandswitch input terminal, all eight divider stages are operative, resulting in division by 256. In the vhf mode, activated by a low level (logical 0) at the vhf input terminal, two divider stages are bypassed, resulting in division by 64. An internal amplifier/multiplexer provides this control while isolating both inputs, amplifying the input signal, and improving sensitivity.

The CA3179E is supplied in the 14-lead dual-in-line plastic package.

Applications:
- *Digital frequency synthesizers for:*
  VHF/UHF receivers
  Satellite communications
  Instrumentation
- *High-frequency divider for:*
  UHF frequency counters
  UHF timers
  High-speed computers
  Frequency standards
  SHF second IF local-oscillator injection
  PCM communications
  Satellite communications
  Radar ranging systems
- *High-frequency up-converters*

Table of Absolute-Maximum Ratings

Term. No.	Min. Volts	Max. Volts	Max. I_{IN} (mA)	Max. I_{OUT} (mA)
1 & 2*	0	5.5	110	0
3	−0.3	20	1	1
4 & 5	—	—	0.1	10
9, 10, 13, 14▲	—	4	0.1	1

*Terms. 1 & 2 tied together.
▲Maximum rf drive = 500 mVRMS.
Terms. 7 & 8 are system ground and tied together.
Terms. 6, 11, 12 = no connection.

File Number **1176**

CA3179

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 5.5 V
DC BANDSWITCH VOLTAGE ..... 20 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
  UP TO T_A = 70 °C ..... 700 mW
  ABOVE T_A = 70 °C ..... derate linearly at 11.1 mW/ °C
AMBIENT TEMPERATURE RANGE:
  OPERATING ..... 0 to 85 °C
  STORAGE ..... −55 to +150 °C
LEAD TEMPERATURE (DURING SOLDERING):
  AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
  FROM CASE FOR 10 SECONDS MAX. ..... +265 °C

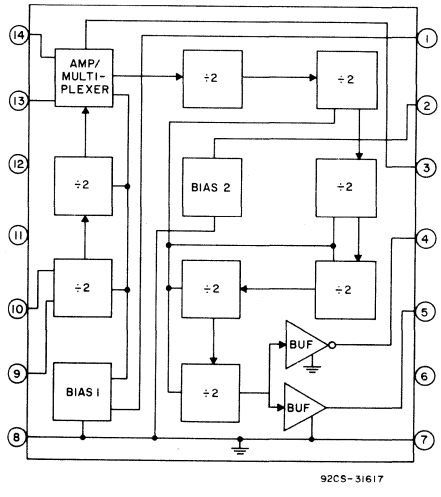


Fig. 1 - CA3179 block diagram.

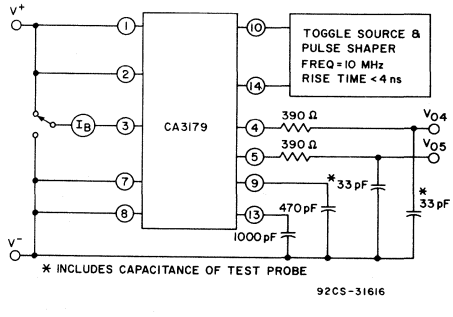


Fig. 2 - DC characteristics test circuit.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 5 V, V− = 0 V

CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	Typ.	Max.	UNITS
Static (See Fig. 2)					
Supply Current, I+	Terms. 1 & 2	30	65	100	mA
Bandswitch Voltage: Low, V_{BL}	Term. 3	2.4	—	—	V
Bandswitch Voltage: High, V_{BH}	Term. 3	—	—	0.8	V
Bandswitch Current: Low, I_{BL}	V3 = 0 V	−1	—	—	mA
Bandswitch Current: High, I_{BH}	V3 = 20 V	—	—	0.5	mA
Dynamic (See Fig. 3)					
Sine Wave Sensitivity (Single-ended)	f_{IN} = 450 to 950 MHz, V3 = 5 V	0	30	80	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 80 to 450 MHz, V3 = 5 V	—	50	160	mVRMS
Sine Wave Sensitivity (Single-ended)	f_{IN} = 90 to 275 MHz, V3 = 0 V	—	5	40	mVRMS
Output Voltage: High, V_{OH}	Term. 4 or 5	—	4.2	—	V
Output Voltage: Low, V_{OL}	Term. 4 or 5	—	3	—	V
Output Voltage: Peak-to-Peak, V_{Op-p}	Term. 4 or 5	0.65	1.1	1.6	V
Output Rise or Fall Time, t_r,t_f		40	70	110	ns
Internal Bias	Term. 13 or 14	$(V_{DD} - 1)$			V
Internal Bias	Term. 9 or 10	$(V_{DD} - 2.7)$			V
DC Input Resistance, R_I	Term. 13 to 14	2000			Ω
DC Input Resistance, R_I	Term. 9 to 10	1000			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 950 MHz	20			Ω
Complex Input Impedance	Term.9 to 10, V_{IN} = 100 mV, f_{IN} = 450 MHz	30 - j80			Ω
Complex Input Impedance	Term.13 to 14, V_{IN} = 100mV, f_{IN} = 275 MHz	35 - j100			Ω

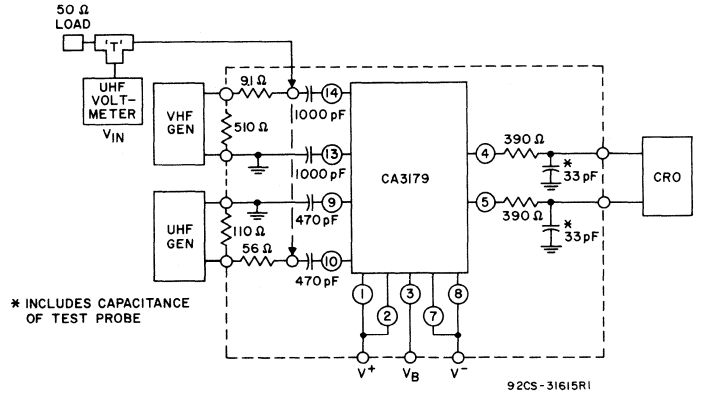


Fig. 3 - AC characteristics test circuit.

CA3179

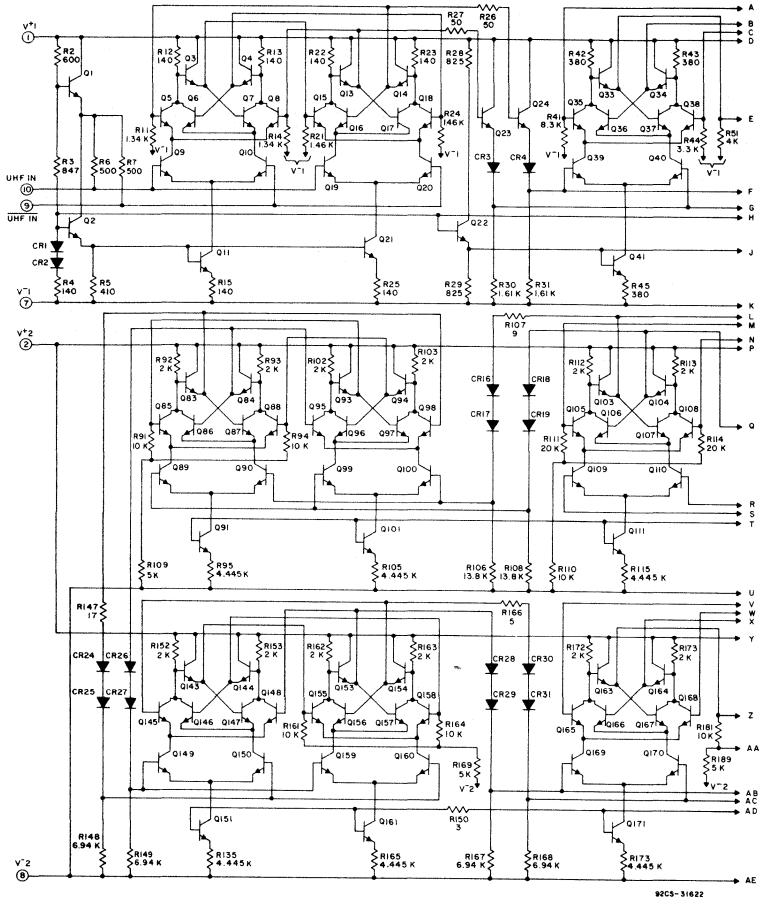


Fig. 4 – Schematic diagram (cont'd on next page).

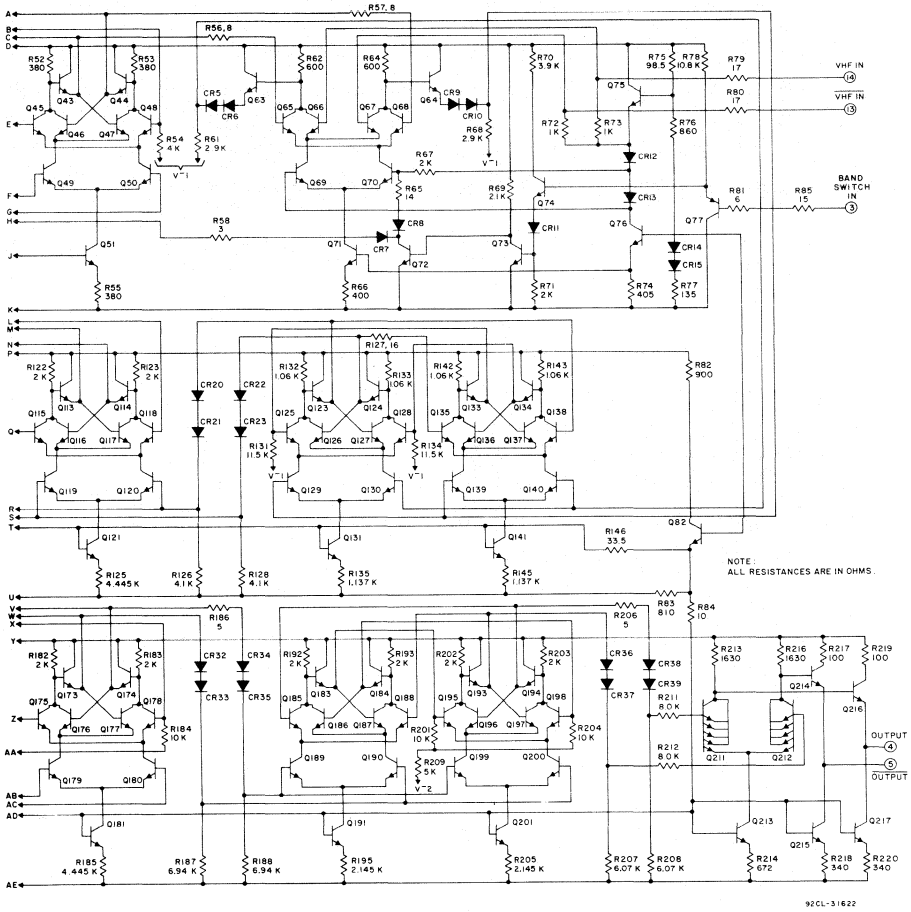


Fig. 4 - Schematic diagram (cont'd from previous page).

CA3179

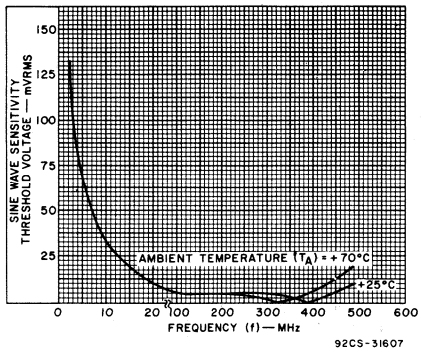


Fig. 5 - Typical threshold sensitivity in the ÷64 VHF mode.

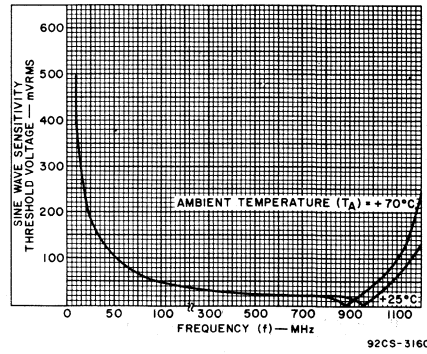


Fig. 6 - Typical threshold sensitivity in the ÷256 UHF mode.

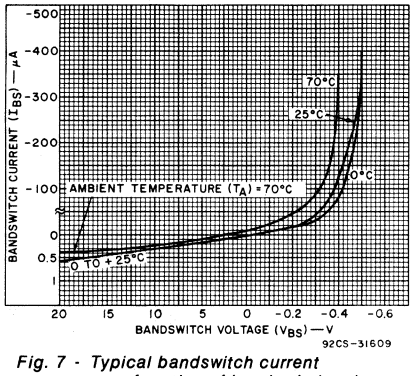


Fig. 7 - Typical bandswitch current as a function of bandswitch voltage and ambient temperature.

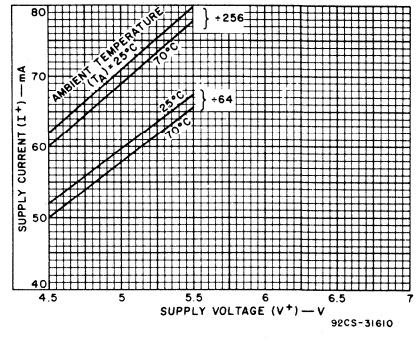


Fig. 8 - Supply current as a function of supply voltage and ambient temperature.

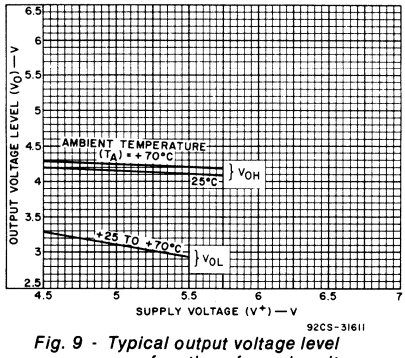


Fig. 9 - Typical output voltage level as a function of supply voltage and ambient temperature.

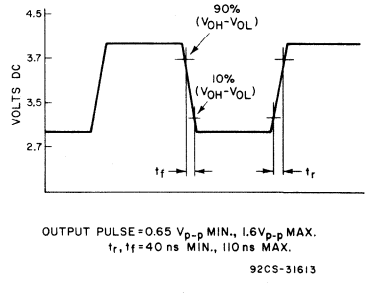


Fig. 10 - Output pulse characteristics.

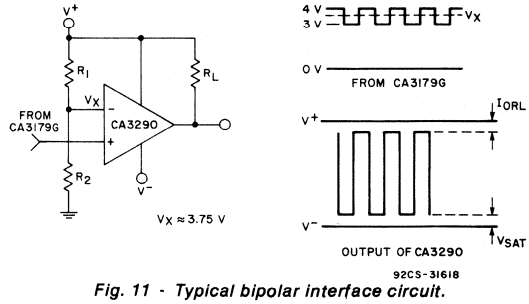


Fig. 11 - Typical bipolar interface circuit.

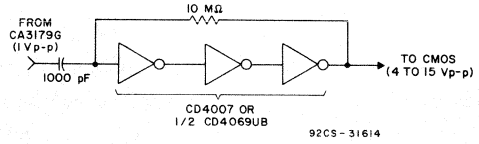
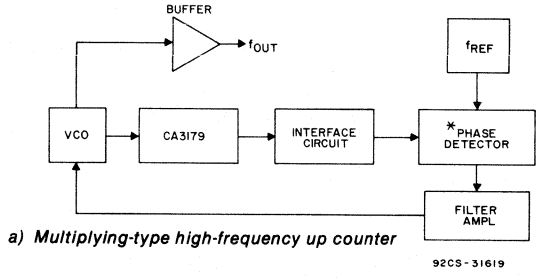
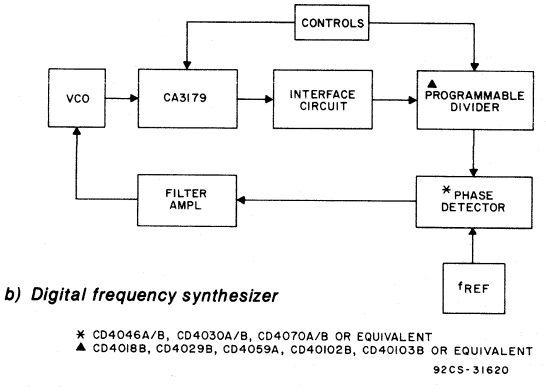


Fig. 12 - Typical CMOS interface circuit.



a) Multiplying-type high-frequency up counter



b) Digital frequency synthesizer

Fig. 13 - Typical system configuration.

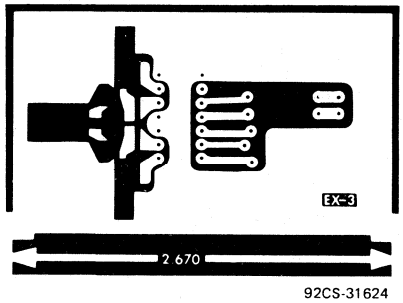


Fig. 14 - Printed-circuit board for the dynamic test circuit.

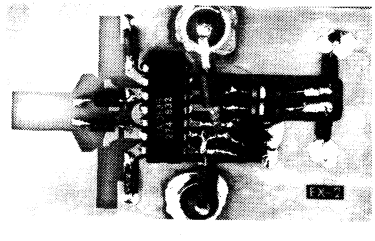
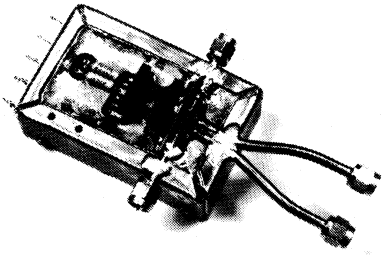


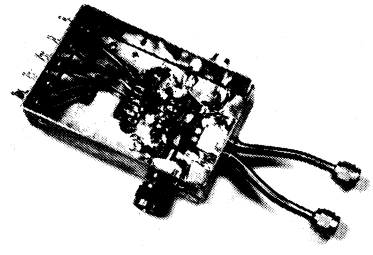
Fig. 15 - Printed-circuit board for the dynamic test circuit with components.

CA3179



TOP VIEW

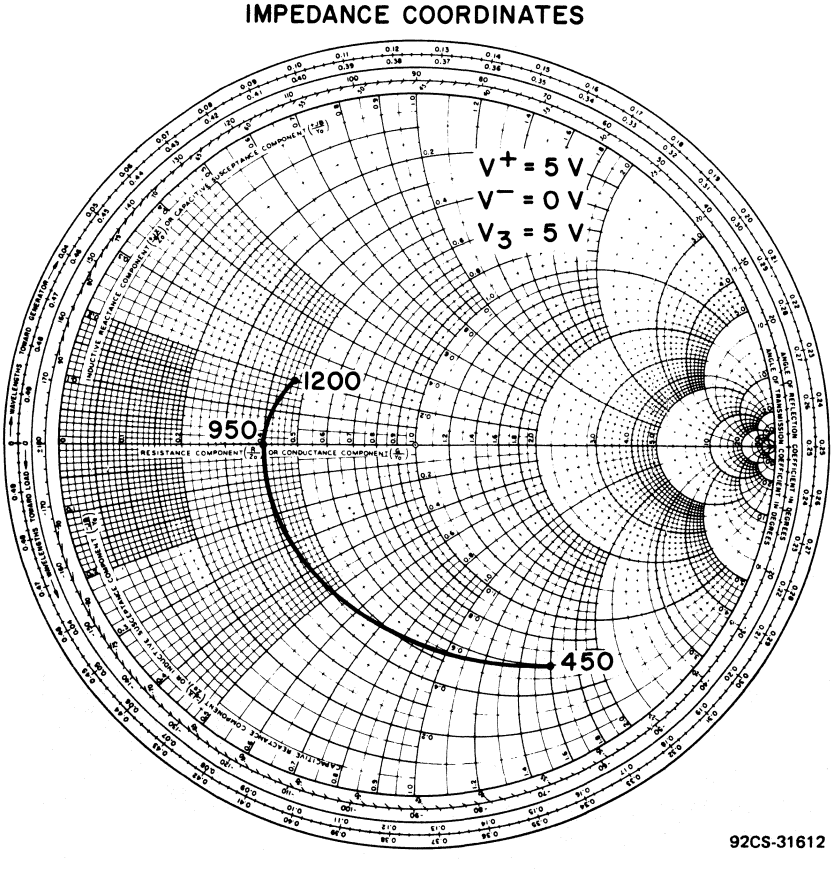
92CS-31652



BOTTOM VIEW

92CS-31653

Fig. 16 - Dynamic test circuit fixture.



92CS-31612

Fig. 17 - Impedance as a function of frequency.

High-frequency construction and design techniques must be followed if the operation of the CA3179G test circuit is to be stable and if the results of repeated tests are to be consistent. The dynamic test circuit is shown in Fig. 3, and a photo of the test fixture that houses it is shown in Fig. 16. Listed below are some precautionary construction considerations for the circuit and test fixture.

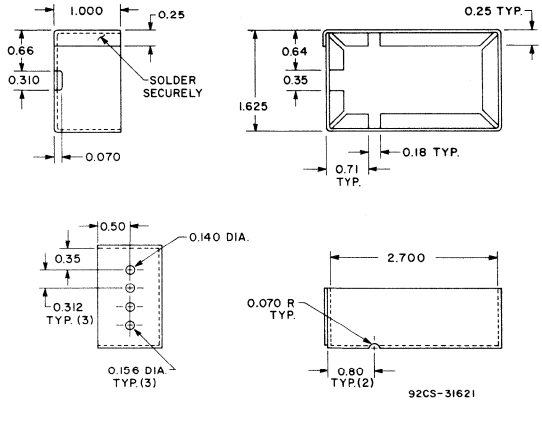
1. Supply the ground plane with frequent ground connections.
2. Use 50-Ω coaxial cable for input connections
3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances
4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces
5. Use leadless ceramic disc capacitors wherever possible
5. Provide capacitor by-passing near active terminals where ac grounds are required

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the p.c. board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

Partial Parts List for the Dynamic Test Circuit and Fixture:

4 Pasternac PE3493-6 SMA cable connectors and semi-rigid coaxial cable
1 Chassis
1 P.C. board
1 14-lead socket
2 1000-pF capacitors, Stettner Trush Inc. No. TEFIC-7
3 470-pF disc capacitors
3 1000-pF disc capacitors
2 33-pF feedthrough capacitors
3 1000-pF feedthrough capacitors
3 Ferrite beads, 0.375 x 0.187 x 0.250
2 Resistors, 390-Ω, ¼-W, 2%
1 Resistor, 56-Ω, 1/8-W, 5%
1 Resistor, 110-Ω, 1/8-W, 5%
1 Resistor, 9.1-Ω, 1/8-W, 5%
1 Resistor, 510-Ω, 1/8-W, 5%

Dimensions of Test Fixture



CA3189

FM IF System

Includes IF Amplifier, Quadrature Detector, AF Preamplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector

For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers

Features:

- *Exceptional limiting sensitivity: 12μV typ. at −3 dB point*
- *Low distortion: 0.1% typ. (with double-tuned coil)*
- *Single-coil tuning capability*
- *Improved S + N/N Ratio*
- *Externally programmable recovered audio level*
- *Provides specific signal for control of interchannel muting (squelch)*
- *Provides specific signal for direct drive of a tuning meter*
- *On channel step for search control*
- *Provides programmable AGC voltage for RF amplifier*
- *Provides a specific circuit for flexible audio output*
- *Internal supply-voltage regulators*
- *Externally programmable "on" channel step width, and deviation at which muting occurs*

The RCA-CA3189E* is a monolithic intergrated circuit that provides all the functions of a comprehensive FM-IF system. Fig. 1 shows a block diagram of the CA3189E, which includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table I.

The CA3189E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40° C to +85° C.

*Formerly Developmental Type No. TA10038.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (between Terms. 11 and 4)	16 V
(between Terms. 11 and 14)	16 V
DC CURRENT (Out of Term. 15)	2 mA
DEVICE DISSIPATION:	
Up to T_A = 85° C	640 mW
Above T_A = 85° C	derate linearly at 9.9 mW/° C
AMBIENT TEMPERATURE RANGE:	
Operating	−40 to +85° C
Storage	−65 to +150° C
LEAD TEMPERATURE (During soldering):	
At distance not less than 1/32 inch (0.79 mm) from case for 10s max.	+265° C

File Number **1046**

ELECTRICAL CHARACTERISTICS, at T_A = 25°C, V^+ = 12 Volts

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		Circuit or Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Static (DC) Characteristics								
Quiescent Circuit Current	I_{11}	No signal input, Non muted		3,4	20	31	40	mA
DC Voltages: Terminal 1 (IF Input)	V_1				1.2	1.9	2.4	V
Terminal 2 (AC Return to Input)	V_2				1.2	1.9	2.4	V
Terminal 3 (DC Bias to Input)	V_3				1.2	1.9	2.4	V
Terminal 15 (RF AGC)	V_{15}				7.5	9.5	11	V
Terminal 10 (DC Reference)	V_{10}				5	5.6	6	V
Dynamic Characteristics								
Input Limiting Voltage (−3 dB point)	V_I(lim)	V_{IN} = 0.1 V, AM Mod. = 30%	f_O = 10.7 MHz,	3,4	–	12	25	μV
AM Rejection (Term. 6)	AMR				45	55	–	dB
Recovered AF Voltage (Term. 6)	V_O(AF)				325	500	650	mV
Total Harmonic Distortion:* Single Tuned (Term. 6)	THD	V_{IN} = 0.1 V	$f_{mod.}$ = 400 Hz,	3	–	0.5	1	%
Double Tuned (Term. 6)	THD		Deviation ±75 kHz	4	–	0.1	–	%
Signal plus Noise to Noise Ratio (Term. 6)	S + N/N			3,4	65	72	–	dB
Deviation Mute Frequency	$f_{DEV.}$		$f_{mod.}$ = 0	3,6,7	–	±40	–	kHz
RF AGC Threshold	V_{16}			3,4	–	1.25	–	V
On Channel Step	V_{12}	V_{IN} = 0.1 V	$f_{DEV.}$ < ±40 kHz	3	–	0	–	V
			$f_{DEV.}$ > ±40 kHz		–	5.6	–	

*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

CA3189

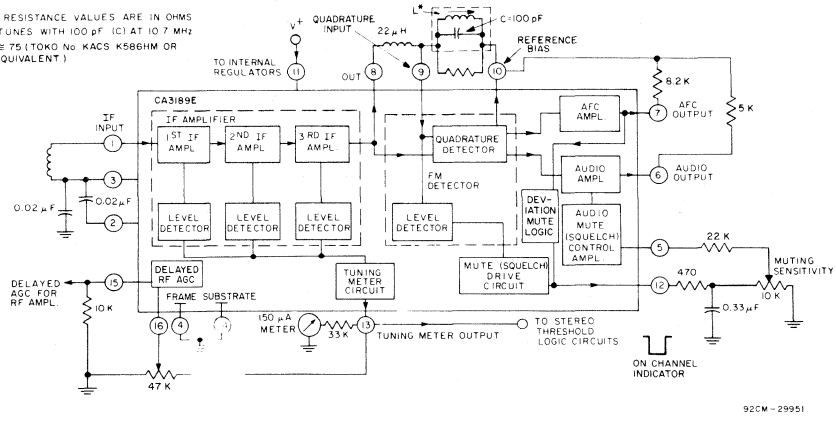


Fig. 1 – Block diagram of the CA3189E.

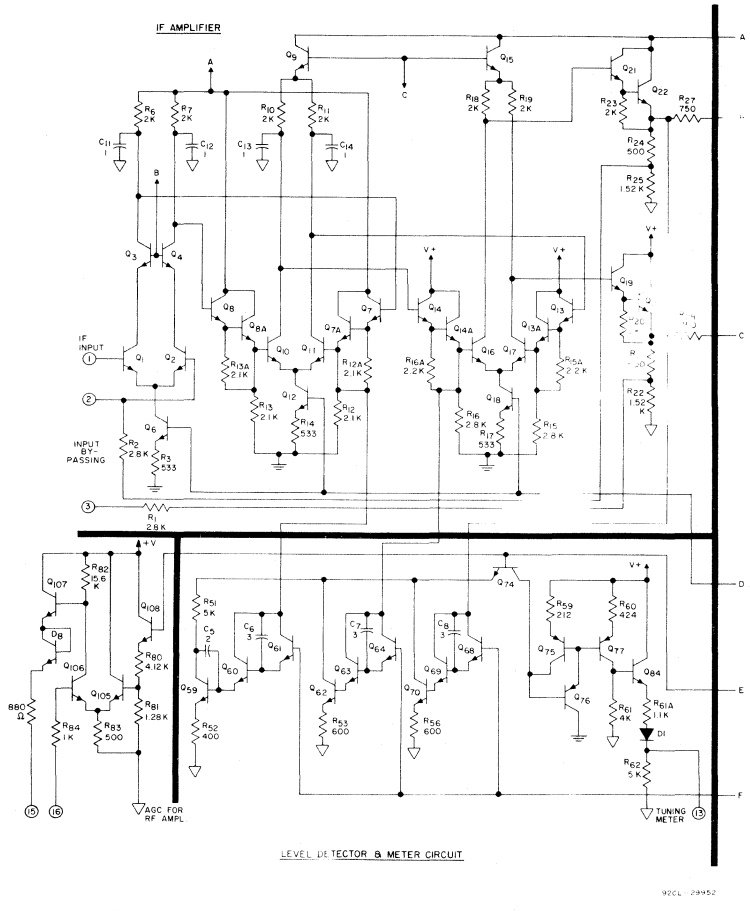


Fig. 2 - Schematic diagram of the CA3189E (cont'd on next page).

TABLE I – CA3189E Features Compared to CA3089E

FEATURES	CA3189E	CA3089E
Low Limiting Sensitivity (12 μV typ.)	Yes	Yes
Low Distortion	Yes	Yes
Single-coil Tuning Capability	Yes	Yes
Programmable Audio Level	Yes	No
S/N Mute	Yes	Yes
Deviation Mute	Yes	No
Flexible AFC	Yes	Yes
Programmable AGC Threshold and Voltage	Yes	No
Typical S + N/N > 70 dB	Yes	No
Meter Drive Voltage Depressed at Very-Low Signal Levels	Yes	No
On-Channel Step Control Voltage	Yes	No

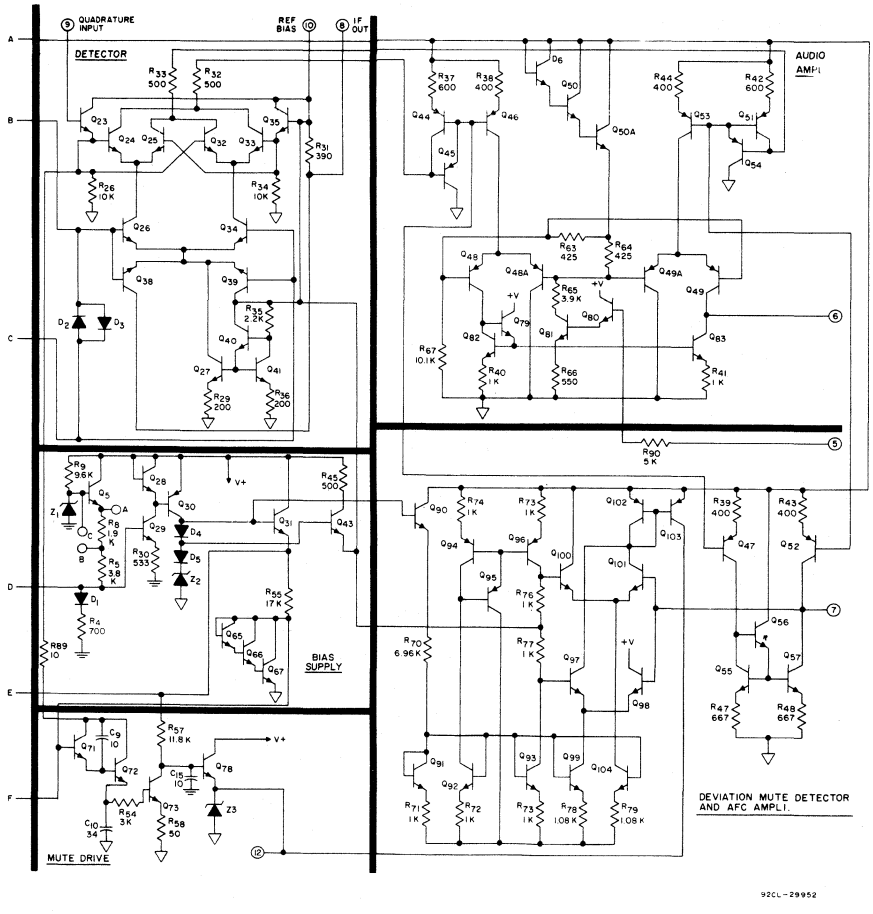
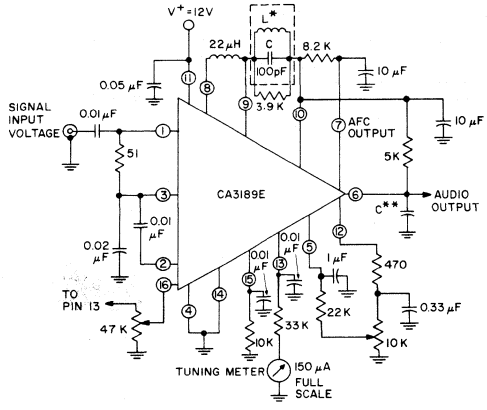


Fig. 2 - Schematic diagram of the CA3189E (cont'd from previous page).

CA3189



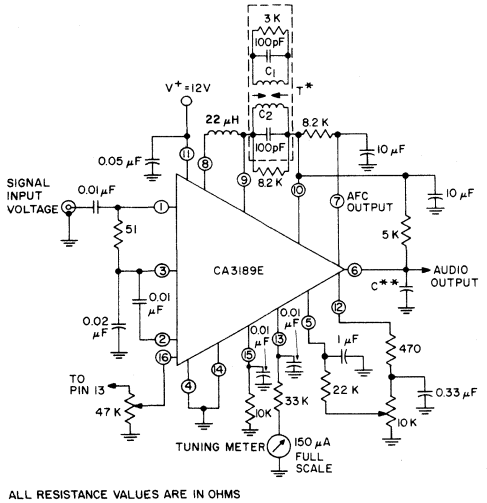
ALL RESISTANCE VALUES ARE IN OHMS

*L TUNES WITH 100 pF (C) AT 10.7 MHz
Q_O(UNLOADED) ≅ 75 (TOKO No. KACS K586HM OR EQUIVALENT)

**C = 0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
= 0.015 μF FOR 75 μs DEEMPHASIS (USA)

92CM-29953

Fig. 3 – Test circuit for CA3189E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS

*T: PRI. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA. FORM
SEC. – Q_O(UNLOADED) ≅ 75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA. FORM
kQ (PER CENT OF CRITICAL COUPLING) ≅ 70%
(ADJUSTED FOR COIL VOLTAGE V_C) = 150 mV

ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT "E" TYPE SLUGS, SPACING 4mm

**C = 0.01 μF FOR 50 μs DEEMPHASIS (EUROPE)
= 0.015 μF FOR 75 μs DEEMPHASIS (USA)

Fig. 4 – Test circuit for CA3189E using a double-tuned detector coil.

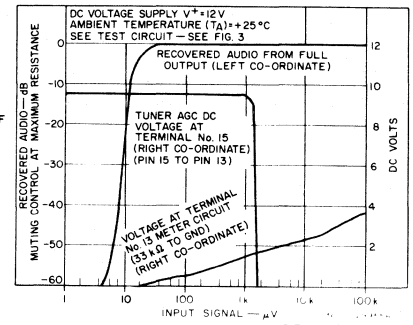


Fig. 5 – Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

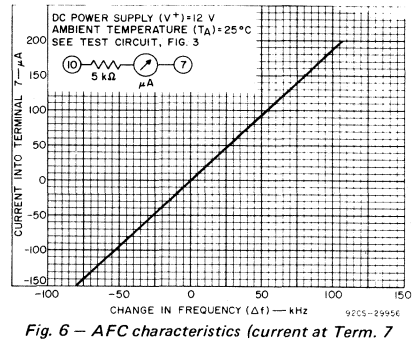


Fig. 6 – AFC characteristics (current at Term. 7 as a function of change in frequency).

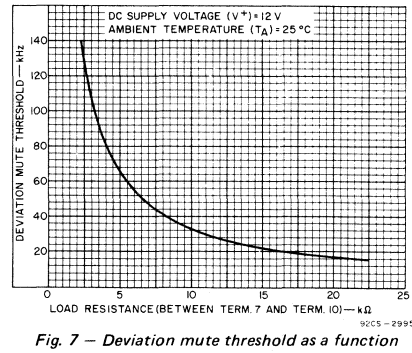


Fig. 7 – Deviation mute threshold as a function of load resistance (between Term. 7 and Term. 10).

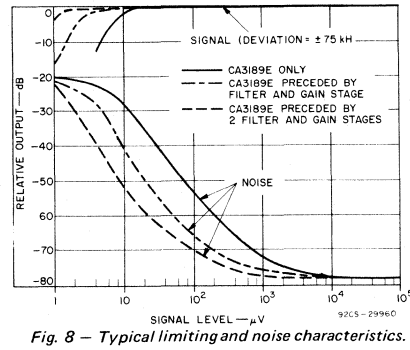


Fig. 8 – Typical limiting and noise characteristics.

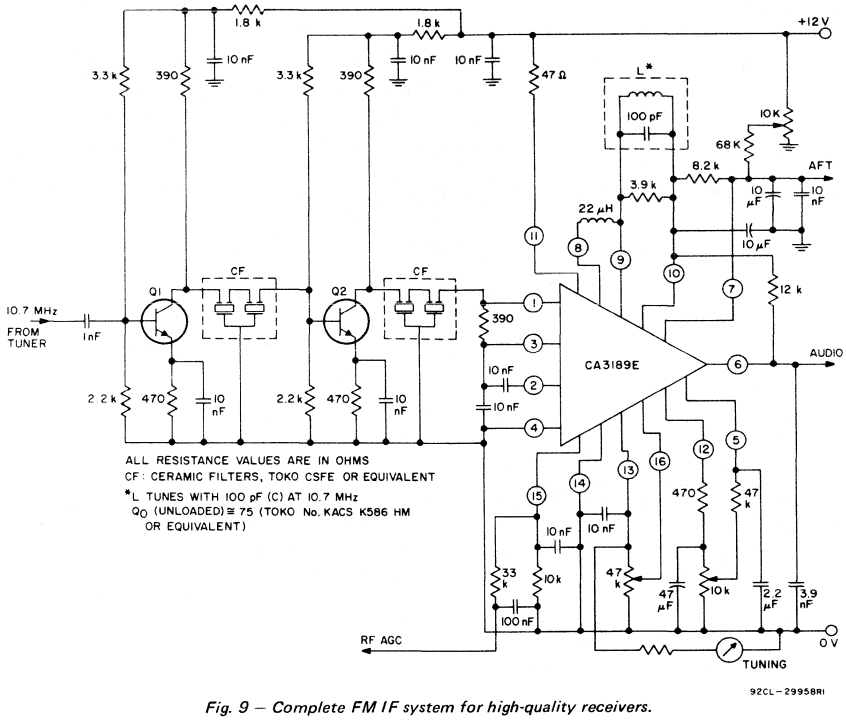


Fig. 9 – Complete FM IF system for high-quality receivers.

CA3195

RC Phase-Lock-Loop Stereo Decoder

For FM Multiplex Systems

Features:

- *Low distortion (THD): 0.4% (typ.)*
- *Excellent SCA rejection: 70 dB typ.*
- *RC oscillator*
- *High-audio-channel separation: 45 dB*
- *Power supply range: 10 to 16 V dc*
- *Requires only one adjustment for complete alignment*
- *Low-impedance output: 40 Ω (typ.) resistance*
- *Stereo indicator lamp drive: 150 mA typ.*

RCA-CA3195 is a monolithic silicon integrated circuit RC phase-lock loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA3195 is similar to the CA758. The CA3195 output resistance is much lower, making it capable of driving low impedance loads without buffering.

The CA3195 decodes the multiplexed stereo input signal into left and right channel audio output signals. The decoder also suppresses SCA (storecast) transmissions when present in the composite stereo signal.

The decoder uses a minimum of external components, a requires one adjustment (oscillator frequency) for co plete alignment. In addition, the CA3195 provides aut matic mono-stereo mode switching and energizes a ste indicator lamp.

The CA3195 is supplied in a 16-lead dual-in-line plas package and operates over an ambient temperature ran of −40 to +85° C.

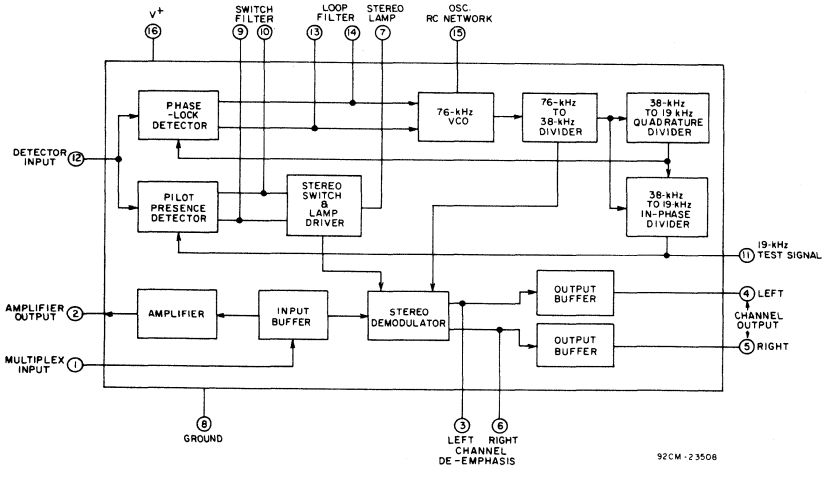


Fig. 1 — Functional block diagram of the CA3195.

File Number **126**

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC Supply Voltage ..... +18 V
DC Supply Voltage (for ≤ a 15-second period) ..... +22 V
DC Voltage at Term. 7 (Lamp Driver Circuit with Lamp "OFF" ..... +22 V
Device Dissipation:
Up to T_A = 70°C ..... 730 mW
Above T_A = 70°C derate linearly ..... 9.1 mW/°C
Ambient Temperature Range:
Operating ..... −40 to +85°C
Storage ..... −65 to +150°C
Lead Temperature (During soldering):
At a distance not less than 1/32" (0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig.3 unless otherwise specified) $V+ = 12$ V, $T_A = 25$°C Multiplex Input Signal (L = R, pilot "OFF") = 300 mV RMS 19-kHz Pilot Level = 30 mV RMS f (modulation) = 400 Hz or 1kHz	LIMTS Min.	Typ.	Max.	UNITS
Static Characteristics					
Total Current	Lamp "OFF"	—	26	35	mA
Maximum Available Lamp Current		75	150	—	mA
DC Voltage at Term. 7 (Lamp Driver)	1 (Lamp) = 50 mA	—	1.3	1.8	V
DC Voltage Shift at either Term.4 or 5 (Output)	Stereo-to-Mono Operation	—	30	150	mV
Dynamic Characteristics					
Power Supply Ripple Rejection	For a 200-Hz, 200-mV RMS Signal	35	45	—	dB
Input Resistance		20	35	—	kΩ
Output Resistance		—	40	150	Ω
Channel Separation (Stereo)	At f = 100 Hz	—	40	—	dB
	f = 400 Hz	30	45	—	dB
	f = 10 kHz	—	45	—	dB
Channel Balance (Monaural)		—	0.3	1.5	dB
Voltage Gain	At f = 1 kHz	0.5	0.9	1.4	V/V
Pilot Input Level: 19-kHz Input	Lamp "ON"	—	15	23	mV RMS
19-kHz Input	Lamp "OFF"	2.0	7.0	—	mV RMS
Hysteresis	Lamp "OFF"	3.0	7.0	—	dB
Capture Range (Deviation from 76-kHz Center Frequency)		±2.0	±4.0	±6.0	%
Total Harmonic Distortion	Multiplex Input Signal = 600 mV RMS (Pilot "OFF")	—	0.4	1.0	%
19-kHz Rejection		25	35	—	dB
38-kHz Rejection		25	45	—	dB
SCA (Storecast) Rejection	Measured Composite Signal: 80% Stereo, 10% Pilot, 10% SCA	—	70	—	dB
Voltage-Controlled Oscillator (VCO) Tuning Resistance	Total Resistance (Term. 15 to 8) required to set f_{REF} = 19 kHz ±10 Hz (Term. 11)	21.0	23.3	25.5	kΩ
Voltage-Controlled Oscillator Frequency Drift	0° ≤ T_A ≤ 25°C	—	+0.1	±2	%
	25° ≤ T_A ≤ 70°C	—	−0.4	±2	%

CA3195

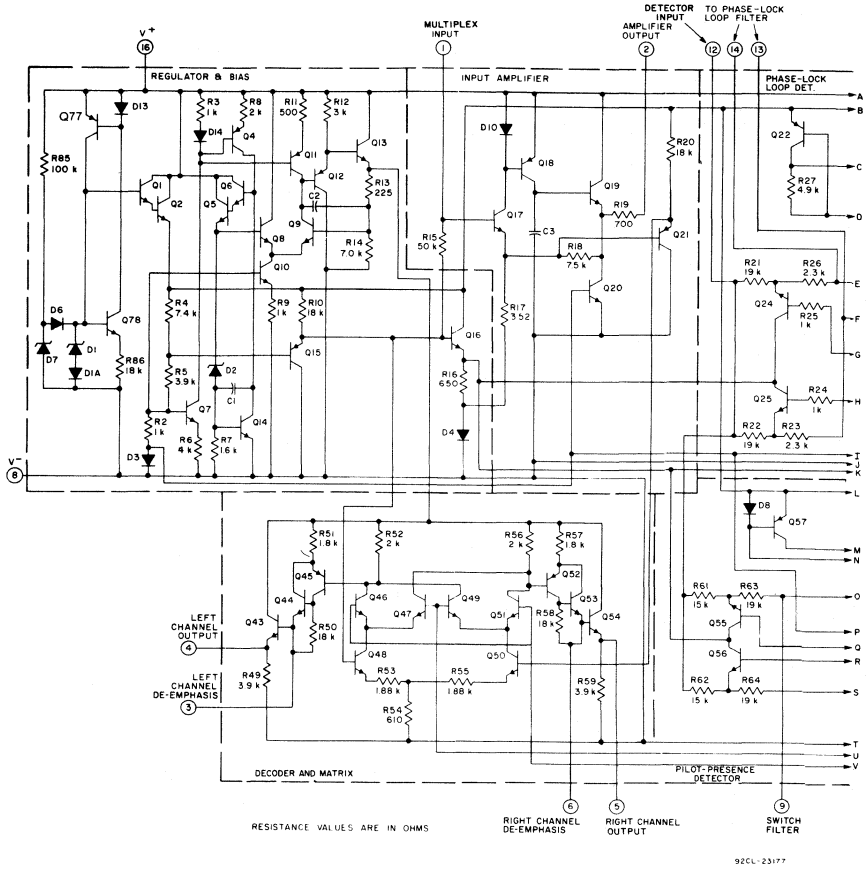


Fig. 2—Schematic diagram of the CA3195 (cont'd on next page).

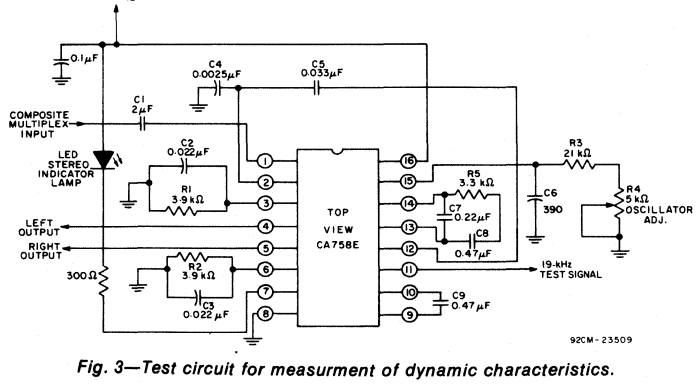


Fig. 3—Test circuit for measurment of dynamic characteristics.

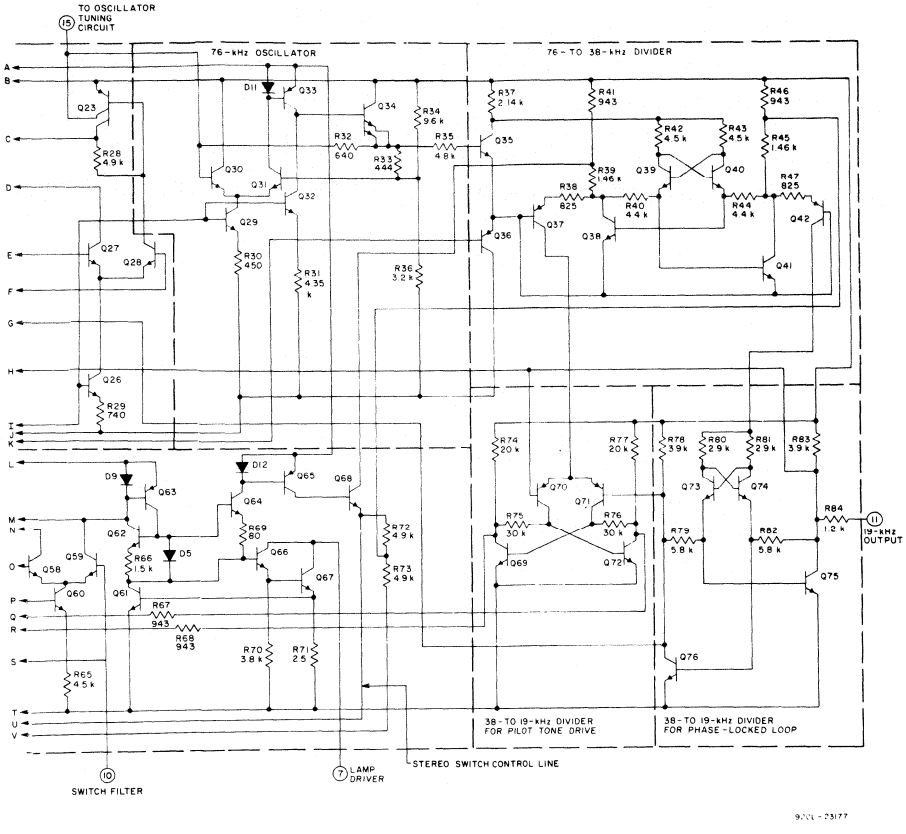


Fig. 2—Schematic diagram of the CA3195 (cont'd from preceded page).

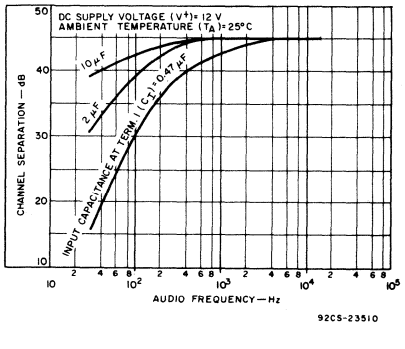


Fig. 4—Channel separation vs. audio frequency.

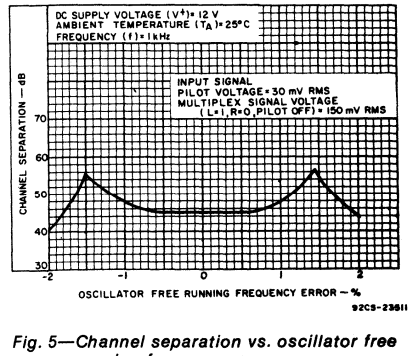


Fig. 5—Channel separation vs. oscillator free running frequency error.

CA3195

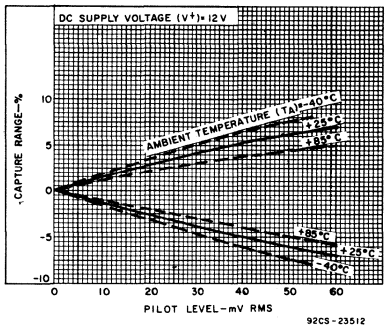


Fig. 6—Capture range vs. pilot level.

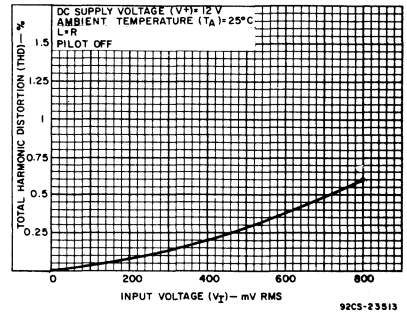


Fig. 7—Total harmonic distoration vs. input level.

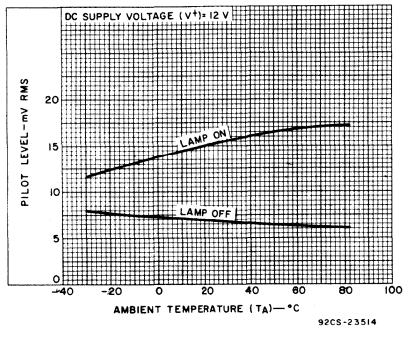


Fig. 8—Lamp turn-on and turn-off sensitivity vs. ambient temperature.

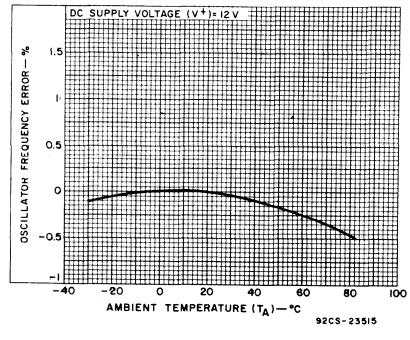


Fig. 9—Oscillator free running frequency error vs. ambient temperature.

CA3199

VHF/UHF ÷ 4 Prescaler

Features:

- *Broadband operation - DC to 1.3 GHz*
- *High sensitivity*
- *Standard T^2L or ECL power supply of 5 V ± 0.5 V*
- *Complementary ECL outputs*
- *High-frequency up-converters*

- *High-frequency divider for:*
  UHF frequency counters
  UHF timers
  High-speed computers
  Frequency standards
  SHF second IF local-oscillator injection
  PCM communications
  Satellite communications
  Radar ranging systems

The CA3199E* is a bipolar integrated fixed-ratio (divide-by-four) counter which operates over the VHF/UHF frequency band (DC to 1.3 GHz). It accepts either single or double-ended ac-coupled input signals and provides complementary emitter follower outputs at standard ECL logic levels.

The CA3199E is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operates over an ambient temperature range of 0 to +85° C.

*Formerly RCA Dev. Type No. TA10853.

Applications:

- *Digital frequency synthesizers for:*
  VHF/UHF receivers
  Satellite communications
  Instrumentation

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE	5.5 V
RMS INPUT VOLTAGE	0.5 V
DEVICE DISSIPATION:	
UP TO T_A = 70° C	630 mW
ABOVE T_A = 70° C	derate linearly at 7.7 mW/° C
AMBIENT TEMPERATURE RANGE:	
OPERATING	0 to 85° C
STORAGE	−55 to −150° C
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 mm) FROM CASE FOR 10 SECONDS MAX.	−265° C

File Number **1302**

CA3199

STATIC CHARACTERISTICS (T_A=25° C, V_{CC}=+5.0 V, V_5=Ground)

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
"1" Output Voltage, V_{OH}	Outputs Unloaded	—	4.2	—	V
"0" Output Voltage, V_{OL}	Outputs Unloaded	—	3.4	—	V
Internal Bias Voltage, V_{BIAS}	Pin #4 Left Floating	—	2.4	—	V
Power Supply Current Drain, I_D		35	60	85	mA

DYNAMIC CHARACTERISTICS (T_A=25° C, V_{CC}=+5.0 V, V_5=Ground)

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Frequency Range (sinusoidal), V_{IN}	Single-Ended Input, 1000 MHz	—	—	400	mVpp
Output Voltage Swing, V_6, V_7		0.6	0.8	—	Vpp
"1" Transition Time, t_{-+}	Output Unloaded	—	0.6	—	ns
"0" Transition Time, t_{+-}	Output Unloaded	—	0.6	—	ns
Input Capacitance, C_{IN}		—	2.5	—	pF
Input Resistance, R_{IN}		—	400	—	Ω

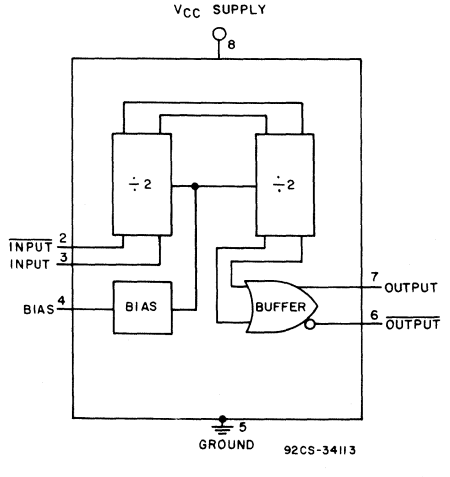
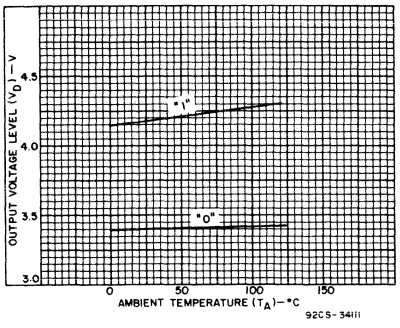


Fig. 1 - Logic diagram for divide-by-four counter.



. 2 – Typical output levels as a function of ambient temperature.

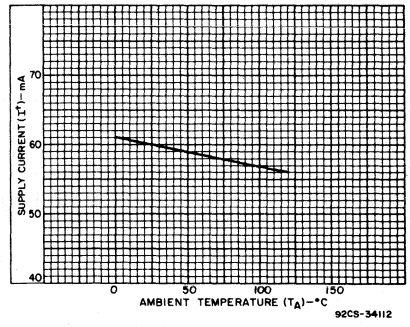


Fig. 3 – Typical power-supply current as a function of ambient temperature.

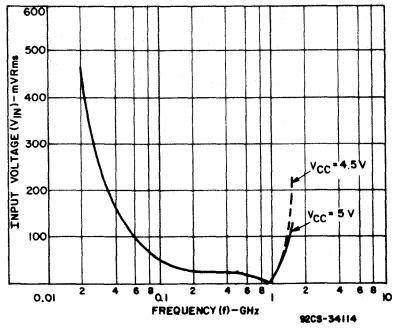


Fig. 4 – Sinusoidal input sensitivity.

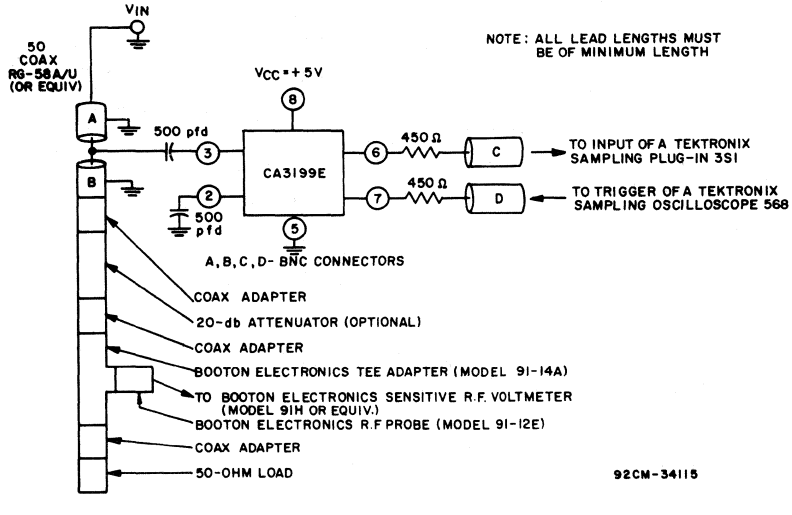


Fig. 5 – Test circuit for CA3199E.

CA3199

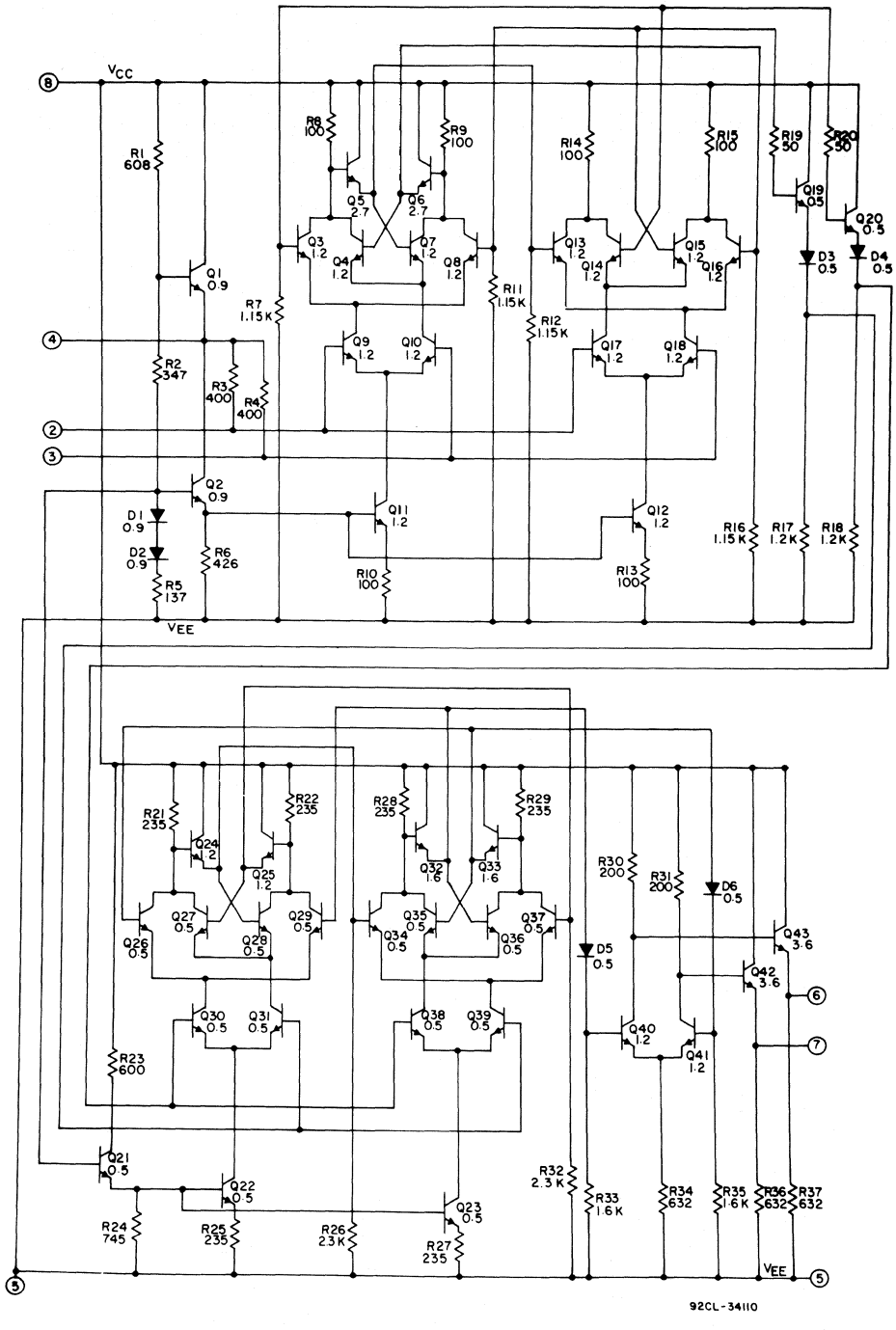


Fig. 6 - Schematic diagram for CA3199E.

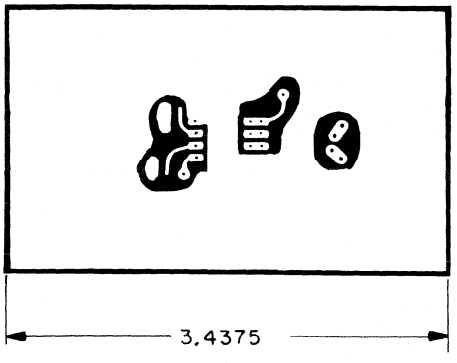


Fig. 7 - Printed-circuit board for the test circuit.

Application and Test Notes

1. Both complementary inputs and outputs are provided. When driven single-ended, normally at pin 3, the unused input (pin 2) should be ac by-passed (500 pF) to ground for best performance.
2. Internal bias monitor, pin 4, is normally left floating or ac by-passed to ground.
3. Device inputs should be ac coupled to the signal source. 500-pF coupling capacitors are adequate above 50 MHz.
4. Input signal voltage (sinusoidal) required is 100 mV RMS (typical) over the frequency range of 100-1000 MHz
5. When the input signal voltage is a square wave, a rise time of $\leq$5 ns is required. The signal should be 400-800 mV peak-to-peak over the frequency range from dc-1000 MHz. This corresponds to an input slew rate minimum of 62.5 V/μs.
6. All test data are for the 8-pin dual-in-line packaged circuit as mounted in a standard IC socket. Somewhat improved higher frequency performance can be obtained by attaching directly to a suitable PC board.
7. High-frequency construction and design techniques must be followed if the operation of the test circuit is to be stable and if the results of repeated tests are to be consistent. Listed below are some precautionary construction considerations for the circuit and test fixture.
    1. Supply the ground plane with frequent ground connections.
    2. Use 50-Ω coaxial cable for input connections.
    3. Use a "dead bug" type socket to minimize lead lengths and reduce series inductances.
    4. Use input pads that reduce impedance mismatch at the generator-test and meter-test input interfaces.
    5. Use leadless ceramic disc capacitors wherever possible.
    6. Provide capacitor by-passing near active terminals where ac grounds are required.

Specific applications may require changes in the procedures listed above. The socket, for instance, can be eliminated by soldering the device directly to the PC board or by using individual board-mounted socket pins. Input and output interface connections and circuitry will also vary according to specific circuit requirements.

CA3209

FM-IF System

For Search and Scan

Features:

- *Exceptional limiting sensitivity: 12 μV typ. at -3 dB point*
- *Exceptional temperature stability of tuning and stop-pulse window*
- *Single-coil tuning capability*
- *Externally programmable stop-pulse window width*
- *Programmable level for AGC action*
- *Forward AGC for pin-diode or bipolar rf amplifier*
- *Required input level to generate a stop-pulse is programmable*

The RCA CA3209E•is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. It is intended for use in FM—IF amplifier applications in high-fidelity, automotive, and communications receivers where the synthesizer counter can be controlled by a stop-pulse for scan and search operation.

•Formerly Developmental Type No. TA10493B

Fig. 1 shows the CA3209E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier.

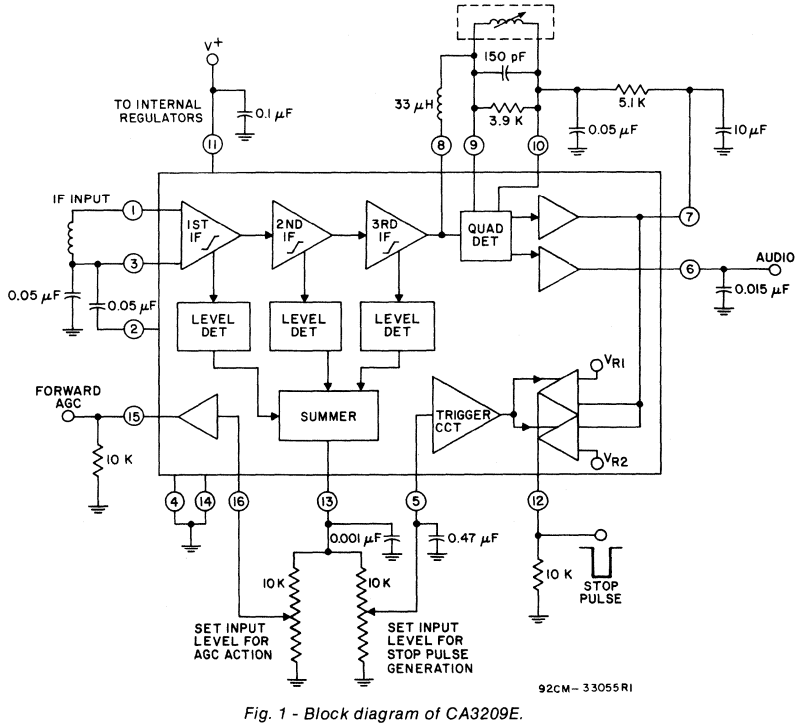


Fig. 1 - Block diagram of CA3209E.

File Number **134**

CA3209

ıe advanced circuit design of the if system includes ɜsirable deluxe features such as delayed AGC for the rf ıner, and an output signal to drive a tuning meter and/or ʳovide stereo switching logic control of stop pulse and GC thyristors. In addition, internal power supply regulators ıaintain a nearly constant current drain over the voltage ɹpply range of +8.5 to +16 volts.

The CA3209E is ideal for high-fidelity operation. Distortion in a CA3209E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3209E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40° C to +85° C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Between terminals 11 and 4 ..... 16 V
- Between terminals 11 and 14 ..... 16 V

DC CURRENT (Out of Terminal 15) ..... 2 mA

DEVICE DISSIPATION:
- Up to T_A = 85° C ..... 735 mW
- Above T_A = 85° C ..... Derate linearly 11.4 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -40 to +85° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At distance not less than 1/32" (0.79 mm) from case for 10 seconds max. ..... +265° C

:LECTRICAL CHARACTERISTICS at T_A = 25° C, V+ = 12 Volts
See Fig. 3 for Test Circuit)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Static (DC) Characteristics					
Quiescent Circuit Current		20	31	44	mA
DC Voltages:					
V_1, V_2, V_3		1.2	1.9	2.4	V
V_{10}		4.9	5.6	6.1	V
V_{15}	V_{16} = 0 V	—	0.005	0.4	V
V_{15}	V_{16} = 1.4 V	4.1	5.1	5.6	V
V_{16}	V_{15} = 1-2 V	—	1.22	—	V
V_{12}	$V_5 \leqq$ 0.24 V	4.3	5.7	6.6	V
V_{12}	$V_5 \geqq$ 0.53 V	—	0.06	0.4	V
V_5 to cause transition of trigger (V_{12}) high to low		—	0.45	—	V
V_5 to cause transition of trigger (V_{12}) low to high		—	0.40	—	V
Dynamic Characteristics					
Input Limiting Voltage (-3 dB point)		—	12	25	μV
Recovered Audio Voltage	400 Hz Input $\geqq$ 1 mV ±75 kHz Deviation	350	520	700	mV
Frequency Window of Stop Pulse	V_5 = 0.6 V Input = 100 μV				
	R_7 -10 = 5.1 K	70	120	200	kHz
	R_7 -10 = 8.2 K	45	75	125	
Total Harmonic Distortion, THD: *			0.50	1.0	%
AM Rejection	30% AM 100 mV Input	50	65	—	dB
	100 μV Input	35	42	—	
S/N Ratio **	100 mV Input	70	80	—	dB
	100 μV Input	55	65	—	
V_{13}	No Signal	0	0.2	0.8	V
	100 μV Input	1.4	2.2	3.2	
	100 mV Input	4.9	6.5	8.5	

* THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

** Measured with a 30-kHz low-pass filter (-3 dB at 30 kHz, 18 dB/octave).

CA3209

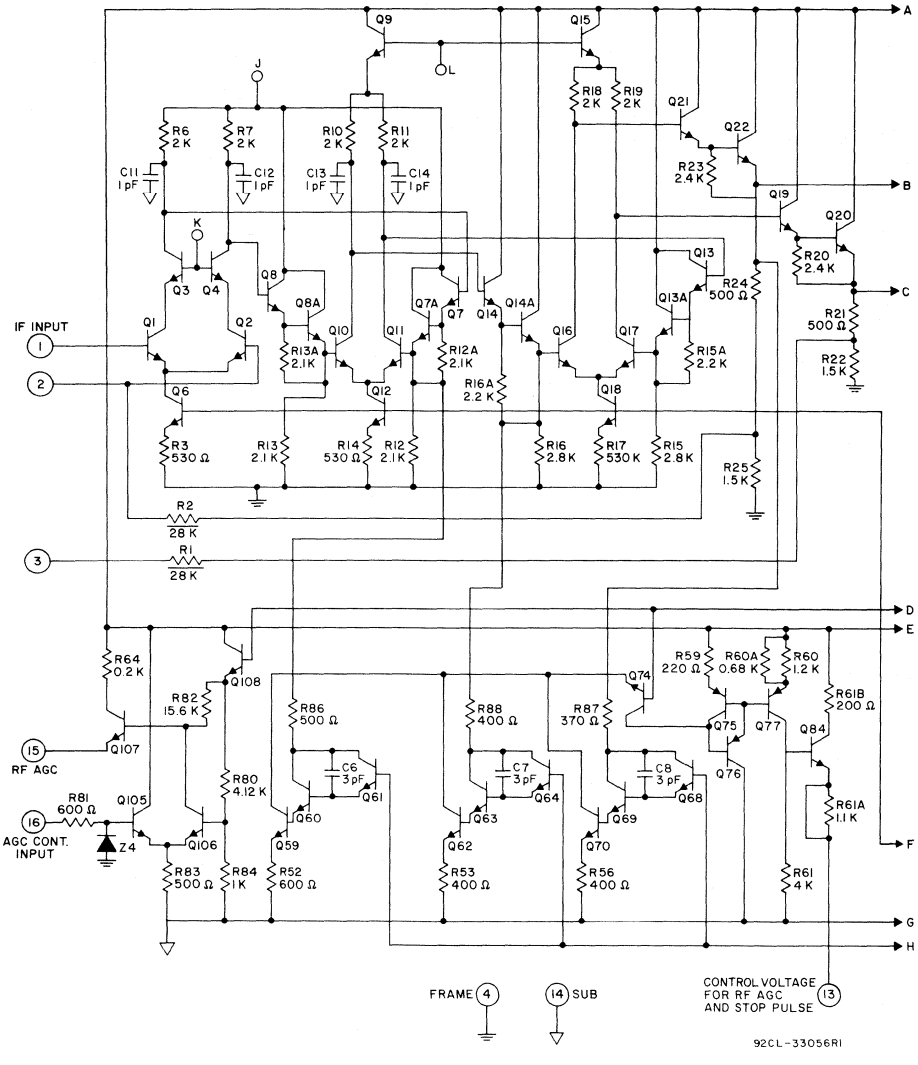


Fig. 2 - Schematic diagram of CA3209E
(continued on next page).

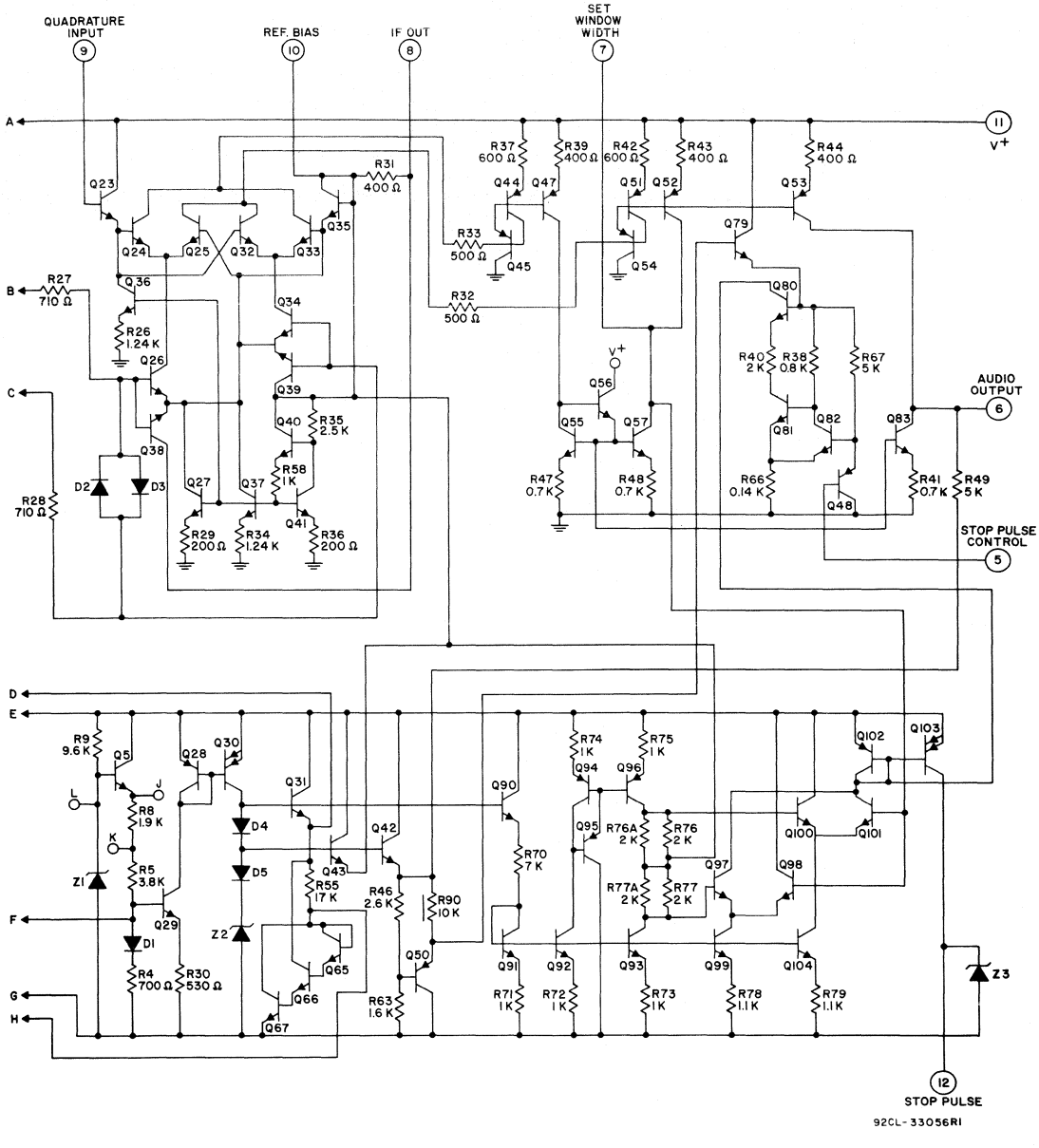


Fig. 2 - Schematic diagram of CA3209E (continued from previous page).

CA3209

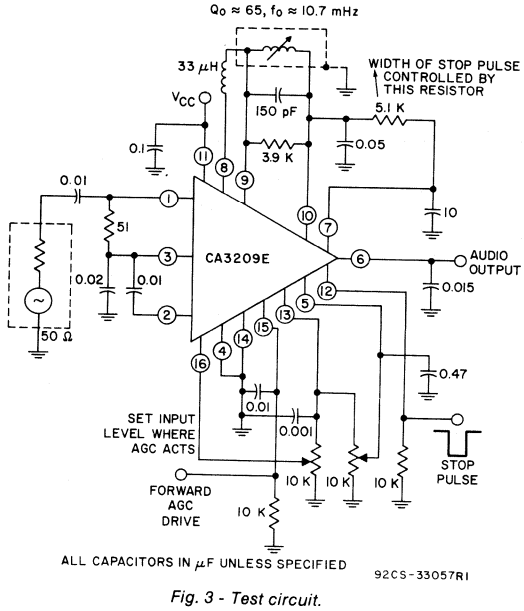


Fig. 3 - Test circuit.

CA3215

M-IF Amplifier/Detector Limiter

atures:

Ideal for video disc playback systems
Phase lock loop FM detector
Linear detection for large deviation at video modulating frequencies
Carrier defect detector
Squelch circuitry
Loss of carrier latch circuitry

ıe RCA CA3215E• monolithic integrated circuit provides system for large-deviation FM detection. The device cludes a two-stage limiter/amplifier, phase detector, ıltage controlled oscillator, wide-band amplifier, carrier ɜfect detector, and output squelch. The phase detector ıd VCO are connected to form a phase-lock-loop detector ıpable of recovering wide deviation modulating signals.

The carrier defect detector provides a logic output signal to control corrective circuitry in the event of an instantaneous loss or serve distortion of the carrier signal. The wide-band amplifier is squelched by the same defect detector output or may be squelched by an external input to the device. In the event of longer duration carrier loss, a latch condition will maintain the amplifier in the squelched condition.

ormerly RCA Dev. Type No. TA10641.

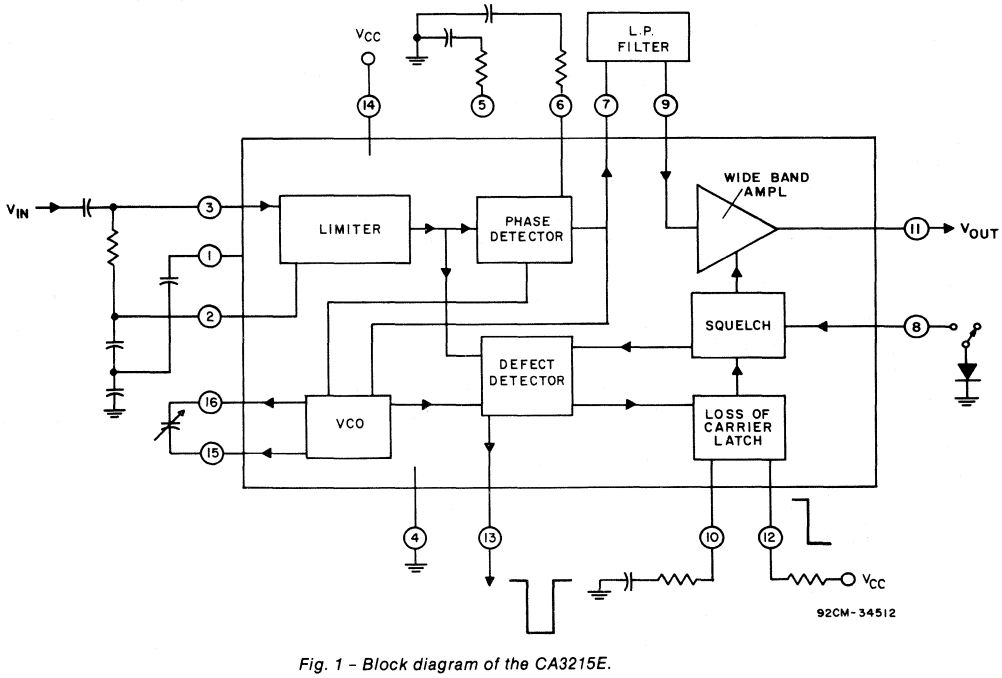


Fig. 1 - Block diagram of the CA3215E.

File Number **1358**

CA3215

The RCA CA3215E is intended for use as the video and audio demodulators for video disc playback. It can operate over the temperature range of -40°C to +85°C.

The CA3215E is supplied in the 16-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
(Pins 12 or 14 to 4) ..... 16 V
DEVICE DISSIPATION:
Up to T_A = 60°C ..... 600 mW
Above T_A = 60°C ..... Derate lineary at 6.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... -40 to +85°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 12 Volts

CHARACTERISTIC	LIMITS			UNITS
	MIN	TYP	MAX	
Static (DC) Characteristics				
Quiescent Current I_{14}	21	28	35	mA
DC Voltage				V
Terminals 1, 2, and 3	3	3.4	4	
Terminals 9 and 11	5.4	5.8	6.3	
Terminal 8	4	4.3	4.7	
Terminal 13		5.8		
Terminal 7		6.5		
Dynamic Characteristics **Conditions: F input = 5 MHz, F mod. = 400 Hz, Deviation = ±1 MHz** **See Figure 2 for test circuit**				
Input limiting voltage for -3 dB output (TP1)			5	mVrms
Demodulated Ouput (TP1)	110		240	mVrms
Total Harmonic Distortion, THD (TP1)			2.5	%
Noise (3 MHz BW) (TP1)		1		mVrms
Open Loop Gain * (Pin 9 to P11) (TP1)		66		x
3 MHz response ** (TP1)		3		dB
5 MHz suppression *** (TP2) no modulation		-40		
Squelched demod. output (TP1)		-55		
Squelched DC shift **** (TP6)			±350	mVDC

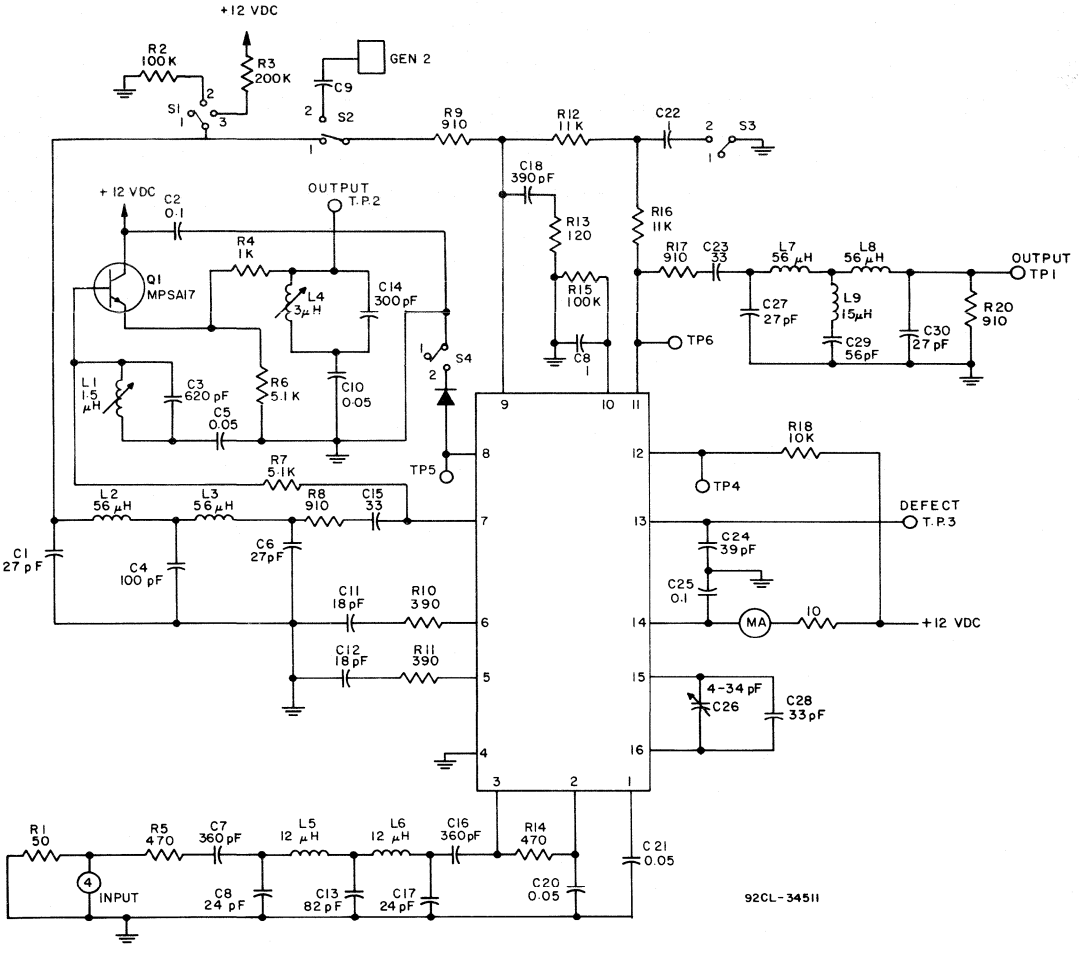
* Use Gen 2 at f = 10,000 Hz; S3 closed

** F mod = 3 MHz; compare reading to demod. output

*** Close S4; compare reading to demod. output

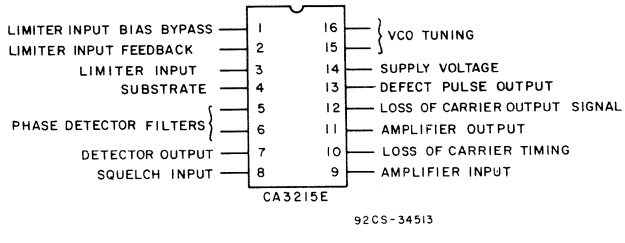
**** Change in Pin 11 DC voltage under squelched and non-squelched condition

CA3215



All capacitances are in μF unless otherwise noted.

Fig. 2 - Test circuit.



TERMINAL DIAGRAM

CA3232

÷20 Prescaler

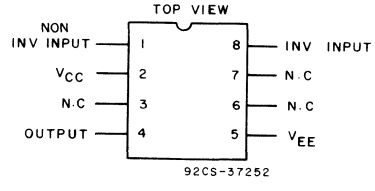
Advance Information/ Preliminary Data

Features:
- *Operation to 200 MHz*
- *TTL and CMOS compatible*
- *5-V power supply*
- *Open collector output stage*
- *Low power dissipation*

Applications:
- *Digital synthesizers*
- *Counters*
- *AM/FM communication circuits*

The CA3232E is a fixed-ratio divide-by-20 counter, operating at frequencies up to 200 MHz. It accepts single- or double-ended AC-coupled input signals. The output is an open-collector stage.

The CA3232 is supplied in an 8-lead dual-in-line plastic (Mini-DIP) package (E suffix).



TERMINAL ASSIGNMENT

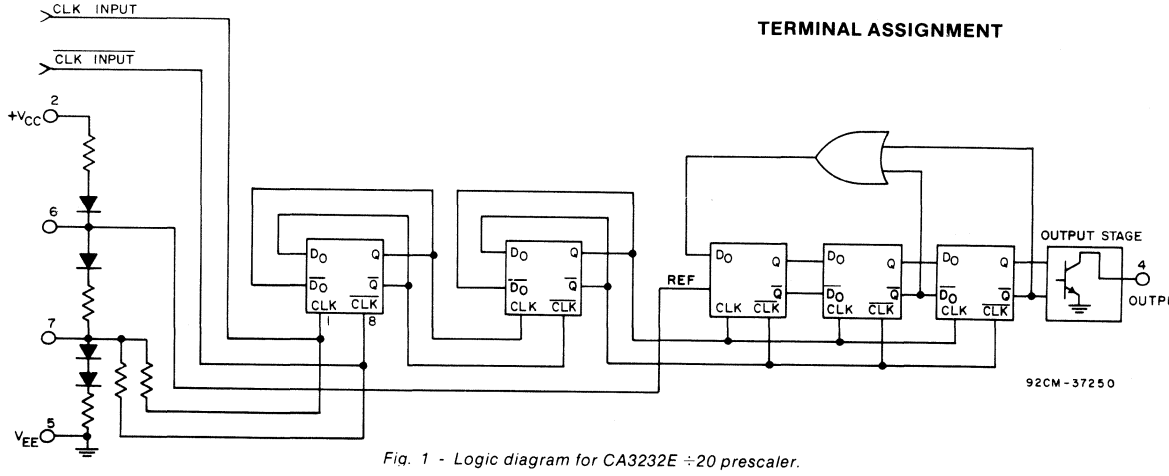


Fig. 1 - Logic diagram for CA3232E ÷20 prescaler.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

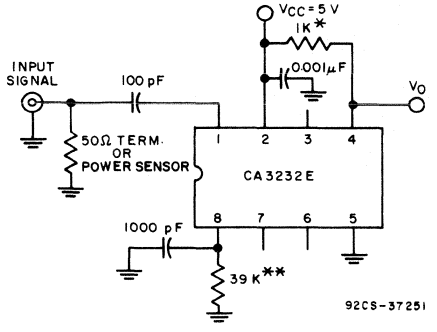
DC SUPPLY VOLTAGE ..... 5.5 V
RMS INPUT VOLTAGE ..... 0.5 V
DEVICE DISSIPATION:
  Up to T_A = 70°C ..... 630 mW
  Above T_A = 70°C ..... Derate linearly at 7.7 mW/°C
AMBIENT TEMPERATURE RANGE:
  Operating ..... -30 to +85°C
  Storage ..... -55 to +150°C
LEAD TEMPERATURE (During Soldering):
  At distance 1/16 ± 1/32 in. (1.59 mm ± 0.79 mm) from case for 10 s max. ..... 265°C

File Number **1506**

CA3232

ELECTRICAL CHARACTERISTICS, T_A = 25°C, V+ = 5 V DC, V- = 0 V DC

CHARACTERISTIC	LIMITS			UNITS
	Min.	Typ.	Max.	
Supply Current, Circuit Fig. 2 @ 5.3 V	—	21	30	mA
Output Level, High	—	4.9	—	V dc
Output Level, Low	—	0.7	—	V dc
Input Level	100	—	400	mV rms
Maximum Input Frequency	—	200	—	MHz



* For higher peak-to-peak output, connect 1 K ohm from pin 4 to 10 V supply
** Optional, to suppress self-oscil[illegible] no input signal

Fig. 2 - Test circuit.

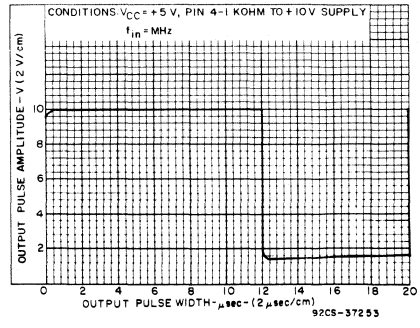


Fig. 3 - Output waveform vs. frequency, f_{in}=1 MHz.

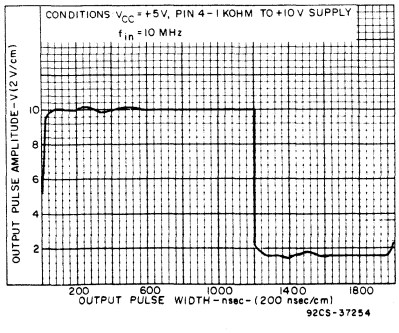


Fig. 4 - Output waveform vs. frequency, f_{in}=10 MHz.

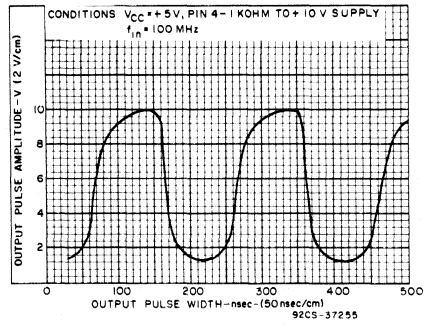


Fig. 5 - Output waveform vs. frequency, f_{in}=100 MHz.

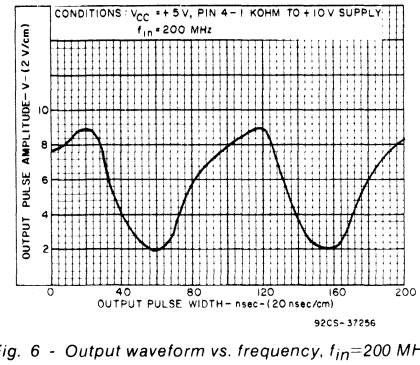


Fig. 6 - Output waveform vs. frequency, f_{in}=200 MHz.

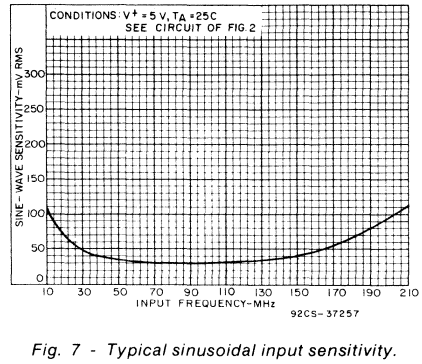


Fig. 7 - Typical sinusoidal input sensitivity.

CA3257

Product Preview

PLL FM Multiplex Stereo Demodulator

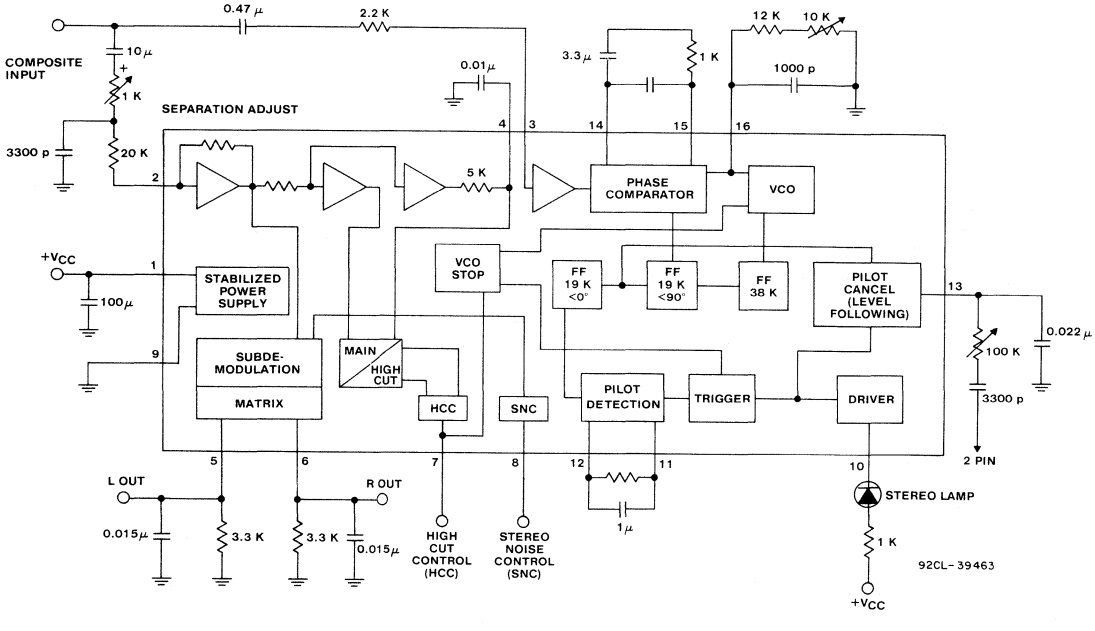
Features:

- *Wide operating voltage range; 6.5V to 14V, 12V nominal*
- *Automatic stereo switching*
- *Low distortion (0.05% typical)*
- *Good power supply ripple rejection (35 dB typical)*
- *Excellent SCA (Storecast) rejection (80 dB typical)*
- *Includes driver for stereo-lamp indicator*

The RCA CA3257* monolithic silicon integrated circuit is a multiplex IC designed for use in FM car stereo applications. It contains a pilot canceller, stereo noise controller, high-cut controller, automatic selection between stereo and monaural, and has VCO oscillator stop.

The CA3257 is supplied in a 16-lead dual-in-line plastic package (E suffix).

*Formerly RCA Developmental Type No. TA13004.



Block diagram and typical application of the CA3257.

Preview data only

Product Preview

CA3258

Noise Blanker

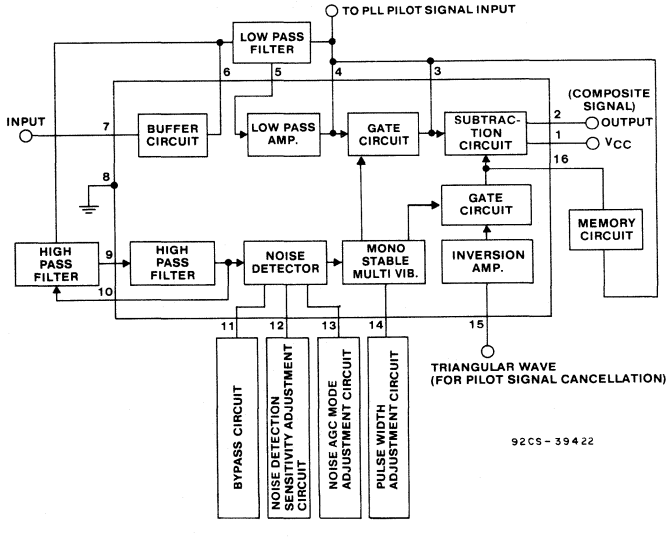
Features:

- *Pilot signal compensation function*
- *Pulse noise is removed without adversely affecting distortion*
- *Low distortion (THD = 0.02%)*
- *When used in conjunction with RCA CA3257, adverse effect caused by pilot signal can be compensated for*
- *Variable input type noise AGC system (adjustable noise detector dynamic range)*

The RCA CA3258* is a monolithic silicon integrated circuit designed to be used in conjunction with a PLL FM multiplex stereo demodulator (such as the RCA CA3257). It has the capability to effectively remove external noise (noise pulse) caused by automobile engines, etc.

The CA3258 is supplied in an 18-lead dual-in-line plastic package (E suffix).

*Formerly RCA Developmental Type No. TA13005.



Block diagram and typical application of the CA3258.

Preview data only

CA3259
Stereo Sound Volume/Tone Control

Product Preview

Features:

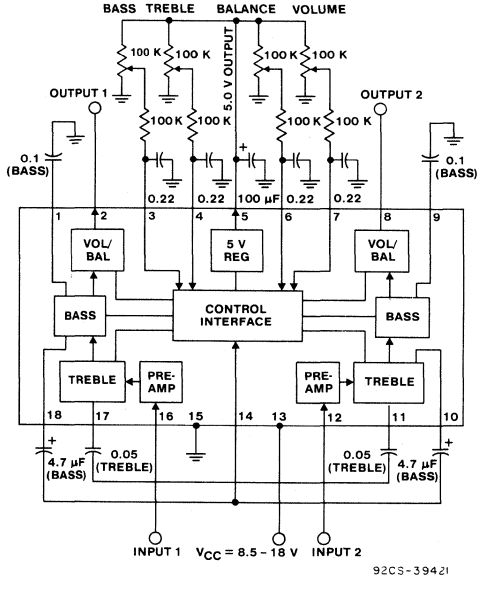
- *Four high impedance dc controls - volume, bass, treble, and balance*
- *A single external capacitor defines each tone control characteristic*
- *Wide power supply range 8.5V to 18V dc*
- *Low Distortion (0.1% typical)*
- *Channel separation better than 45dB*
- *+14dB of tone control*
- *More than 75dB of volume control range*
- *Wide dynamic range (100mV to 500mV (RMS)) input signal*
- *Low output impedance*

The RCA CA3259• monolithic silicon integrated circuit is a single chip stereo balance, volume, bass, and treble control circuit designed for use in car radios, TV, and audio systems.

•Formerly RCA Developmental Type No. TA13042.

Simple dc inputs allow the control to be effected by four inexpensive potentiometers or a remote control system. The bass and treble responses are defined by a single capacitor per control per channel.

The CA3259 is supplied in an 18-lead dual-in-line plastic package (E suffix).



Block diagram and typical application of the CA3259.

Preview data only

Video Monitor Circuits — Technical Data

Video Monitor Circuits (Cont'd)

Type No.	Description	Page No.
Broadband Video Amplifiers (Cont'd)		
CA3094	Programmable Power Switch/Amplifier	275
CA3100	Wideband Single Amplifier	286
CA3130	BiMOS Operational Amplifier	292
CA3183	High Voltage Transistor Arrays	688
CA3227	High Voltage Transistor Array	706
CA3246	High Voltage Transistor Array	706
CA3250	Common-Emitter Array	171
CA3256	Analog Video Switch and Amplifier	925
CA3280	Dual Variable Op Amp	375
CA3410	Quad Operational Amplifier	388
CA3450	Video Line Driver, High Speed	409
CD74HCU04	Hex Inverter (Unbuffered)	—

For data on CD4XXXX types, refer to *DATABOOK SSD-250C*, CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices*.

For data on CD54/74HC/HCTXXX types, refer to *DATABOOK SSD-290*, QMOS High Speed CMOS Logic ICs, or the specific data bulletin for that type shown in the *Index to Devices*.

CA555, CA555C

Timers

For Timing Delays & Oscillator Applications in Commercial, Industrial, and Military Equipment

Features:

- *Accurate timing from microseconds through hours*
- *Astable and monostable operation*
- *Adjustable duty cycle*
- *Output capable of sourcing or sinking up to 200 mA*
- *Output capable of driving TTL devices*
- *Normally ON and OFF outputs*
- *High-temperature stability - 0.005%/°C*
- *Directly interchangeable with SE555, NE555, MC1555, and MC1455*

The RCA-CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the wave-form signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacement for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

Applications

- *Precision timing*
- *Sequential timing*
- *Time-delay generation*
- *Pulse generation*
- *Pulse-width and position modulation*
- *Pulse detector*

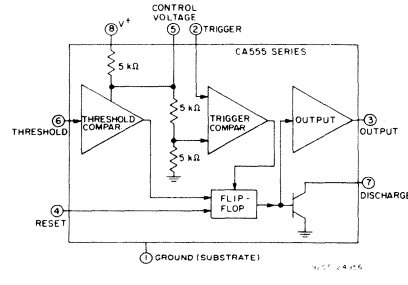


Fig. 1 — Functional diagram of the CA555 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 18 V

DEVICE DISSIPATION:

Up to T_A = 55°C ..... 600 mW

Above T_A = 55°C ..... Derate linearly 5 mW/°C

AMBIENT TEMPERATURE RANGE:

OPERATING

CA555 ..... -55 to +125°C

CA555C ..... 0 to 70°C

STORAGE ..... -65 to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

File Number **834**

CA555, CA555C

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	$(2/3)V^+$	–	–	$(2/3)V^+$	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V, $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V, $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	V
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V, $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V, $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	$R_1, R_2 = 1$ to 100 kΩ, $C = 0.1$ μF, Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/°C
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.

CA555, CA555C

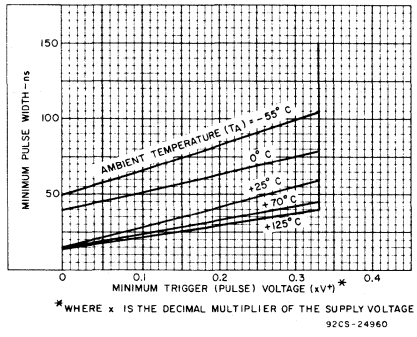


Fig.2 – Minimum pulse width vs. minimum trigger voltage.

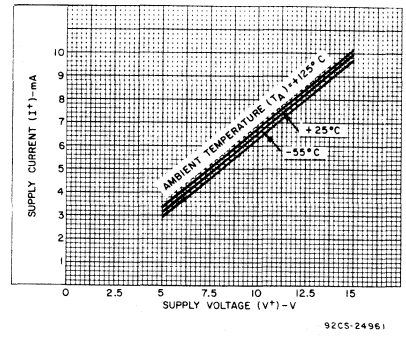


Fig.3 – Supply current vs. supply voltage.

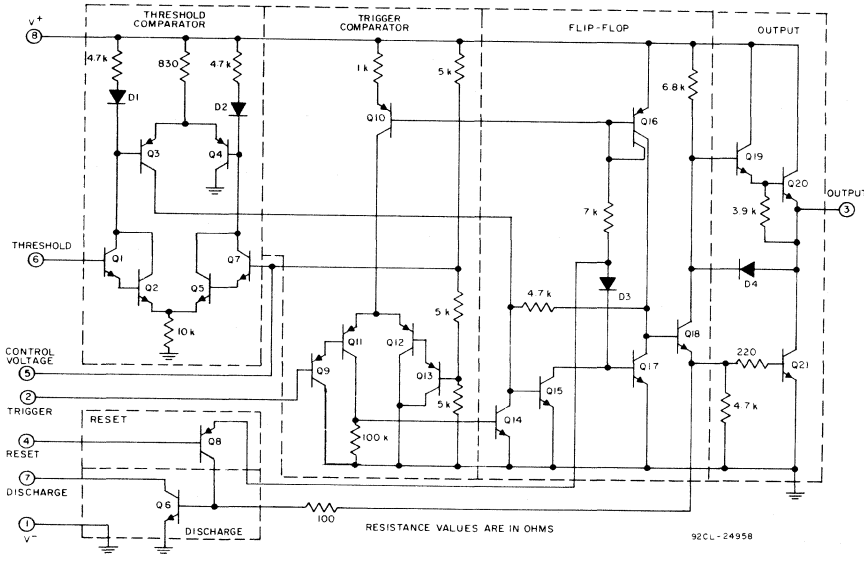
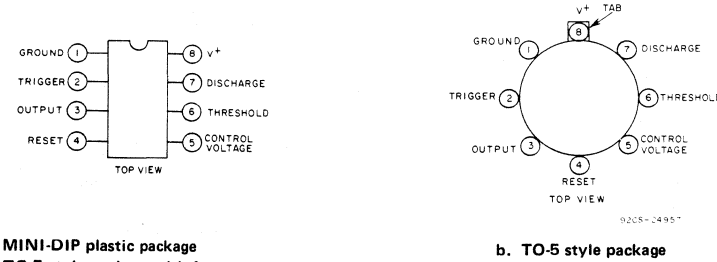


Fig.4 – Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package
TO-5 style package with formed leads

b. TO-5 style package

Fig.5 – Terminal assignment diagrams.

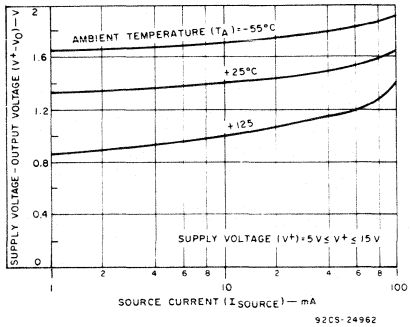


Fig.6 – Output voltage drop (high state) vs. source current.

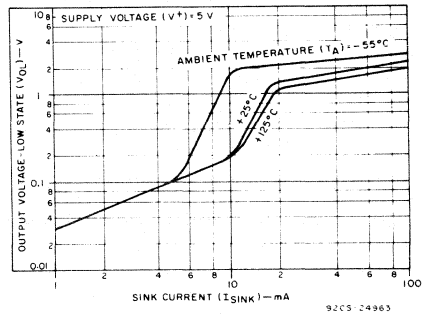


Fig.7 – Output voltage-low state vs. sink current at $V^+ = 5$ V.

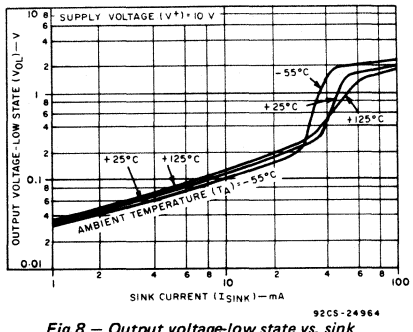


Fig.8 – Output voltage-low state vs. sink current at $V^+ = 10$ V.

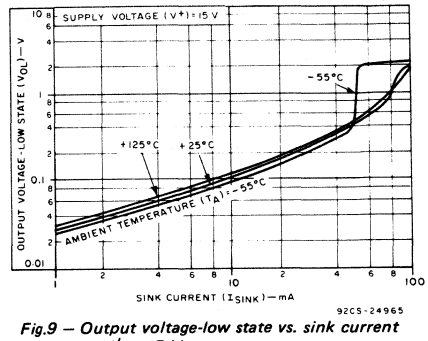


Fig.9 – Output voltage-low state vs. sink current at $V^+ = 15$ V.

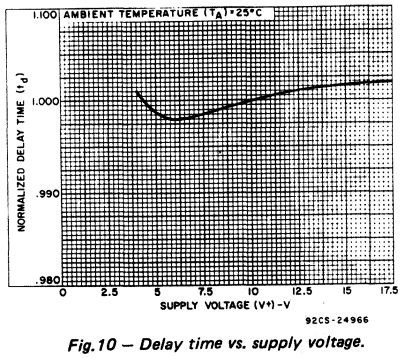


Fig.10 – Delay time vs. supply voltage.

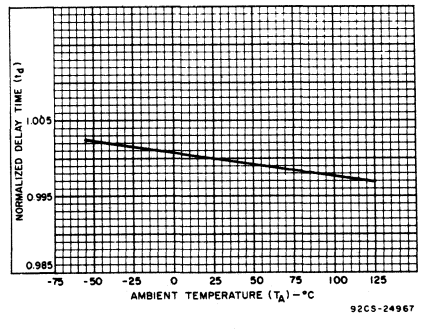


Fig.11 – Delay time vs. temperature.

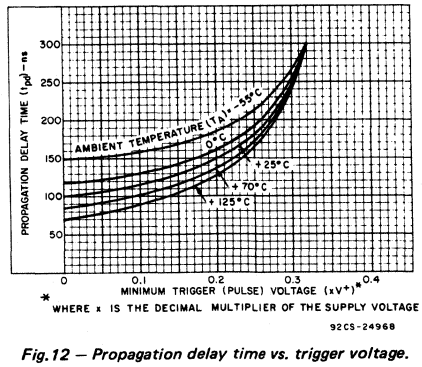


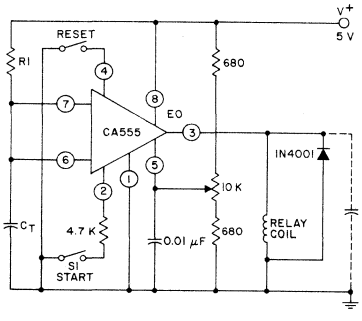
Fig.12 – Propagation delay time vs. trigger voltage.

CA555, CA555C

TYPICAL APPLICATIONS

Reset Timer (Monostable Operation)

Fig.13 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the time constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.



ALL RESISTANCE VALUES ARE IN OHMS

92CS-26780R1

Fig.13 – Reset timer (monostable operation).

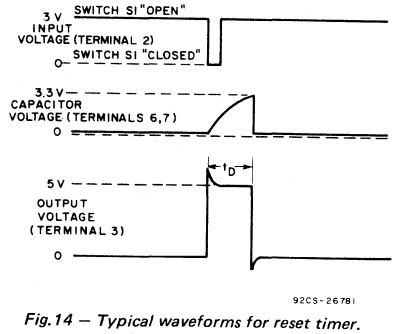
Since the charge rate and threshold level of the comparator are both directly proportional to V^+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1 volt change in V^+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Fig.14 shows the typical waveforms generated during this mode of operation, and Fig.15 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Fig.16 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2;



92CS-26781

Fig.14 – Typical waveforms for reset timer.

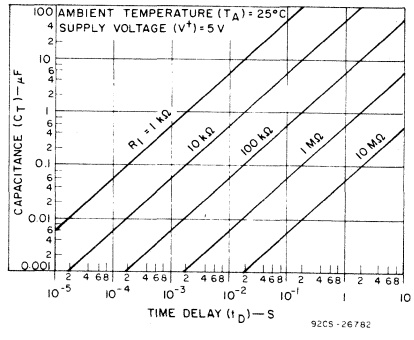


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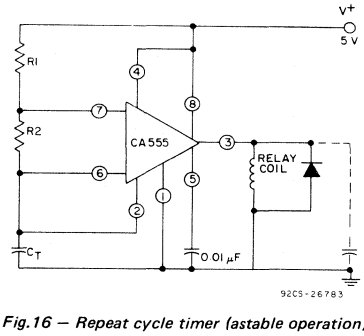
Fig.15 – Time delay vs. resistance and capacitance.



92CS-26783

Fig.16 – Repeat cycle timer (astable operation).

$$T = 0.693(R_1 + 2R_2)C_T = t_1 + t_2$$

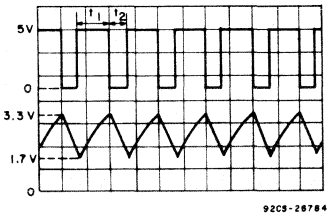
where $t_1 = 0.693(R_1 + R_2)\,C_T$

and $t_2 = 0.693(R_2)C_T$

The duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Fig. 17. Fig. 18 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig.17 – Typical waveforms for repeat cycle timer.

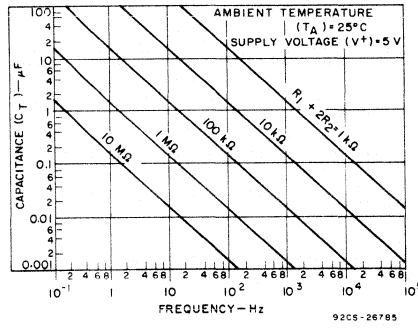


Fig.18 – Free running frequency of repeat cycle timer with variation in capacitance and resistance.

CA1391, CA1394

TV Horizontal Processors

CA1391E – Positive Horizontal Sawtooth Input
CA1394E – Negative Horizontal Sawtooth Input

Features:

- **Internal shunt regulator**
- **Linear balanced phase detector**
- **Preset hold control capability**
- **±300-Hz pull-in (typ.)**
- **Low thermal frequency drift**
- **Small static phase error**
- **Variable output duty cycle**
- **Adjustable dc loop gain**

The RCA-CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

These types are supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operate over an ambient temperature range of 0 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DC SUPPLY CURRENT	40 mA
DC OUTPUT VOLTAGE	40 V
DC OUTPUT CURRENT	30 mA
SYNC INPUT VOLTAGE	5 V_{p-p}
SAWTOOTH INPUT VOLTAGE	5 V_{p-p}
DEVICE DISSIPATION:	
Up to T_A = 25°C	625 mW
Above T_A = 25°C derate linearly	5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+260°C
THERMAL RESISTANCE	200°C/W

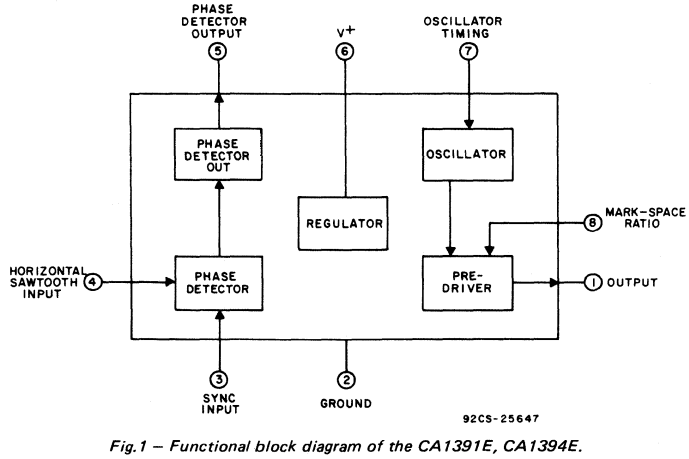


Fig. 1 – Functional block diagram of the CA1391E, CA1394E.

File Number **98**

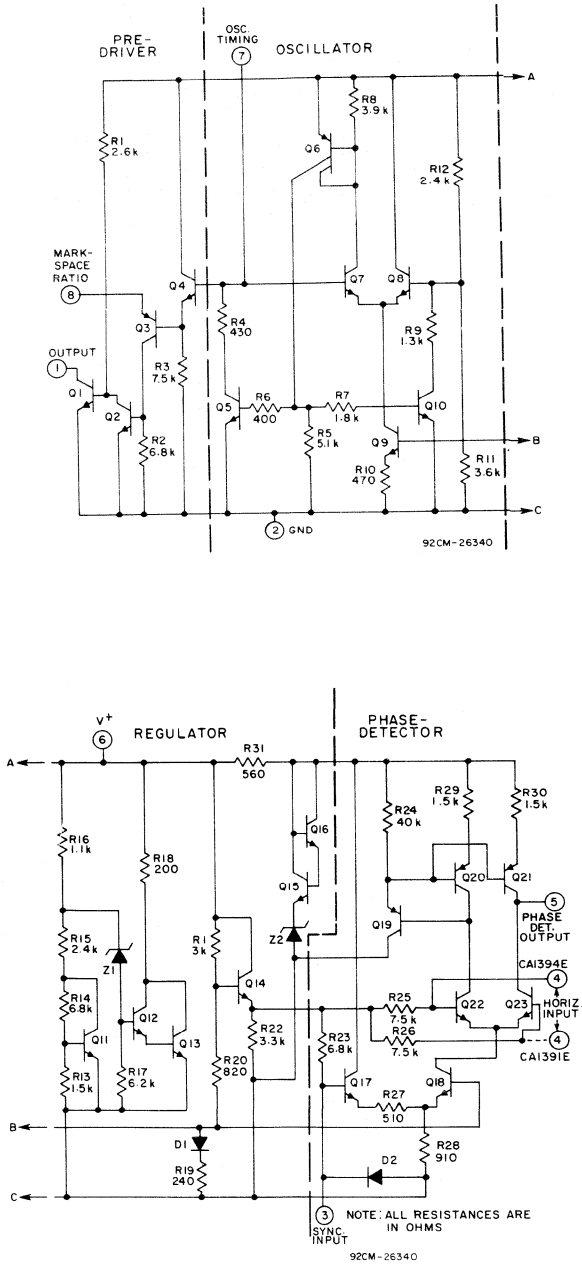


Fig.2 – Schematic diagram of CA1391E, CA1394E.

CA1391, CA1394

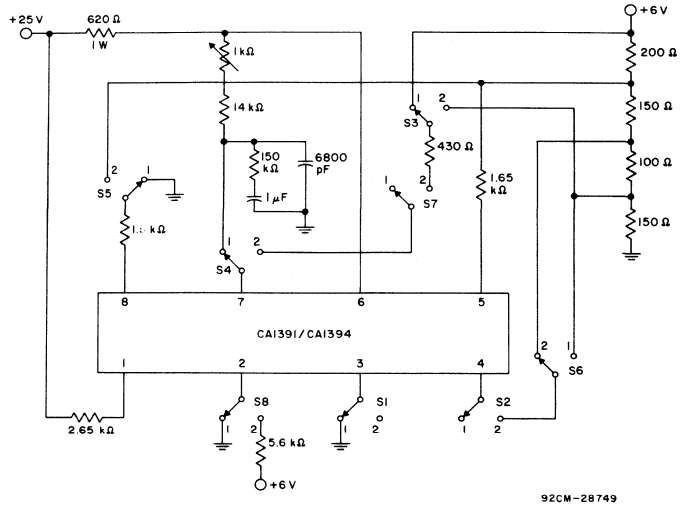


Fig.3 – DC test circuit.

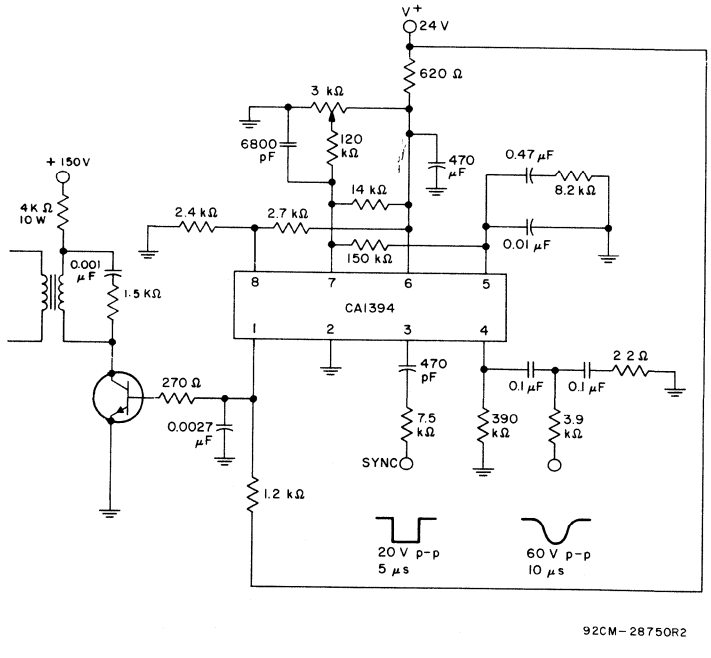


Fig.4 – Typical circuit application.

ELECTRICAL CHARACTERISTICS at T_A = 25°C (See Fig.3)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Measure term. 6 to Gnd	8	–	9	V
Free-Running Frequency	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Counter to term. 1	14734	–	16734	Hz
Output Leakage	S2, S3, S6, S8 = 1 S1, S4, S5, S7 = 2 Measure term. 1 to 25 V	–	10	–	mV
Output Saturation	S2, S3, S5, S6, S8 = 1 S1, S4, S7 = 2 Measure term. 1 to Gnd	–	60	–	mV
Phase Detector Bias	S2, S5, S6, S8 = 1 S1, S3, S4, S7 = 2 Measure term. 3 to Gnd	–	1.9	–	V
Phase Detector Leak	S5, S8 = 1 S1, S2, S3, S4, S6, S7 = 2 Measure term. 5 to +4 V	–2	–	+2	mV
Phase Detector Low	S1, S5, S8 = 1 S2, S3, S4, S6, S7 = 2 Measure term. 5 to +4 V	–0.55*	–	–	V
Phase Detector High	S1, S5, S6, S8 = 1 S2, S3, S4, S7 = 2 Measure term. 5 to +4 V	+0.55*	–	–	V
Phase Detector Balance	$V_{DET2} + V_{DET3}$	–100	–	+100	mV
Sync Diode	S1, S2, S3, S4, S6, S7 = 1 S5, S8 = 2	0.3	–	1.2	V
Static Phase Error	See Fig.4	–	0.5	–	μs
Oscillator Pull-in Range		–	±300	–	Hz
Oscillator Hold-in Range		–	±900	–	Hz

* Polarity reversed in the CA1391.

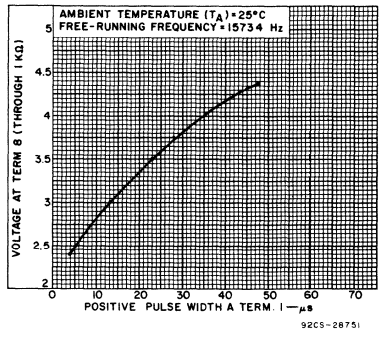


Fig.5 – Duty cycle at the pre-drive output (term.1) as it is affected by the input at term. 8.

CA1391, CA1394

CIRCUIT OPERATION

(See schematic diagram, Fig.2)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with terminal 7 used to control the timing. If it is assumed that Q7 is initially off, then an external capacitor connected from terminal 7 to ground charges through an external resistance connected between terminals 6 and 7. As soon as the voltage at terminal 7 exceeds the potential set at the base of Q8 by resistors R11 and R12, Q7 turns on, and Q6 supplies base current to Q5 and Q10. Transistor Q5 discharges the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time, Q7 turns off, and the cycle repeats.

The sawtooth generated at the base of Q4 appears across R3 and turn off Q3 whenever the sawtooth voltage rises to a value that exceeds the bias set at terminal 8. By adjusting the potential at terminal 8, the duty cycle at the pre-drive output (terminal 1) may be changed.

The phase detector is isolated from the remainder of the circuit by R31, Z2, Q15 and Q16. The phase detector consists of the comparator Q22 and Q23, and the gated current source Q18. Negative-going sync pulses at terminal 3 turn off Q17, and the current division between Q22 and Q23 is then determined by the phase relationship of the sync and the sawtooth waveform at terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q22 and Q23 during each half of the sync pulse period. The current in Q22 is turned around by current mirror Q20 and Q21 so that there is no net output current at terminal 5 for balanced conditons. When a phase offset occurs, current flows either in or out of terminal 5. In circuit applications, this terminal is connected to terminal 7 through an external low-pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a V_{BE} and zener multiplier. Resistors R13 and R14 multiply the V_{BE} of Q11, and the ratio of R15 and R16 multiplies the voltage of the zener diode Z1.

Advance Information/
Preliminary Data

CA1890E

TV Video/Audio, RF Modulator

Features:
- *Single power supply operation 10 V to 15 V, 12 V nominal*
- *Adjustable video dc restoration clamp level*
- *Excellent FM sound oscillator stability*
- *Low intermodulation products*
- *DC channel switching*

The RCA-CA1890E* is a monolithic bipolar integrated circuit designed to generate an RF TV signal from baseband video and audio signals.

It consists of a video dc restoration clamp, sound-carrier oscillator (LC type), two video-carrier oscillators (LC types), and RF modulator to produce one of two low-VHF channel signals. For applications with the standard U.S. television receiver, these are channel 3 and channel 4.

This integrated circuit may also be used as a general-purpose modulator in applications such as cable converters, video disk players, personal computers, and test equipment.

The CA1890E is supplied in a 14-lead, dual-in-line plastic package.

*Formerly RCA Developmental Type No. TA11916B.

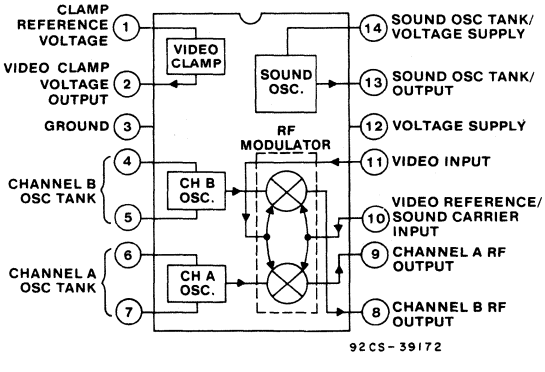


Fig. 1 - Block diagram and terminal assignment of the CA1890E.

File Number **1701**

CA1890

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 15 V

DEVICE DISSIPATION:

Up to T_A = 70°C ..... 900 mW

Above T_A = 70°C ..... derate linearly at 11.2 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to 70°C

Storage ..... -55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, all switches in position 1 and voltage supplies as indicated, unless otherwise specified. (Refer to Fig. 2)

CHARACTERISTIC	TEST PIN	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Supply Current, I_S		S1 and S14 in Position 2 Measure I_S	20	30	45	mA
Sound Oscillator/Modulator (FM)						
Sound Oscillator Current, I13	13	Measure I13	0.7	1	1.7	mA
Sound Oscillator Reference Current, I14	14	S14 in Position 2 Measure I14	0.7	1	1.7	mA
Sound Oscillator Current, ΔI14	14	S14 in Position 2 Change V13 from 13 V to 11 V Measure ΔI14	—	0.1	0.2	mA
Sound Oscillator ΔV	13	S14 in Position 2 Adjust V13 until I14=I14+ΔI14/2	—	40	75	mV
Video Clamp						
Video Clamp Reference Voltage, V2	2	S1 in Position 2 Measure V2 Voltage Difference=V1-V2	—	65	75	mV
Video Oscillator/Modulator (AM)						
Channel A Oscillator Current, I6	6	S10 and S11 in Position 2 Measure I6	0.6	1	1.5	mA
Channel A Oscillator Current, I7	7	S10 and S11 in Position 2 Measure I7	0.6	1	1.5	mA
Channel A Oscillator Balance	9	V_B=11 V Change V_A from 10 V to 12 V Measure ΔV9	40	70	110	mV
Channel A Modulator Conversion Ratio	9	With V10=4 V, V11=5 V and V_B=11 V Change V_A from 10 V to 12 V Measure ΔV9 CR=ΔV9/(V11-V10)	0.3	0.6	0.9	V/V
Channel B Oscillator Current, I4	4	S10 and S11 in Position 2 S A/B in Position 2 Measure I4	0.6	1	1.5	mA
Channel B Oscillator Current, I5	5	S10 and S11 in Positiion 2 S A/B in Position 2 Measure I5	0.6	1	1.5	mA
Channel B Oscillator Balance	8	S A/B in Position 2 V_A=11 V Change V_B from 10 V to 12 V Measure ΔV8	40	70	110	mV
Channel B Modulator Conversion Ratio	8	S A/B in Position 2 With V10=4 V, V11=5 V and V_A=11 V Change V_B from 10 V to 12 V Measure ΔV8 CR=ΔV8/(V11-V10)	0.3	0.6	0.9	V/V

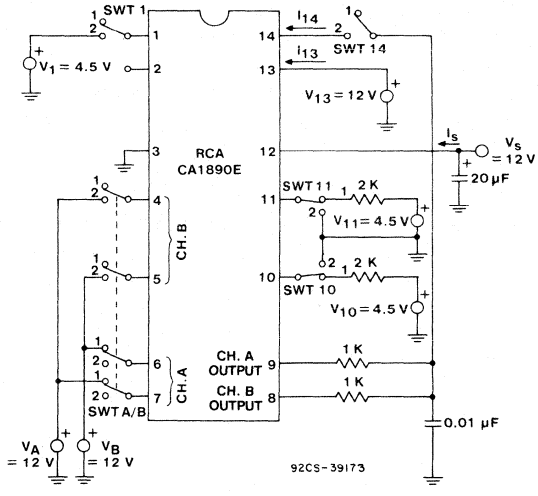


Fig. 2 - Static test circuit.

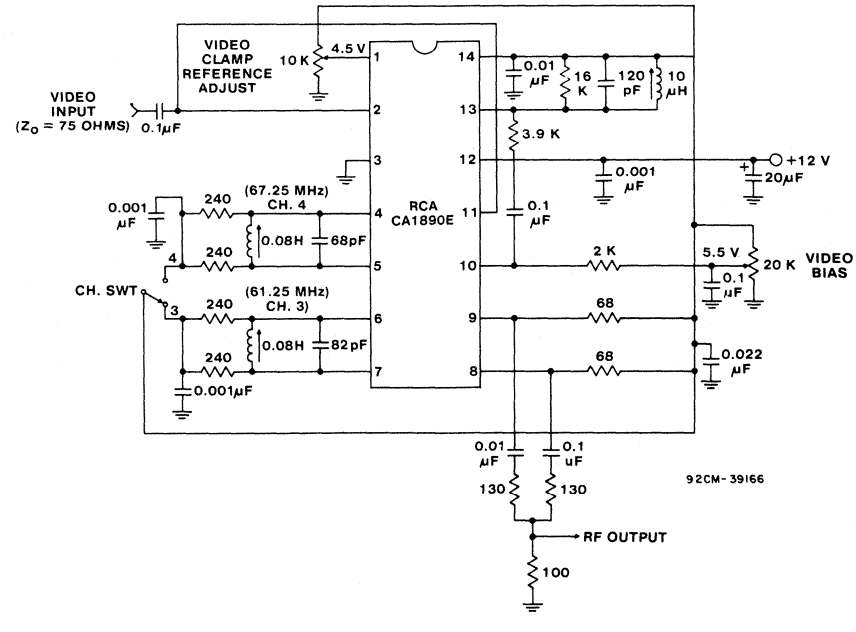


Fig. 3 - Dynamic test circuit.

CA1890

DESIGN ELECTRICAL CHARACTERISTICS, T_A=25°C; all voltage supplies as indicated, unless otherwise specified. Typical values are provided for design guidance only.

CHARACTERISTIC	TEST PIN	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Video Oscillator						
Video Oscillator Maximum Operating Frequency	4,5 and 6,7		—	110	—	MHz
Video Oscillator Stability vs. Temperature	4,5 and 6,7	See Fig. 5 (IC only)				
Channel 3 Video Oscillator Level	6,7	Channel switch in Position 3; f=61.25 MHz Use FET probe	2.7	3.2	4.7	mV_{p-p}
Channel 4 Video Oscillator Level	4,5	Channel switch in Position 4; f=67.25 MHz Use FET probe	2.7	3.2	4.7	mV_{p-p}
RF Modulator						
Input Impedance	10,11		—	1	—	MΩ
	10,11		—	1	—	pF
Input Bias Level	10,11	Pin 11 bias is adjusted to make the upper 3.57945 MHz subcarrier - 12.5 dB with respect to the video carrier	5.9	6.4	6.9	V
Channel 3 Conversion Gain	9	Channel switch in Position 3; f=61.25 MHz $C_G=V_{out}/(V10-V11)$ with rf meter having Z_{in}=75 Ω	—	10	—	mV rms/V
Channel 4 Conversion Gain	8	Channel switch in Position 4; f=67.25 MHz $C_G=V_{out}/(V10-V11)$ with rf meter having Z_{in}=75 Ω	—	10	—	mV rms/V
RF Carrier Suppression	8,9	Adjust Video bias for minimum rf carrier at V_{out} and reference to V_{out} with 3-V offset at pins 10 and 11	—	-30	—	dB
Output Harmonics Below RF Carrier						
2nd, 3rd	8,9		—	-3	—	dB
4th and above	8,9		—	-20	—	dB
Differential						
Gain		2.5 V_{p-p} Video, 87.5% mod.	—	5	—	%
Phase			—	3	—	degree
920-kHz Beat		3.58 MHz @ 30% 4.5 MHz @ 25%	—	-50	—	dB
Sound Oscillator/Modulator (FM)						
Sound Carrier Oscillator Level	13	f_o=4.5 MHz	—	3.4	—	V_{p-p}
Sound Oscillator Bandwidth	13		—	100	—	kHz
Sound Oscillator Deviation Sensitivity	13	f_o=4.5 MHz, $\Delta f/\Delta V_{IN}$	—	250	—	kHz/V
Sound Modulator Audio Distortion, THD	13	f_o=4.5 MHz, f_m=1 kHz, Δf=±25 kHz	—	0.8	—	%
Sound Oscillator Stability vs. Temperature	13	See Fig. 6 (IC only)				
Sound Oscillator Stability vs. Voltage Supply	13	See Fig. 8 (IC only)				

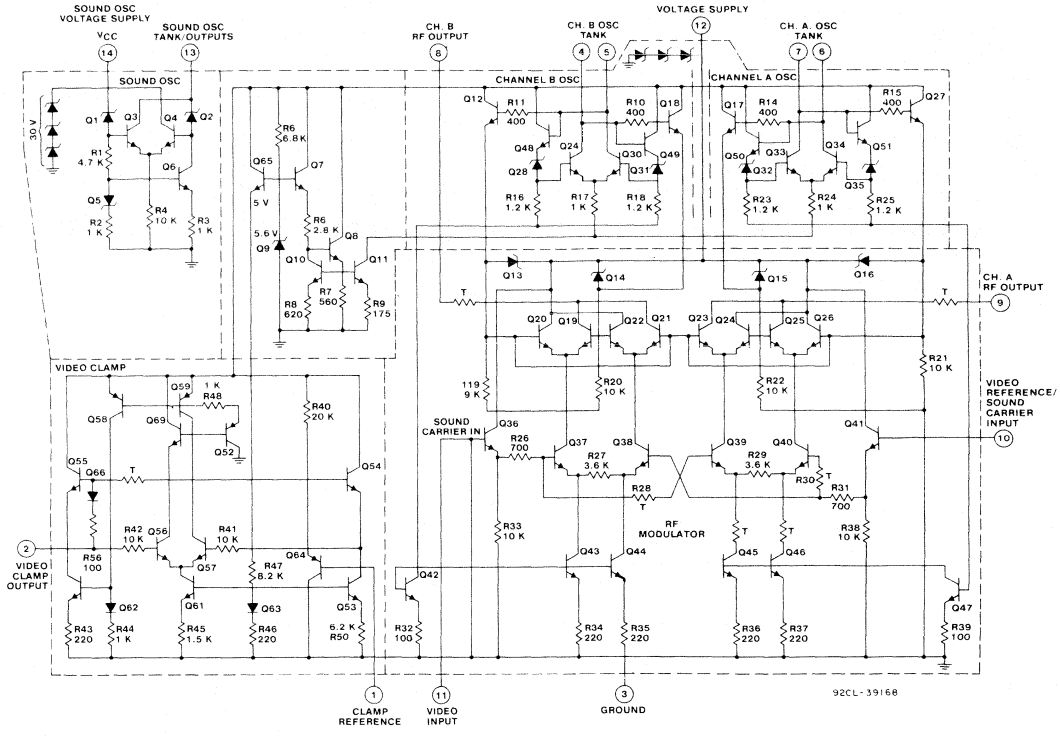


Fig. 4 - Schematic diagram of the CA1890E.

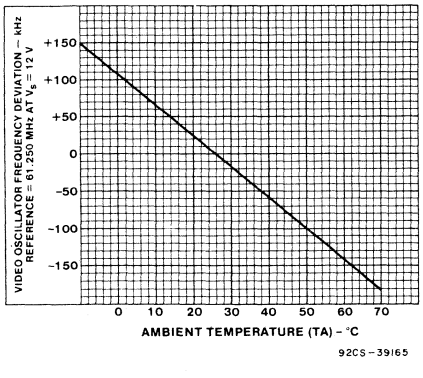


Fig. 5 - Video oscillator frequency as a function of ambient temperature.

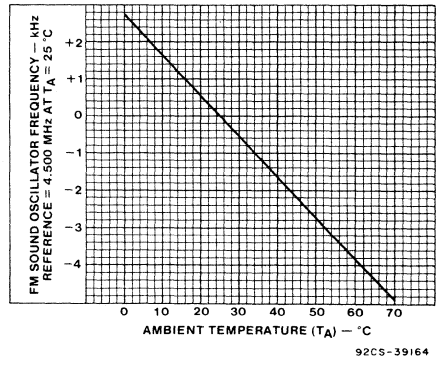


Fig. 6 - FM oscillator frequency as a function of ambient temperature.

CA1890

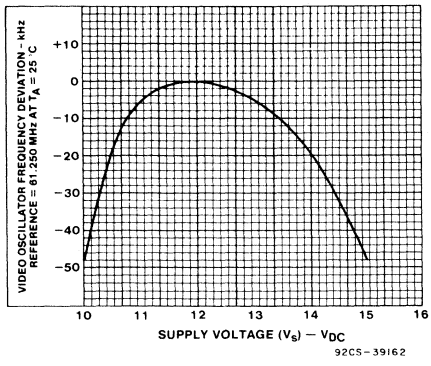


Fig. 7 - Video oscillator frequency as a function of supply voltage.

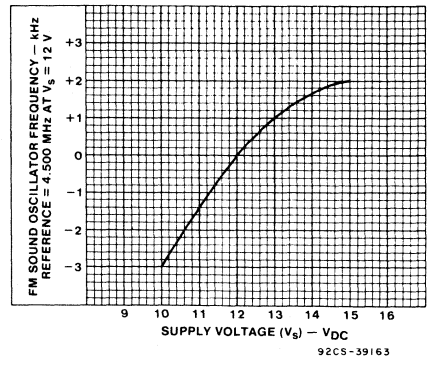


Fig. 8 - FM oscillator frequency as a function of supply voltage.

General Circuit Description

The RCA-CA1890E is used to modulate baseband audio and video signals onto one of two low-VHF TV receiver channels. The audio signal deviates the frequency of the 4.5-MHz sound oscillator. This frequency-modulated carrier and the input video signal are used to amplitude modulate the picture carrier oscillator. The resulting composite RF signal is passed through an external Vestigial Side-Band (VSB) filter and then to the antenna input terminals of the TV receiver. A typical application circuit is shown in Fig. 9.

Sound Oscillator/Modulator (FM)

This oscillator is a differential amplifier with cross-coupled collectors to produce positive feedback for oscillation at a frequency defined by the tank circuitry.

The center frequency is 4.5 MHz and the tank circuitry would be comprised of components as indicated in Fig. 10.

As indicated in Fig. 10, the conventional FM approach is to ac couple the audio to an externally dc-biased varactor diode to deviate the tank frequency up to ±25 kHz from its center frequency of 4.5 MHz.

Please note that the sound carrier oscillator can be disabled by removing the supply voltage from pins 13 and 14.

Video Clamp

In the typical application (see Fig. 9), the input video signal is ac-coupled via capacitor C2. The value of C2 is typically 0.1 μF with the value being chosen depending on the desired noise immunity and the desired dc restoration time.

The video clamp is provided to restore/establish the dc voltage level of the ac-coupled video input signal to a fixed level of the sync tips which will help insure proper rf modulation (i.e., holding the video signal sync tip at a particular level to provide control of modulation depth). The video clamp voltage level can be adjusted so that it can be set to optimize performance for the particular application.

A small offset of approximately 60 mV exists between pin 1 (reference voltage input) and pin 2 (output clamp voltage) due to different current levels in Q64 and Q55. Therefore, the externally applied reference voltage on pin 1 is set approximately 60 mV higher than the desired clamp voltage at pin 2. The video clamp voltage is typically 4.5 volts. It is recommended that both the Video Clamp Reference potentiometer (pin 1) and the Video Bias potentiometer (pin 11) be referenced to the supply voltage V_S to maintain good tracking between the voltages applied to pins 10 and 11.

AM Video Oscillator (Channel A or Channel B)

Two rf channels are available with carrier frequencies up to 110 MHz being determined by external L-C tank circuitry at pins 4 and 5 (Channel B), and 6 and 7 (Channel A). One of two can be selected by means of an applied dc voltage via the Channel Select switch. It is recommended that the R-C (100 ohm, 0.001 μF) decoupling network between the channel select switch and voltage supply be used to minimize the amount of video oscillator rf energy getting to the supply voltage. The frequency of the L-C tank circuitry is determined by the expression: $f=1/2\pi\sqrt{LC}$.

External resistors R4, R5 for Channel B and R6, R7 for Channel A are the oscillator loads which determine the oscillator amplitude and influence the tank Q.

Increasing these resistors increases the resultant Q and therefore the oscillator amplitude. Too large a resistor value would over-drive the RF modulator causing increased output of rf harmonics. Too small a resistor value reduces the resultant tank Q and causes increased drift.

RF Modulator

In addition to the video carrier frequency inputs from either of the selected channel oscillators, the clamped video signal is inputted to pin 11, while the video bias level and modulated sound carrier are inputted to pin 10. (Please note that because of symmetry of the modulator, those inputs could be exchanged if desired.)

When the signal inputs are exactly balanced, ideally there is no rf carrier present at the output. However, when sound transmission is needed, it is particularly important that the largest video signal (peak white) does not suppress the carrier completely. This would cause a "buzz" in the recovered audio due to the interrupted presence of the sound carrier in the TV receiver.

The dc offset between these two signal pins determines the level of the rf carrier output. The video bias level (at pin 10) is set above the largest expected video signal. This voltage would be typically 2 volts. For example, if the video clamp voltage at pin 1 is 4.5 volts, the video bias voltage at pin 10 would be 6.5 volts.

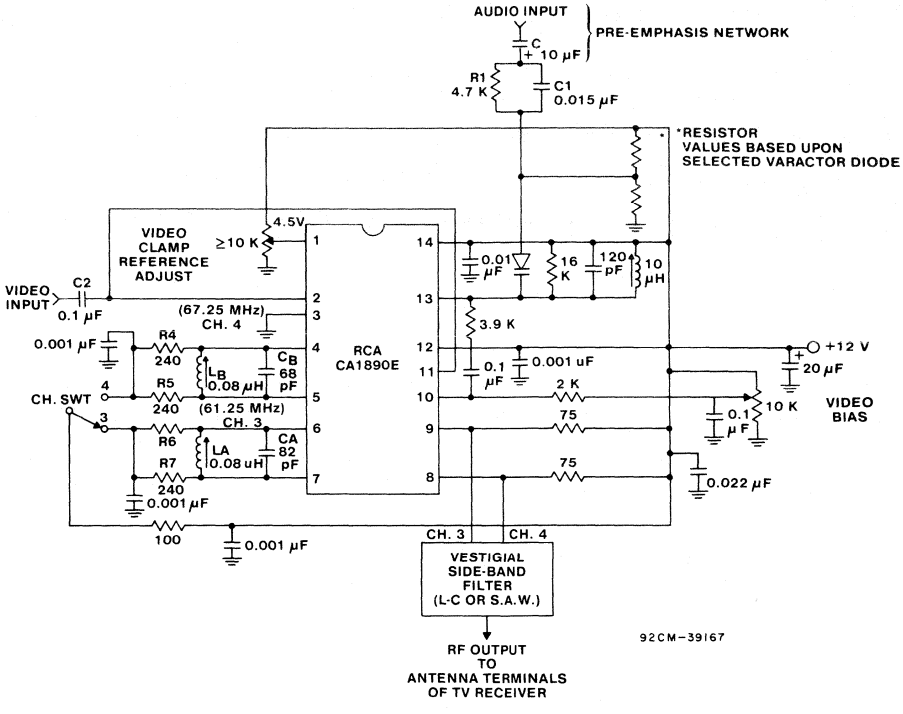


Fig. 9 - Typical application circuit of the CA1890E.

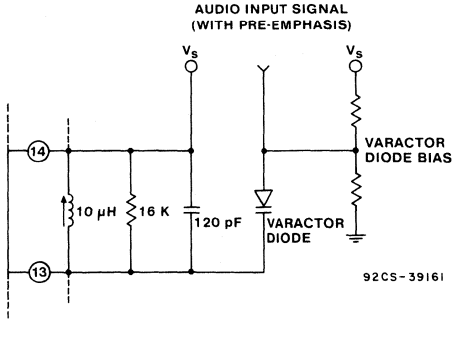


Fig. 10 - Sound oscillator/modulator (FM).

CA3126

TV Chroma Processor

Features:

- *Phase-locked subcarrier regeneration utilizes sample-and-hold techniques*
- *Automatic chrominance control (ACC)/killer detector employs sample-and-hold techniques*
- *Supplementary ACC with an overload detector to prevent oversaturation of this picture tube*
- *Sinusoidal subcarrier output*
- *Keyed chroma output*
- *Emitter-follower buffered outputs for low output impedance*
- *Linear dc saturation control*

RCA-CA3126Q is a monolithic silicon integrated circuit designed for chroma processing applications in color TV receivers. It is compatible with the CA3067 chroma demodulator as well as other chroma demodulators.

The CA3126 is supplied inaa 16-lead dual-in-line plastic package (E Suffix) and in a 16-lead quad-in-line plastic package (Q Suffix).

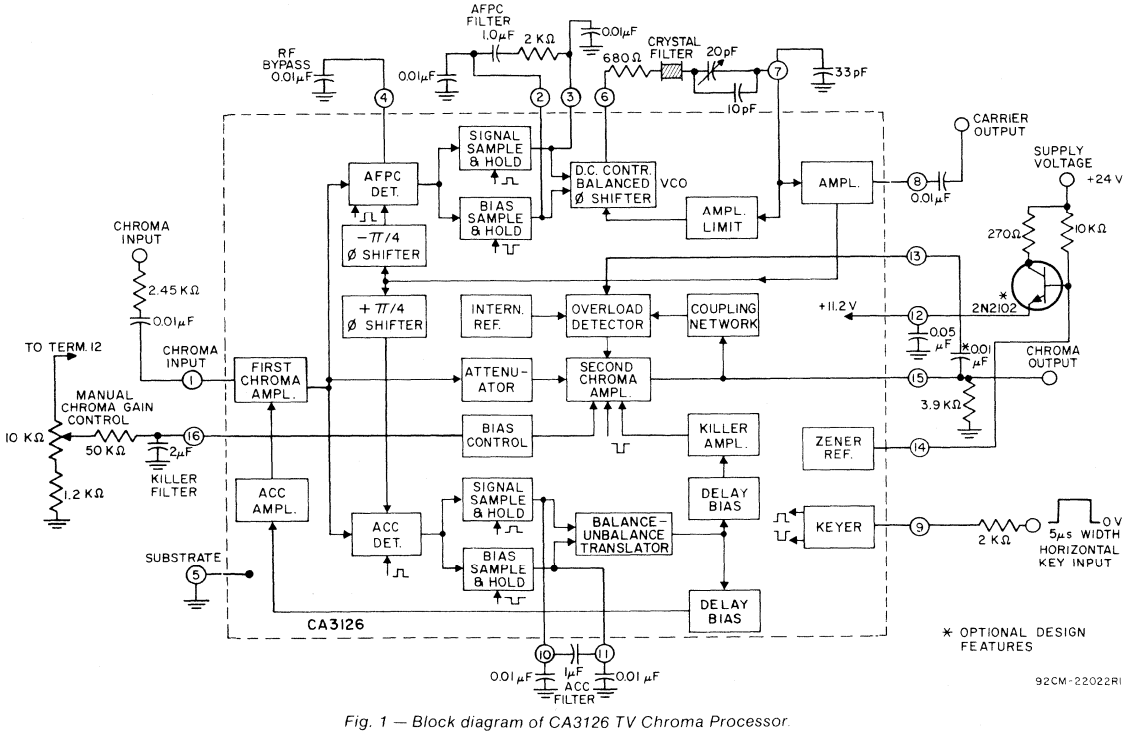


Fig. 1 — Block diagram of CA3126 TV Chroma Processor.

File Number **860**

CA3126

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

DEVICE DISSIPATION:
- Up to T_A = 55° C ..... 750 mW
- Above T_A = 55° C ..... derate linearly 7.9 mW/° C

DC SUPPLY VOLTAGE (Across Terms. 5 and 12)▲ ..... 13.2 V

DC CURRENT:
- Into Term. 12 ..... 38 mA
- Into Term. 14 ..... 20 mA

DC VOLTAGE (Terminal 9):
- Negative Rating ..... -5 V
- Positive Rating ..... 3 V

AMBIENT TEMPERATURE RANGE:
- Operating ..... -40 to +85° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At a distance not less than 1/32 in (0.79 mm) from case for seconds max. ..... +265° C

▲This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, chroma control at maximum position for all characteristics tests except for chroma output test. For this test, control should be set at minimum position. Electrical characteristics referenced to test circuit, Fig.2.

CHARACTERISTIC	TERMINAL, MEASUREMENT, AND SYMBOL	SWITCH POS.		CHROMA INPUT	LIMITS			UNITS
		S1	S2	TP1	Min.	Typ.	Max.	
Static Characteristics								
Voltage Regulator	V_{12}	2	2	0	10.1	11.2	12.1	V
Supply Current	I_{12}	2	2	0	16	25	38	mA
Dynamic Characteristics (See Note 1)								
Pull-in Range*	V_8	*	2	0.5 V_{p-p}	±250	–	–	Hz
Oscillator Output	V_8	2	2	0	0.6	1.0	–	V_{p-p}
100% Chroma Output	V_{15}	1	2	0.5 V_{p-p}	1.4	2.7	–	V_{p-p}
Overload Detector	V_{15}	1	1	0.5 V_{p-p}	0.4	–	0.7	V_{p-p}
Minimum Chroma Output	V_{15}	1	2	0.5 V_{p-p}	–	–	20	mV_{p-p}
200% Chroma Output	V_{15}	1	2	1 V_{p-p}	70	100	140	% of 100% reading
20% Chroma Output	V_{15}	1	2	0.1 V_{p-p}	40	–	105	
Kill Level	V_{TP1}	1	2	vary	5	–	60	mV_{p-p}

Note 1: Except for pull-in range testing, tune oscillator trimmer capacitor for free-running frequency of 3.579545 MHz ± 10 Hz.
*Set Switch 1 to Position 2, detune oscillator ± 250 Hz, set Switch 1 to Position 1, and check for oscillator pull-in.

CA3126

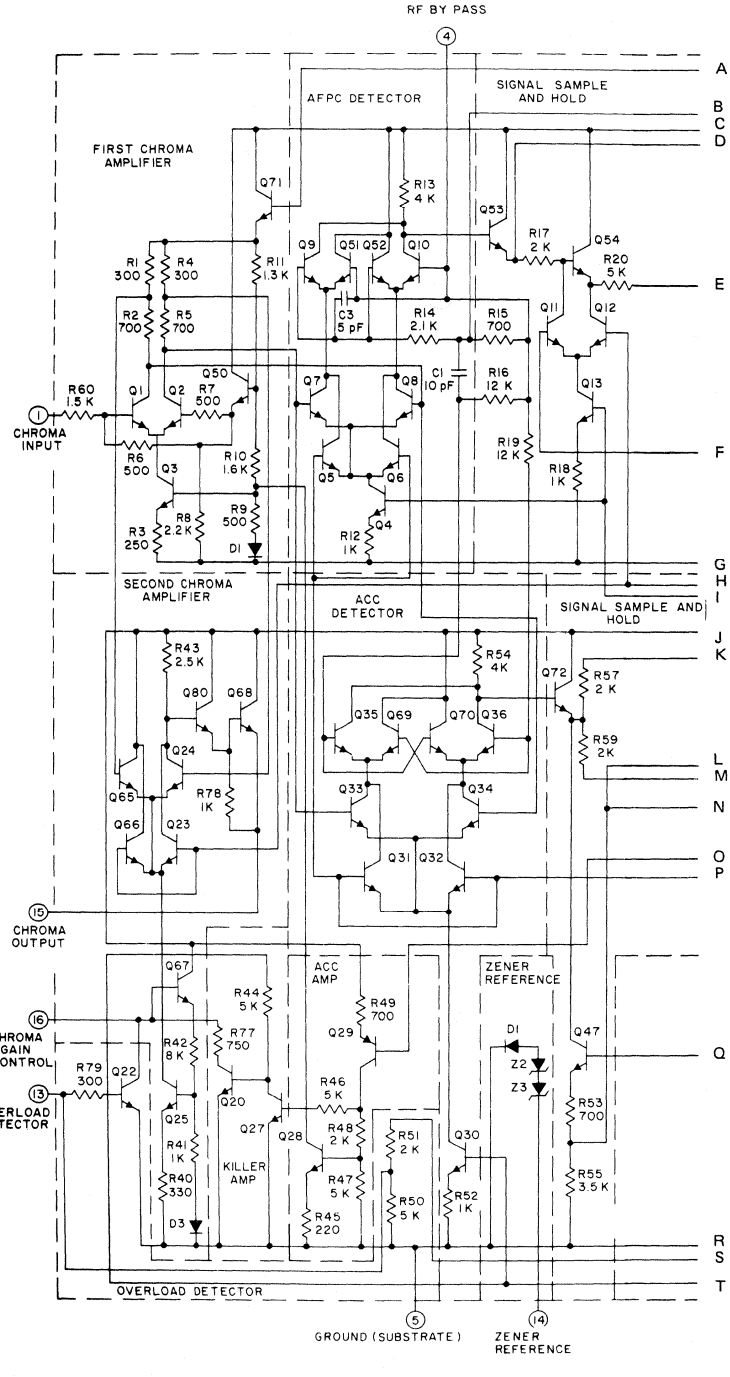


Fig. 2– Schematic diagram of the CA3126.

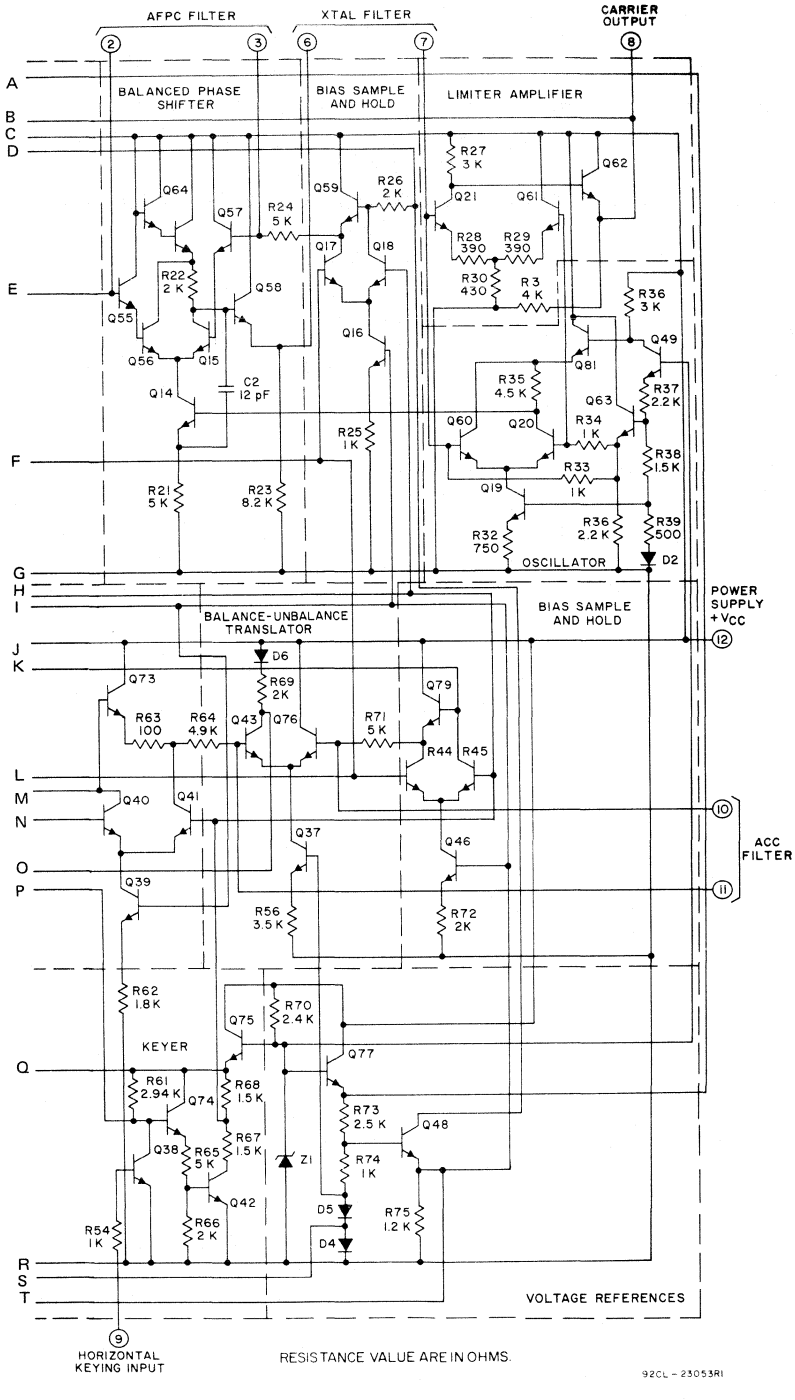


Fig. 2 — Schematic diagram of the CA3126 (cont'd).

CA3126

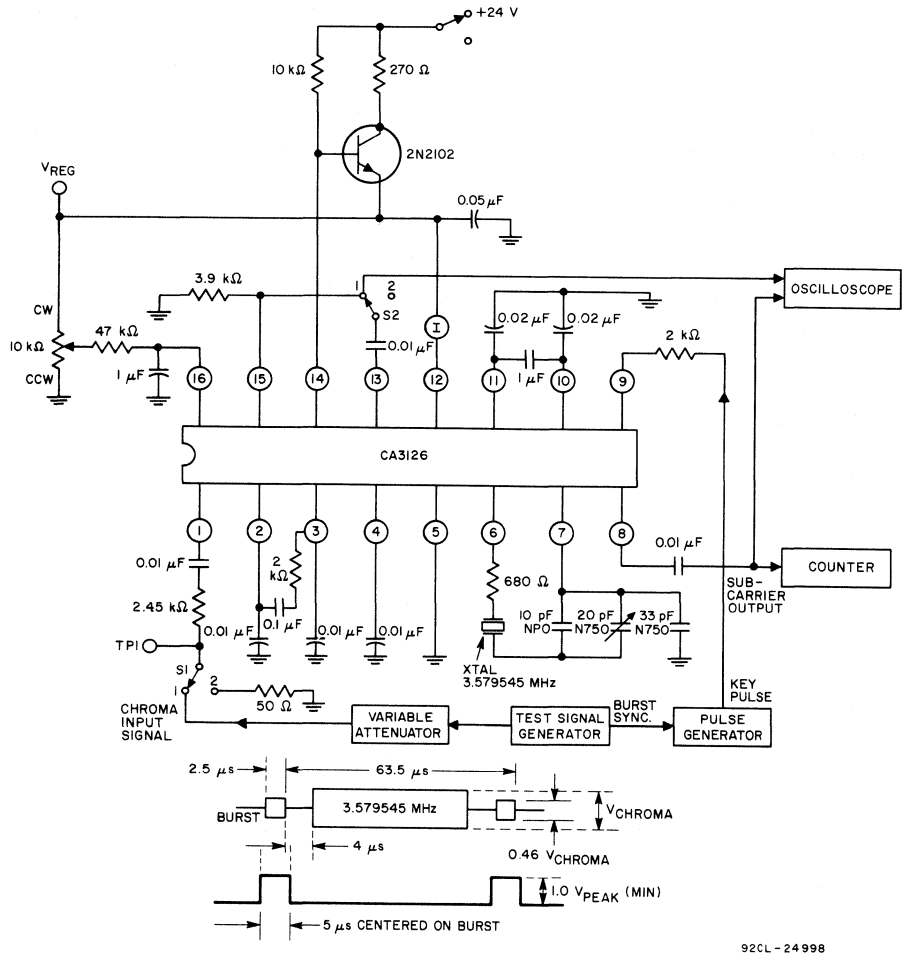


Fig. 3 — Test circuit for CA3126.

CIRCUIT DESCRIPTION

The following paragraphs briefly describe the circuit operation of the CA3126 (shown in Figs. 1 and 2). A detailed description of the operation of various portions of the CA3126 is given in ICAN-6247, "Application of the CA3126 Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450-ohm resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase-shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45- and −45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

APPLICATIONS INFORMATION

General Considerations

The block diagram shown in Fig. 1 is typical of the type of circuit used in the practical application of the CA3126. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450 ohms (or high source impedance) must be used at the chroma input, Terminal 1. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.
2. When the overload detector is used, a large resistor (nominally 47,000 ohms) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5-volt peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126 is shown in Fig. 4.

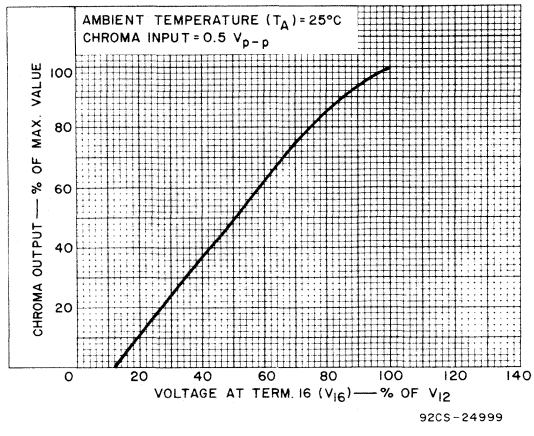


Fig. 4—Chroma gain control.

Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545-MHz crystal, a 680-ohm resistor, and a 10-pF capacitor connected in series across Terminals 6 and 7. A 33-pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher-order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Fig. 5. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40 Hz per degree.

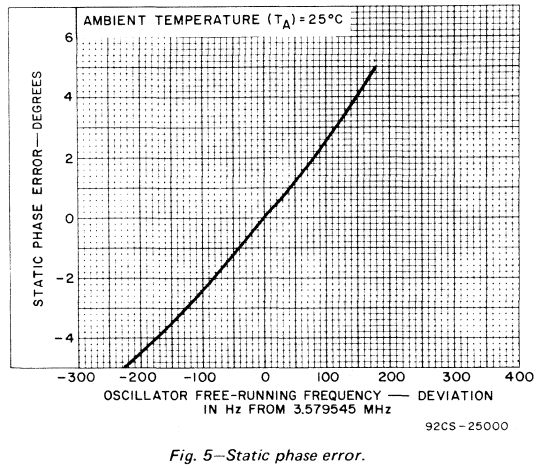


Fig. 5—Static phase error.

CA3126

Thermal Considerations

The circuit of the CA3126 is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figs. 6 and 7 show the oscillator- and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively. Both the oscillator- and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Fig. 8. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Fig. 3.

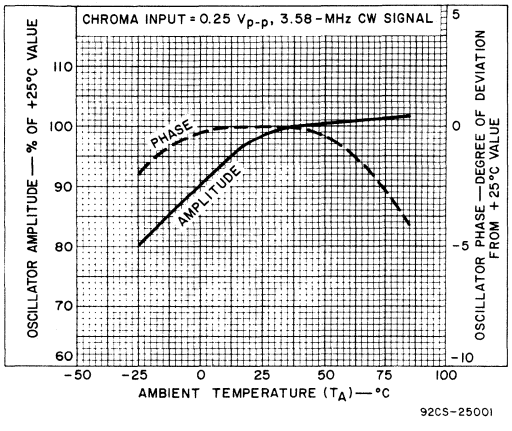


Fig. 6—Amplitude and phase variations of oscillator output vs. temperature.

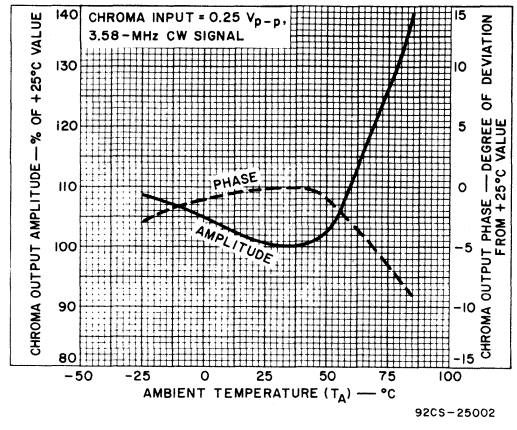


Fig. 7—Amplitude and phase variations of chroma output vs. temperature.

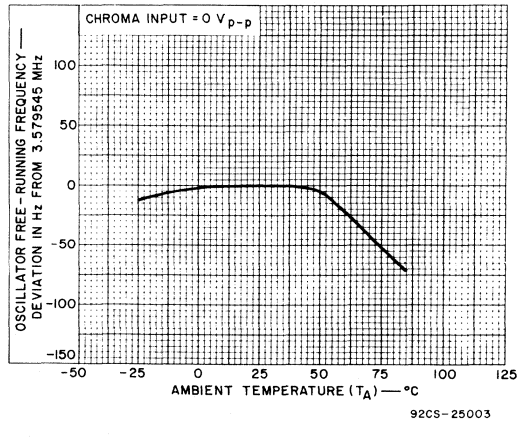


Fig. 8—Variation of oscillator free-running frequency vs. temperature.

CA3135

TV Luminance Processor

FEATURES:

- *Single gain control for luminance and chrominance channels*
- *100% dc restoration with "back porch" clamp*
- *Vertical blanking of both luminance and chrominance channels*
- *Automatic brightness limiting*
- *Operates from a 12-V supply*
- *Silicon-nitride passivated*
- *Platinum-silicide ohmic contacts*

The RCA-CA3135E monolithic silicon integrated circuit operates from a 12-V supply and is used as a low-level luminance processor in TV applications. It performs the function of video and chroma amplification and allows the gain of both channels to be adjusted with a single control voltage. The dc level of "black" is maintained by clamping the level of the "back porch" (back-level reference) of the blanking interval. This clamping feature provides for 100% dc restoration. Vertical blanking is applied to the luminance as well as to the chrominance channel so that vertical interval test signals (VITS) interference is eliminated. Automatic brightness limiting (ABL) is accomplished by gain reduction in the luminance and chrominance channels while maintaining black level.

The CA3135E is supplied in the 16-lead dual-in-line plastic package (E suffix).

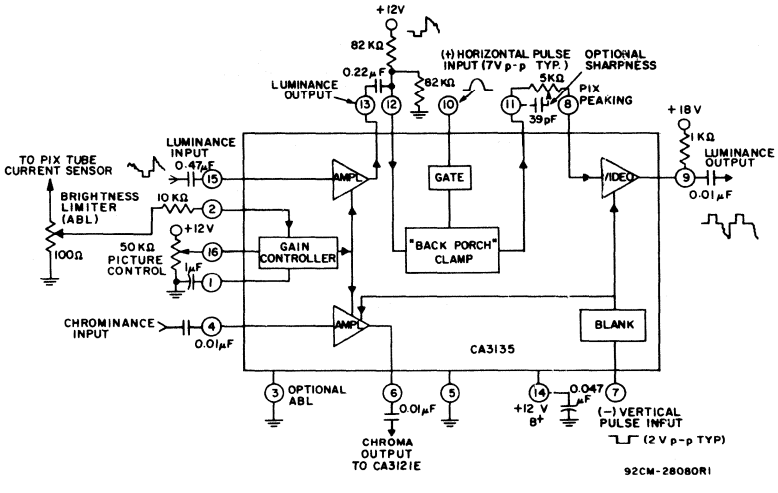


Fig. 1 – Block diagram.

File Number **1021**

CA3135

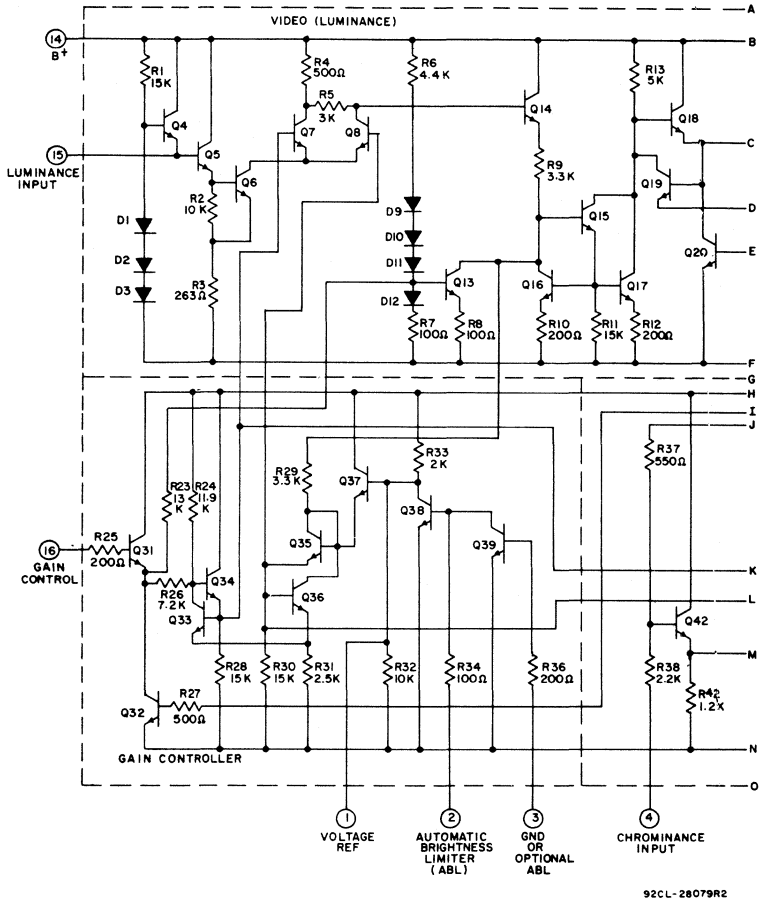


Fig. 2 – Schematic diagram (cont'd on next page).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- At terminal 9 . . . . . 28 V
- At terminal 14 . . . . . 15 V

DC SUPPLY CURRENT:
- At terminal 9 . . . . . 30 mA
- At terminal 14 . . . . . 50 mA

DEVICE DISSIPATION:
- Up to $T_A = 55^\circ C$ . . . . . 750 mW
- Above $T_A = 55^\circ C$ . . . . . Derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating . . . . . −40 to +85°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

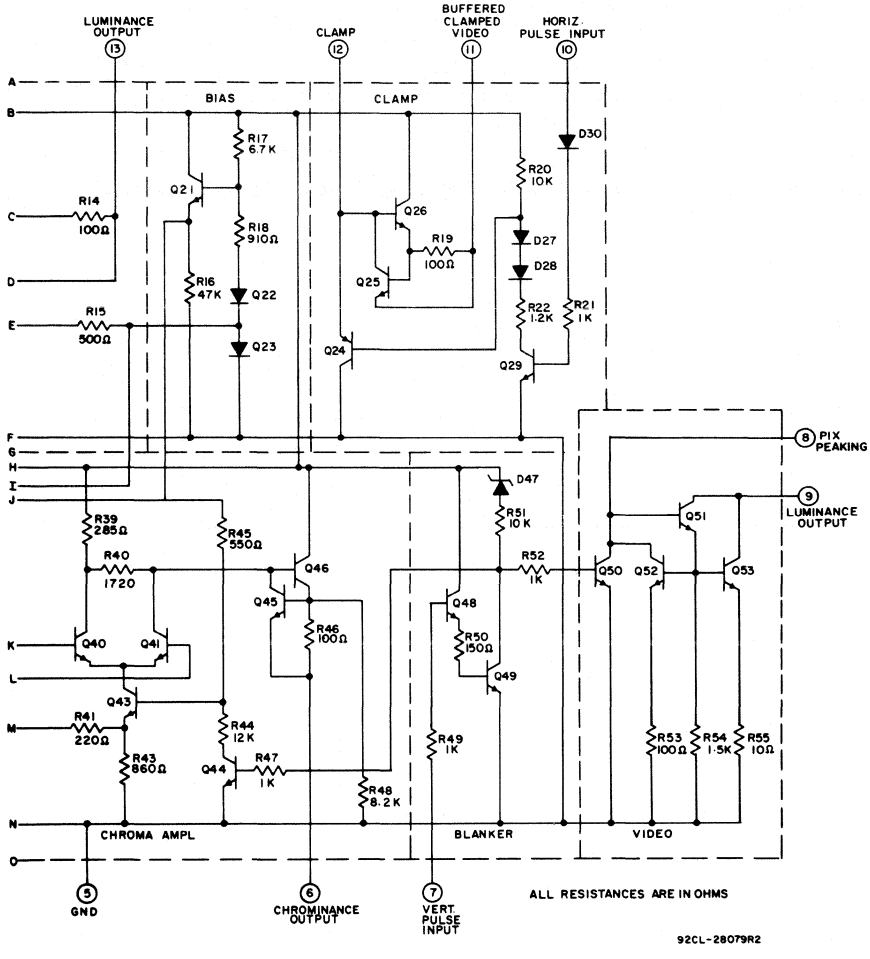
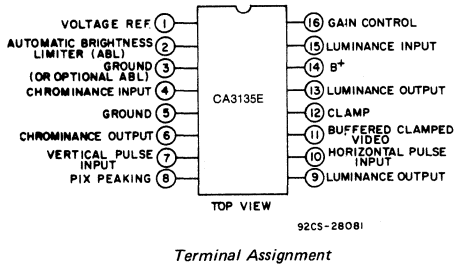


Fig. 2 - Schematic diagram (cont'd from previous page).



Terminal Assignment

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (See Fig. 3)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply-Voltage Drop	S2 = closed S3 = open S1,S4,S5,S6,S7,S8 = 1 Measure across 10 Ω resistor	130	215	300	mV
First-Stage Bias	S2,S3 = closed S1,S6 = 2 S4,S5,S7,S8 = 1 Measure term. 13 to ground	1.7	2.7	3.7	V
Chroma Bias	S2,S3 = closed S1,S4,S5,S7 = 1 S6,S8 = 2 Measure term. 6 to ground	7.3	8	9.1	V
Clamp Video Level	S2 = open Ref.= +12 V S3 = closed S1,S4,S5,S6,S7,S8 = 1 Measure across 82 kΩ	—	−8.7	—	V
Video Bias Level	S2 = open S3 = closed S1 = 1 S4,S5,S6,S7,S8 = 2 Measure across 1 kΩ	–	9	–	V
Luminance Blanking	S2 = open S3 = closed S1,S8 = 1 S4,S5,S6,S7 = 2 Measure across 1 kΩ	–	−50	–	mV
Chroma Blank	Setup same as above, measure term. 6	10.38	11.2	11.58	V
Chroma Input Impedance	Max. horizontal input = 10 V_{p-p} Max. vertical input = 2 V_{p-p}	–	2.5	–	kΩ
Chroma Output Impedance		–	150	–	Ω
Luminance Input Impedance		–	50	–	Ω
Luminance Output Impedance		–	10	–	kΩ

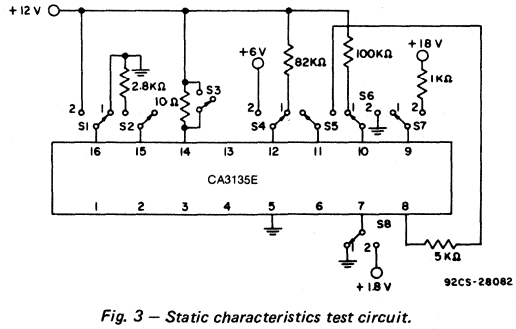


Fig. 3 – Static characteristics test circuit.

DYNAMIC ELECTICAL CHARACTERISTICS at T_A = 25°C (See Fig. 4)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Min. Video Gain	S1, S2 = 1; S3, S4 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 12 V	0.2	0.35	0.5	V_{RMS}
Max. Video Gain	S2 = 1; S1, S3, S4 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 0 V	1.6	2.1	2.6	V_{RMS}
Limited Video Gain	S2, S4 = 1, S1, S3 = 2 V_{IN} = 70 mV_{RMS}, f = 100 kHz, V_{16} = 0 V	–	0.3	–	V_{RMS}
Min. Chroma Gain	S1, S3 = 1; S2, S4 = 2; V_{16} = 12 V; chroma in = 530 mV_{RMS}, f = 3.58 MHz	–	0.095	–	V_{RMS}
Max. Chroma Gain	S3 = 1; S2 = 2, V_{16} = 0 V; chroma in; S1 = 2, S4 = 2 530 mV_{RMS}, f = 3.58 MHz	0.5	0.65	0.8	V_{RMS}
Video Freq. Response	S2 = 1, S1, S3, S4 = 2 V_{IN} = 70 mV_{RMS}; V_{16} = 0 V; f = 3.58 MHz	1	1.9	2.8	V_{RMS}
Chroma Phase Angle	S3 = 1; S2 = 2; V_{16} = 0 V; chroma in; S1 = 2, S4 = 2 530 mV_{RMS}, f = 3.58 MHz	12	19.5	27	Degrees
Chroma Gain with V^+ Variation	Vary V^+ from 10.8 V (REF.) to 13.2 V V_{16} = 50% of V^+; S1, S3 = 1 S2, S4 = 2	–	1.5	–	dB
Video Gain with V^+ Variation	Vary V^+ from 10.8 V (REF.) to 13.2 V V_{16} = 50% of V^+; S1, S2 = 1 S3, S4 = 2	–	1.5	–	dB

Typical max. luminance input before clipping (f = 100 kHz):

V_{16}	INPUT
+12 V	2.5 V_{p-p}
+6 V	0.75 V_{p-p}
0 V	0.45 V_{p-p}

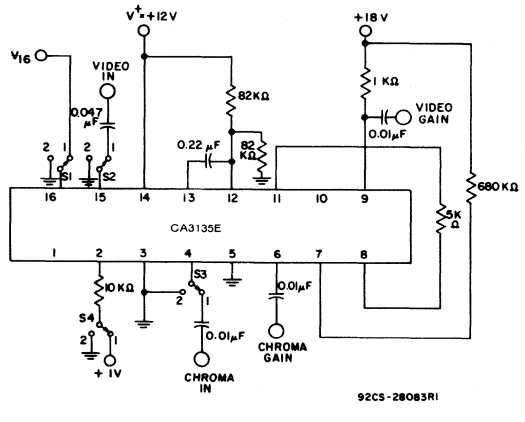


Fig. 4 – Dynamic characteristics test circuit.

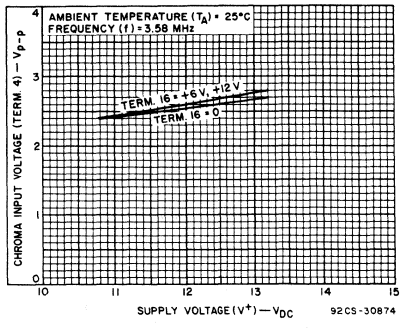


Fig. 5 — Typical chroma amplifier maximum linear voltage as a function of supply voltage.

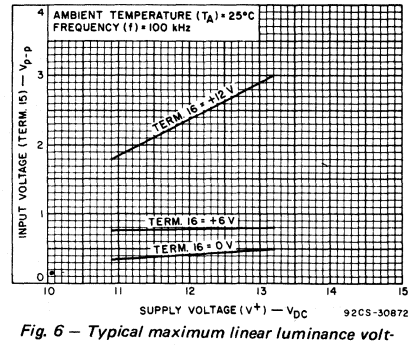


Fig. 6 — Typical maximum linear luminance voltage at terminal 15 as a function of supply voltage.

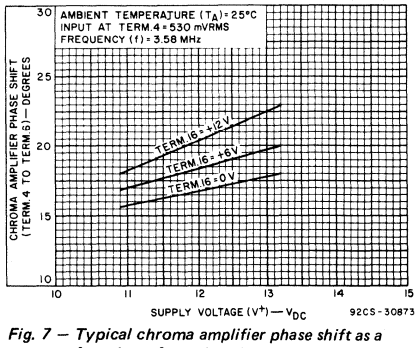


Fig. 7 — Typical chroma amplifier phase shift as a function of supply voltage.

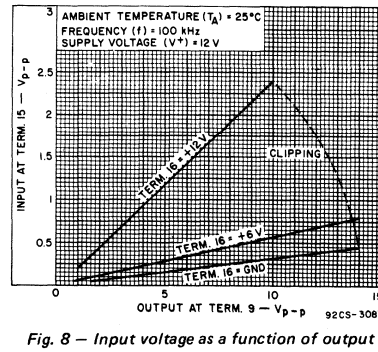


Fig. 8 — Input voltage as a function of output voltage.

CIRCUIT DESCRIPTION

(See fig. 2 for schematic diagram).

A video (luminance) signal from the receiver's "second detector" is coupled through a capacitor to term. 15 with sync-negative polarity. For purposes of the following amplifier, the level is clamped at the most negative point (sync tips) at the input (this is not the point at which the final "black"-level clamping, or dc restoration, is performed). The capacitor at term. 15 is charged on the most negative excursions of the signal by conduction of Q4. Positive signal excursions lift the emitter of Q4 into cutoff. The signal voltage on R3 develops a signal current in Q6. The current passes through Q7 and Q8, the division of current depends on the condition of the gain-adjusted signal voltage on the load resistors (discussed below). The gain-adjusted signal voltage on the load resistors is converted to current by the emitter-follower Q14 into R9, and fed into the current mirror, Q15, Q16, and Q17. The output of the current mirror develops a voltage across R13. The dc level is shifted by withdrawing some current from the input to the mirror. The fixed dc-level shifting current is developed in R6 and its diode string and is mirrored in Q13. Because the dc level is altered by adjustment of the gain, compensating dc currents that depend on these adjustments are fed into the mirrors through

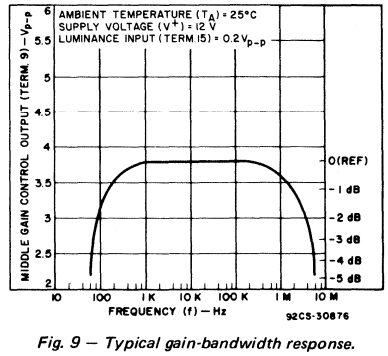


Fig. 9 — Typical gain-bandwidth response.

R13 and R29. The compensations are arranged so that, as gain is varied, the dc level of "black" is approximately constant at the output term. 13. The output is driven by emitter follower Q18, which has a short-circuit pulldown protection circuit, R14 and Q19. A constant-current source Q20 loads the emitter-follower to prevent distortion in the emitter-follower that may result from using a resistive load. The constant current is derived by mirroring the current in the diode D23. The resistor R15 prevents serious interaction with another current source mirrored from this point in case Q20 saturates.

The video output signal at term. 13 is coupled by a capacitor to term. 12. The polarity has not been inverted by the first amplifier, and sync is in the negative direction at this point. Black-level clamping is accomplished by application of a flyback pulse to term. 10. Between pulse peaks, Q29 is not conducting, and the base of Q24 goes up to the supply voltage so that term. 12 can be at any voltage between ground and the supply. While the flyback pulse is positive, that is during the blanking interval, the base of Q24 is held at about 2.8 volts. The most positive signal excursion during that time will cause Q24 to conduct with the result that the capacitor feeding term. 12 is charged until the most positive point of the signal is just at the conduction point, about 3.5 volts. The most positive part of the signal *during blanking* is the "back porch" or black-level reference. During trace time, the signal swings more positive, but the dc level of black is preserved regardless of the levels of sync or video signals. Term. 12 is a high-impedance point, and the emitter-follower Q26 is used to bring the signal out to term.11.

The signal voltage at term. 11 is directly coupled through a resistor to term. 8, generating a current in term. 8. This current is amplified 10 times by the current mirror Q51, Q52, and Q53. Blanking during the vertical retrace interval is accomplished at Q50 via term. 7. Term. 7 is normally high enough to keep Q49 in saturation. A negative pulse from the vertical circuit cuts Q49 off, allowing some of the current through R51 to saturate Q50. When Q50 sinks the term. 8 input current, there is no output from term. 9 — as if the signal were blacker-than-black. The output current from term. 9 is used to drive the receiver's RGB matrix and the amplifiers that drive the picture tube.

The chrominance signal is taken from the first chroma amplifier following the automatic chroma control (ACC) and coupled through a capacitor to term. 4. The signal is attenuated by R38 and R37 and applied to an emitter-follower amplifier which drives the emitter of Q43. The current is steered through Q40 and Q41 depending on the gain-control conditions to the load resistors. An emitter-follower Q46 feeds term. 6, and R46 and Q45 provide short-circuit protection. The chroma amplifier is also blanked via the input at term. 7. The negative pulse at term. 7 allows the current through R51 to feed the base of Q44 (as well as the base of the video blanker, Q50). When Q44 saturates, the current is cut off in Q43 to disable the amplifier.

The combined gain control for the video and chroma sections is operated by varying the voltage on term. 16 between ground and the positive supply. Term. 16 has an emitter-follower Q31 loaded by a current source Q32. The voltage on term. 16 then determines whether the flow of current in R31 goes through Q36 or through Q33 to the resistors R24 and R26. The current on the Q33 side, a portion of the total current, is varied linearly by the control voltage. The gain-control amplifiers are slaves which follow the linear current control. The transistors Q34 and Q35 are driven as Darlington stages to reduce base-current effects in the control circuit. The normal gain-control function causes a change in the voltage on the base of Q34 with respect to the reference voltage at the base of Q35. The gain can also be changed by altering this reference voltage. This change in reference voltage is also used for "brightness limiting". The picture-tube current is sensed, and, when it exceeds some predetermined level, a voltage applied to term. 2 turns Q38 ON to reduce the reference voltage, thereby reducing the gain. Under these conditions, there is a closed feedback loop; the gain is set at a point such that the picture-tube current is just sufficient to cause a little conduction in Q38.

CA3154

TV Sync/AGC/Horizontal Signal Processor

FEATURES:

- *Horizontal oscillator with AFC*
- *Sync separator with noise immunity*
- *Strobed AGC system*
- *IF AGC output*
- *Delayed outputs for forward or reverse AGC tuners*
- *Internal noise threshold*
- *High-impedance video input*
- *Choice of dual external time constants for sync separator noise immunity*
- *RF AGC delay externally controlled*
- *Output short-circuit protection*

The RCA-CA3154E is a monolithic integrated circuit TV signal processor designed for use in color or monochrome receivers. Circuit functions include a horizontal oscillator with AFC, a sync separator, and a key AGC system. The AGC system provides output signals for IF (reverse) and tuner (forward and/or reverse). The wide frequency-range horizontal oscillator has high stability at 503.3 kHz. When the CA3154E is used in conjunction with the CA3157 horizontal/vertical countdown circuit, the need fc horizontal and vertical hold controls is eliminated.

The CA3154E is supplied in a 16-lead dual-in-line plasti package.

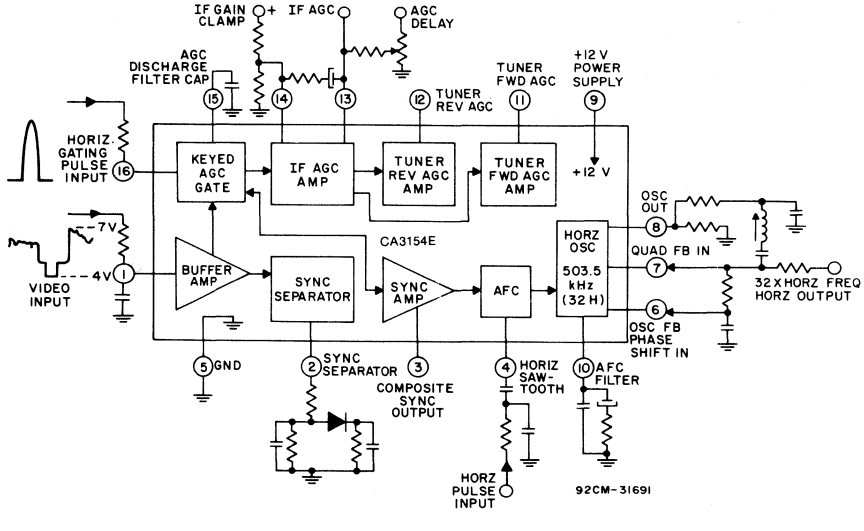


Fig. 1 — Functional block diagram of CA3154E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE . . . . . 15 V

DEVICE DISSIPATION:

Up to $T_A = 55^\circ C$ . . . . . 750 mW

Above $T_A = 55^\circ C$ . . . . . derate linearly 7.9 mW/°C

AMBIENT-TEMPERATURE RANGE:

Operating . . . . . −40 to +85°C

Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During soldering):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

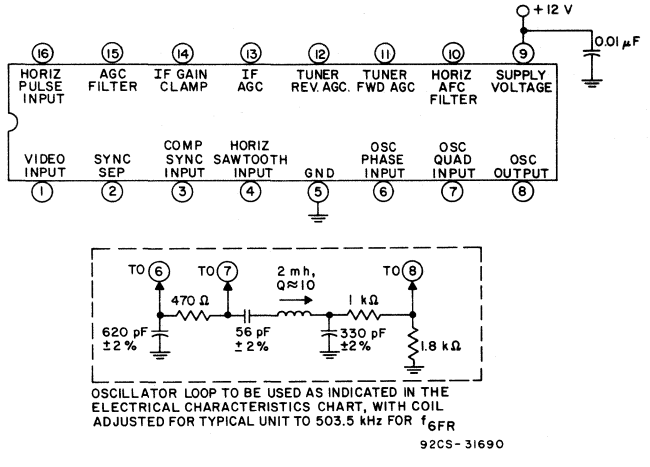


Fig. 2 — Electrical characteristics test circuit.

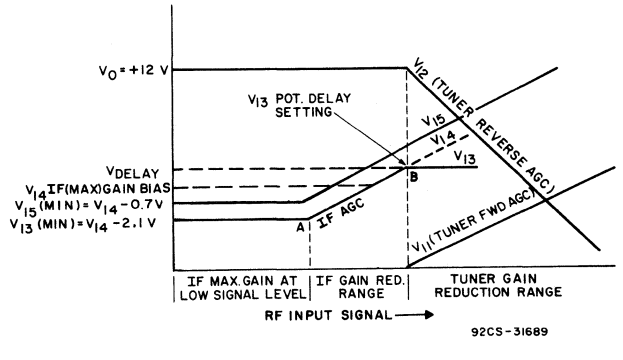


Fig. 3 — Typical operation of AGC circuits using the CA3154E.

CA3154

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, terminal 5 to Gnd, and terminal 9 to +12 V unless otherwise specified.*

CHARACTERISTIC	TEST CONDITIONS Terminals Connected As Shown Below	LIMITS Min.	Typ.	Max.	UNITS
Power Supply Current, I_9	Measure (9)	10	–	22	mA
Video Inverter Voltage, V_2	(1) to +14V, (2) 12 kΩ to Gnd, (3) 27 kΩ to Gnd, Measure (2)	5.2	–	6.4	V
Sync Separator High Output Voltage, V_{3H}	Same as above	10.7	–	–	V
Sync Separator Low Output Voltage, V_{3L}	(1) to +4V, (3) 27 kΩ to Gnd, Measure (3)	–	–	1.3	V
Video Noise Clamp Voltage, V_3 Clamp	(1) to +3.1V, (3) 27 kΩ to Gnd, Measure (3)	10.7	–	–	V
AGC Discharge Current, I_{15} Discharge	(1) to +4.4V, (2) 10 kΩ to Gnd, (15) 470 Ω to +6V, (16) 27 kΩ to 12V, Measure (15)	0.6	–	1.4	mA
AGC Charge Current, I_{15} Charge	(1) to +3.45V, otherwise same as above	–2.1	–	–4.8	mA
AGC Comparator Leakage, I_{15} Leakage	(1) to +3.45V, (2) 10 kΩ to Gnd, (15) 4.7 kΩ to +6V, Measure (15)	–20	–	+20	μA
AGC Threshold Voltage, V_{1TH}	Adj. (1) for I_{15} = 0 ±0.1 mA, (2) 10 kΩ to Gnd, (15) 4.7 kΩ to +6V, (16) 27 kΩ to +12V, Measure (1)	3.8	4	4.3	V
Minimum IF AGC, V_{13L}	(11) 10 kΩ to Gnd, (12) 10 kΩ to +12V, (13) 22 kΩ to +5V, (14) 1 kΩ to +2.95V, (16) 1 kΩ to +2.2V, Measure (13)	0.75	–	1.25	V
Forward Tuner AGC Leakage Current, I_{11} Leakage	(11) 10 kΩ to Gnd, (12) 10 kΩ to 12V, (13) 2.2 kΩ to +5V, (14) 1 kΩ to +2.95V, (15) 1kΩ to +5.3V, Measure (11)	–20	–	+20	μA
Reverse Tuner AGC Leakage, I_{12} Leakage	Same as above, but Measure (12)	–10	–	+10	μA
IF AGC High Voltage, V_{13H}	Same as above, but Measure (13)	3.65	–	4.15	V
Forward Tuner AGC Low Voltage, V_{11L}	(11) 3.6 kΩ to Gnd, (12) 3.16 kΩ to +12V, (13) 2.2 kΩ to +5V, (14) 1 kΩ to +2.95V, (15) 1 kΩ to +7.9V, Measure (11)	0.8	–	3.2	V
Reverse Tuner AGC Low Voltage, V_{12L}	Same as above, but Measure (12)	1.65	–	3.25	V
Maximum IF AGC Voltage, V_{13H}	(11) 10 kΩ to Gnd, (12) 10 kΩ to +12V, (13) 2.2 kΩ to +5V, (14) 1 kΩ to +2.95V, (15) 1 kΩ to +7.9V, Measure (13)	4.85	–	5.2	V

(continued)

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C, terminal 5 to Gnd, and terminal 9 to +12 V unless otherwise specified.*

CHARACTERISTIC	TEST CONDITIONS Terminals Connected As Shown Below	LIMITS Min.	Typ.	Max.	UNITS
Phase Detector Leakage Current, I_{10L}	(2) 10 kΩ to Gnd, (3) to Gnd, (4) 5 kΩ to +3.8V, (10) 10 kΩ to +6V, Limit Gnd at (3) to 10 sec., Measure 10	−5	–	+5	μA
Phase Detector Bias Voltage, V_4		2.65	–	3.1	V
Oscillator Output Voltage, V_6	Connect osc-loop shown in test circuit to (6),(7),(8); (3) to Gnd for 10 sec. max., Measure (6)	0.6	–	1.6	V_{p-p}
Oscillator Free-Running Frequency f_{6FR}	Same as above	475	–	535	kHz
Oscillator Frequency High, f_{6H}	Connect osc-CKT shown in test CKT to (10),(7),(8); (2) 10 kΩ to Gnd, (4) 5 kΩ to +18V, Measure (6)	520	–	–	kHz
Oscillator Frequency Low, f_{6L}	Same as above except (4) 5 kΩ to +3.8 V	–	–	485	kHz
Sync Separator Short Circuit, I_3 Max.	(3) 10 Ω to Gnd 10 sec. max.	–	–	40	mA
Oscillator Output Short Circuit, I_8 Max.	(8) 10 Ω to Gnd for 10 sec. max. (3) 10 Ω to Gnd for 10 sec. max.	–	–	130	mA

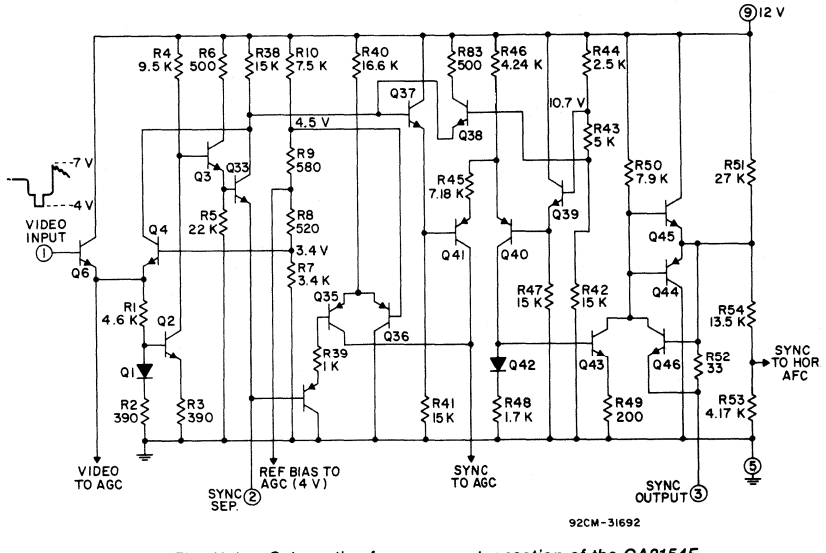


Fig. 4(a) — Schematic of sync separator section of the CA3154E.

CA3154

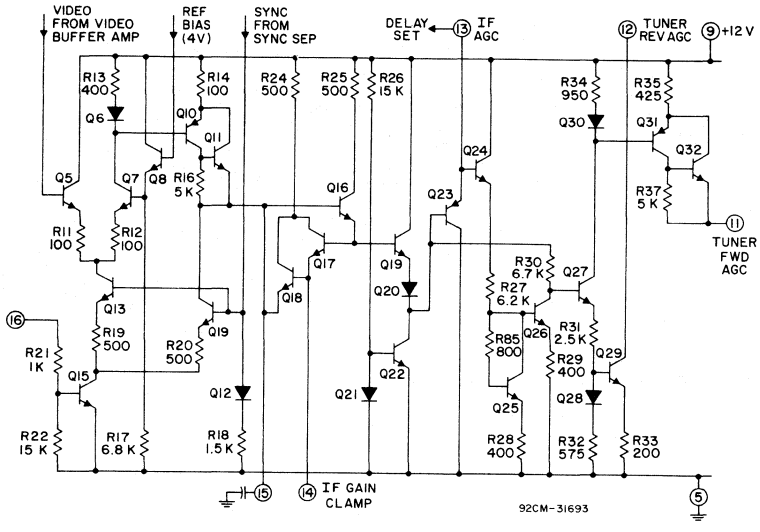


Fig. 4(b) — Schematic of AGC section of the CA3154E.

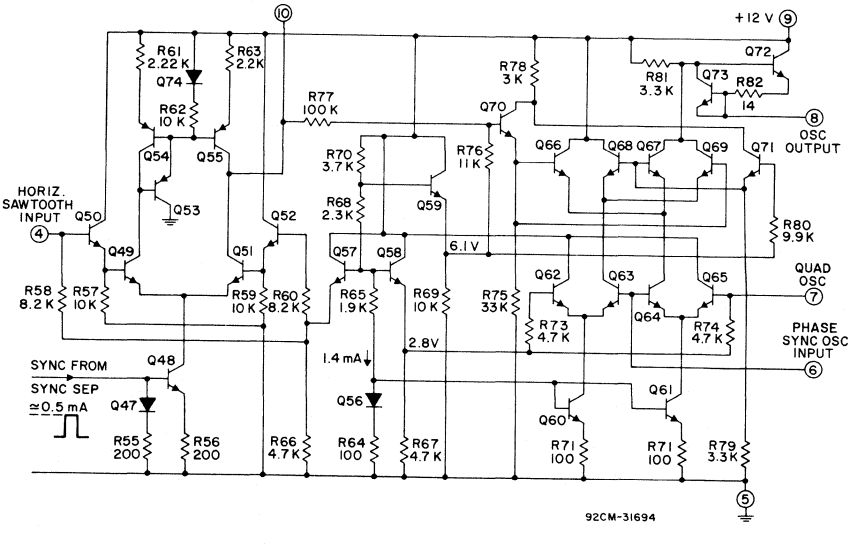


Fig. 4(c) — Schematic of AFC-oscillator section of the CA3154E.

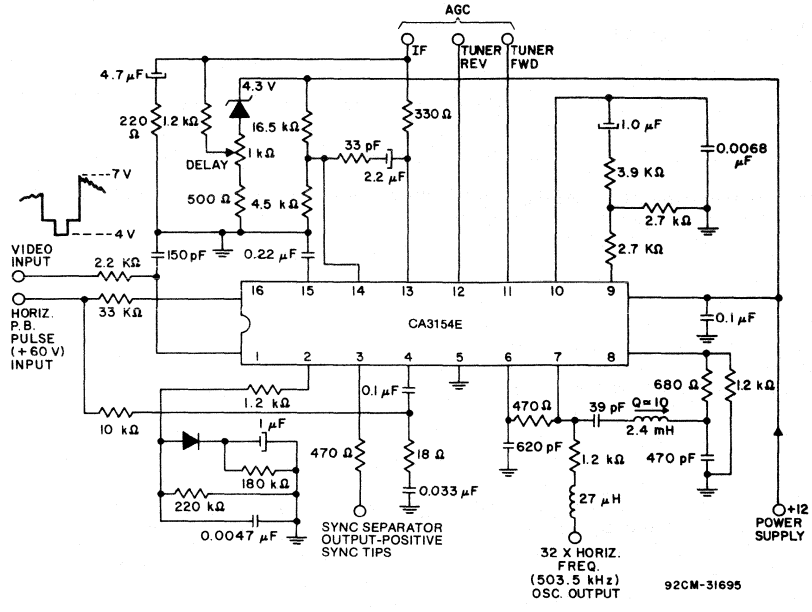


Fig. 5 — Typical application of the CA3154E.

CA3194

Single-Chip PAL Luminance/Chroma Processor

System Features:

- *All PAL luminance and chrominance processing circuitry on a single chip in a 24-lead plastic package*
- *Phase-locked subcarrier regeneration utilizing sample-and-hold*
- *DC controls for brightness, contrast, and color-saturation functions*
- *Input for average beam-current limiting*
- *Contrast control having excellent tracking of luma and chroma channels*
- *Low-impedance RGB outputs with excellent tracking for direct coupling to video driver circuitry*

The RCA CA3194E* is a silicon monolithic integrated circuit designed to perform all of the signal processing functions for both the chroma and luminance signals of PAL color television receivers.

This circuit performs all the functions needed between the video detector and the video RGB output stages. DC contrast, brightness, and saturation controls and average beam limiting functions are included. The RGB buffer stages are capable of delivering 5 mA of current into the video output stages.

The CA3194E is supplied in the 24-lead dual-in-line plastic package.

*Formerly RCA Dev. No. TA10313.

Circuit Description (See Figs. 1 and 6.)

The chroma signal is externally separated from the vide signal by means of a bandpass or high-pass filter an applied to pin 4. The burst is separated in the first chrom stage and applied to the synchronous detector whic provides information to sample-and-hold circuits for APC (phase-locked loop), ACC (automatic chroma gain control and identification and killing. The 4.43-MHz cryst oscillator is phase-locked to the burst and provides 0° an 90° (via an external phase shifter) carriers to the chrom demodulators. The burst and chroma amplitude at th output of the first chroma amplifier is kept constant by th automatic gain control.

The second chroma stage provides saturation control (pi 3) which tracks the contrast control in the luminanc channel. This stage is also used for color killing.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE AND CURRENT:

Pin 12 Voltage Range ..... 11 Min. to 13 Max. V

Pin 12 Current Range ..... 45 Typ. to 60 Max. mA

DEVICE DISSIPATION:

Up to T_A=+55°C ..... 825 mW

Above T_A=+55°C, ... Derate linearly at 8.7 mW/°C

θ_{JC} Max.=115°C/W, T_J Max.=150°C

AMBIENT TEMPERATURE RANGE:

Operating ..... −40 to +85°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

File Number **1270**

TERMINAL VOLTAGE AND CURRENT RATINGS

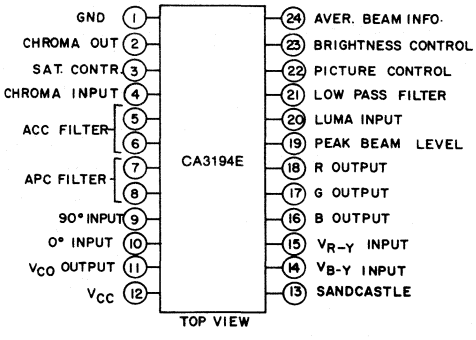
Terminal	Voltage* - V		Current - mA	
	Min.	Max.	I_{IN}	I_{OUT}
1	—	—	—	—
2	0	13	0	30
3	0	8	10	—
4	0	5	—	—
5	0	Note	—	—
6	—	—	0.1	0.5
7	0	Note	—	—
8	0	Note	—	—
9	0	8	—	—
10	0	8	—	0.7
11	0	13	—	10
12	0	13	—	—
13	0	12	—	—
14	0	5	—	1.5
15	0	5	—	1.5
16	0	13	—	10
17	0	13	—	10
18	0	13	—	10
19	0	Note	—	—
20	0	5	—	—
21	0	Note	—	—
22	0	8	—	—
23	0	5	—	—
24	0	12	—	—

NOTE:
The maximum should not exceed the V_{CC} voltage.
*Voltage with respect to Terminal 1 for V_{CC} (Terminal 12) of 12 V ± 10%.

A buffer stage drives the external PAL delay line. The separated U and V signals are applied to pins 14 and 15, respectively, and demodulated. A standard G-Y matrix is included on the chip.

The luminance signal passes through the subcarrier trap and through the luminance delay line and enters the chip at pin 20. Contrast and brightness control is provided before the luminance signal is combined with the color difference signals in the Y matrix. Average and peak beam limiting circuits are controlled from pins 24 and 19.

TERMINAL ASSIGNMENT



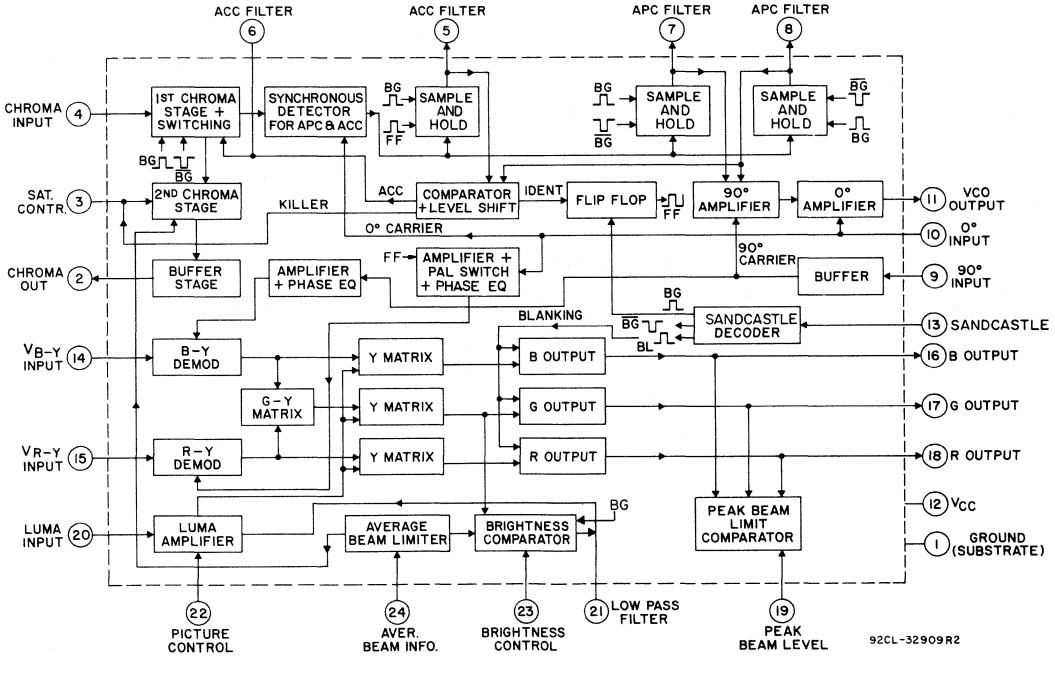


Fig. 1 - Block diagram.

CA3194

ELECTRICAL CHARACTERISTICS at T_A=25° C, V_{CC}=12 V, V_S=2.85 V V_C=2.85 V, V_{AB}=V_{PB}=V_{CC}, V_B adjusted for V18=6.3 V, C_X adjusted for F_{OSC}=4.43361875 MHz, Sandcastle: V_{BG}=8.0 V, V_{BLANK}=3.5 V-Burst Gate centered on Burst. These conditions exist except as otherwise noted. See Fig. 5 for test circuit.

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUE	UNITS
LUMINANCE SECTION			
Input Impedance-Term. 20		6 5	kΩ pF
Luminance Channel Input Voltage	Luma Input Signal=30% Sync	0.5	V_{p-p}
Bandwidth of Luminance Channel	Luma Input Signal: 0.5 V_{p-p} (30% Sync) modulated CW Adj. modulation frequency for −3 dB at color outputs	8	MHz
Brightness Control Range-Term. 23	For control characteristics, See Fig. A	0 - 3.5	V dc
Output Black Level: Range Offset	Luma Input Signal: 0.5 V_{p-p} (30% Sync) V_B 0 - 5 V Measured at Pin 18 black level. See Fig. A.	 5.9 - 9.7 0.6 Max.	V dc
Contrast Control Range-Term. 22	Luminance input: 0.5 V_{p-p} (30% Sync), for control characteristics. See Fig. B.	0 - 5	V dc
Luminance Gain Control Range	Luminance Input: 0.5 V_{p-p} (30% Sync), V_C=0.5 - 5 V measure Pin 18 black level to maximum white level. See Fig. C.	32	dB
RGB Output Swing	Luminance Input: 0.5 V_{p-p} (30% Sync), V_C=5 V, read black level to peak white. See Fig. D.	4	V_{p-p}
CHROMINANCE SECTION			
Input Impedance-Term. 4	See Fig. E.	4.5 5	kΩ pF
Chroma Channel Input Voltage	Chroma	220	mV_{p-p}
	Burst	100	mV_{p-p}
ACC Range		+6 - −20	dB
Input Burst Level for Kill	Adjust chroma input Pin 2 ≤ 25 mV_{p-p}. Measure Burst level at Pin 4.	10*	mV_{p-p}
Contrast Control Chroma/Luma Tracking	Chroma Input: Burst=100 mV_{p-p} Chroma=220 mV_{p-p} Luminance Input: 0.35 V_{p-p} V_S adjusted for Chroma at Pin 18=2 V_{p-p} V_C is adjusted for luminance at Pin 18=2 V_{p-p}. V_C is again adjusted for luminance of +6 and −9 dB. Then read chroma percentage difference. See Fig. F.	±5	%
Saturation Control Range-Term. 3	For control characteristic, see Fig. G.	0 - 5	V dc
Max. Chroma Output Voltage-Term. 2	Chroma Input: Burst=100 mV_{p-p} Chroma=220 mV_{p-p}. Adjust V_C and V_S for max. Pin 2 output.	2.5	V_{p-p}

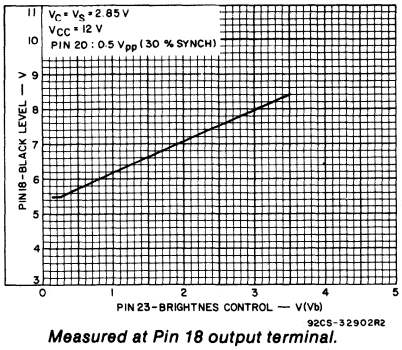
*If a different value is desired, see the Threshold Adjustment Circuit of Fig. 3.

CHARACTERISTIC	TEST CONDITIONS	TYPICAL VALUE	UNITS
OSCILLATOR SECTION			
Pull-In Range	Chroma Input: Burst=100 mV_{p-p} Chroma=220 mV_{p-p}. Adjust C_X for HI/LO f_{OSC} without Chroma signal. Apply signal to lock.	±500	Hz
Static Phase Error		2	DEG/100 Hz
DEMODULATOR SECTION			
R-Y Demodulator Conversion Gain	Chroma Input: Burst=100 mV Chroma=220 mV_{p-p}, Vϕ. Adjust V_C for V18=1 V. Read V_{15}. Calculate V18/V15.	10	Ratio
B-Y Demodulator Conversion Gain	Chroma Input: Burst=100 mV_{p-p}, Uϕ. Read V16 and V14. Calculate V/16/V14. V_C remains as for R-Y gain	18	Ratio
G-Y/B-Y Matrix Ratio	Chroma Input: Burst=100 mV_{p-p}, Chroma=220 mV_{p-p}, Uϕ read V17 and V16. Calculate V17/16. V_C remains as above.	0.2	Ratio
G-Y/R-Y Matrix Ratio	Chroma Input: Burst=100 mV_{p-p} Chroma=220 mV_{p-p}, Vϕ. Read V17 and V18. Calculate V17/18. V_C remains as above.	0.5	Ratio
Sub-Carrier and Harmonic Content at Outputs	No Chroma or Luma Input. Read residual carrier at outputs.	30	mV_{p-p}
SANDCASTLE PULSE			
Horizontal and Vertical Blanking Pedestal		2 - 5	V
Burst Gate Pulse		6.5 - V_{CC}	V

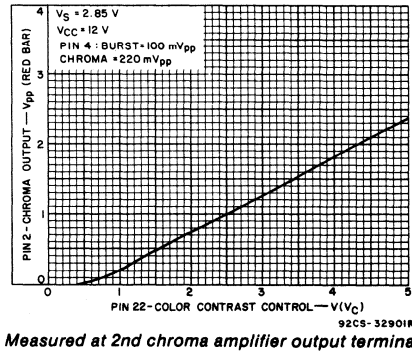
NOTE:
Use of the circuit of Fig. 4 is suggested to prevent increased color saturation at low level RF signals.
The reference voltage can be adjusted by changing the values of the voltage divider.

TYPICAL CHARACTERISTICS (Refer to Fig. 5 for Test Circuit)

A. BRIGHTNESS CONTROL (V_B)



Measured at Pin 18 output terminal.

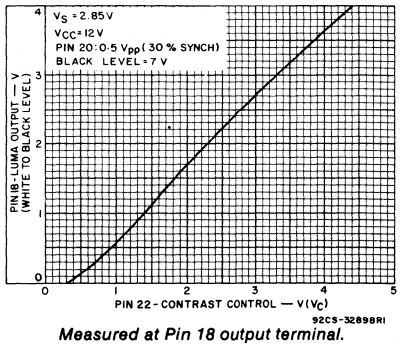


Measured at 2nd chroma amplifier output terminal.

CA3194

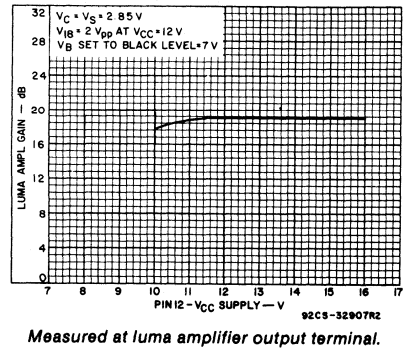
TYPICAL CHARACTERISTICS (Cont'd)

B. CONTRAST CONTROL (V_C)



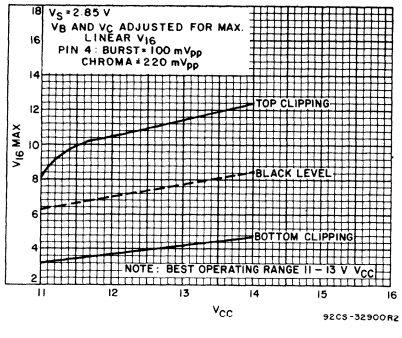
Measured at Pin 18 output terminal.

C. LUMA GAIN VS. SUPPLY VOLTAGE (V_{CC})

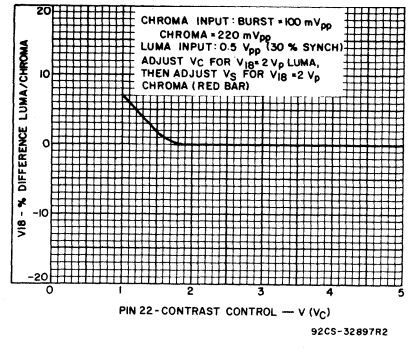


Measured at luma amplifier output terminal.

D. LINEAR OPERATING RANGE AS A FUNCTION OF V_{CC}

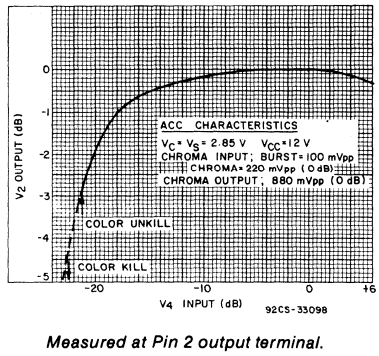


Measured at Pin 16 output terminal.

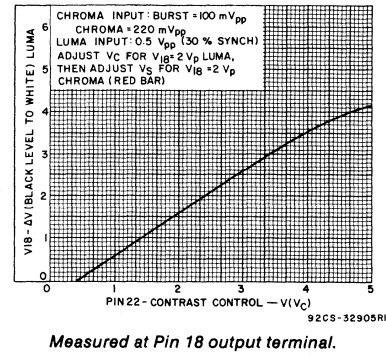


Measured at Pin 18 output terminal.

E. ACC CHARACTERISTICS



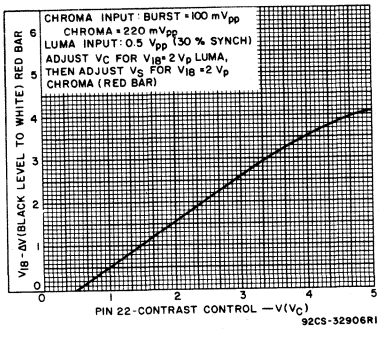
Measured at Pin 2 output terminal.



Measured at Pin 18 output terminal.

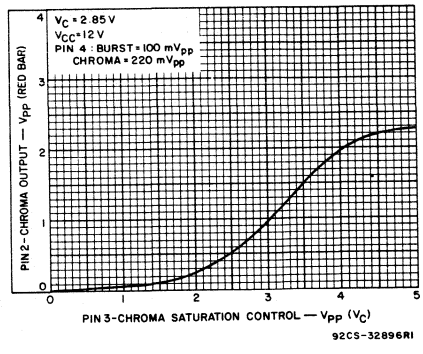
TYPICAL CHARACTERISTICS (Cont'd)

F. LUMA/CHROMA TRACKING WITH CONTRAST CONTROL



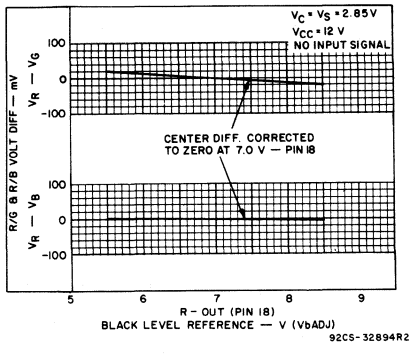
Measured at Pin 18 output terminal.

G. SATURATION CONTROL (V_S)



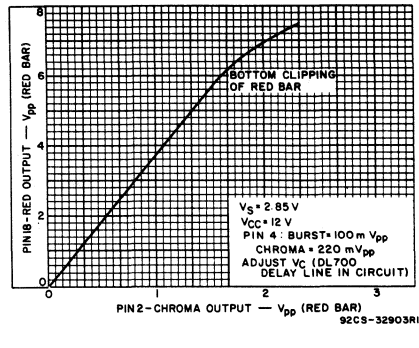
Measured at chroma amplifier output terminal Pin 2.

H. DIFFERENTIAL BLACK-LEVEL TRACKING



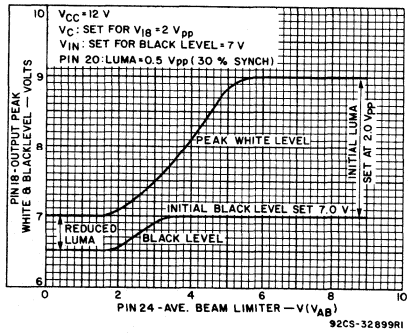
Measured at RGB output terminals.

I. PIN 18 OUTPUT VS. PIN 2 VOLTAGE

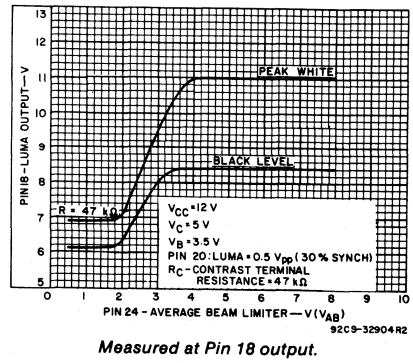


Measured at chroma output terminals and R output.

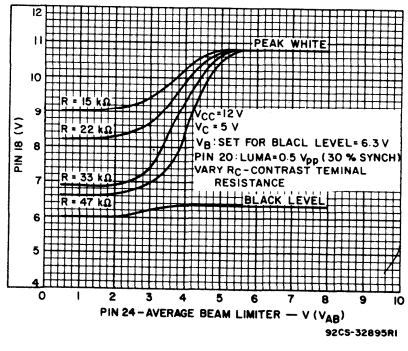
J. AVERAGE BEAM LIMITER (V_{AB})



Measured at Pin 18 output.



Measured at Pin 18 output.



Measured at Pin 18 output.

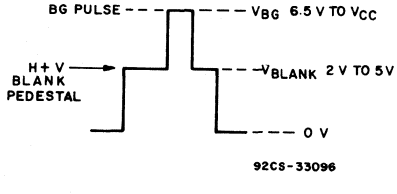


Fig. 2 - Sandcastle input waveform.

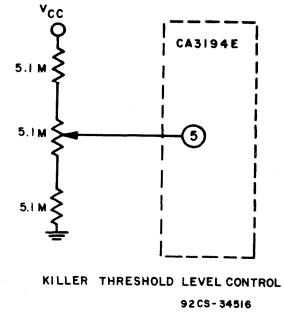


Fig. 3 - Killer-threshold level control.

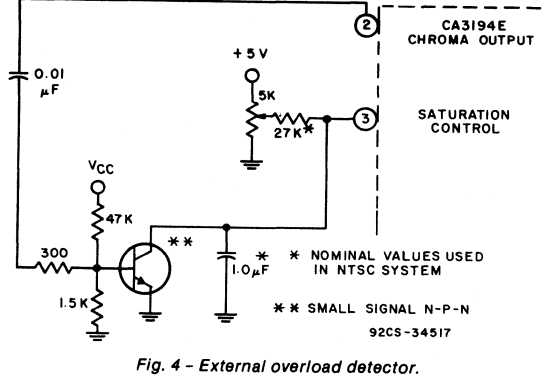


Fig. 4 - External overload detector.

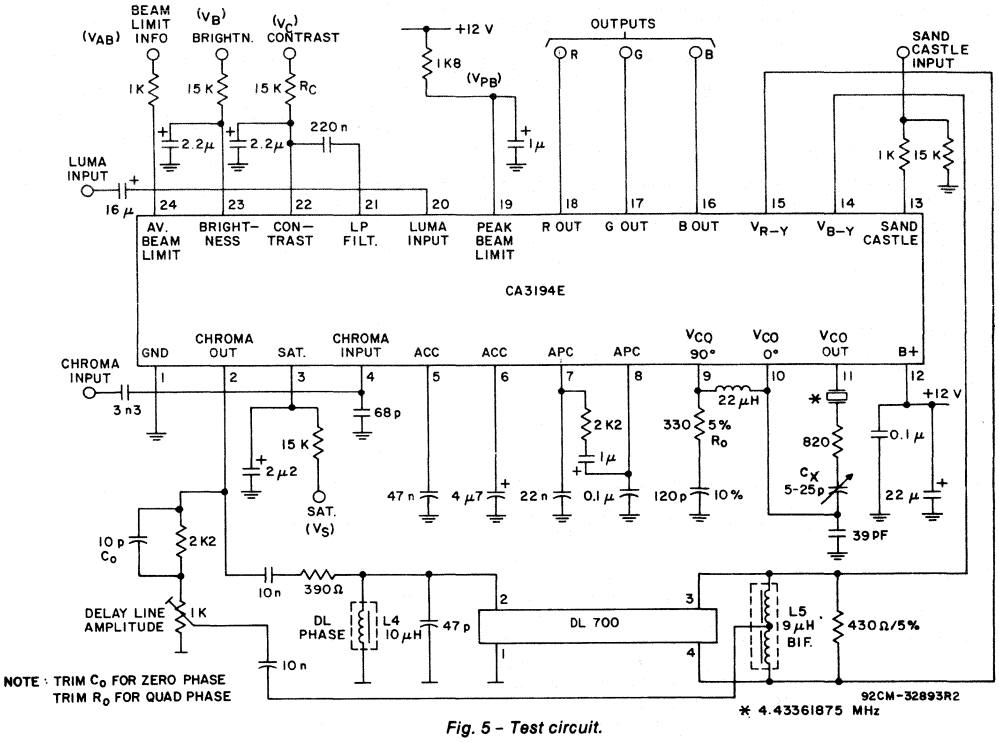


Fig. 5 - Test circuit.

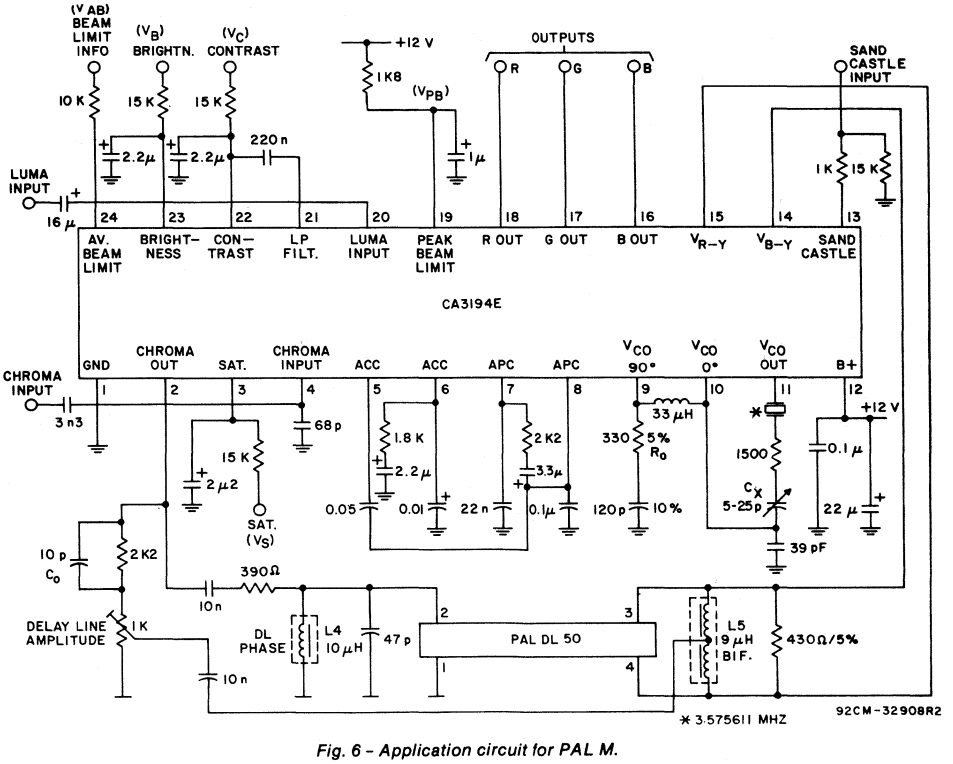


Fig. 6 - Application circuit for PAL M.

CA3210, CA3223

TV Horizontal/Vertical Countdown Digital Sync System

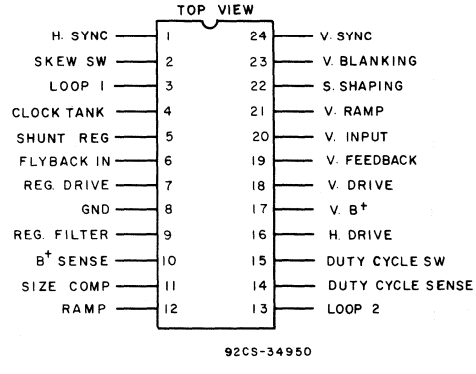
For 525-Line (CA3210E) or 625-Line (CA3223E) Operation

Features:
- *Horizontal Driver*
- *Two Phase-Lock Loops*
- *Horizontal Oscillator*
- *Vertical Countdown*
- *Vertical Blanking*
- *Vertical Ramp Generator*
- *Pulse-Width Voltage Regulator*
- *Tape-Recorder Skew Compensation*
- *Internal Shunt Regulator*

The RCA-CA3210E and CA3229E• are MSI integrated-circuit digital sync systems, designed for use in consumer TV applications which combine horizontal oscillator and vertical countdown sections, as well as a pulse-width voltage-regulator driver for color or monochrome receivers. They feature dual-mode operation and accept either standard signals or nonstandard signals. An automatic mode-recognition system forces the operation into the nonsynchronous mode for non-standard sync signals. The CA3210E is intended for use with 525-line systems and the CA3223E is intended primarily for use with 625-line systems. The CA3223E will also operate in the direct sync mode with 525-line signal sources.

The CA3210E and CA3223E are supplied in the 24-lead dual-in-line plastic package.

• Formerly RCA Dev. Type Nos. TA10955 and TA11324, respectively.



TERMINAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY:
- Terminal 17 ..... 10 V
- Terminal 22 ..... 15 V
- Terminal 5 — Shunt Regulator ..... 30 mA

DEVICE DISSIPATION:
- Up to +70°C ..... 695 mW
- Above +70°C ..... Derate linearly at 8.7 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... 0 to +70°C
- Storage ..... −55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A=+25 to +70° C

See Fig. 3, Test Points 4 and 18=27 V, Test Point 16=2.3 V, and Test Point 20=10 V.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Supply Current	Note 1, Test pt. 5=9 V, Test pt. 4=adjusted	8	16	mA
Shunt Regulator Output	Test pt. 5	8.7	11	V
$4f_H$ Coincidence	Note 2, Test pin 21	24	45	μs
V. Count (÷262.5) *	Note 3, Test pin 21	16.6	16.7	ms
V. Count (÷312.5) **		19.9	20.1	
V. Count 7 Fields after Loss of Sync:	Note 4, S1=2, Test pin 21			
(÷262.5) *		16.6	16.7	
(÷312.5) **		19.9	20.1	
V. Count 8 Fields after Loss of Sync:	Note 5, S1=2, Test pin 21			
(÷296) *		18.7	18.9	
(÷232.5) **		22	22.2	
V. Count Low	Note 6, S1=2, Test pin 21			
(÷232) *		14.6	14.9	
(÷232.5) **		14.7	15	
V. Ramp Pulse Width at 7 V	Note 7, Test pin 21			
*		503	516	μs
**		506	518	
V. Blanking Pulse Width	Note 8, Test pin 23			
*		1.140	1.148	ms
**		1.148	1.156	
V. Blanking Sat. Voltage	Note 9, Test pin 21	1.2	1.8	V
V. Sync SVC SW.	Note 10, Test pt. 20=0.7 V, Test pin 21	12	14	
Vertical Loop Gain:	Note 11(a),(b)			
Low	Test pin 18=0.3 V	11	11.7	
Medium	Test pin 18=4.5 V	10.89	11.81	
High	Test pin 18=8 V	10.89	11.85	
Regulator Driver Out	Test pin 7	6.2	7.5	
Horizontal Pulse Width	Note 12, Test pin 16			
*		31.5	34.6	ns
**		31.7	34.9	
Horizontal Drive Shutdown	Note 13, Test pin 16, Clock disabled	4.9	5.1	V
Horizontal Drive Sat. Voltage	Note 14, Test pin 16 at 15 mA	—	0.42	
Nominal Loop Phase	Note 15, Test pin 16	11.25	13.6	ns
Ramp Voltage (p-p)	Test pin 12	3.8	7.5	V_{p-p}

*CA3210E—525-Line system.
**CA3223E—625-Line system.

NOTES:

1. Adjust 27-V supply for pin 5 voltage=9 V ± 0.1 V and measure current into pin 5.
2. Measure of the time delay between the output pulse at pin 21 and the input vertical sync at J1.
3. Measure the period of the waveform at pin 21. The frequency at pin 16 should be 262.5* or 312.5** times the frequency at pin 21. This corresponds to a frequency of 59.939* or 50.000** Hz at 21 when 16 is 15734* or 15625** Hz.
4. Remove vertical sync (SW1=2), and remeasure period of waveform at pin 21 6 fields later (100* or 120** ms). Period should remain the same as in previous test.
5. Keep vertical sync off and remeasure period of waveform at pin 21 after 2 additional fields. The frequency at pin 16 should be 296* or 346** times the frequency at pin 21.
6. With no vertical sync and pin 24 connected through 10 KΩ to +5 V, measure the period of the waveform at 21. The frequency at pin 16 should be 232* or 232.5** times that at pin 21.
7. Measure pulse width of waveform in pin 21 at +7-V trip points.
8. Measure pulse width at pin 23 at 4-V trip point.

CA3210, CA3223

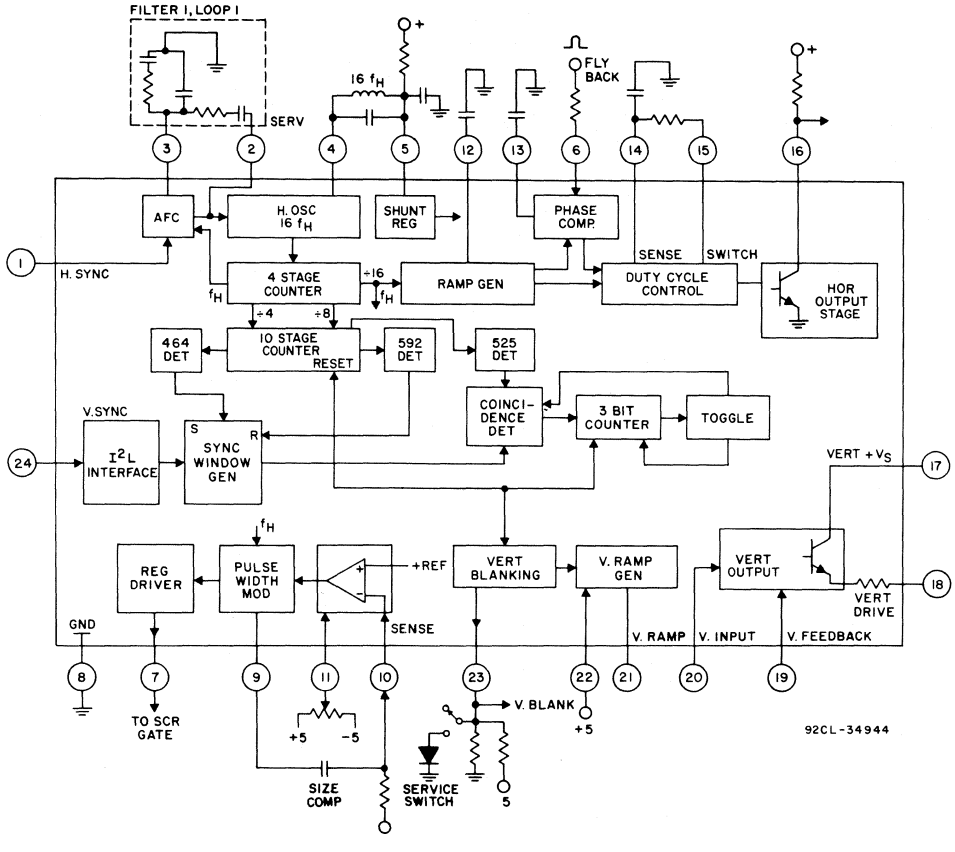


Fig. 1 - Functional block diagram of the CA3210E (525 line).

NOTES: (Cont'd)

9. Measure voltage at pin 21 when pin 23 is at low state. Clock may be stopped during measurement or measurement may be made on the "fly".
10. Set test point 20 to 0.7 V. Measure voltage at pin 21.
11. (a) Adjust test point 16 until pin 18 is 0.3 V. Measure voltage at pin 19.
    (b) Adjust so that the voltage on pin 18 is 4.5 and 8.0 V, respectively.
12. Measure width of negative-going pulse at pin 16 at the 2-V level.
13. When pin 16 goes low, disable clock by applying 18 V. The purpose of this test is to verify that pin 16 will then go from low to high with the clock (pin 14) disabled.
14. Measure amplitude of pulse at pin 16 at its low state.
15. Measure delay of horizontal sync pulse (positive leading edge) with respect to the positive leading edge of pin 16.

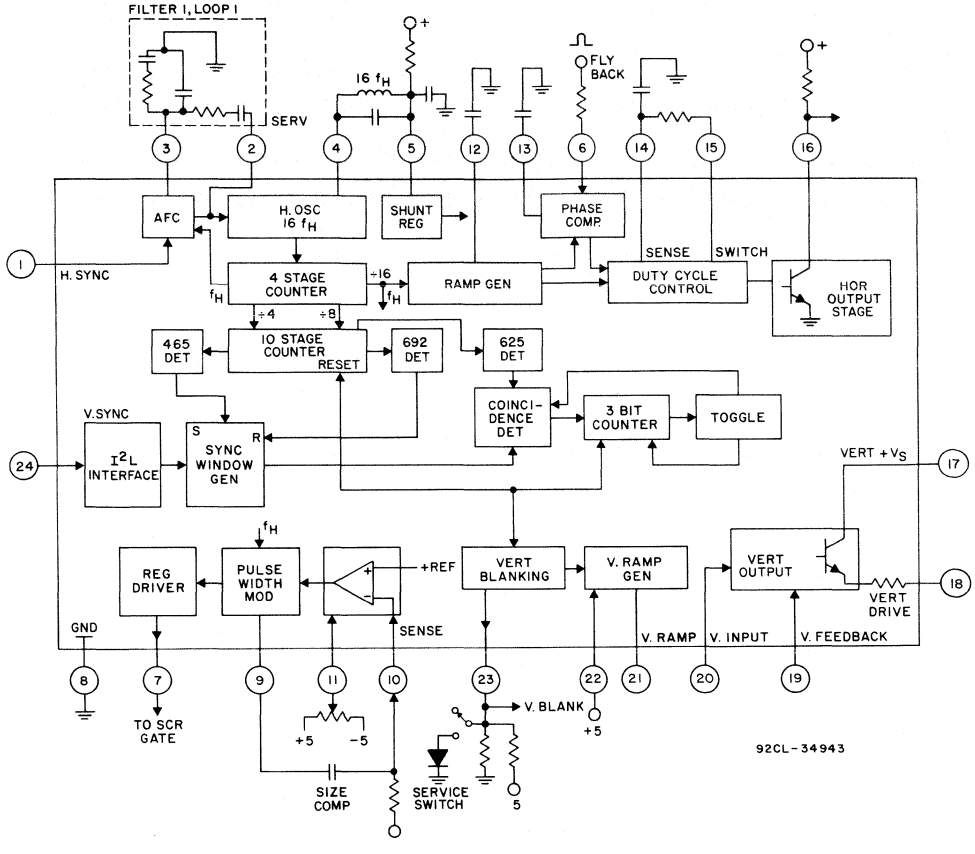


Fig. 2 - Functional block diagram of the CA3223E (625 line).

Horizontal/Vertical Processor

Circuit Operation

Figs. 1 and 2 of the block diagrams show the major functional elements of the RCA-CA3210E and CA3223E.

The master oscillator operates at 16 times the horizontal rate, f_H, as determined by an external LC tank connected between pins 4 and 5. The master oscillator is divided by 4, 8, and 16. The divide by 16 output is used to compare its phase with the incoming horizontal synchronization signal in the first APC loop which acts to synchronize the system. This output is also used to generate a horizontal ramp whose output is used to control the phase of the horizontal output pulse with respect to a flyback pulse input in the second APC loop. The deviation of the horizontal output pulse is adjusted and then connected to the horizontal driver stage. The divide by 4 and 8 outputs are used to drive a 10 section counter for the vertical circuits. The use of the countdown system and associated logic circuits assures good noise immunity and the absence of a vertical hold control in the TV receiver.

CA3210, CA3223

As shown in Figs. 1 or 2 the 464th (CA3210E) or 465th (CA3223E) clock pulse is used to set a SYNC WINDOW generator. If the incoming SYNC signal occurs at the same time the 525th (CA3210E) or 625th (CA3223E) clock pulse occurs, the YES output of a coincidence gate is used to reset a 3-bit counter and to generate the start of vertical blanking and vertical sweep. If the incoming SYNC pulse is removed (by noise, for example), the 10-stage counter will continue to provide an output pulse at the 525th (CA3210E) or 625th (CA3223E) clock but the 3-bit counter will count the number of fields where no coincidence occurred. If incoming SYNC is regained before the 3-bit counter accumulates 8 fields, the 3-bit counter will reset and normal action will continue. If no coincidence is detected in 8 sequential fields, the 3-bit counter energizes the togg which shifts the mode of operation from countdown synchronization.

In the sync mode, vertical scan is initiated by the sy pulse. If no sync pulse is present, the system will free run a frequency determined by the 592 (CA3210E) or 6 (CA3223E) count. A non-standard sync signal circ operates if the incoming sync occurs regularly between 4 (CA3210E) or 465 (CA3223E) and 592 (CA3210E) or 6 (CA3223E) counts.

The divide by 16 output is also used in the pulse wid modulator which generates a triggered constant pul width signal which in turn drives the deflection circuit.

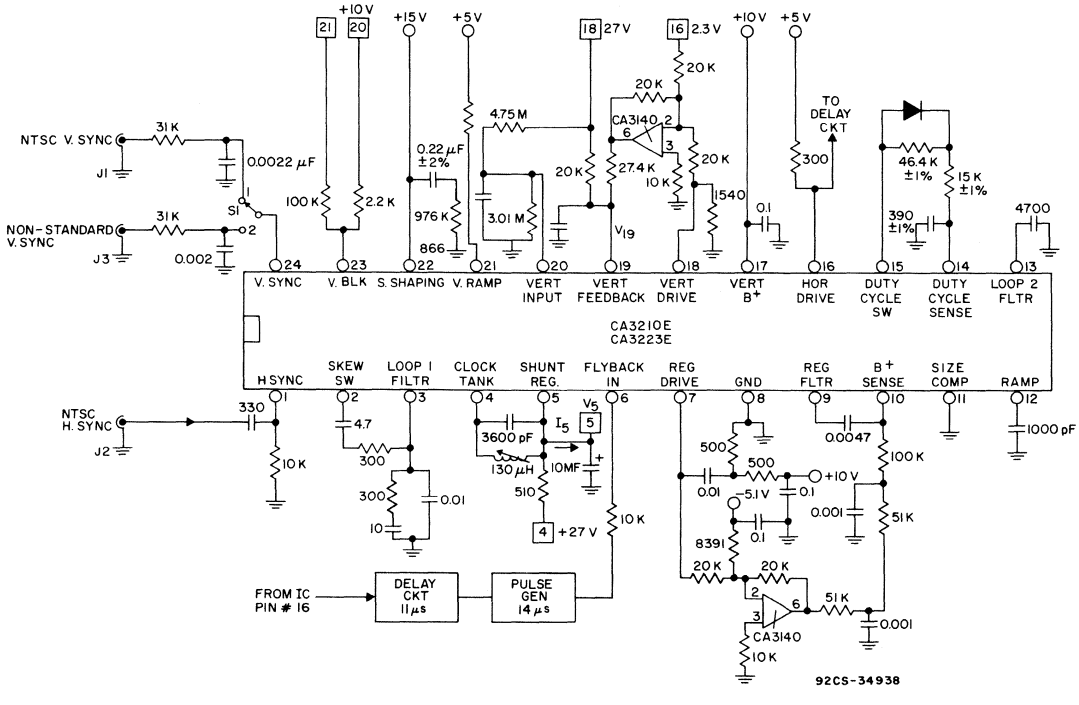


Fig. 3 - Testing circuit.

rcuit Description

art-up Circuit

ıe start-up circuit provides power to the integrated circuit turn-on until horizontally derived B+ is sufficient to wer the chip. The start-up circuit protects the horizontal stem of the TV receiver by insuring the IC is in the correct ode by delaying operation until the chip supply voltage s reached 8.0 V. After the circuit starts, should the chip pply decrease to 4.0 V, the start-up circuit will turn the IC f.

ew Switch

frequency selector circuit is used to route two frequency gnals to the AFC (see Figs. 1 and 2). Vertical signals ntrol both the selector circuit and the external Filter 1 ne constants. During most of the vertical scan time, signal is routed to AFC and the Filter 1 time constant is selected r a slow loop 1 response time. For the remaining part of e vertical scan, signal $2f_H$ is fed to the AFC and the Filter 1 ne constant is selected to give the loop a fast response ne. This dual time constant feature allows the system to ıase synchronize rapidly with non-standard signals enerated by equipment such as a VCR.

Internal Shunt Regulator

The shunt regulator maintains the IC's main supply rail at constant voltage. As the voltage V+ (Fig. 4) increases from zero, the zener voltage eventually becomes conductive, and current flows through R50, R51, and R52. As the voltage across R51 increases, transistor Q119 becomes conductive, maintaining a fixed voltage between the collector and emitter of Q119. Increasing voltage V+ still further increases the voltage across resistor R52, eventually turning on Q120. At this point, voltage V+ becomes regulated due to the varying conduction of shunt transistor Q120.

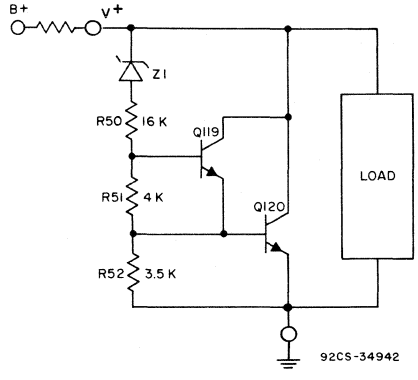


Fig. 4 - Shunt regulator.

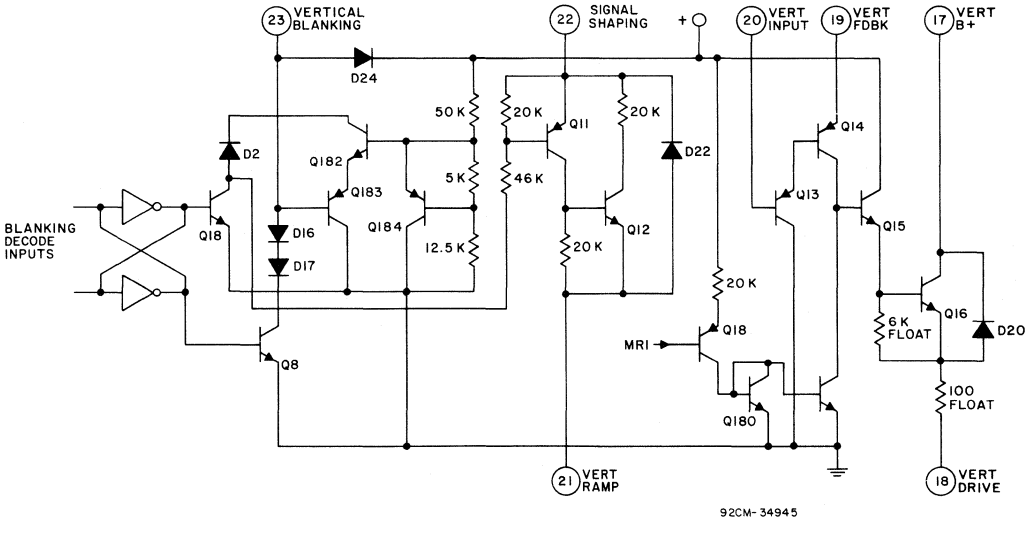


Fig. 5 - Vertical system signals.

CA3210, CA3223

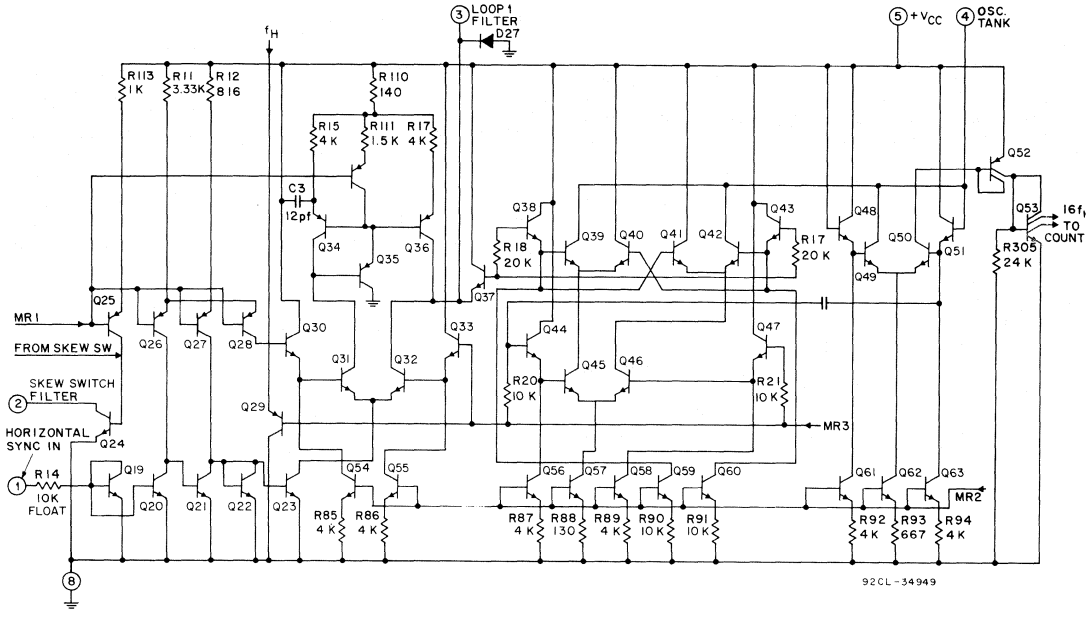


Fig. 6 - 1st loop phase detector of master oscillator.

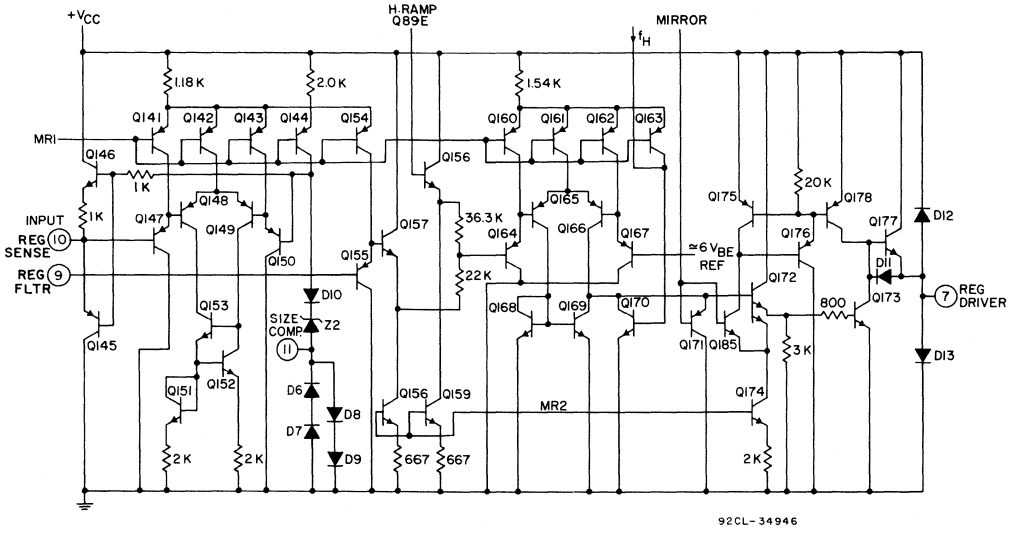


Fig. 7 - Regulator driver and pulse width modulator.

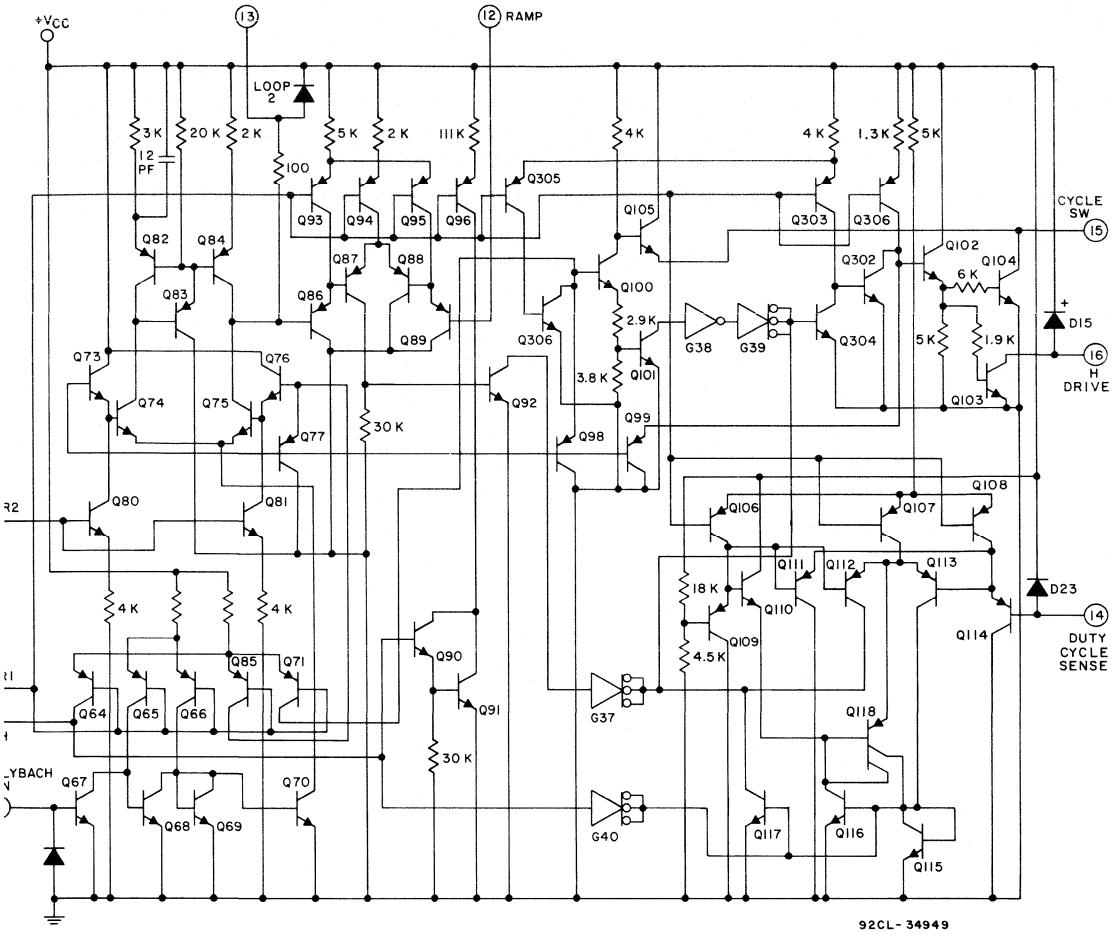


Fig. 8 – Horizontal ramp, control, and drive.

CA3210, CA3223

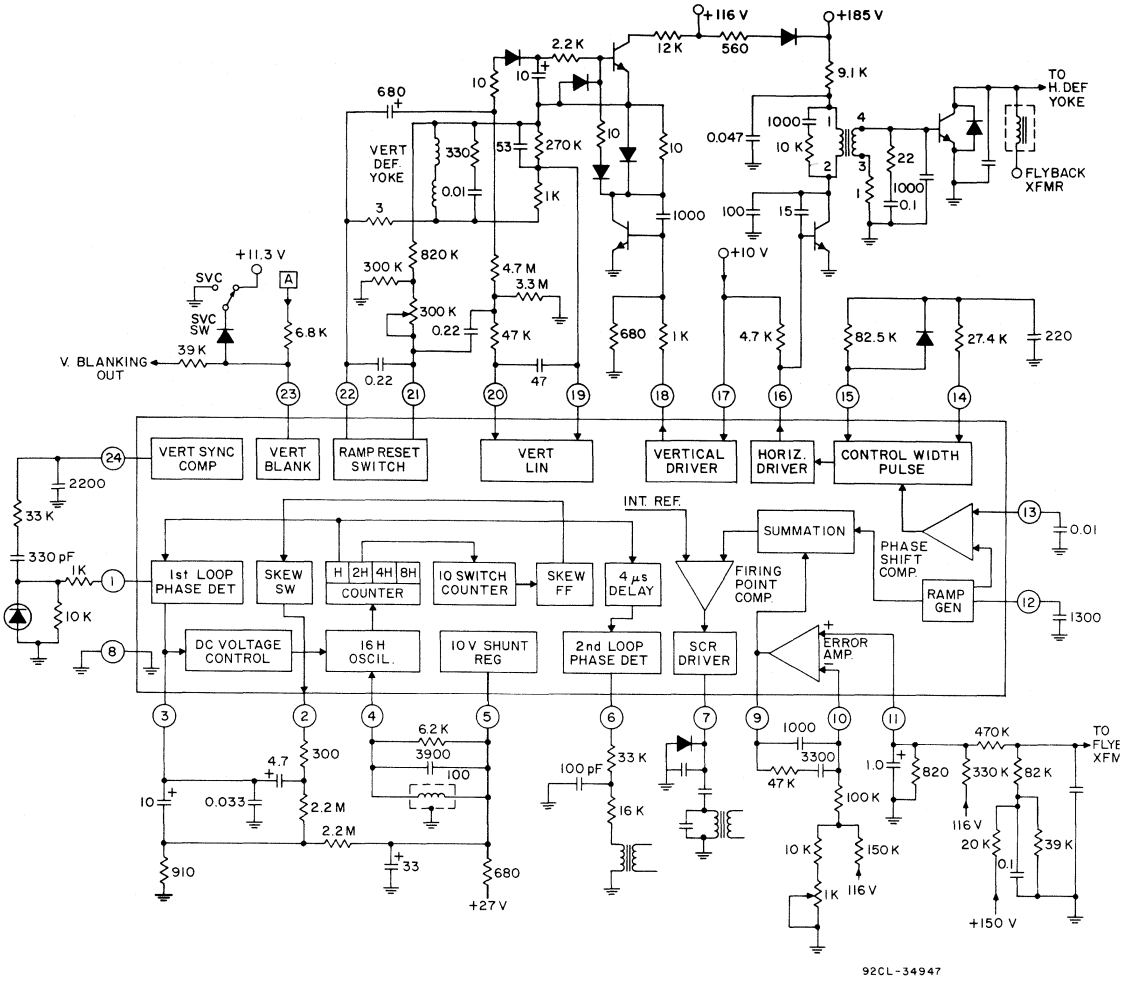


Fig. 9 - Application circuit.

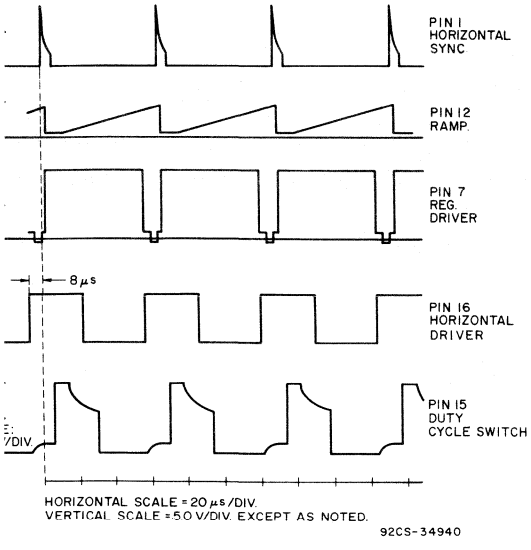


Fig. 10 – Timing relationship between various waveforms for typical circuit application.

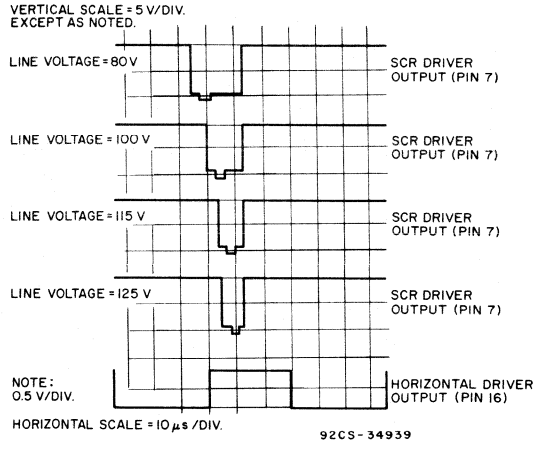


Fig. 11 – Relationship between SCR driver output and horizontal driver output vs. line voltage.

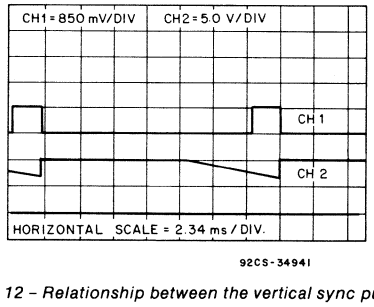


Fig. 12 – Relationship between the vertical sync pulse and the vertical ramp.

CA3217

Single Chip TV Chroma/Luminance Processor

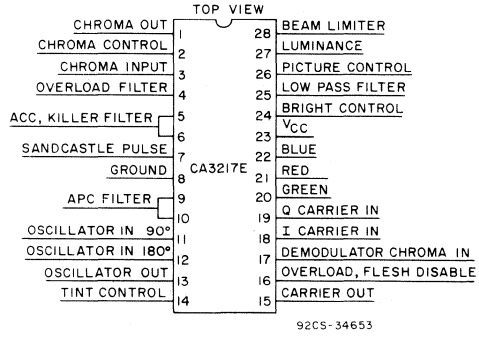
System Features:

- *All chroma processing and demodulating circuitry on a single chip in a 28-lead plastic package*
- *Phase-locked subcarrier regeneration utilizing sample-and-hold techniques*
- *Supplementary ACC with overload detector to prevent over saturation of the picture tube*
- *Linear dc controls for chroma gain and tint*
- *Dynamic "flesh correction" - corrects purple and green flesh colors without affecting primary colors*
- *Balanced chroma demodulators with low output impedance for direct coupling*
- *Internal rf filtering*
- *Requires few external components*
- *Automatic beam limiter*
- *Chroma luminance tracking picture control*

The RCA CA3217E• is a monolithic silicon integrated circuit. It contains all the required circuits functions between the video detector and the picture tube RGB driver stages of a color television receiver. The CA3217E decodes the chrominance signals and then produces three different color signals that are internally combined with the luminance to develop the RGB signals. The picture saturation, hue and brightness DC controls are externally adjustable by the viewers. The AFPC, ACC, Dynamic flesh control, Beam limiting and Gate black level (Brightness) control are servo loops used to stabilize the RGB output and reduce frequent manual adjustment. The automatic beam limiter circuit reduces picture contrast and brightness to prevent excessive drive output at the picture tube.

The CA3217E is supplied in a 28-lead dual-in-line plastic package, (E Suffix).

•Formerly RCA Dev. Type No. TA10806.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
Between Terms. 23 and 8 ..... 14.0 V
DEVICE DISSIPATION:
Up to T_A = 55°C ..... 1.27 W
Above T_A = 55°C ..... Derate lineraly at 13.3 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... -40 to +85°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch
(1.59 ± 0.79 mm) from case
for 10 seconds max. ..... +265°C

File Number **133**

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS											LIMITS			UNITS
	Test	S_2	S_3	S_4	S_5	S_6	mV_{p-p} Chroma	mV_{p-p} Burst In	mV_{p-p} Luma	Relays Energized	Note	Min.	Typ.	Max.	
STATIC (Test 1-5)															
Dissipation	Pin 23	6.3 V	11.2 V	4.0 V	6.3 V	11.2 V						30	48	66	mA
Pin 1 Bal	XPT1	1.2 V	11.2 V	4.0 V	6.3 V	11.2 V							10.5		Vdc
Pin 3 Bal	XPT1	1.2 V	11.2 V	4.0 V	6.3 V	11.2 V							2.2		
Pin 17 Bal	XPT9	1.2 V	11.2 V	4.0 V	6.3 V	11.2 V							3.0		
Pin 13 Bal	XPT13	1.2 V	11.2 V	4.0 V	6.3 V	11.2 V							7.5		
DYNAMIC (Test 6-26)															
Oscillator Pull-In	"D"	6.3 V	11.2 V	4.0 V	6.3 V	11.2 V	25	25		K4, K7	1	-350		+350	Hz
Oscillator Level	"D"	6.3 V	11.2 V	4.0 V	6.3 V	11.2 V	0	0		K7			0.7		V_{p-p}
100% Acc	P21	Vary	11.2 V	4.0 V	6.3 V	11.2 V	125	125		K4, K7	2		1.5		
200% Acc	P21	T8	11.2 V	4.0 V	6.3 V	11.2 V	250	250		K4, K7	3		100		%
20% Acc	P21	T8	11.2 V	4.0 V	6.3 V	11.2 V	25	25		K4, K7	3		90		
Tint Center	S5	Vary	11.2 V	4.0 V	Vary	11.2 V	250	125		K4, K7	4		6.5		Vdc
R-Y Maximum	P21	11.2 V	11.2 V	6.0 V	T11	11.2 V	250	125		K1, K4, K7			6.0		V_{p-p}
Unkill	P21	11.2 V	11.2 V	4.0 V	T11	11.2 V	25	12.5		K4, K7			4.5		
Kill	P21	11.2 V	11.2 V	4.0 V	T11	11.2 V	25	2.5		K4, K7				150	mV p-p
Chroma Reserver	P21	11.2 V	11.2 V	4.0 V	T11	11.2 V	12.5	125		K2, K4, K7			2.0		V_{p-p}
Maximum Luma	P21	11.2 V	11.2 V	4.0 V	T11	11.2 V			125	K1, K3, K7	5		2.2		
Luma Ratio	P21	11.2 V	6.3 V	4.0 V	T11	11.2 V			125	K1, K3, K7	6		50		%
Linearity	P21	11.2 V	Vary	3.0	T11	11.2 V			425	K3, K7	7		4		V_{p-p}
T19 = T19/T18	P21	11.2 V	T18	3.0	T11	11.2 V			212.5	K3, K7			50		%
4.78 MHz Response	P21	11.2 V	11.2 V	4.0 V	T11	11.2 V			125	K3, K6, K7	8	-3		3	dB
Contrast Limit 1	P24	11.2 V	11.2 V	4.0 V	T11	11.2 V			250	K3, K5, K7	9		3.9		Vdc
Contrast Limit 2	P26	11.2 V	11.2 V	4.0 V	T11	11.2 V			250	K3, K5, K7	9		8.2		
Bright Limit 1	P24	11.2 V	11.2 V	4.0 V	T11	11.2 V			250	K3, K5, K7	10		3.1		
Bright Limit 2	P26	11.2 V	11.2 V	4.0 V	T11	11.2 V			250	K3, K5, K7	10		5.6		
G-Y Ratio	P20	Vary	11.2 V	4.0 V	T11	11.2 V	250	125			11		0.33		R
B-Y Ratio	P22	T25	11.2 V	4.0 V	T11	11.2 V	250	125			11		1.20		

Notes:

1. With K7 energized and frequency counter at D vary C1 for 3.579175 MHz. Then with K4 energized, check for pull-in. Repeat for frequency tuned to 3.579875 MHz. For all other tests tune to 3.579545 MHz ±10 Hz.
2. Vary S2 for 1.5 V_{p-p} at Pin 21.
3. % of 100% ACC.
4. Adjust C1 for 3.579545 MHz ±10 Hz. Adjust S2 for 1.6V V_{p-p} at Pin 22 and 0 reference; then adjust S5 for minimum at P21. Read and record S5 voltage
5. Black to White.
6. T17 = T17/T16.
7. Adjust S3 for 4.0 V_{p-p}.
8. AC amplitude = 50 mV_{p-p} reference 15 kHz.
9. Adjust beam limiter to 10.7 V.
10. Adjust beam limiter to 9.8 V.
11. Adjust S2 for 1.5 V_{p-p} at Pin 21, then calculate P20/P21 and P22/P21.

CA3217

TYPICAL PERFORMANCE OF THE CA3217E

Function	Typical Data	
Nominal Supply	11.2V	
Nominal Dissipation	500 mW	
Oscillator Stability		
Supply Variation 10^{-14} V	5 Hz	
Variation with Temperature (ΔT = 50°C)	25 Hz	
AFPC Characteristics		
dc Loop Gain	33 Hz/degree	
Pull-in Range	±500 Hz	
ACC Characteristic		
100% Chroma Input Level	250 mV_{p-p} on red bar	
3-dB Point	at 20% nominal input level	
Hue-Control Range	100°	
Saturation-Control Range	40 dB min	
Demodulator Characteristics:	**Relative Amplitude**	**Angle**
R — Y	1.0	93°
B — Y	1.2	2°
G — Y	0.3	258°
Bandwidth (Chroma)	900 kHz	
Flesh Control	Primary control in the +1 half-plane	
Chroma Overload Control	Two levels	
Picture Control	40 dB	
Brightness Control	Black level clamped on 3 V to 5 V level	
Beam Limiting	On picture and brightness controls	
Luma Bandwidth	5 MHz min	
Sandcastle Input		
1.2 — 2.3 V	Blanking	
>3.3 V	Burst gate	
Maximum Linear Output		
R	5 V	
G	3 V	
B	3.7 V	

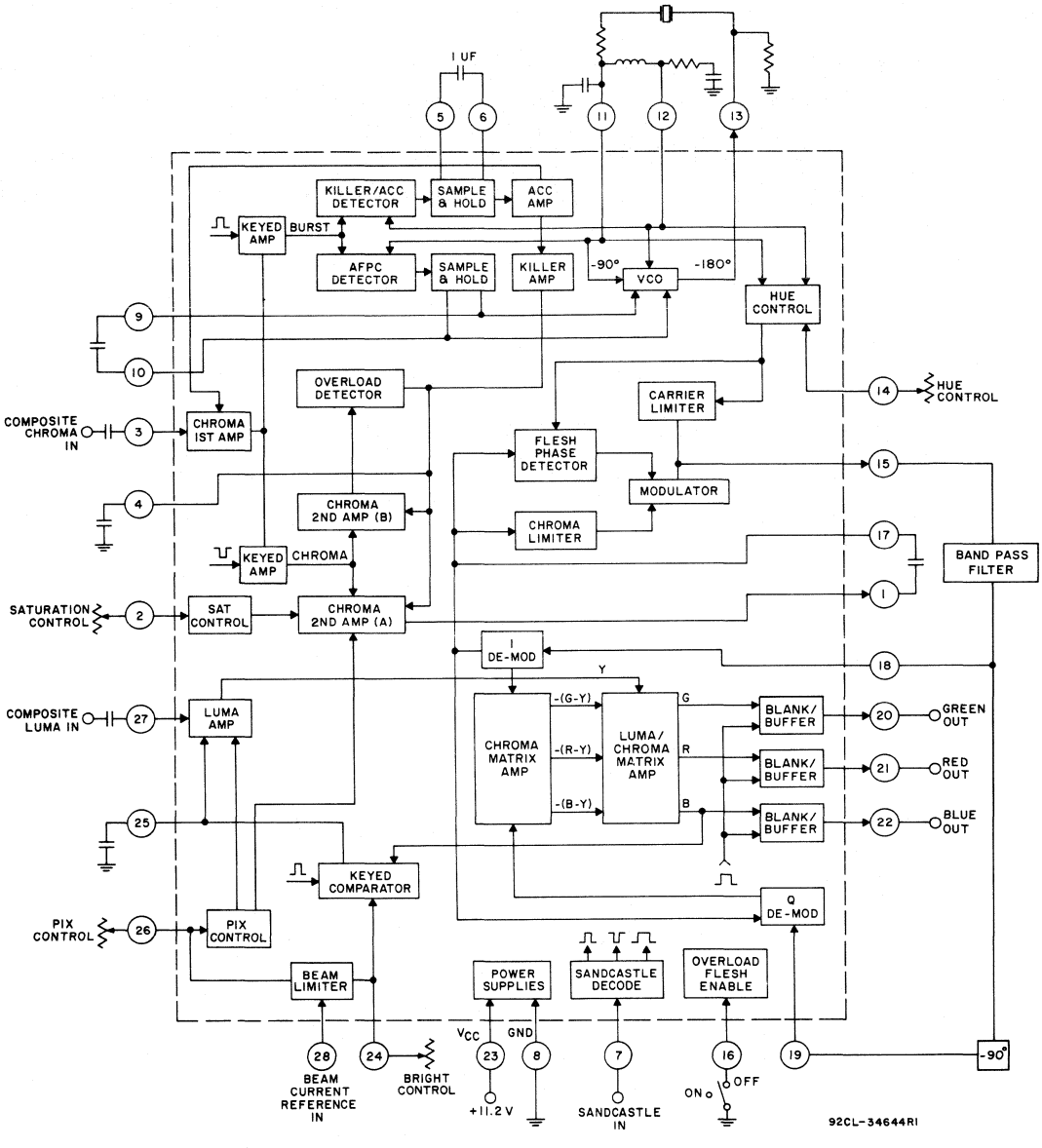


Fig. 1 - Functional block diagram of the CA3217E.

CA3217

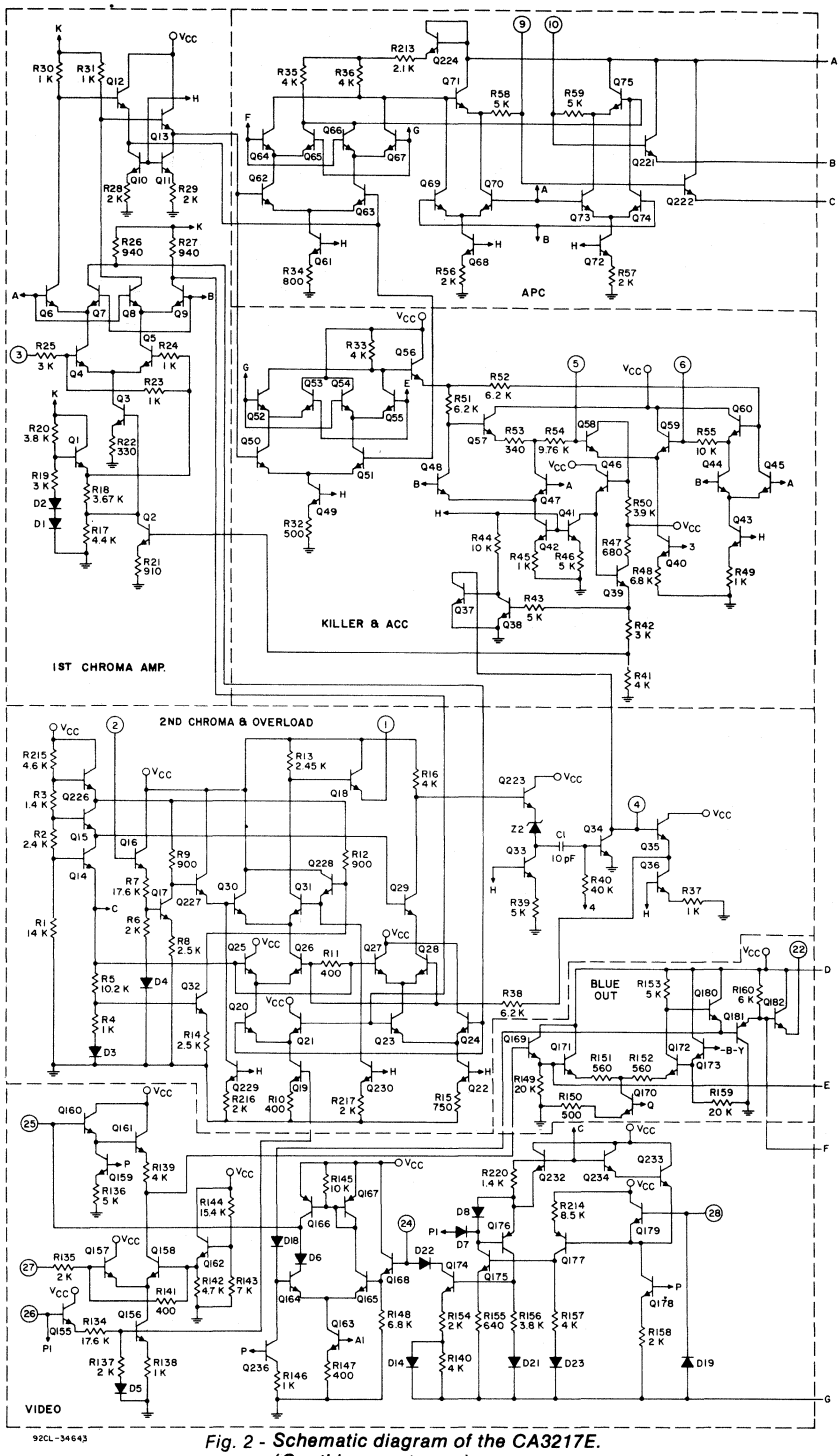


Fig. 2 - Schematic diagram of the CA3217E.
(Cont'd on next page).

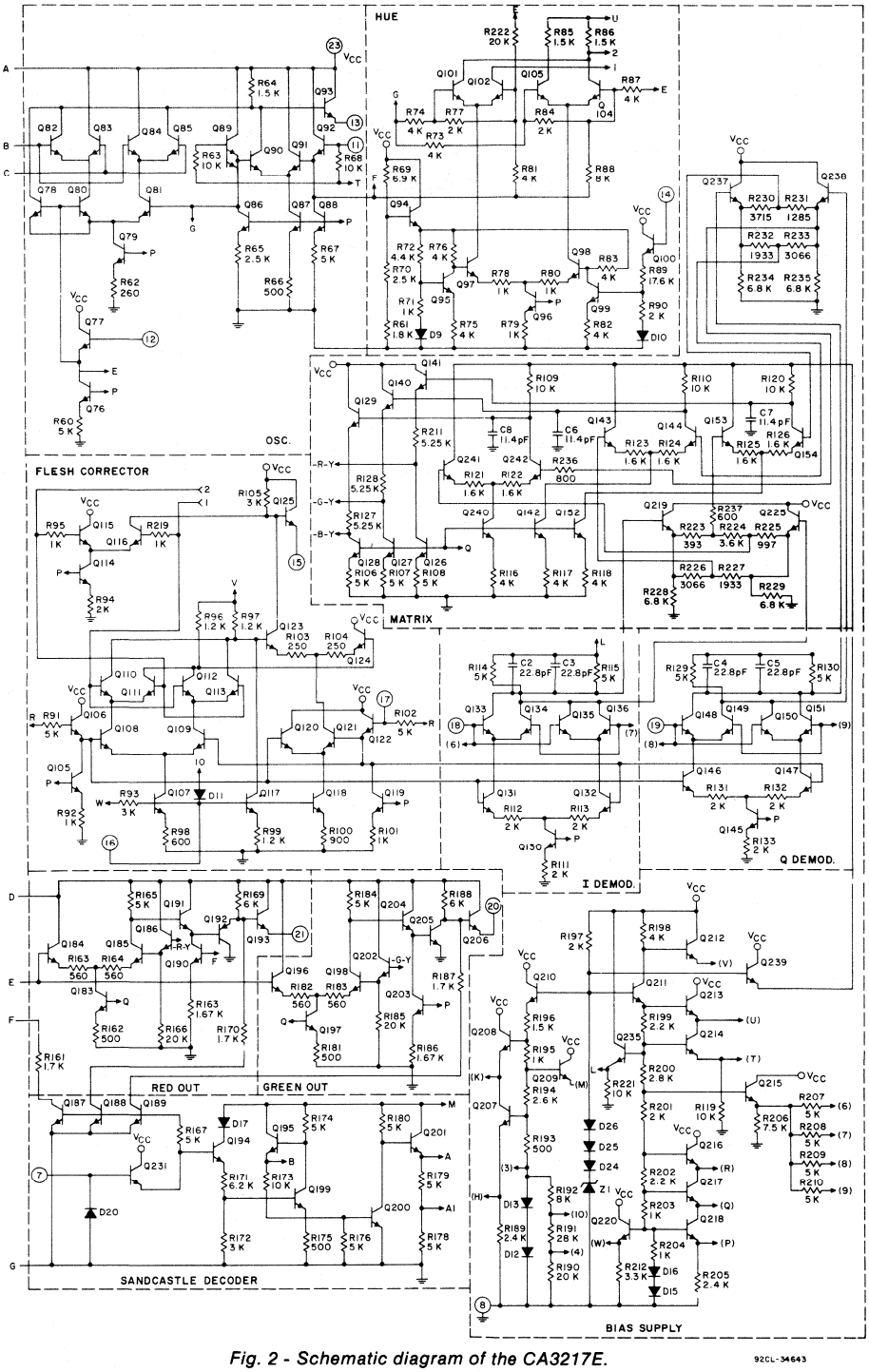


Fig. 2 - Schematic diagram of the CA3217E.
(Cont'd from previous page).

CA3217

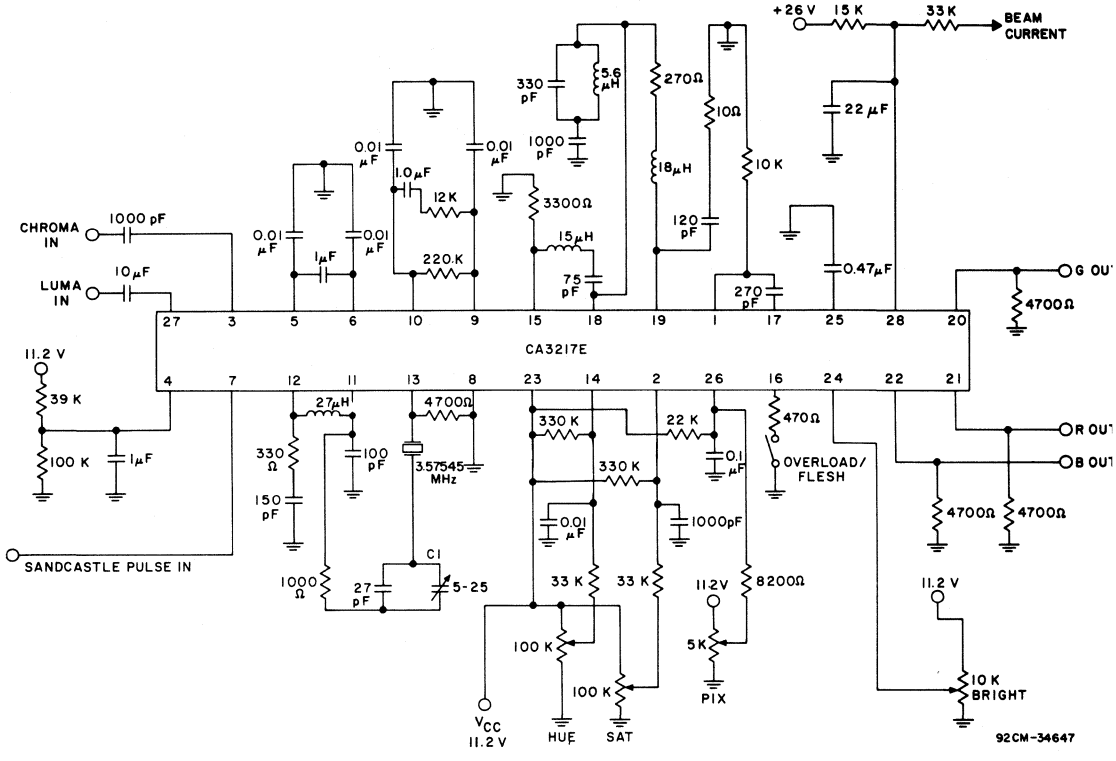


Fig. 3 - Typical application circuit.

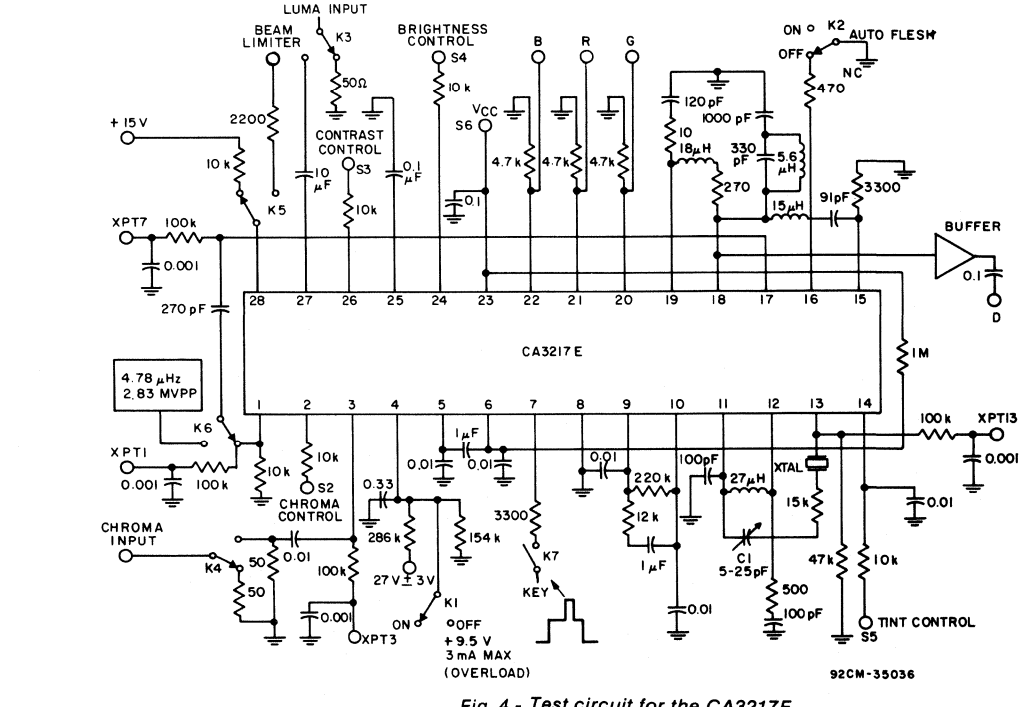


Fig. 4 - Test circuit for the CA3217E.

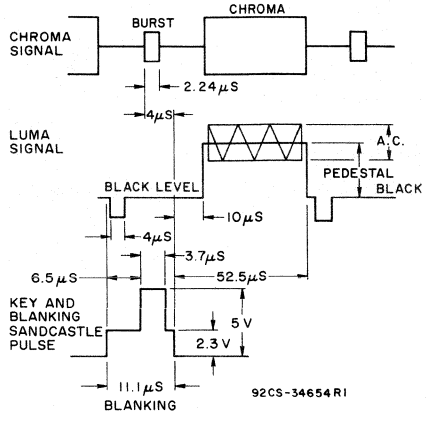


Fig. 5 - Test signals for the CA3217E.

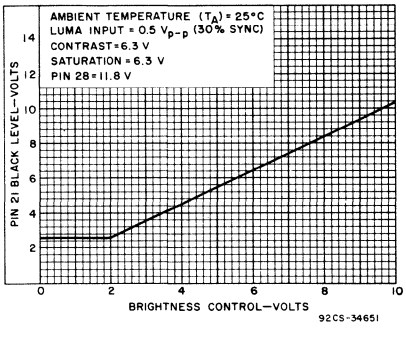


Fig. 6 - Typical P21 black level versus brightness control.

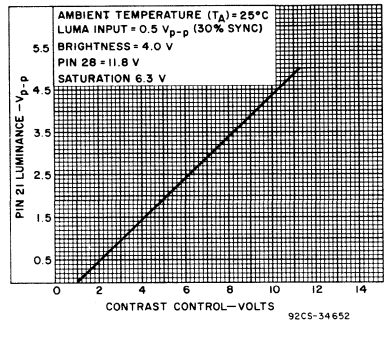


Fig. 7 - Typical P21 luminance output versus contrast control.

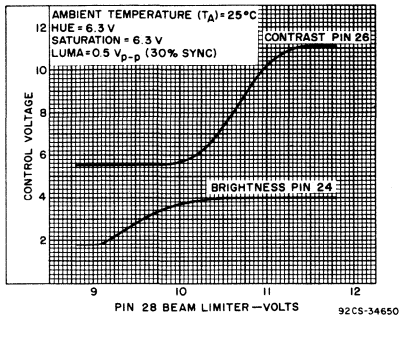


Fig. 8 - Typical beam limiter versus contrast and brightness.

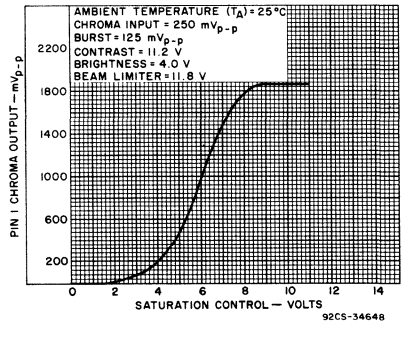


Fig. 9 - Typical P1 chroma output versus saturation control.

CA3217

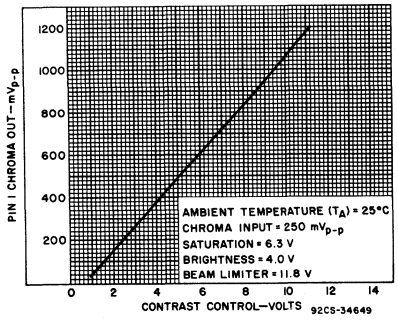


Fig. 10 - Typical P1 chroma output versus contrast control.

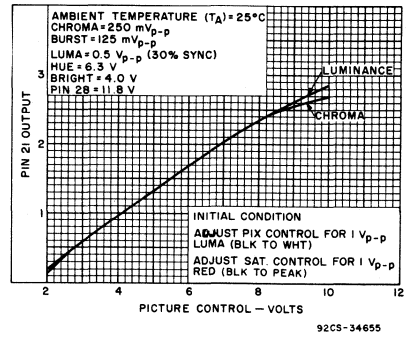


Fig. 11 - Typical luma/chroma track.

Advance Information/
Preliminary Data

CA3218

TV Horizontal/Vertical Countdown Digital Sync System

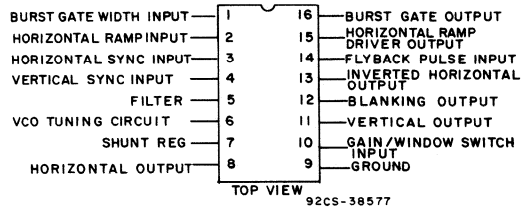
Features:
- *Horizontal oscillator*
- *Vertical countdown*
- *Composite blanking output*
- *Burst-gate output*
- *Horizontal ramp generator*
- *Internal shunt regulator*

The RCA - CA3218E* is a video sync system designed for use in television, monitor or video display products. The CA3218E contains a horizontal phase-locked oscillator and vertical countdown. It also features composite blanking and burst-gate outputs which, when externally summed, produce the sandcastle pulse necessary for the operation of most chroma/luma circuits.

The CA3218E is intended for use in 525-line systems and operates with standard or nonstandard input signals. An automatic mode-recognition circuit forces operation into the nonsynchronous mode for nonstandard sync input signals.

The CA3218E is supplied in a 16-lead dual-in-line plastic package (E suffix).

*Formerly RCA Developmental Type No. TA11419.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY CURRENT, PIN 7 ..... 50 mA
INPUT VOLTAGE (ALL INPUTS) ..... -1 V to V^+ + 1 V
DEVICE DISSIPATION:
  Up to T_A = 85°C ..... 900 mW
  Above T_A = 85°C ..... derate linearly 14 mW/°C
AMBIENT-TEMPERATURE RANGE:
  Operating ..... -40 to +85°C
  Storage ..... -65 to +150°C
LEAD TEMPERATURE (During soldering):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

File Number **1637**

CA3218

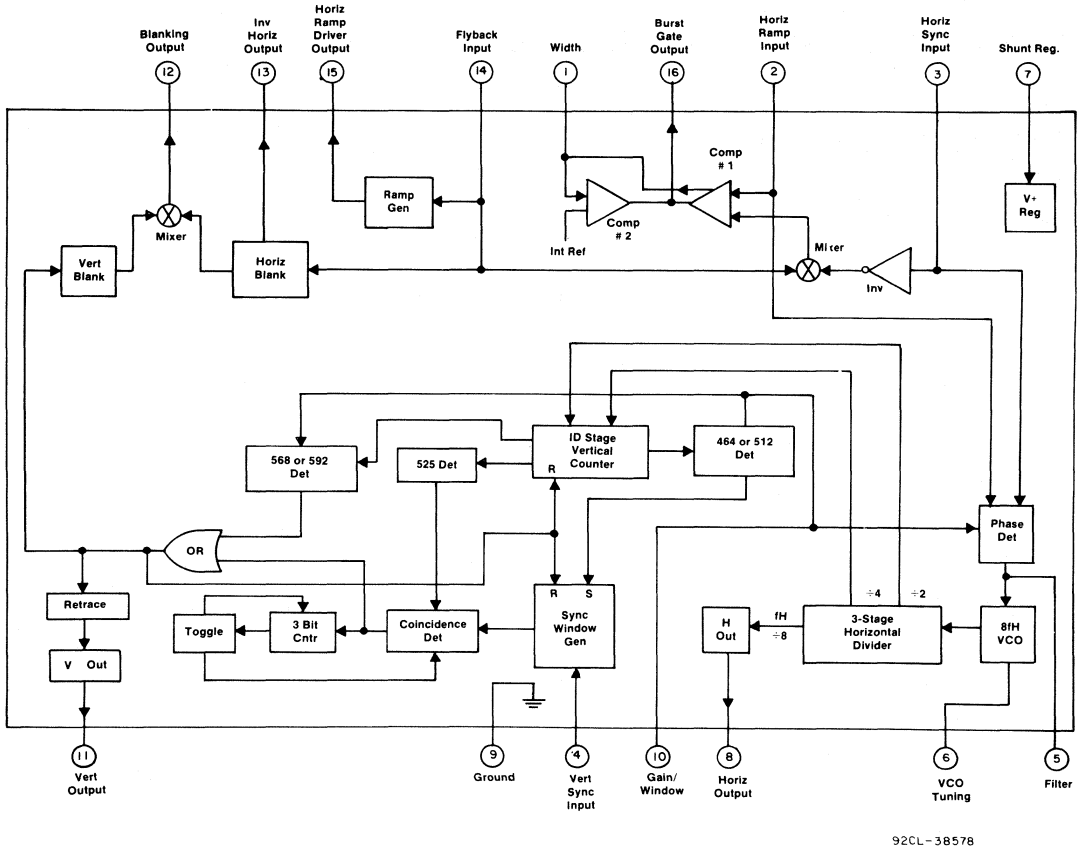


Fig. 1 - Functional block diagram.

CIRCUIT OPERATION (See Fig. 1)

The master oscillator operates at 8 times the horizontal rate, fH, as determined by the external LC connected between pins 5 and 6. The master oscillator is divided by 2, 4, and 8 and is then fed to the horizontal output amplifier and also to a 10-stage vertical countdown circuit. Horizontal AFC is performed by comparing the horizontal ramp input signal on pin 2, derived from the flyback pulse, to the horizontal sync signal on pin 3, producing a correction voltage. The correction voltage then is applied to the master oscillator to phase lock the system.

The divide by 2 and 4 outputs are used to drive a 10-stage counter for the vertical circuits. The use of the countdown system and associated logic circuits assures good noise immunity and the deletion of the vertical hold control.

The Gain/Window switch input on pin 10 is a logic input which controls the digital window in which the system looks for the occurrence of a vertical sync pulse; it also adjusts the phase detector gain for the two corresponding vertical windows. The 464th (Pin 10=Low) or the 512th (Pin 10=High) clock pulse (at 2fH) from the horizontal divider is used to set the start of the vertical sync window. The end of the sync window occurs at the 592nd (Pin 10=Low) or the 568th (Pin 10=High) clock pulse. If the incoming vertical sync pulse occurs regularly at the same time the 525th clock pulse occurs, it is used to generate the start of the vertical blanking and vertical sweep; the system is in the standard sync mode. If the incoming vertical sync pulse is absent (removed by noise, for example), the 10-stage counter will continue to provide an output pulse at the 525th clock pulse; a 3-bit counter will count the number of fields where no sync pulse occurred coincident with the 525th clock pulse. If no coincidence is detected in 8 sequential fields, the 3-bit counter energizes the toggle which shifts the mode of operation from standard sync to nonstandard sync.

In the nonstandard sync mode vertical scan is initiated by the incoming vertical sync pulse. Nonstandard sync operation results when the incoming vertical sync pulse occurs regularly within the vertical sync window; 464 to 592 counts (Pin 10=Low) or 512 to 568 counts (Pin 10=High) but not at the 525th count (Standard Sync Mode). In the nonstandard sync mode if no sync pulse is present, the system will free run at a frequency determined by the 592 (Pin 10=Low) or 568 (Pin 10=High) count.

The CA3218E generates a composite blanking signal and a burst-gate (key pulse) which, when summed externally, produce the sandcastle pulse necessary for the operation of most Chroma/Luminance integrated circuits. Also generated by the CA3218E is an inverted horizontal sync signal on pin 13 which can be used to drive the CA3224E Automatic Picture Tube Bias integrated circuit.

Electrostatic Protection*

The SCR ESD-EOS protection structures used on the CA3218E are shown schematically in Fig. 6. These structures have proven to be highly effective enabling circuits to be protected in excess of 4 KV. The horizontal and vertical outputs (pins 8 and 11) are simply protected with internal diodes since their output transistors are large; these pins are also capable of withstanding 4 KV ESD. Although ESD-EOS protection is included in the CA3218E, proper circuit board layout and grounding techniques should be observed.

*For further information on CA3218E protection structures, refer to: "Using SCR's as Transient Protection Structures in Integrated Circuits", by L. R. Avery, RCA ICAN-7304 Reprint.

ELECTRICAL CHARACTERISTICS, AT +25 TO +70° C
TEST CONDITIONS SHOWN IN FIG. 3 UNLESS OTHERWISE SPECIFIED.

CHARACTERISTIC	PIN	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Supply Current	7	Adjust 24-V Supply for 7 V on Pin 7	7	—	14	mA
Regulator Voltage	7		7.4	—	8.6	V
Saturation Voltages						
Horiz. Output & Inv. Horiz. Output	8 13		0	—	0.4	V
Vert. Output	11		0	—	0.2	V
Blanking Output & Burst Gate Output	12 16		0	—	0.175	V
Horiz. Ramp Output	15		0	—	0.08	V
Horiz. V_{CO} Free-Running Frequency	8	No Sync Applied S1 = B	15547	—	15854	Hz
Horiz. V_{CO} Oscillator Pull-In	8	For 15734 ± 1 Hz	-300	—	+300	Hz
Blanking Width						
Horizontal	12	Std NTSC Sync Applied	9.5	—	10.5	μs
Vertical	12	Std NTSC Sync Applied	1140	—	1148	μs
Burst Gate Width	16	Std NTSC Sync Applied	2.98	—	3.42	μs
Burst Gate Delay	16	From End of Horiz. Sync (Pin 3) To Start of Burst Gate (Pin 16)	20	—	215	ns
Horiz. Pulse Width	8	Std NTSC Sync Applied	31.4	—	32.1	μs
Vert. Pulse Width	11	Std NTSC Sync Applied	504	—	516	μs
Horiz. Sync Input	—		—	10	—	V_{p-p}
Vert. Sync Input	—		—	10	—	V_{p-p}

CA3218

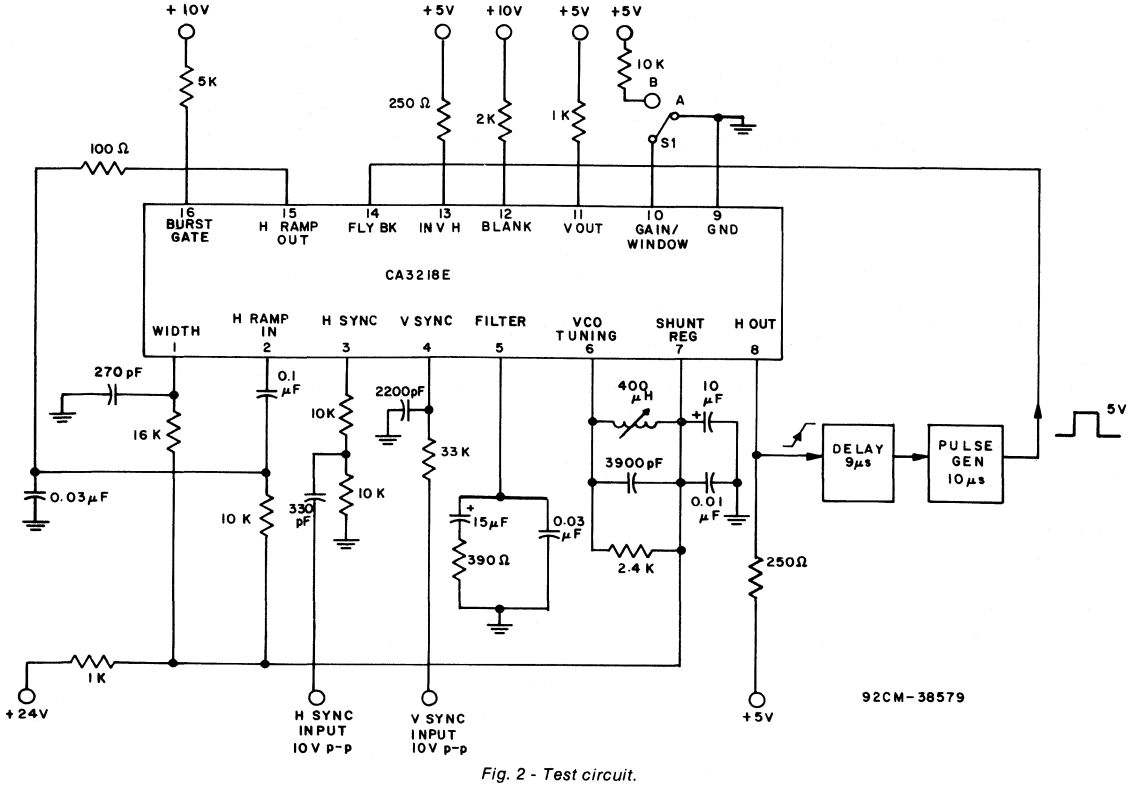


Fig. 2 - Test circuit.

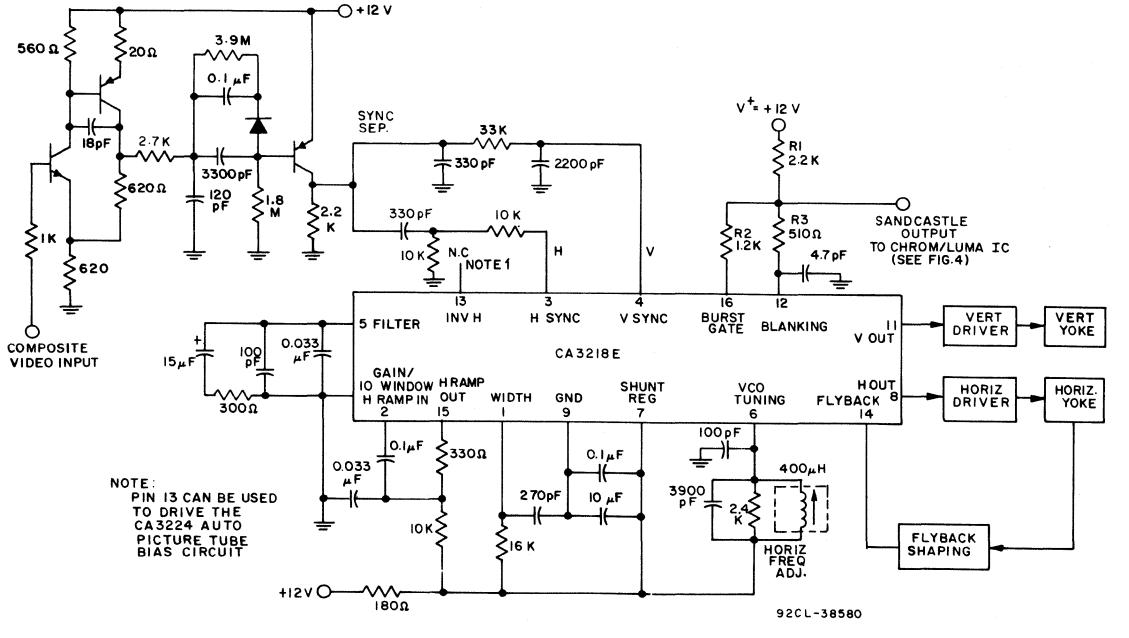


Fig. 3 - Typical application circuit.

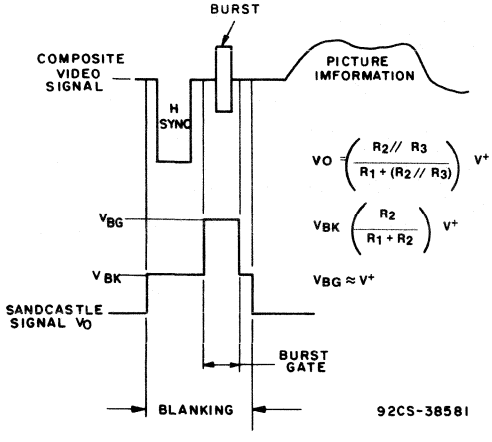


Fig. 4 - Sandcastle signal.

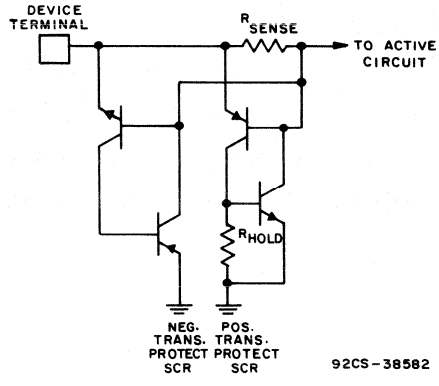


Fig. 5 - ESD protection structure.

CA3224

Advance Information/ Preliminary Data

Automatic Picture Tube Bias Circuit

For TV Picture Tube and CRT Cutoff Bias Control Applications

Features:

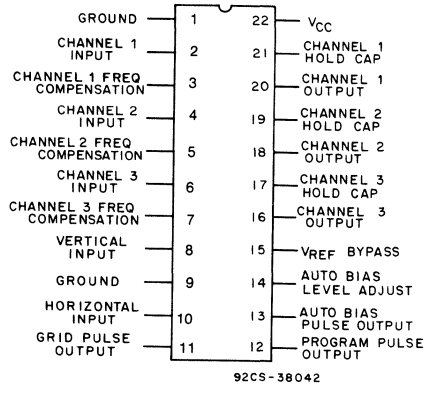
- *Automatic picture tube bias cutoff control*
- *Automatic background color balance*
- *Eliminates grey scale adjustments*
- *Compensates for cathode-to-heater leakage*
- *Electrostatic protection on all pins*
- *Servo loop design*
- *Wide dynamic range*
- *Three-gun control*
- *Minimal external components*

The RCA CA3224E* is an automatic picture tube bias control circuit used in color TV receiver CRT drive circuits. It is used to provide dynamic bias control of the grey scale both initially and over the CRT operating life, compensating for CRT cutoff changes.

The CA3224E provides automatic continuous control of the cutoff current in each gun of a three-gun color CRT. From an input pulse amplitude proportional to the difference between the desired and the actual CRT cutoff, a gated sample/hold circuit generates a DC correction voltage which correctly biases the CRT driver circuit. The sample/hold bias correction takes place each frame following the vertical blanking. Fig. 1 shows a block diagram of the CA3224E. The functions include three identical servo loop transconductance amplifiers with a sample/hold switch and buffer amplifier plus control logic, internal bias and a mode switch.

The CA3224E is supplied in a 22-lead dual-in-line plastic package (E suffix).

*Formerly RCA development type TA13010.



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE	11 V_{CC}
INPUT VOLTAGE (ALL INPUTS)	-1 to V_{CC}
DEVICE DISSIPATION:	
Up to T_A = +85°C	750 mW
Above T_A = +85°C	Derate linearly at 13 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	-40 to +85°C
Storage	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

File Number **1553**

DEVICE DESCRIPTION AND OPERATION - (See Figs. 1, 3, 6, and 7)

During the vertical retrace interval, 13 horizontal sync pulses are counted. On the 14th sync pulse the auto-bias pulse output goes high. This is used to set the RGB drive of the companion chroma/luma circuit to black level. The auto-bias pulse stays high for 7 horizontal periods during the auto-bias cycle.

On the 15th horizontal sync pulse, the internal logic initiates the setup interval. During the setup interval, the cathode current is increased to a reference value (A in Fig. 7) through the action of the grid pulse. The cathode current causes a voltage drop across R_S. This voltage drop, together with the program pulse output results in a reference voltage at V_S (summing point) which causes capacitor C_1 to charge to a voltage proportional to the reference cathode current. The setup interval lasts for 3 horizontal periods.

On the 18th horizontal sync pulse the grid pulse output goes high, which through the grid pulse amplifier/inverter, causes the cathode current to decrease. The decrease in cathode current results in a positive recovered voltage pulse with respect to the setup reference level at the VS summing point. The positive recovered voltage pulse is summed with a negative voltage pulse caused by the program pulse output going low (cutting off Diode D_1 and switching in resistors R_1 + R_2). Any difference between the positive and negative pulses is fed through capacitor C1 to the transconductance amplifier. The difference signal is amplified in the transconductance amplifier and charges the hold capacitor C_2, which, through the buffer amplifier, adjusts the bias on the driver circuit.

Components R_S, R_1, and R_2 must be chosen such that the program pulse and the recovered pulse just cancel at the desired cathode cutoff level.

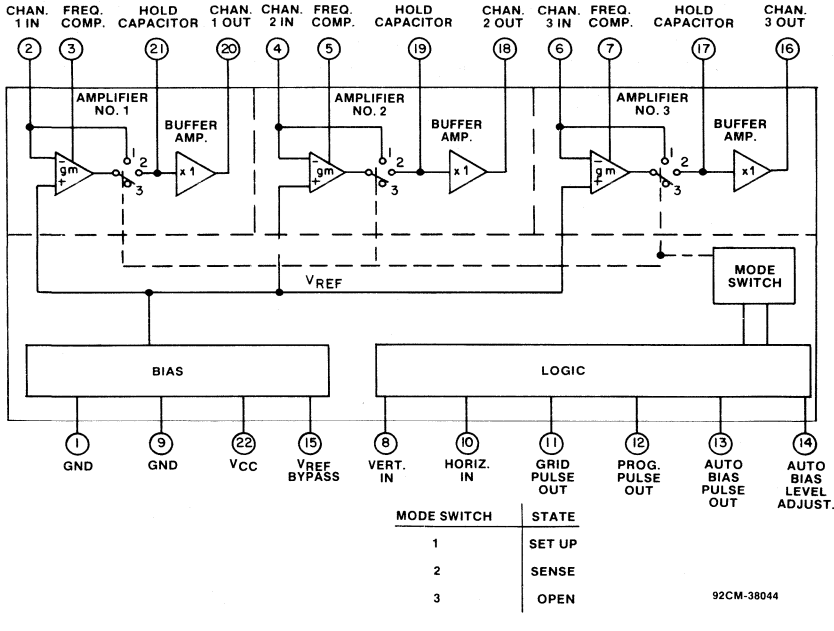


Fig. 1 - Functional block diagram.

CA3224

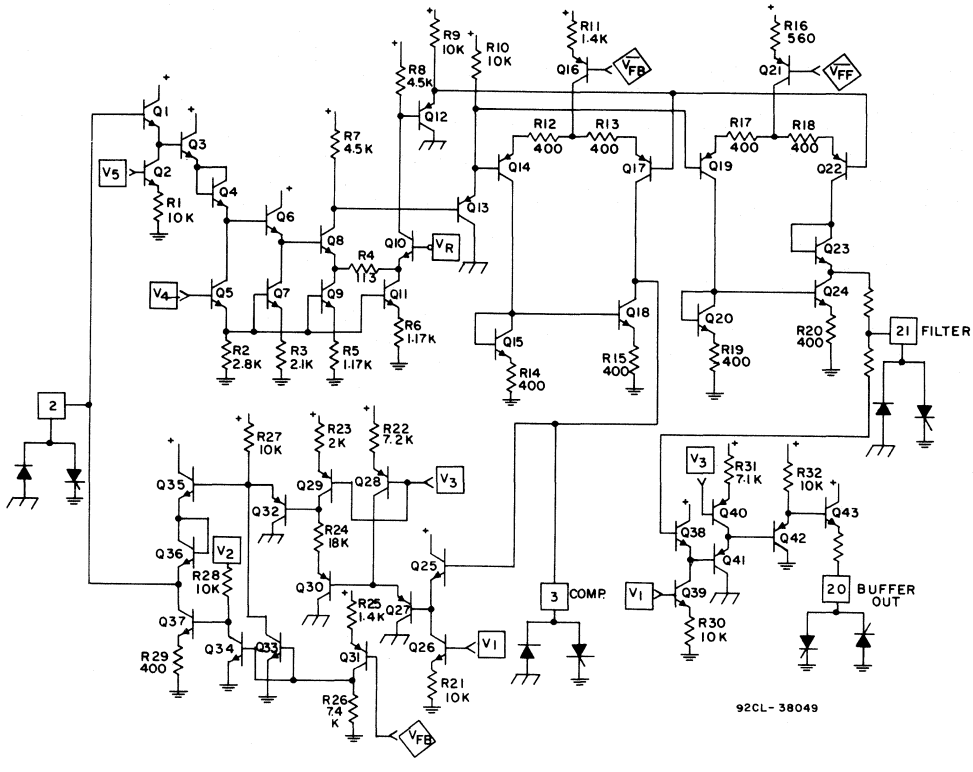


Fig. 2 - Schematic diagram (continued on next page).

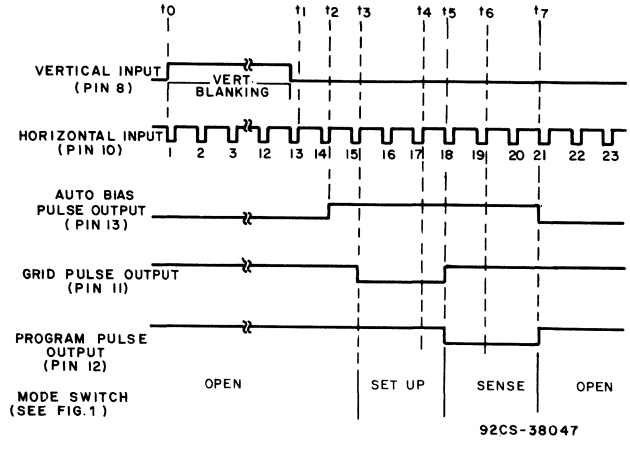


Fig. 3 - Functional timing diagram.

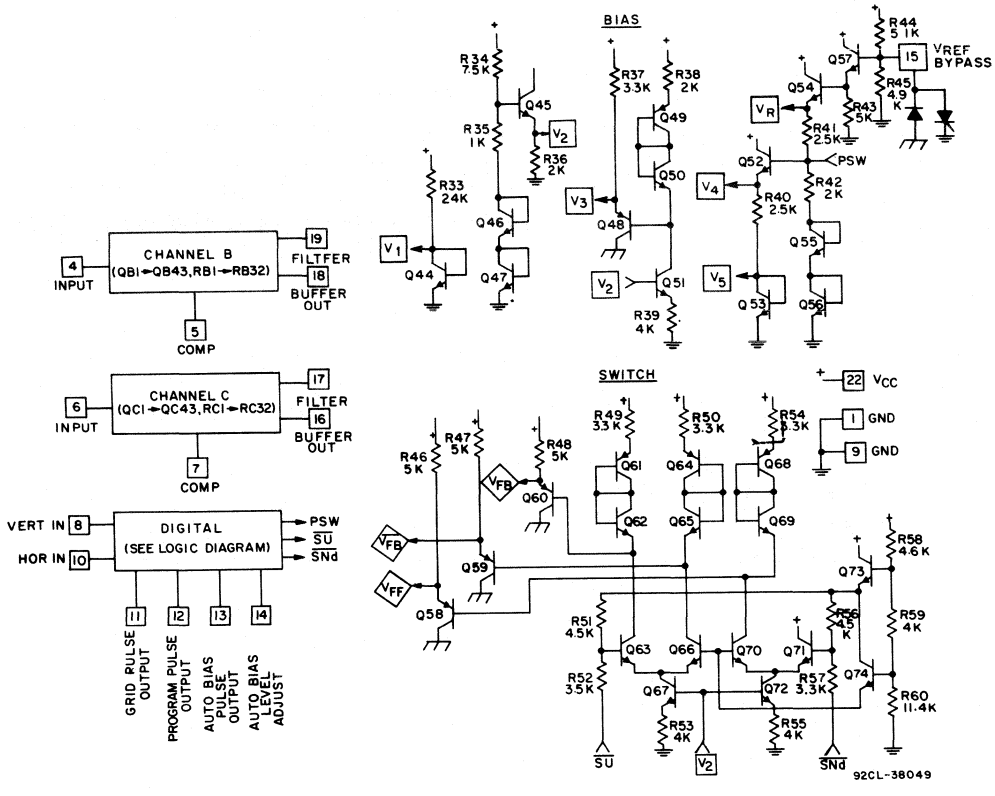


Fig. 2 - Schematic diagram (continued from previous page).

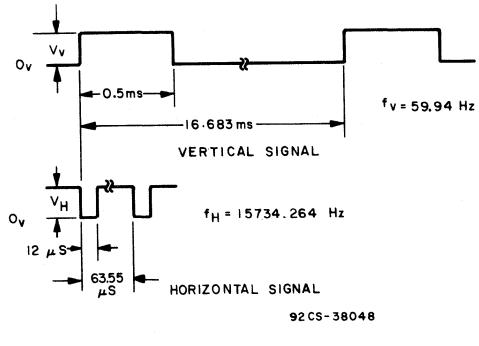


Fig. 4 - Vertical and horizontal input signals.

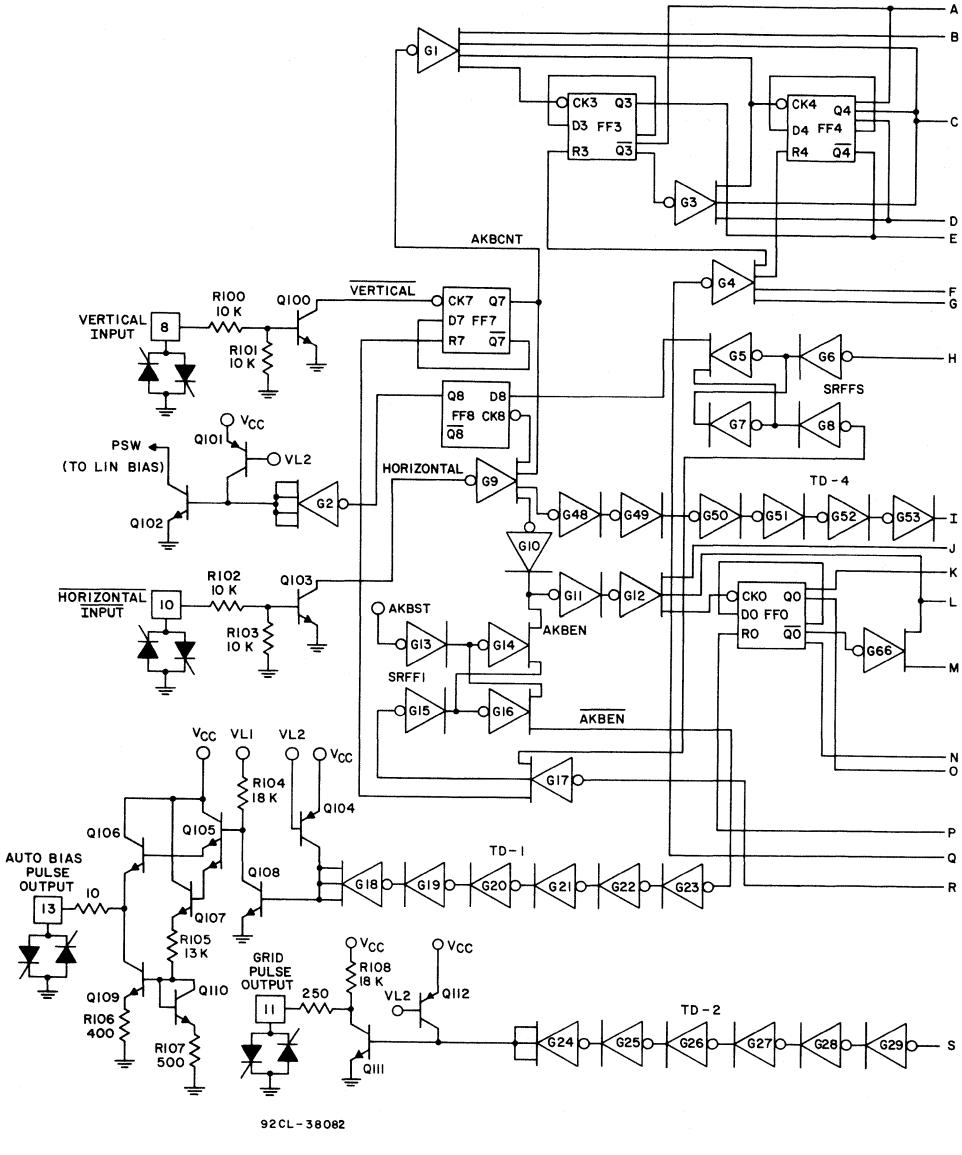


Fig. 5 - Logic diagram (continued on next page).

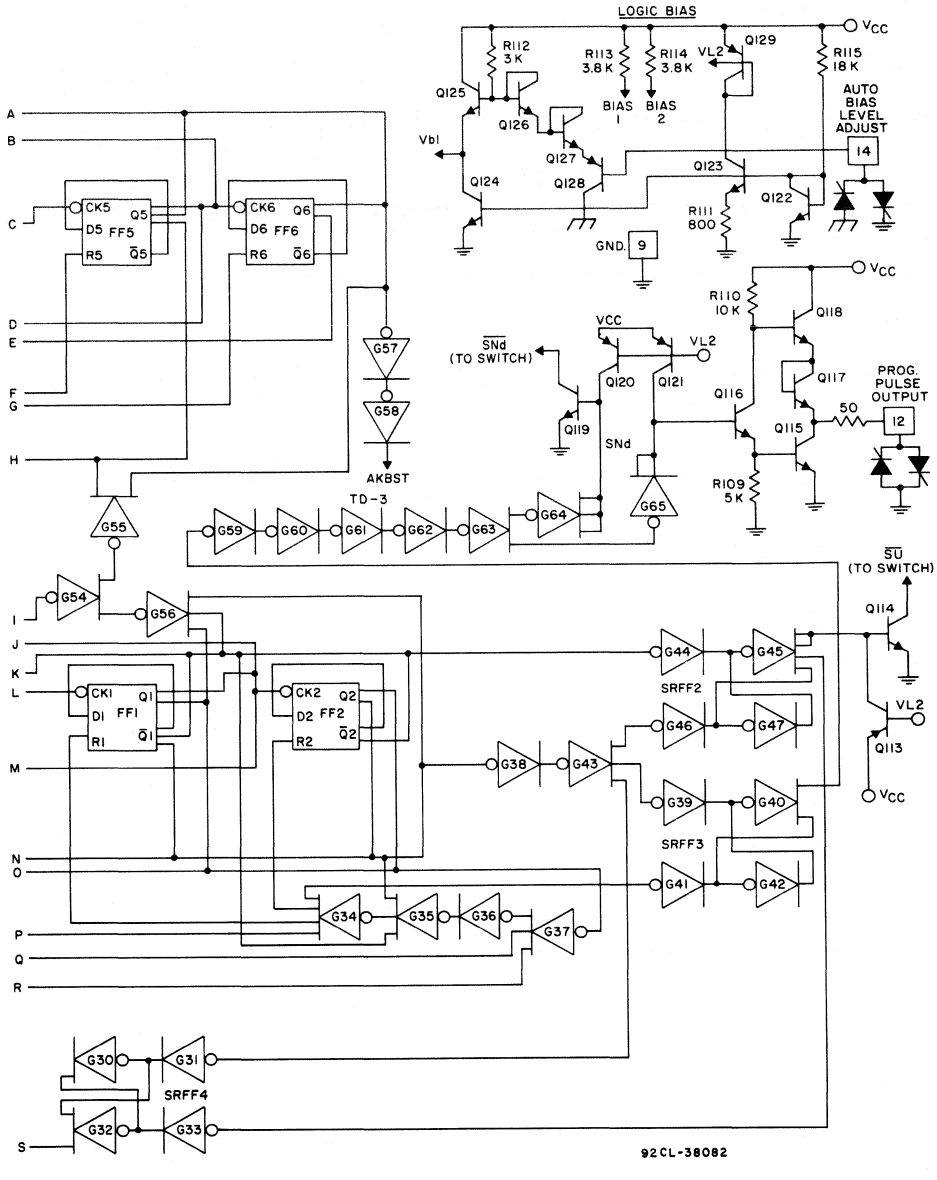


Fig. 5 - Logic diagram (continued from previous page).

CA3224

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{CC} = 10 V, V_{BIAS} = 3.75 V, V_V = V_H = 6.0 V, S_1 = A, S_2 = A Unless otherwise specified

CHARACTERISTIC	TEST PIN NO.	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
				MIN.	TYP.	MAX.	
Supply Current	22	I_C				65	mA
Reference Voltage	2, 4, 6	V_{REF}	Measure at t_4	5.6	6.0	6.4	V
Input Current	2, 4, 6	I_I	V_{IN} = 7.2 V, S1 = B			250	nA
Output Current	17, 19, 21		Measure at t_6, S1 = B				
Source		I_{OM}^+	V_{BIAS} = 0.5 V			-0.8	mA
Sink		I_{OM}^-	V_{BIAS} = 7.0 V	0.8			mA
Output Buffer	17, 19, 21		Measure at t_4, S1 = B				
Input Current		I_I	V_{OUT} = 6.5 V, V_{IN}			150	nA
Voltage Gain		A_V	@ pins 16, 19, 20	0.97		1.07	—
Transconductance	17, 19, 21	gm	Measure at t_6, V_{IN}=8mVp-p @ 40 kHz, S1 = B	50		100	mmho
Auto Bias Pulse	13						
Output Low		V_{OL}	Measure at t_1			0.3	V
High		V_{OH}	Measure at t_4	6.05			V
Current Sink		I_{OM}^-	Measure at t_4, S2 = B	2.5			mA
Grid Pulse Output	11						
Low		V_{OL}	Measure at t_4			0.4	V
High		V_{OH}	Measure at t_1	4.2			V
Program Pulse Output	12						
Low		V_{OL}	Measure at t_6			0.4	V
High		V_{OH}	Measure at t_1	8.2			V
Vertical Input	8	V_V	See Fig. 3		6.0		V
Horizontal Input	10	V_H	See Fig. 3		6.0		V
Auto Bias Pulse	13		Note 1				
Timing Start			t_0 to t_2	835		842	μs
Finish			t_0 to t_7	1270		1275	μs
Grid Pulse Timing	11		Note 1				
Start			t_0 to t_3	899		905	μs
Finish			t_0 to t_5	1080		1084	μs
Program Pulse Timing	12		Note 1				
Start			t_0 to t_5	1080		1084	μs
Finish			t_0 to t_7	1270		1275	μs

Note 1: All time measurements are made from 50% point to 50% point.

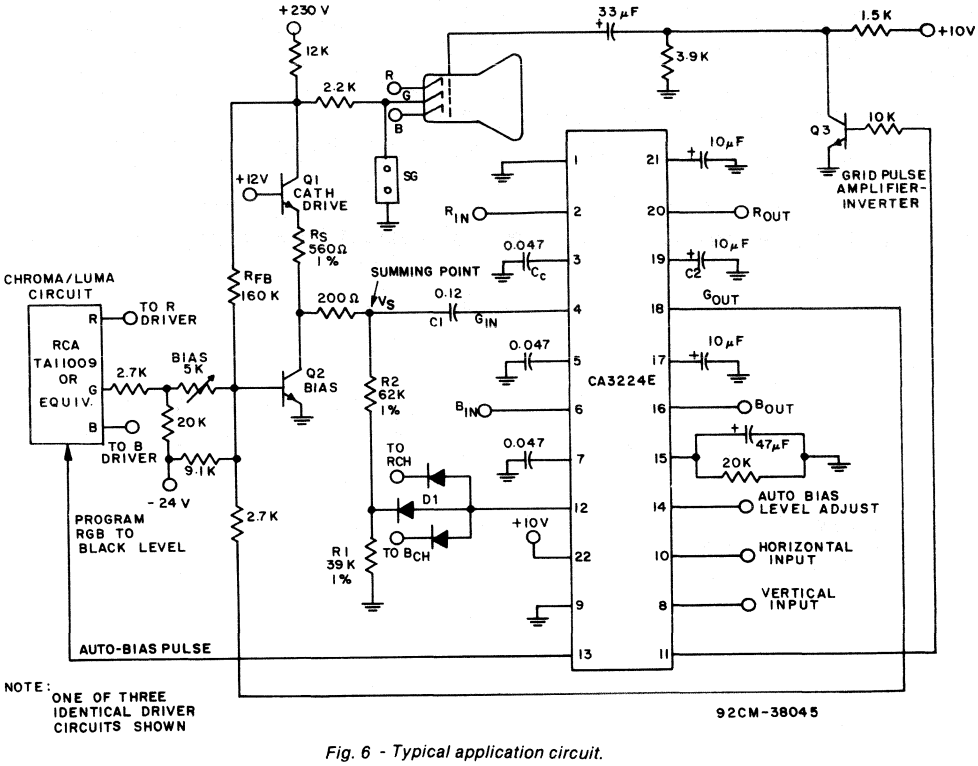


Fig. 6 - Typical application circuit.

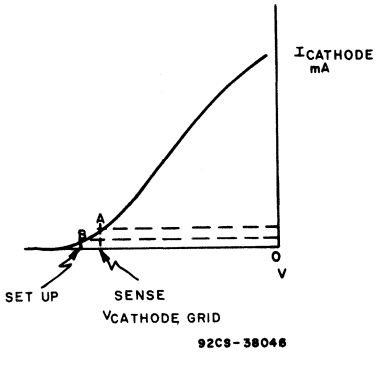


Fig. 7 - Picture tube V-I curve.

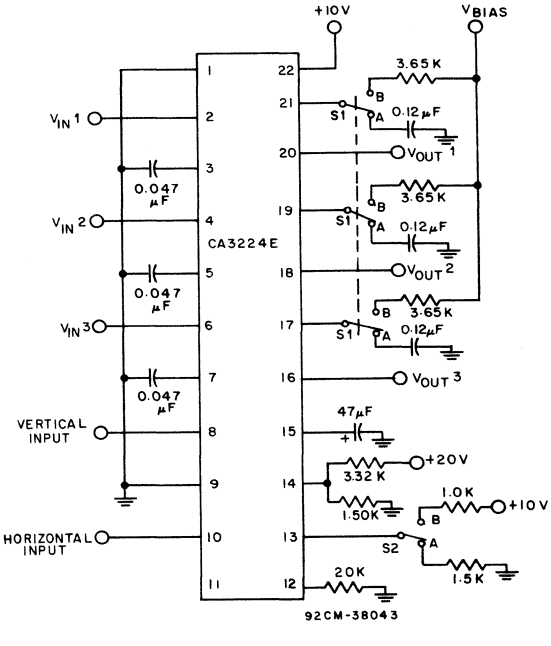


Fig. 8 - Test circuit.

CA3224

ELECTRO STATIC PROTECTION *

When correctly designed for ESD protection, SCRs can be highly effective, enabling circuits to be protected to well in excess of 4 KV. The SCR ESD-EOS protection structures used on each terminal of the CA3224E are shown schematically in either Fig. 9a. or 9b. Although ESD-EOS protection is included in the CA3224E, proper circuit board layout and grounding techniques should be observed.

* For further information on CA3224E protection structures refer to: "Using SCR's as transient protection structures in Integrated Circuits", by L.R. Avery, RCA ICAN-7304 reprint.

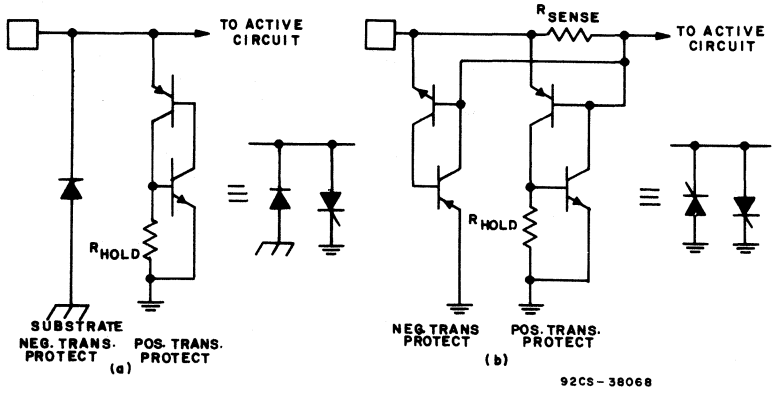


Fig. 9 - Transient protection.

Product Preview

CA3254, CA3255

RS-170 Sync Generator (CA3254)

Features:

- *Single LSI IC with multiple genlock capability*
- *EIA RS-170 Sync with 2:1 Interlace*
- *PLL for lock to power line zero crossing*
- *Genlocks to RS-170, RS-330 or random interlace*
- *Crystal control mode sync option*
- *Four modes of genlock control*
- *Maximum of external components*
- *I^2L injection configured to work in series with the camera tube filament*

The RCA CA3254• is an integrated circuit sync generator with all functions required to provide EIA RS-170 standard sync for signal processing in cameras and video applications where RS-170 2:1 interlaced sync is needed. The CA3254 is processed in integrated injection logic which provides advantages of combined linear integrated circuit compatibility with functions that enhance the performance of the sync system. These functions include a 60 Hz phase locked loop to synchronize to the power line frequency, horizontal and vertical drive processing circuits which process the drive signals for logic and V_{CO} control.

Horizontal and vertical drive may be applied to their respective inputs for genlock operation. When external drive is present, the system automatically switches to external control. Composite sync may be applied in parallel directly to the horizontal and vertical drive inputs as an option. Operation from a dc power source requires the use of the 64 times horizontal frequency crystal reference. The genlock accepts RS-170, RS-330, or random interlace sync.

The CA3255• is available for 625-line, 50-Hz systems.

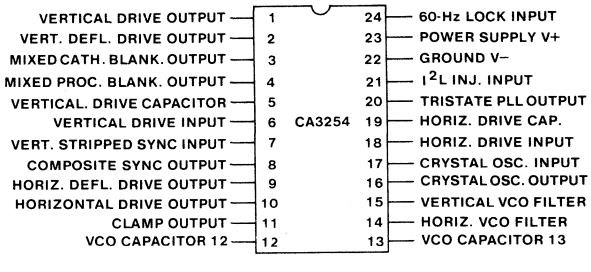
•Formerly RCA Development Type No. TA10466 (CA3254) and TA10985 (CA3255).

Applications:

- *All RS-170 Sync systems*
- *Security cameras*
- *CCTV systems*
- *Cable systems*
- *Text encoder sync*
- *Computer display systems*
- *Graphics systems*

The PLL synchronizes the V_{CO} to the power line zero crossing which provides clean switching, splitting and time lapse V_{CR} performance. The available output signals are as follows: horizontal drive, horizontal deflection drive, clamp, vertical drive, vertical deflection drive, mixed cathode blanking, mixed process blanking, and composite sync (RS-170, 2:1 interlace).

The CA3254 device is supplied in a 24-lead dual-in-line plastic package (E suffix).



TERMINAL ASSIGNMENT

File Number **1705**

CA3254, CA3255

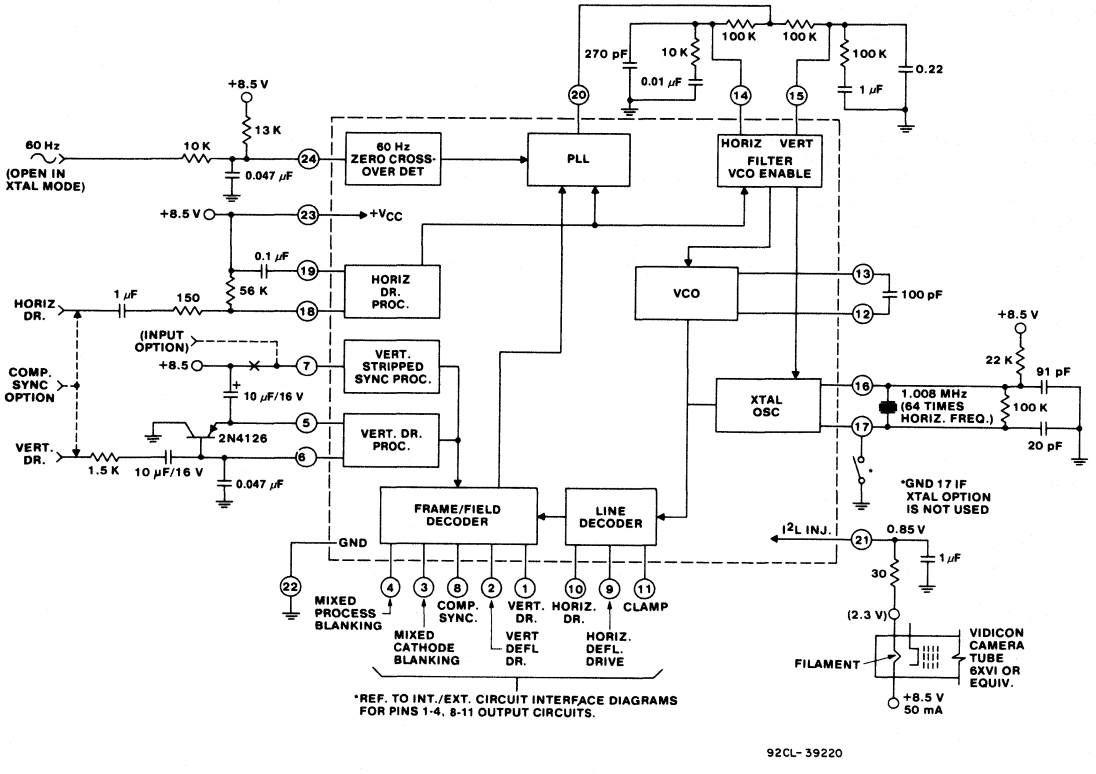


Fig. 1 - Functional block diagram of the CA3254 sync generator.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY:
- Terminal 23, V_{CC} ..... 11 V
- Terminals 1, 2, 3, 9, 10 I_{SINK} ..... 5 mA
- Terminals 4, 8, 11 I_{SINK}, I_{SOURCE} ..... ±5 mA

DEVICE DISSIPATION:
- Up to +70° C ..... 695 mW
- Above +70° C ..... Derate linearly at 8.7 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating ..... 0 to 70° C
- Storage ..... -55 to +150° C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... 265° C

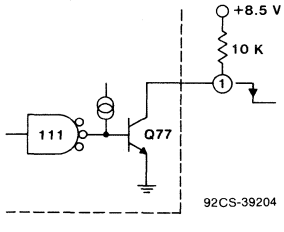
CA3254, CA3255

PERFORMANCE CHARACTERISTICS
(See Internal Circuit Interface for loads)

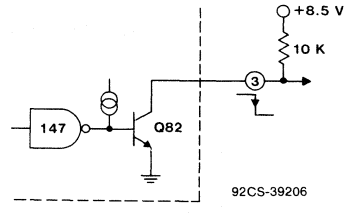
Typical Power Supply	8.5 V
Supply Voltage Range	7.5 to 10.5 V
Power Supply Current @ 8.5 V	20 mA
Injection Current Input @ Pin 21	50 mA
60-Hz Power Line Sync Input	8 V_{p-p}
Typical Horizontal and Vertical Drive Input	4 V_{p-p}
Horizontal/Vertical Drive Input Range	3 to 6 V_{p-p}
Vertical Stripped Sync Input Range	3 to 6 V_{p-p}
Vertical Drive Output	8 V_{p-p}
Vertical Deflection Drive Output	8 V_{p-p}
Horizontal Drive Output	8 V_{p-p}
Horizontal Deflection Drive Output	8 V_{p-p}
Mixed Cathode Blanking Output	8 V_{p-p}
Clamp Output	8 V_{p-p}
Mixed Process Blanking Output	8 V_{p-p}
Composite Sync Output	8 V_{p-p}
TIMING - HORIZONTAL:	
Horizontal Blanking	0 to 11 μsec.
Horizontal Sync	1.5 to 6 μsec.
Equalization	1.5 to 4 μsec.
Serration	-3.5 to 1.5 μsec.
Clamp	3 to 5 μsec.
Horizontal Drive	0 to 6 μsec.
Horizontal Deflection Drive	0 to 11 μsec.
Cathode Blanking	1.5 to 8.5 μsec.
TIMING - VERTICAL:	
Vertical Blanking	0 to 20H
Equalization	0 to 3H and 6 to 9H
Serration	3 to 6H
Vertical Drive	0 to 9H
Vertical Deflection Drive	3 to 9H
Reset Disable	510 to 18+ serrations

CA3254 INTERNAL/EXTERNAL CIRCUIT INTERFACE

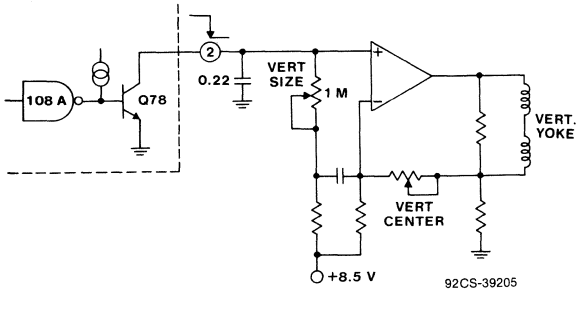
PIN 1: VERTICAL DRIVE OUTPUT



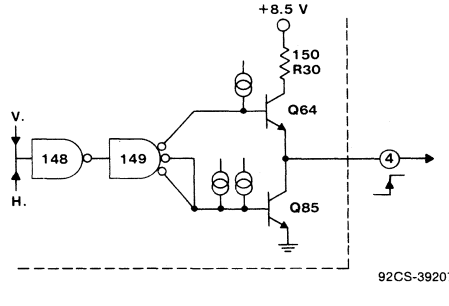
PIN 3: MIXED CATHODE BLANKING OUTPUT



PIN 2: VERTICAL DEFLECTION DRIVE OUTPUT



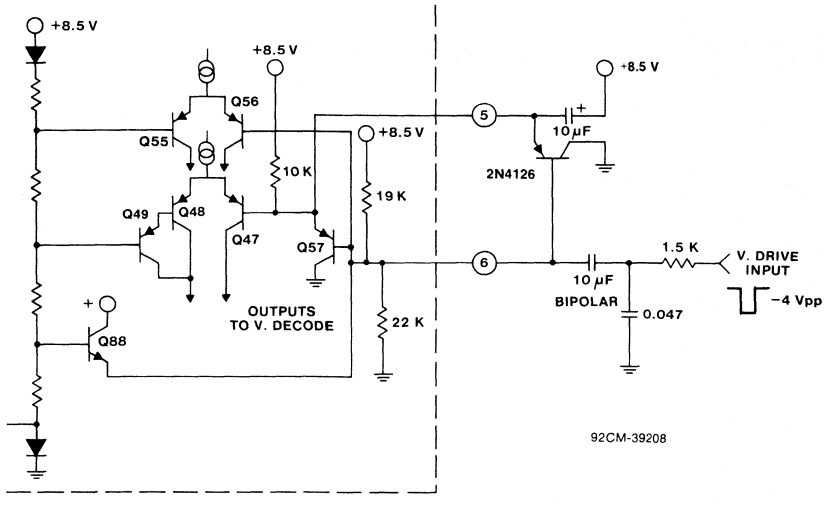
PIN 4: MIXED PROCESS BLANKING OUTPUT



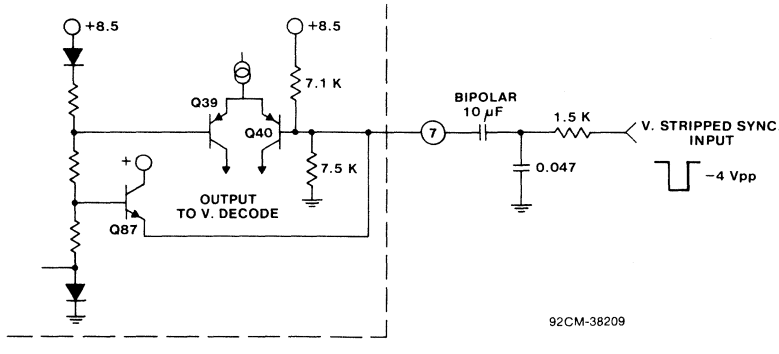
CA3254, CA3255

CA3254 INTERNAL/EXTERNAL CIRCUIT INTERFACE (Continued)

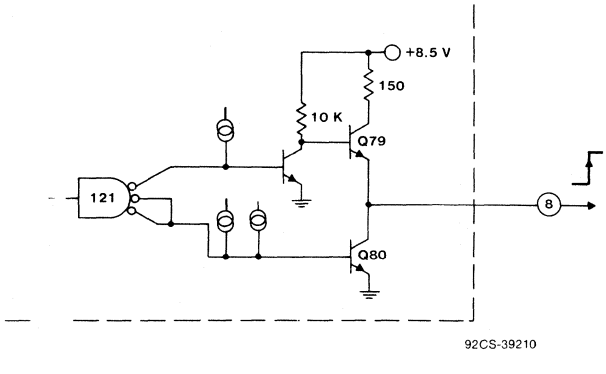
PIN 5 & 6: VERTICAL CAP. AND VERTICAL DRIVE INPUT



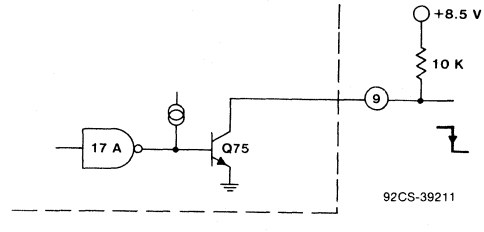
PIN 7: VERTICAL STRIPPED SYNC INPUT



PIN 8: COMPOSITE SYNC OUTPUT

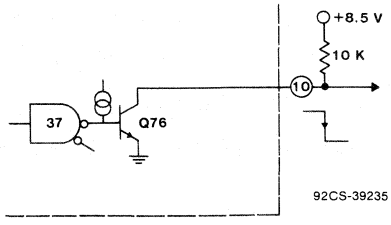


PIN 9: HORIZONTAL DEFLECTION DRIVE OUTPUT

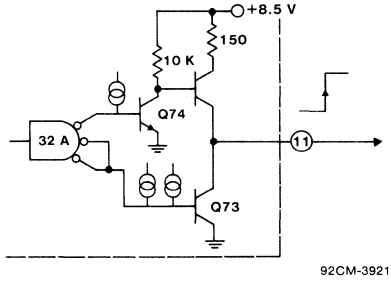


CA3254 INTERNAL/EXTERNAL CIRCUIT INTERFACE (Continued)

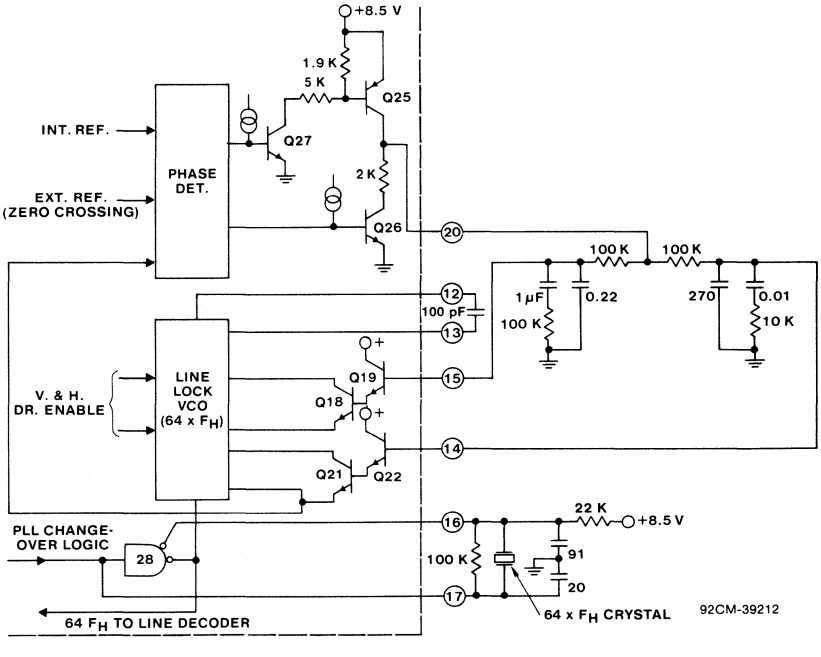
PIN 10: HORIZONTAL DRIVE OUTPUT



PIN 11: CLAMP OUTPUT



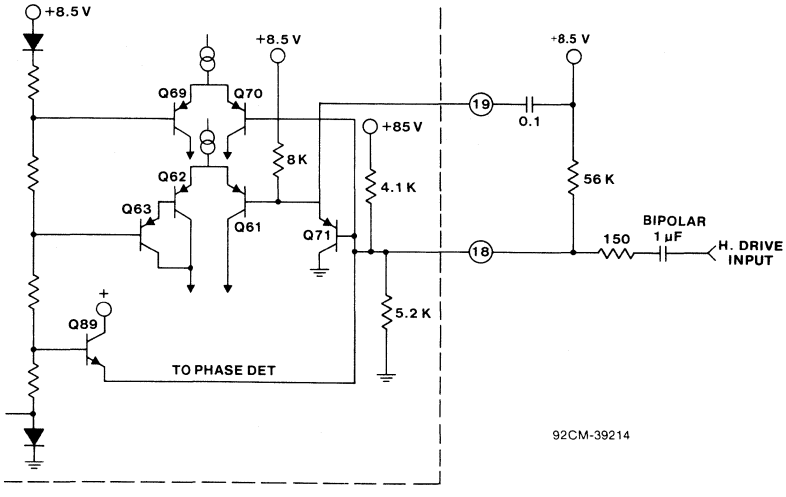
PINS 14 & 15: VERTICAL AND HORIZONTAL FILTER
PINS 16 & 17: CRYSTAL OSCILLATOR
PIN 24: 60 HZ SIGNAL INPUT FOR LINE LOCK
PIN 20: TRISTATE PHASE DETECTOR OUTPUT
PINS 12 & 13: VCO CAPACITOR



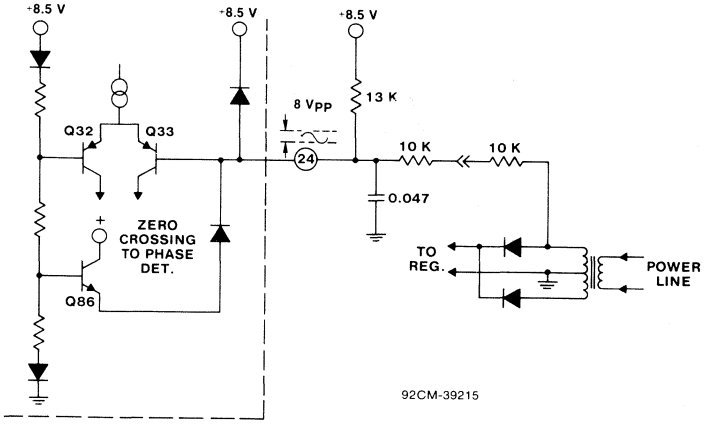
CA3254, CA3255

CA3254 INTERNAL/EXTERNAL CIRCUIT INTERFACE (Continued)

PINS 18 & 19: HORIZONTAL DRIVE INPUT



PIN 24: 60-HZ SIGNAL INPUT



APPLICATION INFORMATION

SYNC GENERATOR

The sync generator is a 24 pin IC requiring a single +8.5 V_{DC} power source. It supplies all pulses required for 2:1 interlaced 525/60 Hz EIA RS-170 sync timing.

For 625/50 Hz operation, a CA3255 IC is available. A 24-pin IC socket permits easy changing of the sync generator IC for either 525/60 Hz or 625/50 Hz.

The normal mode of operation is a zero crossing line lock mode, but the generator may operate crystal controlled or be externally driven.

For crystal operation, the 525/60 Hz crystal frequency is 1.008 MHz and for 625/50 Hz, the crystal frequency is 1 MHz. For NTSC sync operation the 64 times horizontal crystal frequency is 1.006993 MHz and is externally phase locked to the 3.579545 MHz (f_c) color sub carrier, where $f_H = 2f_c/455$.

Circuit Operation

An AC sine wave signal is fed into Pin 24 to synchronize to the zero crossing of the power line. R44 and R45 form a voltage divider to optimize the zero crossing point. There is also a short circuit protection resistor in the externally power supply in series with R44 - (10K). This resistor is part of the zero crossing voltage divider. C33 filters any spikes which might occur at the zero crossing.

Pin 23 is the +8.5 V_{DC} input and is filtered by C34.

Pin 22 is the common and is tied to case ground.

Pin 21 is the injector input to operate part of the logic. The injector requires +0.85 V_{DC} at approximately 50 mA DC. To save power, the injector voltage is taken in series with the filament of the vidicon. C35 is a filter for the injector. A 150-ohm/0.5 watt resistor to +8.5 V may be used in place of the 30-ohm resistor and vidicon filament in series.

Circuit Operation (cont'd)

Pin 20 is a filter for the internal Phase Line Lock Loop with components R52, R54, C41, and C42 forming the filter required for vertical stability.

Pin 19 detects the presence of horizontal by the charging of C36 when external sync is used.

Pin 18 is the external horizontal input with an input impedance of about 2 K. R120 is part of the input bias of the stage - the remainder is inside the IC. C37 provides DC blocking and R48 is a series limiting resistor. Typical input is 4 V p-p, but will operate between 3 V p-p and 6 V p-p.

Pin 17 is grounded in the normal Line Lock mode of operation by a jumper wire in place of C38.

Pins 17 and 16 are used in the Crystal mode of operation - refer to the Crystal Option section of the drawing. R49 is the load resistor for the crystal oscillator. Capacitor C38 and C39 establish the 180° phase shift required for Crystal Y1 to oscillate, and R51 assists in starting the oscillator.

Pin 15 is the Vertical Voltage Controlled Oscillator (VCO) input. The vertical VCO is operational in the line lock mode, but not in the crystal mode.

Pin 14 is the Horizontal Voltage Controlled Oscillator (VCO) input and is automatically switched in when horizontal drive or sync is present.

Pins 12 and 13 are terminals to the internal circuit and add the required capacitor C48 to operate the Voltage Controlled Oscillator (VCO) used during the line lock and external drive modes.

Pin 11 is a horizontal rate 8 V p-p positive output pulse which is 2 μs wide and is used to drive the clamp circuit in the video amplifier.

Pin 10 is the horizontal drive output.

Pin 9 is a horizontal rate negative going output pusle driving the horizontal deflection. It is 10 μs wide and has a 0.65 V p-p amplitude. The amplitude is limited to 0.65 V p-p by the emitter base junction of Q7 in the Horizontal Deflection Circuit.

Pin 8 is the composite sync output and delivers 8 V p-p positive going pulses to the video amplifier to add to video. The signal contains vertical sync, horizontal sync, equalizing and serrating pulses per RS-170 specifications.

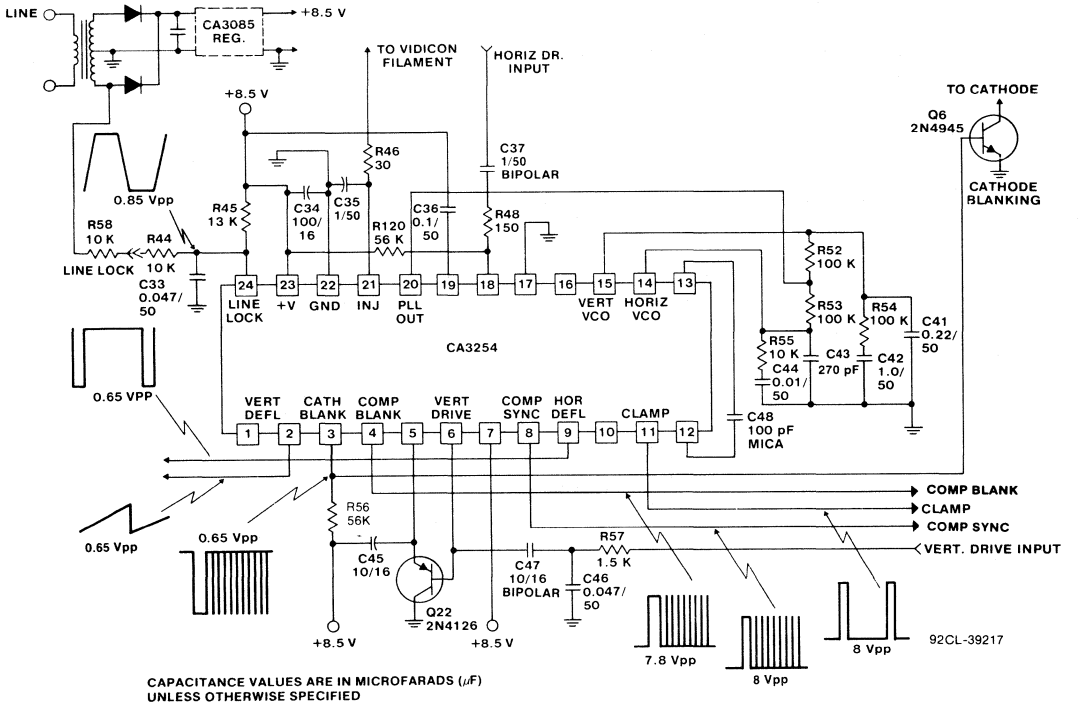


Fig. 2 - Application of the CA3254 device.
(Shown in line lock mode)

CA3254, CA3255

Circuit Operation (cont'd)

Pin 7 if not used is tied to the +8.5 V_{DC}. It is a vertical stripped sync input equivalent to vertical drive input.

Pin 6 is the external vertical drive or composite sync input normally requiring 4 V p-p, but will operate between 3 and 6 V p-p. R57 and C46 integrate the signal to remove horizontal and C47 is a DC blocking capacitor.

Pin 5 detects the presence of external vertical drive by the charge placed on C45. Q22 is a follower used to prevent C45 loading the vertical drive input on Pin 6.

Pin 4 supplies positive going 7.8 V p-p mixed horizontal and vertical blanking pulses to the video amplifier per RS-170 specifications. Vertical blanking is approximately 1.3 ms and horizontal blanking is approximately 11 μs.

Pin 3 supplies negative going horizontal and vertical 0.65 V p-p pulses to the cathode blanker Q6. The amplitude of the pulses are limited to 0.65 V p-p by the emitter base of Q6. The width of the vertical pulses are approximately 200 μs and the horizontal is 7 μs. R56 is a pull up resistor for Pin 3 bias.

Pin 2 supplies negative going pulses to the vertical deflection circuit. These pulses act as a switch during vertical retrace time and appear as a sawtooth due to capacitor C32 in the vertical deflection circuit. This sawtooth is typically near 0.65 V p-p.

Pin 1 is the vertical drive output.

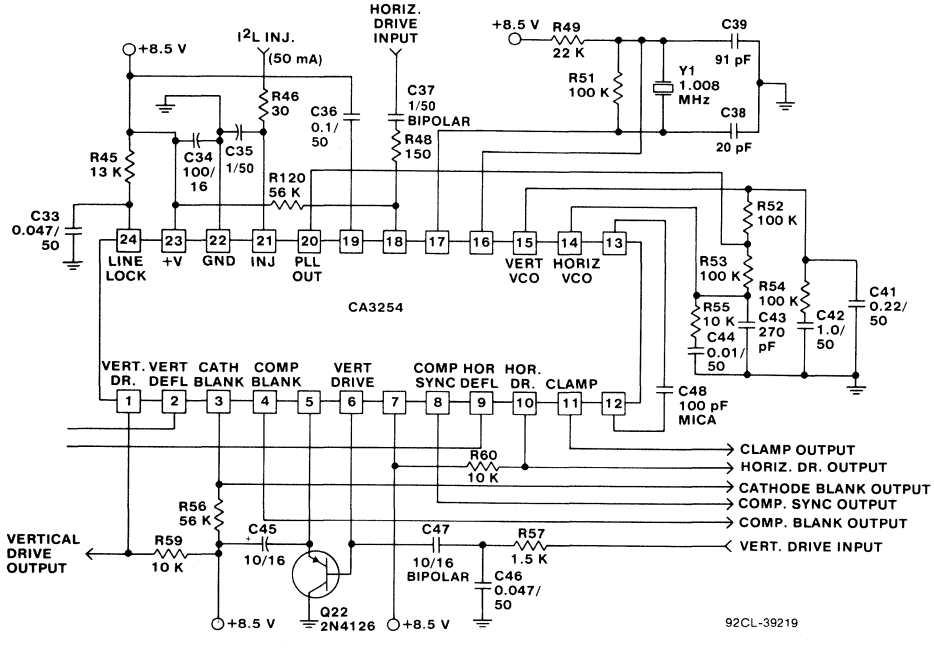
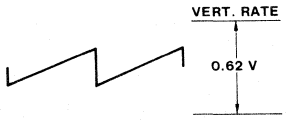
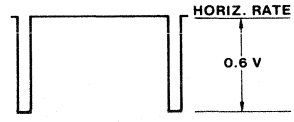


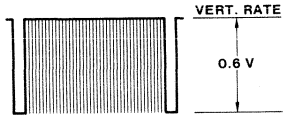
Fig. 3 - Crystal mode of operation.



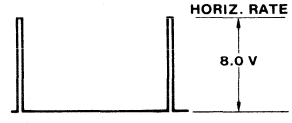
PIN 2 — VERTICAL DRIVE



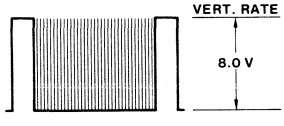
PIN 9 — HORIZONTAL DRIVE



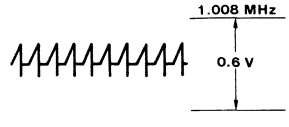
PIN 3 — CATHODE BLANKING



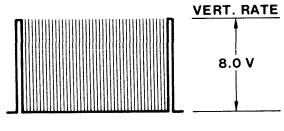
PIN 11 — CLAMP



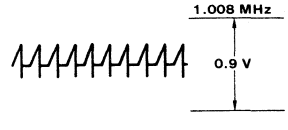
PIN 4 — COMPOSITE BLANKING



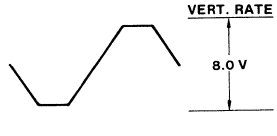
PIN 12 — OSCILLATOR



PIN 8 — COMPOSITE SYNC



PIN 13 — OSCILLATOR



92CM-39216

PIN 24 — LINE LOCK

Fig. 4 - Waveforms (See Fig. 2)

CA3254, CA3255

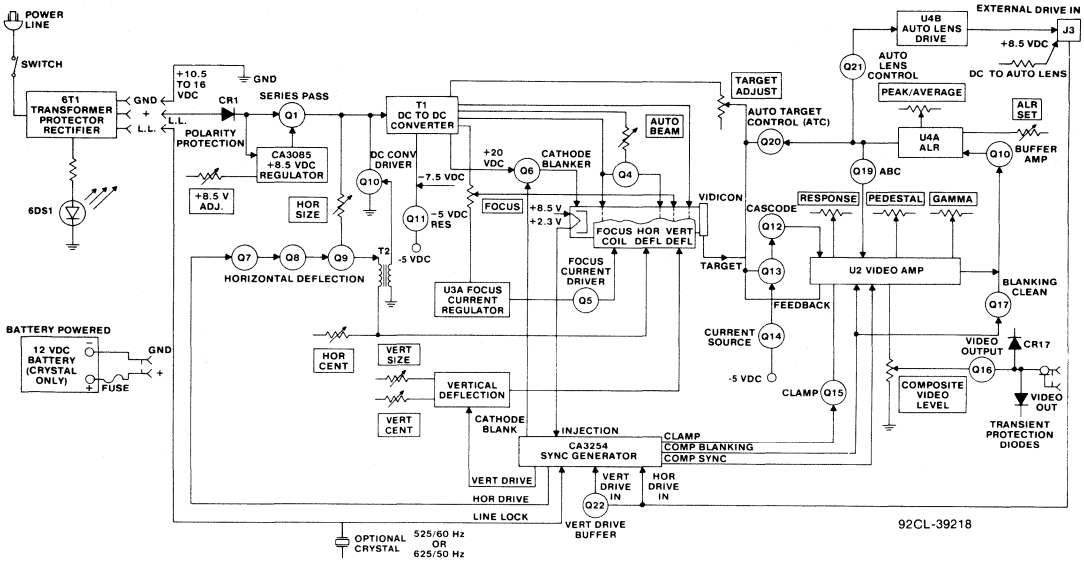


Fig. 5 - Block diagram of camera system.
(RCA-TC2000 series CCTV camera)

Product Preview

CA3256

CMOS/BiMOS Analog Video Switch and Amplifier

Features:
- *5 Multiplex video channels*
  1 independent channel
  4 channels with inhibit
- *4 LED channel indicator outputs with 30-mA sink/source current*
- *Wideband video amplifier - 25-MHz unity gain*
- *Programmable video amplifier gain*
- *High signal-drive capability*

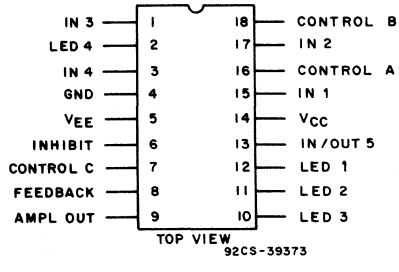
The RCA-CA3256* CMOS/BiMOS analog video switch has five channels of CMOS multiplex switching for general-purpose video signal control. One of four CMOS channels may be selected in parallel with channel 5. The CMOS switches are inputs to the video amplifier but may be used in bilateral switching between channels 1 to 4 and channel 5. The analog switches of channels 1 to 4 are digitally controlled with logic level conversion and binary decoding to select 1 of 4 channels. The inhibit function controls channels 1 to 4 but does not affect channel 5. LED output drivers are selected with the channel 1-to-4 switch selection to indicate the ON-channel. Channel 5 may be used as a monitor output for data or signal information on channels 1 to 4. The transmission gate switches shown in the block diagram of the CA3256 are configured in a "T" design to minimize feedthrough. When the switch is off, the shunt or center of the "T" is grounded.

The amplifier has high input impedance to minimize the R_{on} transmission gate insertion loss. The amplifier output impedance is typically less than 10 ohms in a complementary symmetry output. The amplifier can directly drive a nominal 75-ohm coaxial cable to provide line-to-line video switching. The gain of the amplifier is programmable by different feedback resistor values between pins 12 and 13. Compensation may also be used between these pins for an optimally flat frequency response. An internal regulated 5-V dc bias reference with temperature compensation permits stable direct-coupled output drive and minimizes dc offset during signal switching.

The CA3256 device is available in an 18-lead dual-in-line plastic package (E suffix).

*Formerly RCA Developmental Type No. TA13041.

Applications:
- *Video multiplex switch*
- *75-ohm video amplifier/line driver*
- *Video signal level control*
- *Monitor switching control*
- *TV/CATV audio/video switch*
- *Video signal adder/fader control*



TERMINAL ASSIGNMENT

File Number **1769**

CA3256

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE, V_{CC}(Ref. to V_{EE}) ..... 10 to 18 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... V_{EE} to V_{CC} V
AMPLIFIER OUTPUT CURRENT ..... 30 mA
DC LED SINK CURRENT ..... 30 mA
DEVICE DISSIPATION:
  Up to T_A = 55° C ..... 630 mW
  Above T_A = 55° C ..... Derate linearly at 6.67 mW/° C
TEMPERATURE RANGE:
  Operating ..... -40 to +85° C
  Storage ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

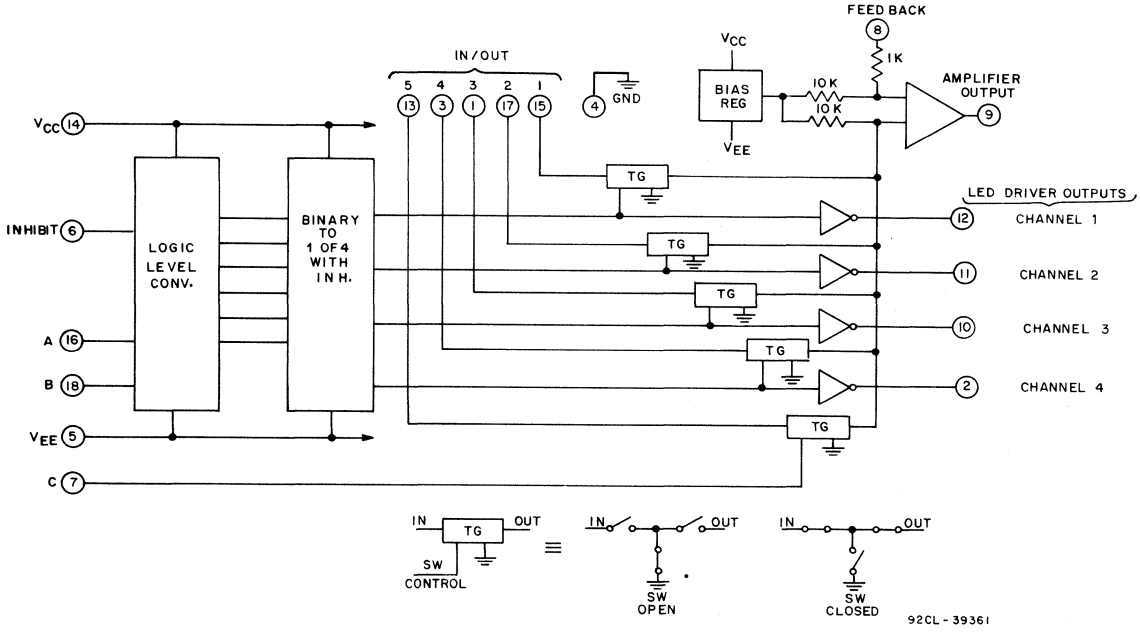


Fig. 1 - Block diagram of the CA3256.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TYPICAL VALUES		UNITS
Power Supply Voltage	10 to 18		V dc
Power Supply Current	20		mA
	SWITCH	AMPLIFIER	
Open Loop Gain A_{OL}	—	40	dB
Prog. Gain, FB Adj. 1% Linearity Range	—	-0.8 to +15	
Power Bandwidth	40	10	MHz
Unity Gain Bandwidth, 1 KΩ, 2 pF Compensation	—	24	
Distortion, 1 V Input	0.1	—	%
7 V_{p-p} in 1 KΩ	—	1	
2 V_{p-p} in 75 Ω	—	1	
Insertion Loss	-0.8	—	dB
Signal Feedthrough, 5 MHz	-66	—	
Clock Feedthrough	—	TBD	
Input Impedance Z_{IN}	—	10	KΩ
Output Impedance Z_{OUT}	—	5 to 10	Ω
Maximum Input Voltage V_I(max.)	3	2.5	V_{p-p}
Maximum Output Voltage V_O(max.)	—	7	
Reference Bias Output Voltage	—	5±2% (ABS)	V dc
DC Output Bias Stability Gain 5X	—	100	ppm/°C
Differential Gain	—	1	%
Differential Phase	—	1	°C
DC Offset, Reference Switch Input	—	1 to 2	mV dc
DC Offset, Between Inputs	—	1 to 2	
DC Offset, Switch to Amplifier Output, Gain 2X	—	25	
Off Isolation, Channel to Channel, Z_{IN} = 75 Ω	-66	—	dB
Switch Turn On/Off Time Delay	—	60	ns
Maximum Switch Frequency	—	8	MHz
Maximum LED Sink Current	—	30	mA

CA3256

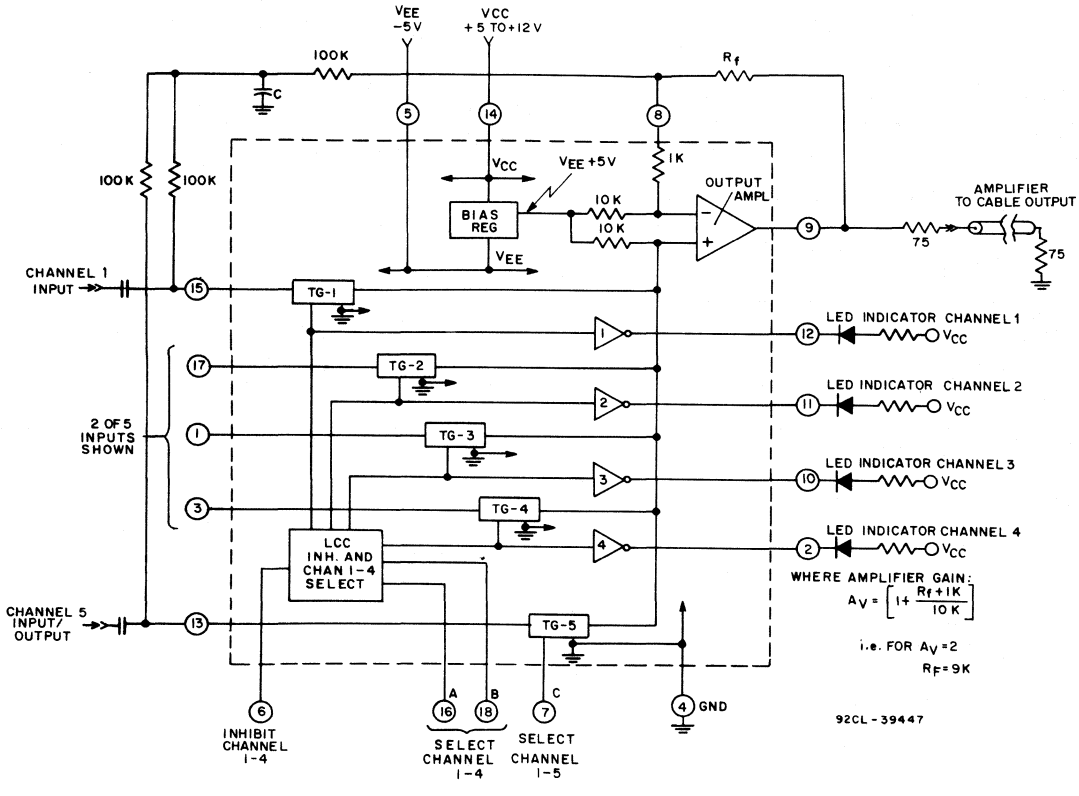


Fig 2 - (a) Typical application bias circuit direct-coupled output with V_{EE} = -5 V.

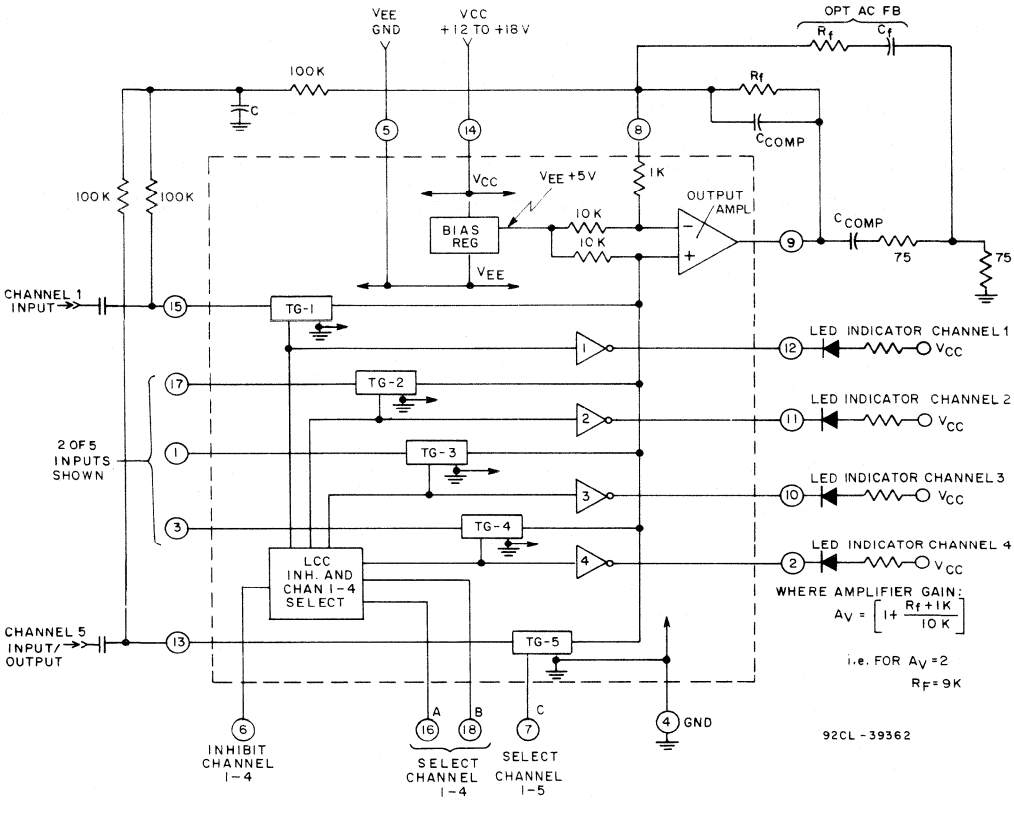


Fig. 2 – (b) Typical application bias circuit ac-coupled input with optional ac feedback, V_{EE} = Gnd.

CD22402

CMOS LSI Sync Generator

For TV Applications and Video Processing Systems

Features:
- *Interlaced composite sync output*
- *Automatic genlock capability*
- *Crystal oscillator operation*
- *525 or 625 line operation*
- *Vertical reset option*
- *Wide power supply operating voltage, 4-15 V*

The RCA CD22402• is a CMOS LSI sync generator that produces all the timing signals required to drive a fully 2-to-1 interlaced 525-line 30-frame/second, or 625-line 25-frame/second TV camera or video processing system. A complete sync waveform is produced which begins each field with six serrated vertical sync pulses, preceded and followed by six half-width double frequency equalizing pulses. The sync output is gated by the master clock to preserve horizontal phase continuity during the vertical interval.

The CD22402 can be operated either in "genlock" mode, in which it is synchronized with a reference sync pulse train from another TV camera, or in "stand-alone" mode, in which it is synchronized with a local on-chip crystal oscillator (the crystal and two passive components are off chip). Also, the circuit can sense the presence or absence of a reference sync pulse train, and automatically select the "genlock" or "stand-alone" mode.

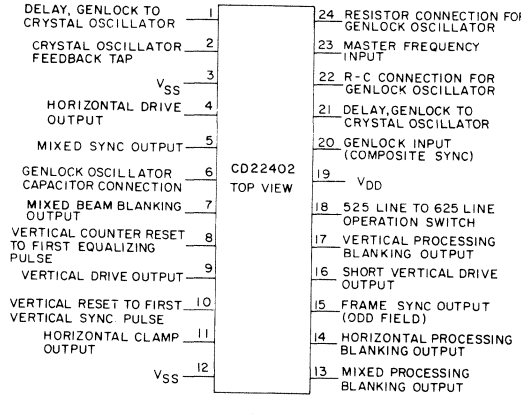
A frame sync pulse is produced at the beginning of every odd field. The vertical counter can be reset to either the first equalizing pulse or the first vertical sync pulse of the vertical interval.

The interlaced sync provided by the CD22402 differs from RS-170 by having slightly narrower sync and equalizing pulses. The clock frequency of 32 times horizontal rate allows for approximately 4 μs horizontal pulse widths and 2 μs equalizing pulses. Otherwise operation can be phase locked to a color sub-carrier for a full interlaced operating system.

The CD22402 is operable with a single supply over a voltage range of from 4 to 15 volts. It is supplied in a 24-lead dual-in-line ceramic package (D suffix) or a 24-lead dual-in-line plastic package (E suffix).

•Formerly RCA Developmental Type No. TA6993.

Applications:
- *Cameras*
- *Monitors and Displays*
- *CATV*
- *Teletext*
- *Video Games*
- *Sync Restorer*
- *Video Service Instruments*



92CS-26631R1

TERMINAL ASSIGNMENT

File Number **1686**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... 15 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... $V_{SS} \leq V_I \leq V_{DD}$
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A=+60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A=-55 to +100°C (PACKAGE TYPE D) ..... 500 mW
For T_A=+100 to 125°C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A=FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

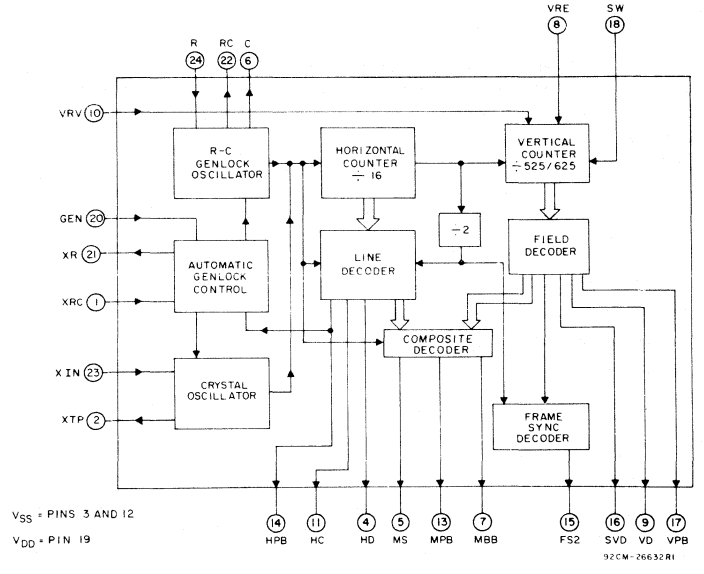


Fig. 1 - Block diagram of CD22402 monochrome TV sync generator with automatic genlock.

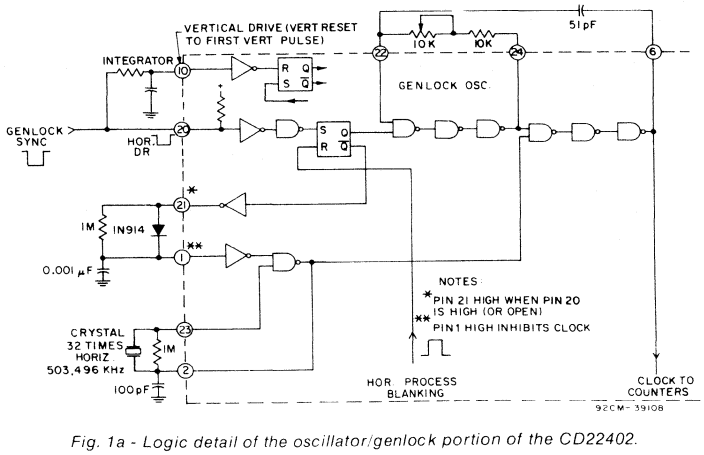


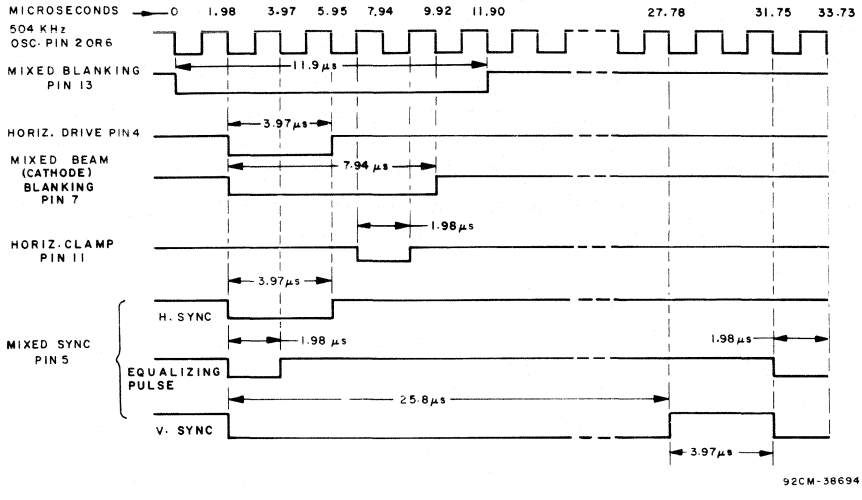
Fig. 1a - Logic detail of the oscillator/genlock portion of the CD22402.

CD22402

TERMINAL DEFINITIONS FOR RCA CD22402 SYNC GENERATOR

Terminal No.	Symbol	Function
1	XRC	**Delay, Genlock to Crystal Oscillator.** Resistor, diode and capacitor connection for delay that automatically turns on the crystal oscillator when the genlock input is removed. When the signal on terminal 1 is high the crystal oscillator is inhibited. Typical values for R and C are 1 MΩ and 0.001 μF. For operation as a crystal-controlled stand-alone sync generator without genlock, terminal 1 should be hard-wired to V_{SS}.
2	XTP	**Crystal Oscillator Feedback Tap.** Feedback connection (tap) for crystal oscillator. When a crystal (shunted by a 1 MΩ resistor) is connected between this terminal and terminal 23, and a 100-pF capacitor is connected from this terminal to V_{SS}, the sync generator creates its own master frequency. For a 525-line, 30-frame/second raster, the crystal frequency is 504.000 kHz*; and for a 625-line, 25-frame/second raster, the crystal frequency is 500.000 kHz*.
3	V_{SS}	**Negative Power Supply Voltage.** This terminal must be hard-wired to terminal 12 (V_{SS}).
4	HD	**Horizontal Drive Output.**
5	MS	**Mixed Sync Output.**
6	C	**Capacitor Connection for R-C Genlock Oscillator.**
7	MBB	**Mixed Beam Blanking Output.**
8	VRE	**Vertical Counter Reset to First Equalizing Pulse.** A low-level signal on this terminal resets the vertical counter to the first equalizing pulse of a field. When not in use this terminal should be connected to V_{DD}.
9	VD	**Vertical Drive Output.**
10	VRV	**Vertical Counter Reset to First Vertical Sync Pulse.** A low-level signal on this terminal resets the sync generator to the first vertical sync pulse of a field. For genlock operation, terminal 10 is used as a resistor and capacitor connection for an integrator network that detects vertical sync pulses in a master sync waveform to which the sync generator is to be genlocked. R is 22 KΩ, and C is 0.001 pF. When not in use this terminal should be connected to V_{DD}.
11	HC	**Horizontal Clamp Output.**
12	V_{SS}	**Negative Power Supply Voltage.**
13	MPB	**Mixed Processing Blanking Output.**
14	HPB	**Horizontal Processing Blanking Output.**
15	FS2	**Frame Sync Output (Odd Field).** A pulse coinciding with the first equalizing pulse is produced at the beginning of every odd field.
16	SVD	**Short Vertical Drive Output.**
17	VPB	**Vertical Processing Blanking Output.**
18	SW	**Operation Switch for 525-Line or 625-Line Raster.** A high-level signal on terminal 18 causes the sync generator to generate a 625-line raster. An internal pull-down resistor is connected to terminal 18, so in the absence of an applied input to this terminal, a 525-line raster is produced.
19	V_{DD}	**Positive Power Supply Voltage.** V_{DD} can be any voltage between +4 and +15 relative to V_{SS}.
20	GEN	**Genlock Input Composite Sync.** A negative-going reference mixed sync waveform applied to terminal 20 disables the crystal oscillator and locks the R-C genlock oscillator to the horizontal pulses of the reference sync waveform. Vertical sync detection is achieved by an R-C integrator connected from terminal 20 to terminal 10 (vertical reset to first vertical sync pulse). An internal pull-up resistor is connected to terminal 20 so that in the absence of an applied input the crystal oscillator is enabled and the R-C genlock oscillator is disabled.
21	XR	**Delay, Genlock to Crystal Oscillator, Resistor and Diode Connection for Delay, Genlock to Crystal Oscillator.** Automatically turns on the crystal oscillator when the input to terminal 20 is removed.
22	RC	**Resistor and Capacitor Connection for Genlock Oscillator.** If the genlock oscillator is not used this terminal should be connected to V_{SS}. C should be 100 pF, and R should be a 10-KΩ potentiometer.
23	XIN	**Master Frequency Input.**
24	R	**Resistor Connection for Genlock Oscillator.**

*32 times horizontal frequency.



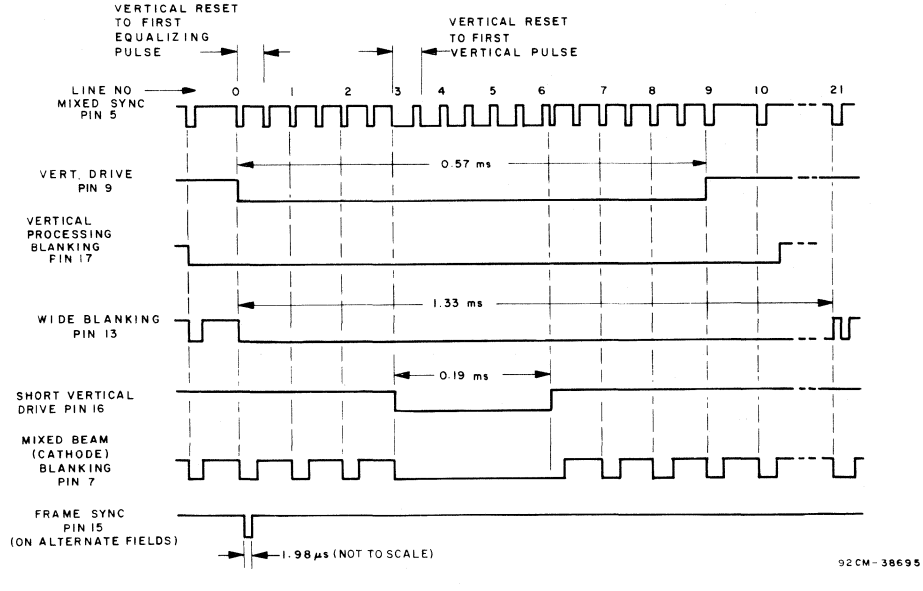
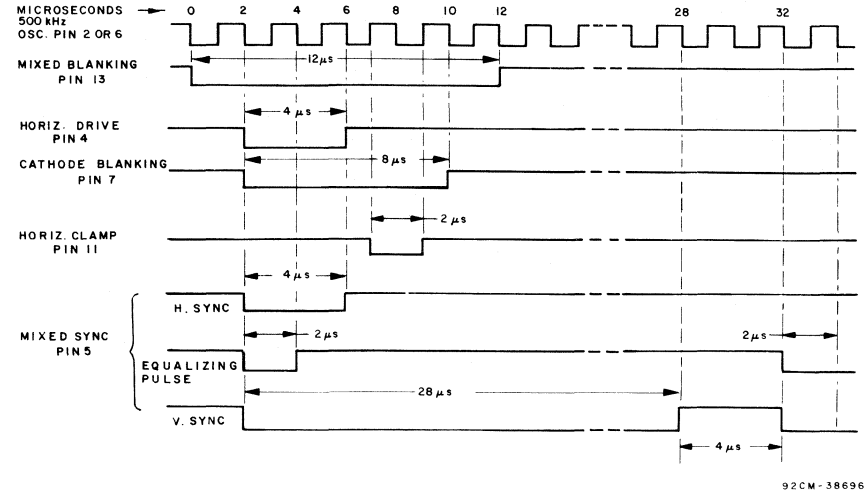


Fig. 2 - Sync generator timing - 525/60 Hz.

CD22402



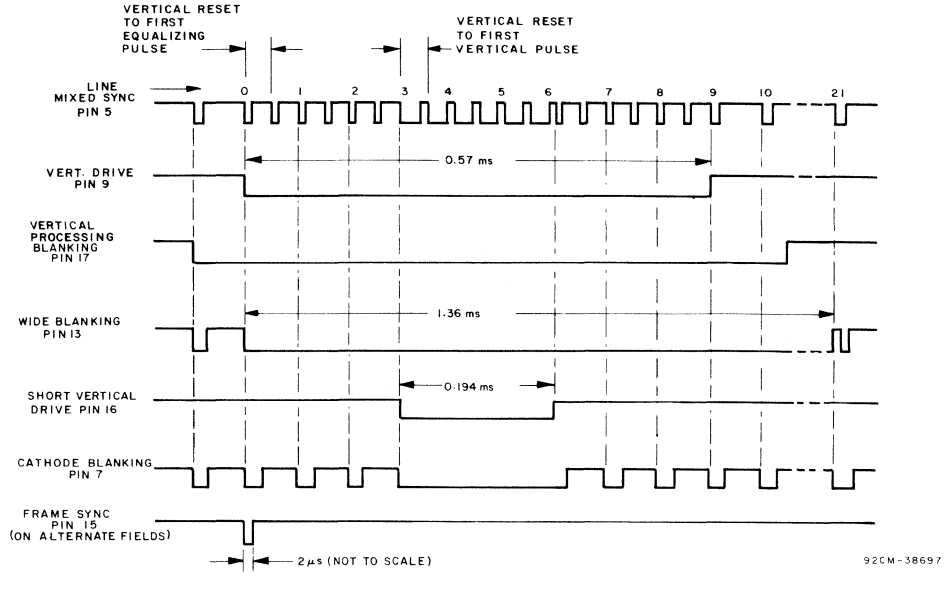


Fig. 3 - Sync generator timing - 625/50 Hz.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS		LIMITS									UNITS
				-55°C			+25°C			+125°C			
		V_O (V)	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}		5	—	—	—	0.5	0.75	1	—	—	—	mA
			10	—	—	—	1.5	2	2.5	—	—	—	
			15	—	—	—	3	4	5	—	—	—	
Output Voltage Low-Level	V_{OL}		5	—	—	0.01	—	—	0.01	—	—	0.05	V
			10	—	—	0.01	—	—	0.01	—	—	0.05	
High-Level	V_{OH}		5	4.99	—	—	4.99	—	—	4.95	—	—	
			10	9.99	—	—	9.99	—	—	9.95	—	—	
Threshold Voltage (N-Channel)	$V_{TH}N$	I_D = 10 μA		—	1.7	—	1	1.5	2.6	—	1.3	—	
(P-Channel)	$V_{TH}P$	I_D = -10 μA		—	-1.7	—	-1	-1.5	-2.6	—	-1.3	—	
Noise Immunity (Any Input)	V_{NL}		5	1.5	—	—	1.5	2.25	—	1.4	—	—	
			10	3	—	—	3	4.5	—	2.9	—	—	
	V_{NH}		5	1.4	—	—	1.5	2.25	—	1.5	—	—	
			10	2.9	—	—	3	4.5	—	3	—	—	
Output SINK Current (N-Channel)	I_DN	0.5	5	100	—	—	80	160	—	56	—	—	μA
		5		1200	—	—	960	1920	—	672	—	—	
		0.5	10	248	—	—	200	400	—	140	—	—	
		10		3000	—	—	2400	4800	—	1680	—	—	
Output SOURCE Current (P-Channel)	I_DP	4.5	5	200	—	—	80	160	—	56	—	—	
		0		1200	—	—	960	1920	—	672	—	—	
		9.5	10	248	—	—	200	400	—	140	—	—	
		0		3000	—	—	2400	4800	—	1680	—	—	
Input Current (Each Input)	I_I		—	—	—	—	—	10	—	—	—	—	pA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C and C_L = 15 pF

Typical Temperature Coefficient for All Values of V_{DD} = 0.3%/°C

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
		V_{DD} (V)	MIN.	TYP.	MAX.	
Output State Propagation Delay Time (50% to 50%)						ns
Low-to-High Level	t_{PLH}	5	—	40	80	
High-to-Low Level	t_{PHL}	10	—	20	40	
Transition Time (10% to 90%)						
Low-to-High	t_{TLH}	5	—	45	90	
High-to-Low	t_{THL}	10	—	30	60	
Input Capacity (Per Input)	C_I		—	5	—	pF

CD22402

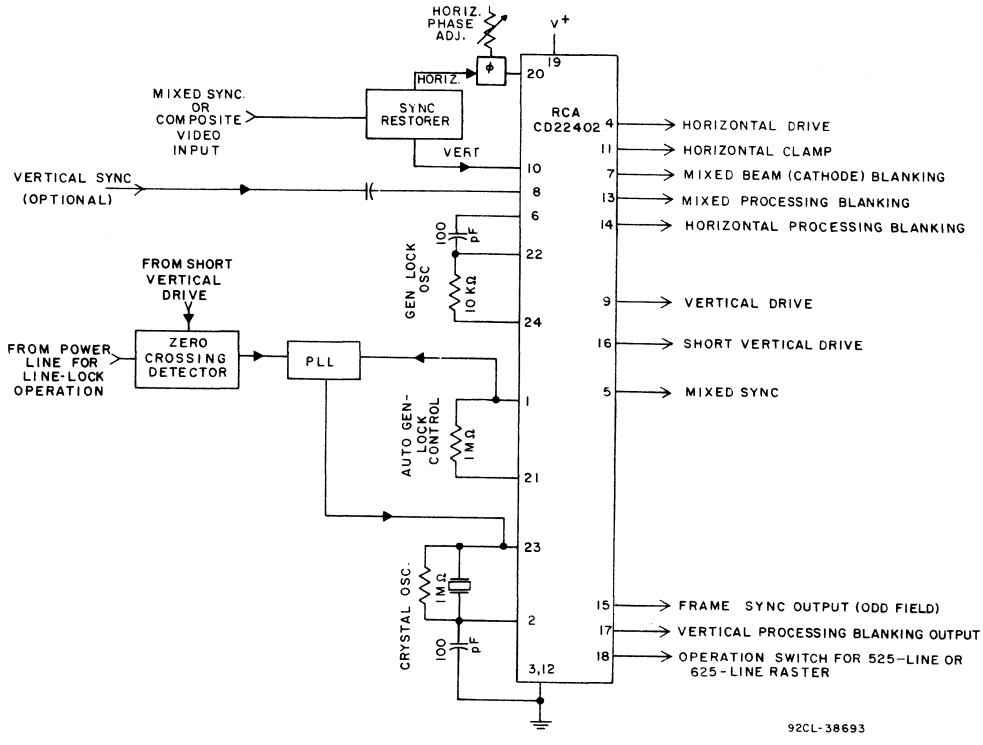


Fig. 4 - Typical application in a TV camera.

TV/CATV Circuits — Technical Data

TV/CATV Circuits (Cont'd)

Type No.	Description	Page No.
Sync Generators		
CA3254	RS-170 Sync Generator	915
CA3255	RS-170 Sync Generator	915
CD22402	LS1 Sync Generator	930
Stereo Sound SAP Detector		
CA3215	FM-IF Amplifier/Detector Limiter	825
Sound IF/Audio		
CA1190	Output Subsystems	940
CA1191	Output Subsystems	944
CA2111A	FM IF Amplifier-Limiter and Quadrature Detector	743
CA2136A	FM IF Amplifier-Limiter and Quadrature Detector	748
CA3011	Wideband Amplifier	750
CA3012	Wideband Amplifier	750
CA3013	Wideband Amplifier Discriminators	756
CA3014	Wideband Amplifier Discriminators	756
CA3065	IF Amplifier-Limiter, FM Detector, Electronic Attenuator, audio driver	953
CA3134	Output Subsystems	990
CA3259	Stereo Sound Volume/Tone Control	832
Display Drivers		
CA3081	Common-Emitter Transistor Array	151
CA3082	Common-Collector Transistor Array	151
CA3161	BCD-to-7-Segment Decoder/Driver Current Output Drive, Common Anode	154
CA3168	BCD-to-7-Segment Decoder/Driver, Common Anode	158
CA3207	Divide-by-14 Counter 1 of 14 Decoder/Driver for Vacuum Fluorescent Anode Drive	162
CA3208	14-Bit Shift Register with Output Latch/Driver	162
CD4094	8-Stage Shift-and-Store Bus Register	—
CD7211	Four-Digit LCD Decoder/Driver	174
CD7211A	Four-Digit LCD Decoder/Driver	174
CD7211M	Four-Digit LCD Decoder/Driver	179
CD7211AM	Four-Digit LCD Decoder/Driver	179
Video Switch		
CA3256	CMOS/BiMOS Analog Video Switch and Amplifier	925
Auto CRT Bias		
CA3224	Automatic Picture Tube Bias Circuit	906
RF Modulator		
CA1890	TV Video/Audio RF Modulator	847

For data on CD4XXXX types, refer to *DATABOOK SSD-250C,* CMOS Integrated Circuits, or the specific data bulletin for that type shown in the *Index to Devices.*

CA1190

TV Sound IF and Audio Output Subsystems

Features:

- *Nominal power output: 4 W at V+ = 24 V, R_L = 16 Ω, dist. = 10%, 2 W at V+ = 12 V, R_L = 8 Ω, dist. = 10%*
- *Wide power-supply range: 9 to 28 V*
- *Low quiescent current: 25 mA typ.*
- *5-kHz deviation sensitivity: 1 W output typ.*
- *3-dB limiting sensitivity: 50 μV typ.*
- *Excellent AM rejection: 50 dB typ.*
- *Differential peak detector – requires one tuned coil*
- *Electronic volume control with improved taper and single wire control*

The RCA-CA1190 combines sound IF and audio output subsystems on a single monolithic integrated circuit to provide a television sound system. Each device includes a multistage IF amplifier-limiter, an FM detector, and an audio power amplifier that is designed to drive, primarily, an 8- 16-, or 32-ohm speaker.

The CA1190 is electrically and mechanically equivalent to industry type TDA1190Z.

The CA1190 differs from the TDA1190Z in that it includes provisions for a lower value volume control.

The CA1190 is supplied in the 16-lead quad-in-line plastic package having an integral bent-down wing-tab (Q-suffix) heat sink intended for PC board mounting.

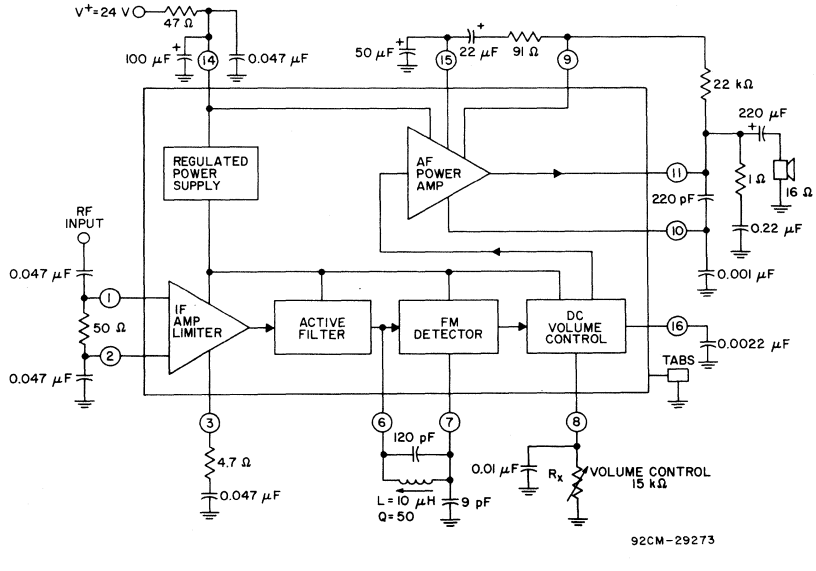


Fig. 1 - CA1190 typical application.

File Number **113**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

		UNITS
DC SUPPLY-VOLTAGE (Between Term. 14 V+ and ground tabs)	+28	V
OUTPUT PEAK CURRENT:		
Repetitive	1.5	A
Non-repetitive	2	A
INPUT SIGNAL VOLTAGE (Between Terms. 1 and 2)	±3	V
DEVICE DISSIPATION:		
With Infinite Heak Sink —		
Up to T_A = 90°C	5	W
Above T_A = 90°C, derate lineary	83.3	mW/°C
With No Heat Sink — (free air) —		
Up to T_A = 25°C	1.75	W
Above T_A = 25°C, derate lineary	14	mW/°C
THERMAL RESISTANCE:		
Junction to ground tabs	12	°C/W
Junction to ambient	70	°C/W
AMBIENT TEMPERATURE RANGE:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
LEAD TEMPERATURE (During Soldering): At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 24 V, DC Volume Control R_X = 0 Ω, R_L = 16 Ω unless otherwise indicated. Refer to Fig. 1.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
Current into Term. 14	P_O = 0	10	25	40	mA
Dynamic Characteristics					
IF Amplifier: Input Limiting Voltage, (At — 3 dB point), V_1 (lim)	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz	—	50	100	μV
AM Rejection, AMR	f_O = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{IN} = 1 mV	40	50	—	dB
Deviation Sensitivity	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_I = 1 mV, R_X = 0, Deviation necessary to obtain 4 Vrms across 16 Ω (1 W)	—	5	—	kHz
Minimum Audio Output	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_I = 1 mV, R_X = 15 kΩ	—	—	10	mVrms
Distortion at P_O = 1.5 W	f_O = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_{IN} = 1 mV	—	—	3	%
Signal to Noise Ratio	V_{out} at Δf = 0 with R_X adjusted for V_{out} = 4 Vrms at Δf = ± 25 kHz	50	—	—	dB

CA1190

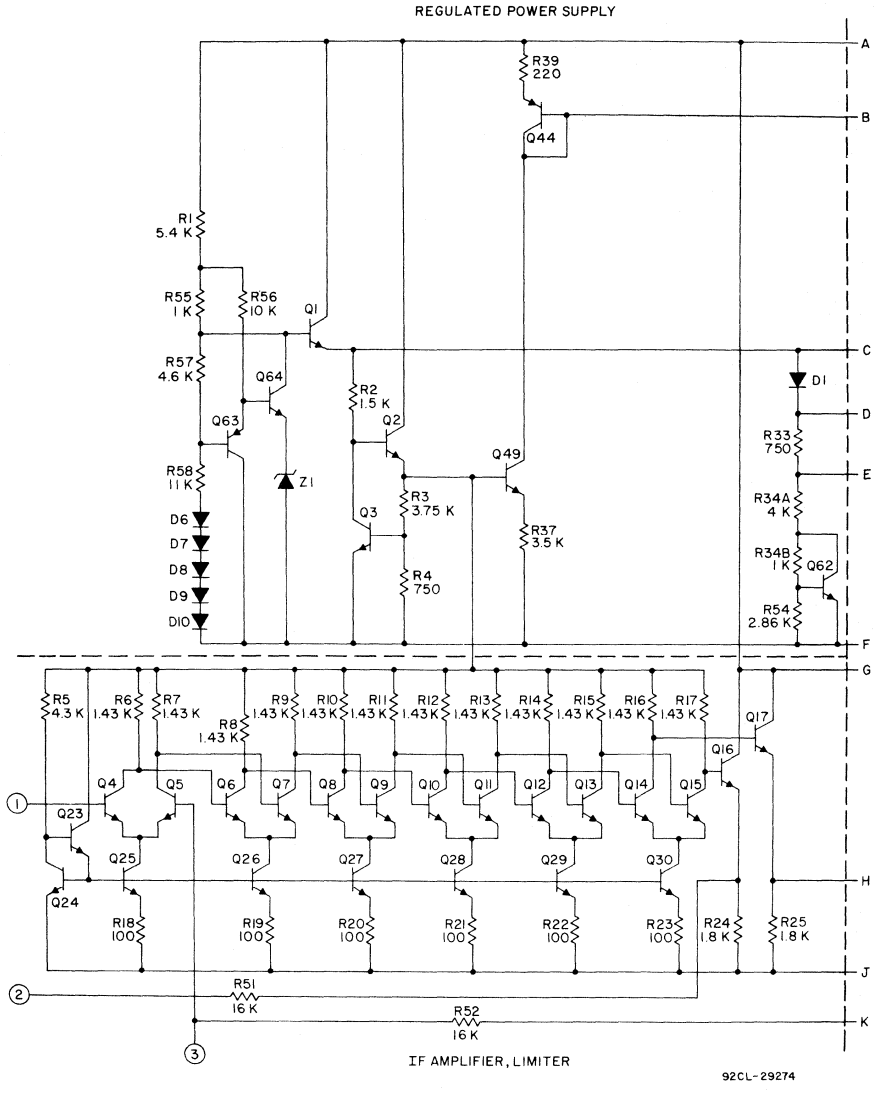


Fig. 2 - CA1190 (cont'd on next page).

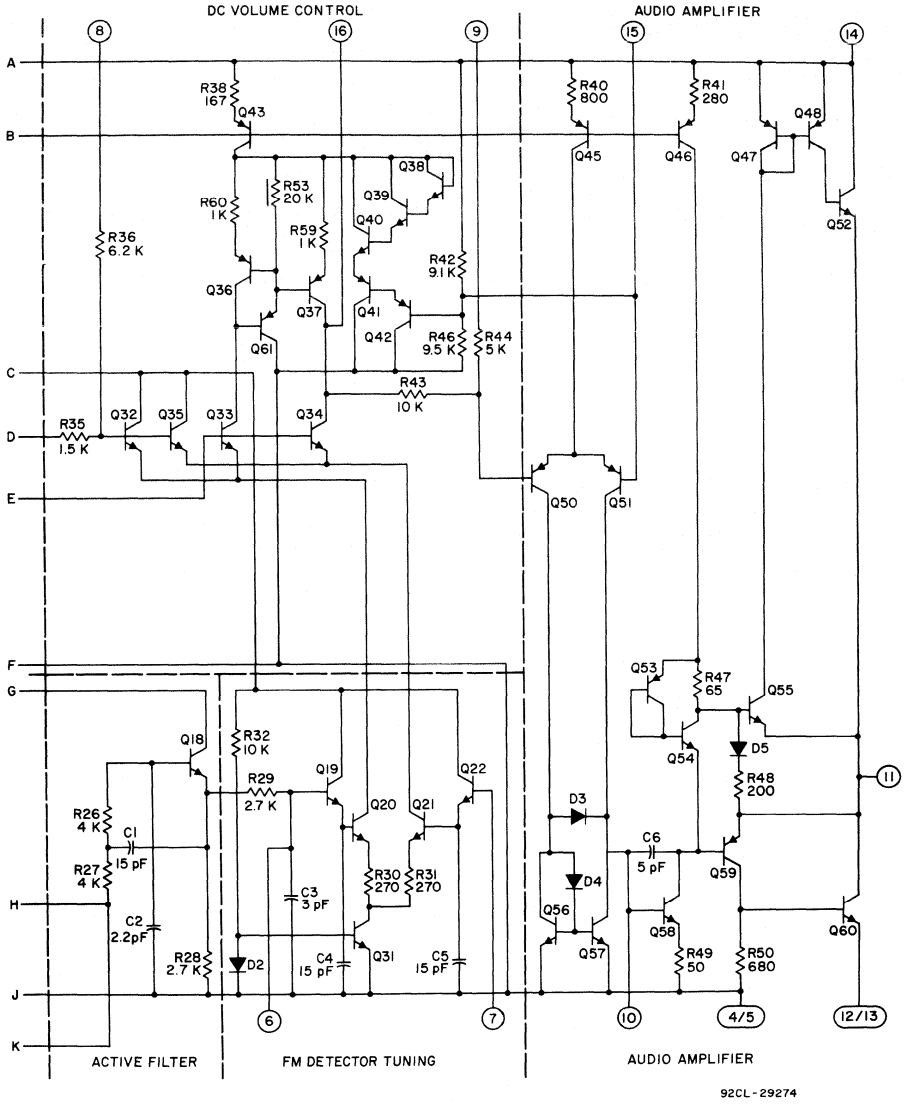


Fig. 2 - CA1190 (cont'd from previous page).

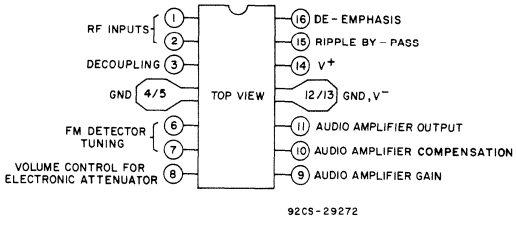


Fig. 3 - Terminal diagram.

CA1191

TV Sound IF and Audio Output Subsystems

Features:

- *Nominal power output: 4 W at V + = 24 V, R_L = 16 Ω, dist. = 10%, 2 W at V + = 12 V, R_L = 8 Ω dist. = 10%*
- *Wide power-supply range: 9 to 28 V*
- *Low quiescent current: 25 mA typ.*
- *5-kHz deviation sensitivity: 1 W output typ.*
- *3-dB limiting sensitivity: 50 μV typ.*
- *Excellent AM rejection: 50 dB typ.*
- *Differential peak detector - requires one tuned coil*
- *Electronic volume control with improved taper and single wire control*

The RCA-CA1191* combines sound IF and audio output subsystems on a single monolithic integrated circuit to provide a television sound system. Each device includes a multi-stage IF amplifier-limiter, an FM detector, and an audio power amplifier that is designed to drive, primarily, an 8-, 16, or 32 ohm speaker.

* Formerly RCA Dev. No. TA11029

The CA1191 is electrically and mechanically equivalent t industry type TDA 3190.

The CA1191 differs from the TDA3190 in that it include provisions for a lower value volume control.

The CA1191 is supplied in the 16-lead dual-in-line plasti package (E suffix).

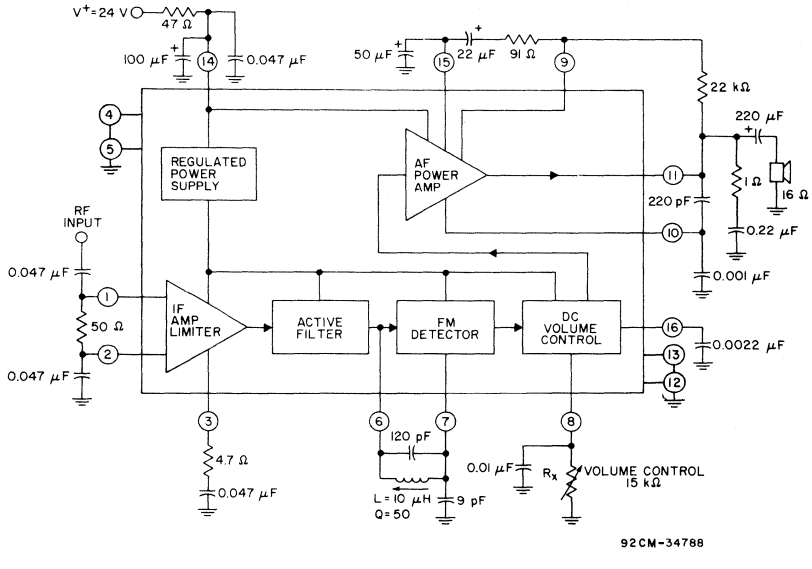


Fig. 1 - Block diagram of the CA1191 in a typical application.

File Number 134

AXIMUM RATINGS, *Absolute-Maximum Values:*

C SUPPLY VOLTAGE (Between Term. 14 V^+ and ground tabs)	+28	V
UTPUT PEAK CURRENT:		
Repetitive	1.5	A
Non-repetitive	2	A
IPUT SIGNAL VOLTAGE (Between Terms. 1 and 2)	±3	V
EVICE DISSIPATION:		
Vith Infinite Heat Sink —		
Up to T_A = 90° C	4.3	W
Above T_A = 90° C, derate linearly	71.7	mW/° C
Vith No Heat Sink — (free air) —		
Up to T_A = 25° C	1.6	W
Above T_A = 25° C, derate linearly	12.8	mW/° C
HERMAL RESISTANCE:		
Junction to ground pins	14	°C/W
Junction to ambient	80	°C/W
MBIENT TEMPERATURE RANGE:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
EAD TEMPERATURE (During Soldering):		
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

ELECTRICAL CHARACTERISTICS *at T_A = 25° C, V^+ = 24 V, DC Volume Control Rx = 0 Ω, R_L = 16 Ω unless otherwise indicated. Refer to Fig. 1.*

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Static Characteristics					
Current into Term. 14	P_o = 0	10	25	40	mA
Dynamic Characteristics					
IF Amplifier: Input Limiting Voltage, (At −3 dB point), V_I (lim)	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz	—	50	100	μV
AM Rejection, AMR	f_o = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{IN} = 1 mV	40	50	—	dB
Deviation Sensitivity	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_I = 1 mV, Rx = 0, Deviation necessary to obtain 4 Vrms across 16 Ω (1 W)	—	5	—	kHz
Minimum Audio Output	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_I = 1 mV, Rx = 15 kΩ	—	—	10	mVrms
Distortion at P_o = 1.5 W	f_o = 4.5 MHz, f_m = 400 Hz, Δf = ± 25 kHz, V_{IN} = 1 mV	—	—	3	%
Signal to Noise Ratio	V_{out} at Δf = 0 with Rx adjusted for V_{out} = 4 Vrms at Δf = ± 25 kHz	50	—	—	dB

CA1191

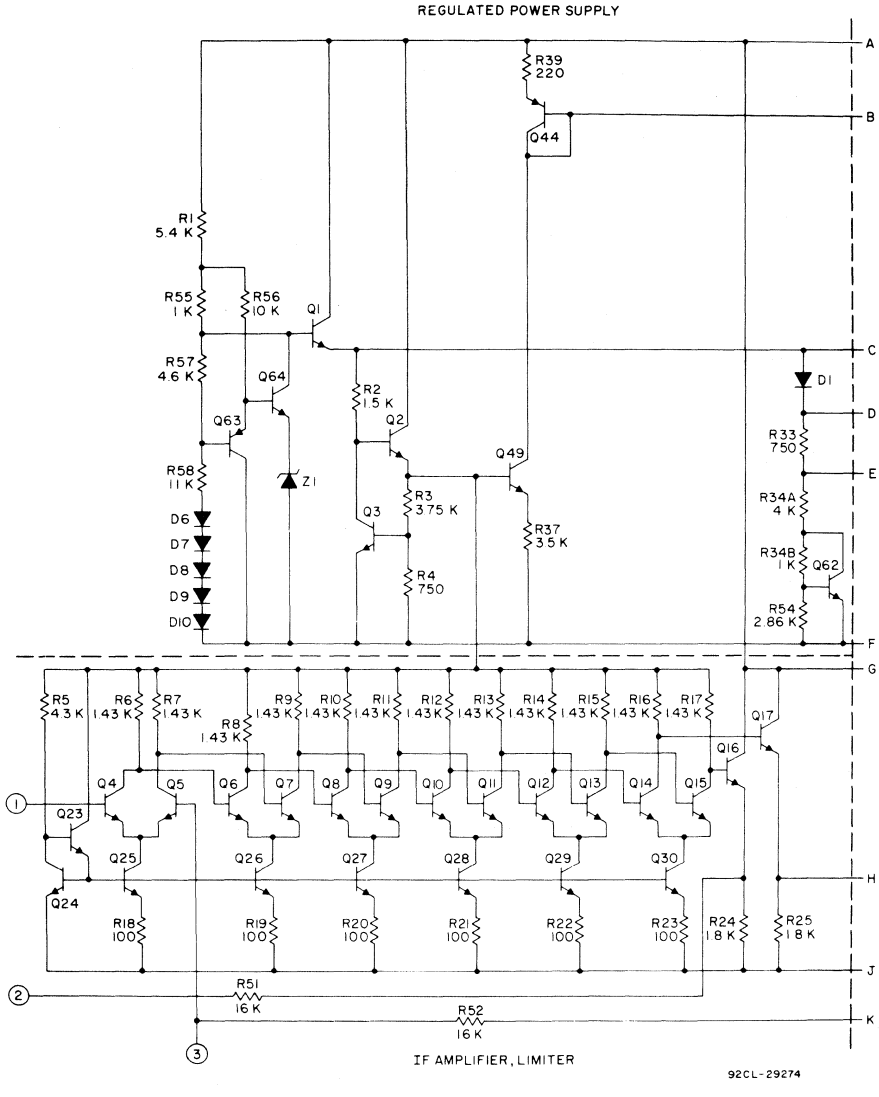
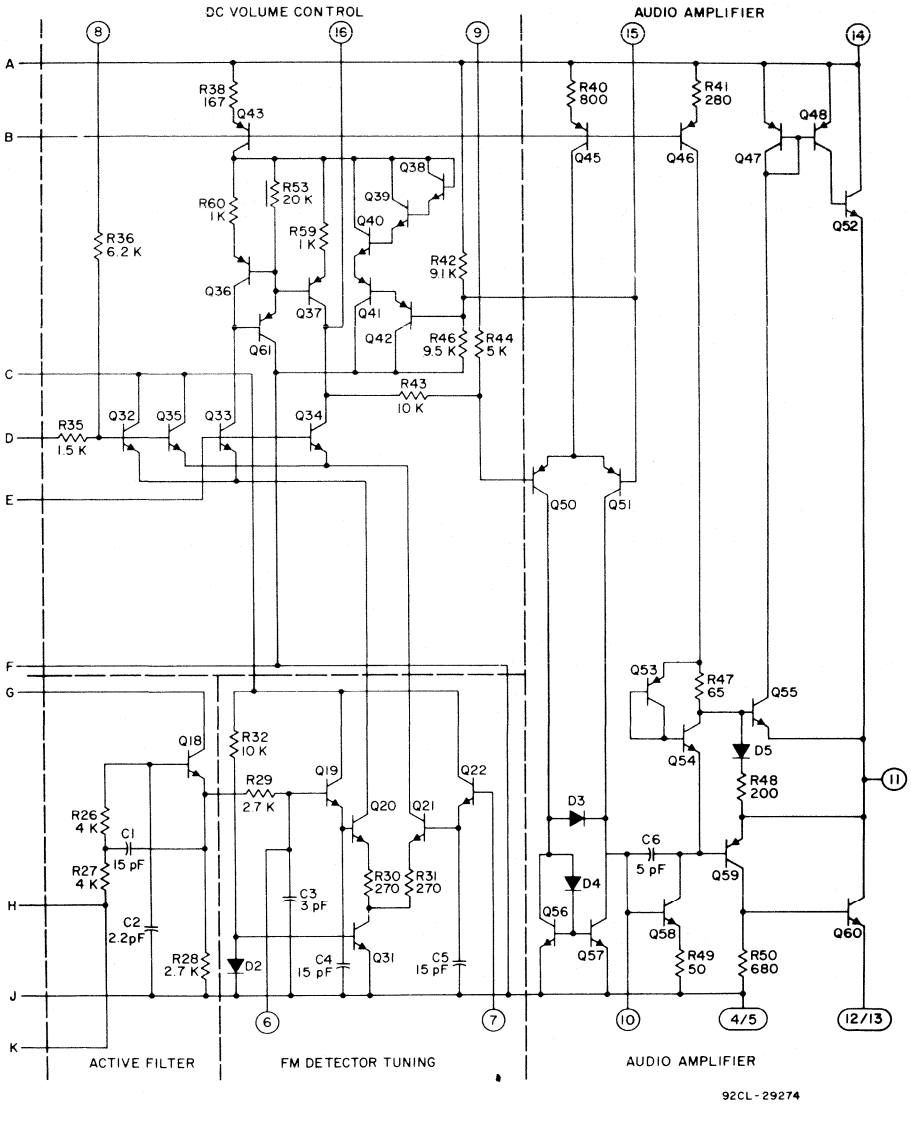


Fig. 2 - CA1191 Schematic diagram.



CA1191 Schematic diagram (con't.)

CA1398

Television Chroma Processor

Features

- **Minimum number of external components required**
- **Injection-lock oscillator with internal feedback**
- **DC chroma gain control and hue control circuits**
- **Low-impedance internal voltage regulation**

RCA-CA1398E is a monolithic silicon integrated-circuit chroma processor containing chroma-amplifier and gain-control, color-killer, color subcarrier oscillator, hue control, and ACC circuitry. It has been designed for interchangeability with other "1398"-type chroma-processor devices. It functions compatibly with the RCA-CA3125E Chroma Demodulator as well as other commercially available chroma demodulators in color-TV receivers. Fig. 2 shows a functional block diagram of a 2-package TV chroma system incorporating the CA1398E and CA3125E. The CA1398E is supplied in a 14-lead dual-in-line plastic package.

Maximum Ratings, *Absolute-Maximum Values at* $T_A = 25^\circ C$

Peak Horizontal-Pulse Input Current	250
Supply Current (Terminal 14)	35 r
Ambient Temperature Range:	
Operating	−40 to +8
Storage	−65 to +15
Lead Temperature (During Soldering):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	26

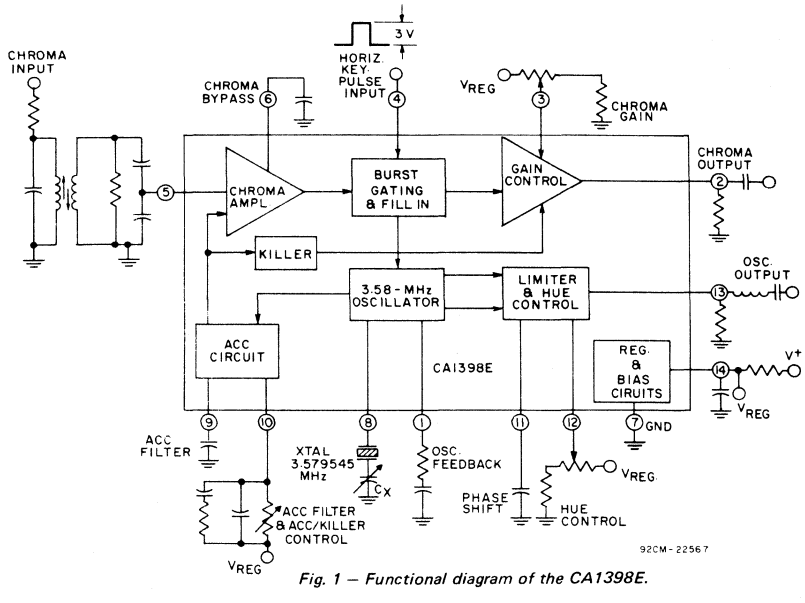


Fig. 1 – Functional diagram of the CA1398E.

File Number **686**

ELECTRICAL CHARACTERISTICS at T_A = 25°C and Referenced to Test Circuit (Fig. 4)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS						LIMITS			UNITS
		SWITCH POSITION (S1)	CONTROL SETTING CHROMA	CONTROL SETTING HUE	CONTROL SETTING KILLER	V_{BURST} mV p-p	V_{CHROMA} mV p-p	MIN.	TYP.	MAX.	
Static Characteristics											
Regulated Supply Voltage	V_{14}	2	max.	max.	max.	0	0	8.9	9.5	11.5	V
Chroma Output Bias	V_{14} to V_2	2	max.	max.	max.	6	0	1.2	2.4	3.6	V
Regulator Impedance	See Note 1	2	max.	max.	max.	0	0	–	12	25	Ω
Dynamic Characteristics (Refer to Test Set-Up Procedure for Oscillator)											
Max. Chroma Gain	V_2	1	max.	max.	See Note 2	6	5	310	425	–	mV p-p
Min. Chroma Gain	V_2	1	min.	max.		6	5	–	–	7	mV p-p
ACC Action	V_2 (dB up from gain test)	1	max.	max.		50	50	2	7	11	dB
Killer Function:											
Kill	V_2	2	max.	max.		0	5	–	–	7	mV p-p
Unkill	V_2	1	max.	max.		15	5	100	–	–	mV p-p
Oscillator Lock-Up:											
Voltage	V_{13}	1	max.	max.		6	0	250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	max.		6	0	–20	0	+20	degrees
Hue Control Range:											
Voltage	V_{13}	1	max.	min.		6	0	250	340	390	mV p-p
Phase (Referenced to burst)	ϕ_{13}	1	max.	min.		6	0	95	110	140	degrees

Note 1 – Measure V_{14} at I_{SUPPLY} = 38 mA and 18 mA. Calculate the regulator impedance:
$Z_{reg.} = [V_{14}$ (at 38 mA)$-V_{14}$ (at 18 mA)$]/0.02$

Note 2 – Increase the killer potentiometer resistance from minimum until the circuit unkills. This condition is evidenced by a shift in bias voltage at Term. 6. Maintain this potentiometer setting for all the dynamic tests.

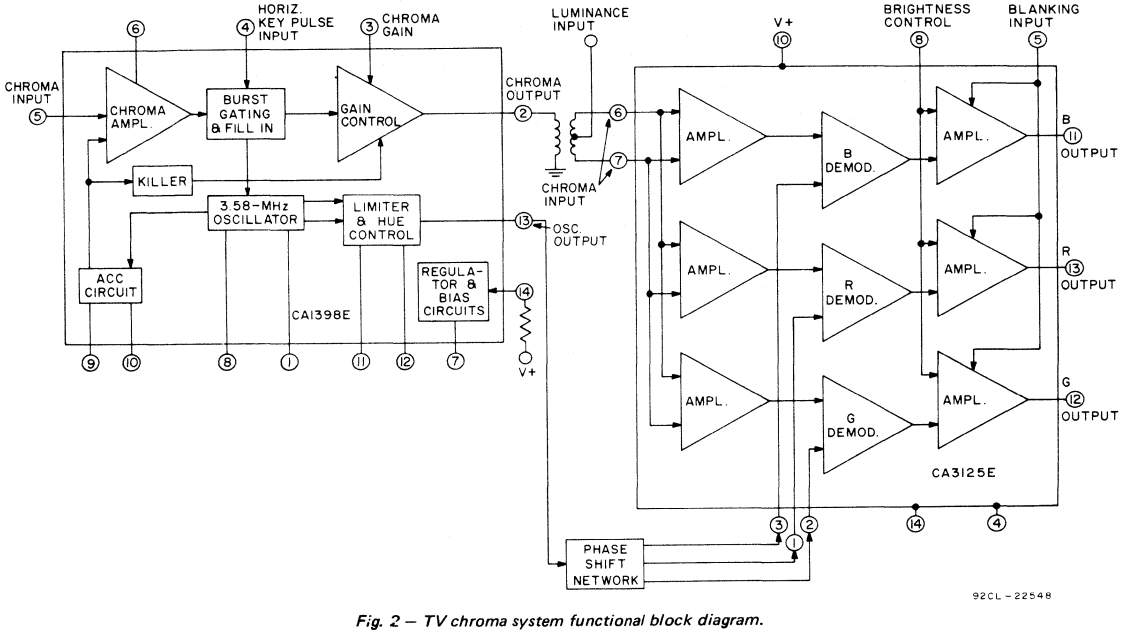


Fig. 2 – TV chroma system functional block diagram.

CA1398

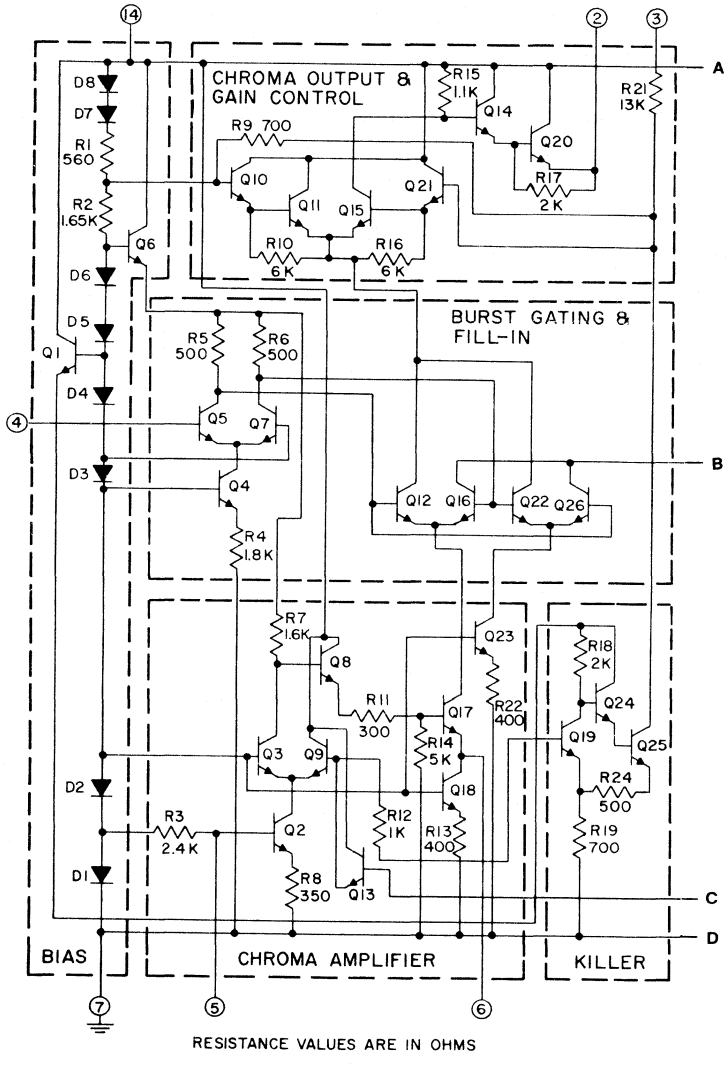


Fig. 3 - Schematic diagram of the CA1398E (cont'd on next page).

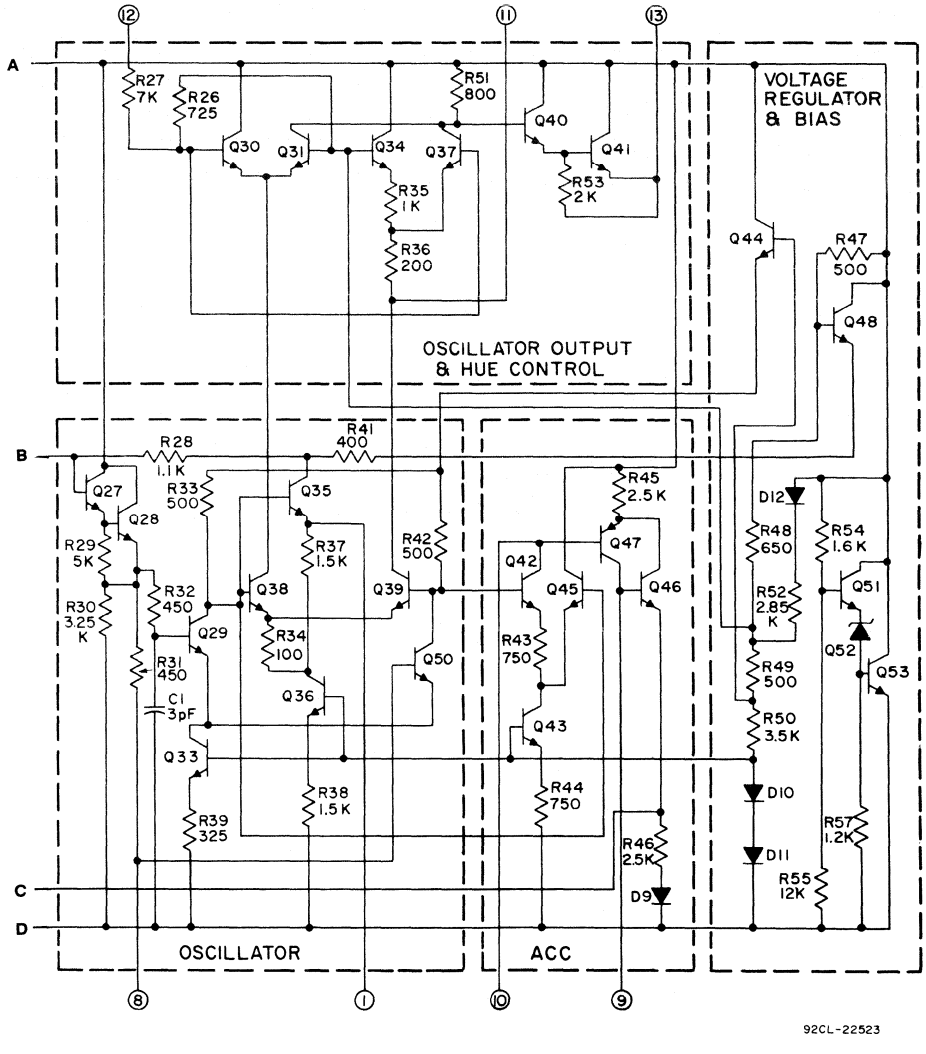


Fig. 3 - Schematic diagram of the CA1398E (cont'd from previous page).

CA1398

TEST SET-UP PROCEDURE FOR OSCILLATOR

Remove the horizontal keying and chroma inputs and adjust C_X to obtain a free-running oscillator frequency of 3.579545 MHz ±10 Hz. Under the same Test Conditions described in t Electrical Characteristics Chart for Oscillator Lock-Up, vary (approx. 20 μH) and/or C1 (approx. 1000 pF) to obtain t initial conditions for amplitude and phase oscillator lock-up.

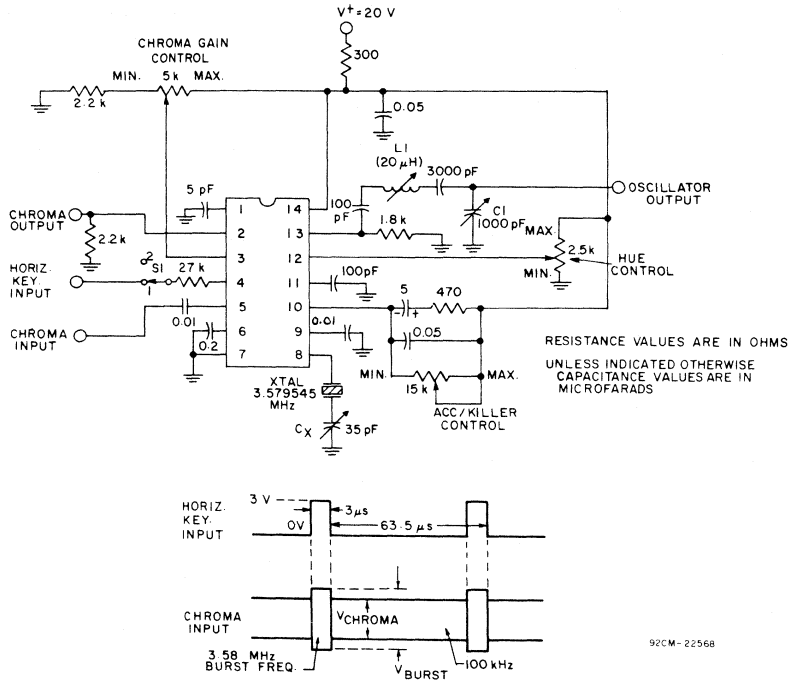


Fig. 4 – Typical static and dynamic characteristics test circuit for the CA1398E.

CA3065

IF Amplifier-Limiter, FM Detector, Electronic Attenuator, Audio Driver

For Television Sound-System Applications

Features:

- *Electronic attenuator – replaces conventional volume control*
- *Differential peak detector – requires on single tuned coil*
- *Internal Zener diode regulated supply*
- *Inherent high stability*
- *Excellent AM rejection – 50 dB typ. at 4.5 MHz*
- *Low harmonic distortion*
- *High sensitivity – 200 μV limiting (knee) at 4.5 MHz*
- *Audio drive capability – 6 mA p-p*
- *Undistorted audio output voltage – 7 V p-p*

The RCA CA3065• Television Sound System is a monolithic integrated circuit which combines a multistage IF amplifier limiter, an FM detector, an electronic attenuator, a zener diode regulated power supply, and an audio amplifier-driver that is designed to directly drive an n-p-n power transistor or high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. A block diagram of the integrated circuit television sound system is shown in Fig. 1.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between Terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the IF board and the variable resistor (volume control).

The CA3065 is supplied in the 14-lead dual-in-line plastic package (E suffix), in the 14-lead quad-in-line plastic package, and is also available in chip form.

•Formerly Dev. Type No. TA5814

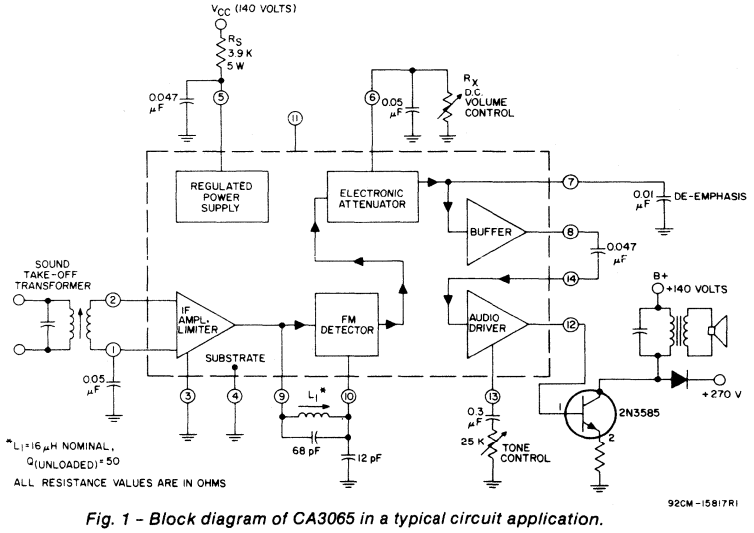


Fig. 1 – Block diagram of CA3065 in a typical circuit application.

File Number **412**

CA3065

MAXIMUM RATINGS, *Absolute Maximum Values*, at T_A = 25°C

Input Signal Voltage (between Terminals 1 and 2) . . .	±3	V
Power Supply Current (Terminal 5)	50	mA
Power Dissipation:		
Up to T_A = 25°C	850	mW
Above T_A = 25°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	- 40 to + 85	°C
Storage	- 65 to + 150	°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 3 is 0 to +4 volts.

TERMINAL No.	4	5	6	7	8	9	10	11	12	13	14	1	2	3
4		SUBSTRATE CONNECTION – ALWAYS CONNECT TO TERMINAL 3												
5			+13 0	+13 0	+13 0	*	*	INTERNAL CONNECTION DO NOT USE	+13 0	+13 0	*	*	*	NOTE 1
6				*	*	*	*		*	*	*	*	*	+13 −5
7					+1 −4	*	*		*	*	*	*	*	+13 0
8						*	*		*	*	*	*	*	*
9							*		*	*	*	*	*	+4 0
10									*	*	*	*	*	+4 −5
11									INTERNAL CONNECTION DO NOT USE					
12										+4 −1	*	*	*	*
13											*	*	*	*
14												*	*	+3 −5
1													+5 −5	+5 −5
2														+4 −5
3														

MAXIMUM CURRENT RATINC

TERMINAL No.	I_{IN} mA	I_{OU} mA
4	SUBSTRATE CONNECT TI TERMINAL 3	
5	50	1
6	1	1
7	1	1
8	0.5	6
9	1	1
10	1	0.1
11	INT. CONN. DO NOT USE	
12	0.5	6
13	1	2
14	1	0.1
1	1	0.1
2	1	0.1
3	0.1	50

Note 1: Terminal No. 5 may be connected to any positive voltage through a suitable resistor provided that the current and dissipation ratings of the CA3065 are not exceeded.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if specified limits between all other terminals are not exceeded.

ELECTRICAL CHARACTERISTICS *at T_A = 25° C, V_{CC} = +140 V applied to Terminal 5 through R_S = 3.9 kΩ, and DC Volume Control (R_x) = 0 unless otherwise indicated.*

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig. No.	SPECIAL TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics							
Zener Regulating Voltage Terminal No. 5	V_5	–		10.3	11.2	12.2	V
Current into Terminal 5	I_5	–	Connect Terminal 5 to +9 V	10	16	24	mA
Total Device Dissipation	P_T	–		343	370	400	mW
Terminal Voltages: 1	V_1	–		–	2	–	V
6	V_6			–	4.8	–	
7	V_7			–	6.1	–	
9	V_9			–	3.7	–	
12	V_{12}			4	5.1	5.8	
Dynamic Characteristics							
IF AMPLIFIER Input Limiting Voltage (at −3 dB point)	$V_{i(lim)}$	3	f_0 = 4.5 MHz. f_m = 400 Hz, Deviation = ±25 kHz,	–	200	400	μV
AM Rejection	AMR	3	Amplitude Modulation = 30% f = 4.5 MHz	40	50	–	dB
Transconductance Magnitude	$\lvert G_m \rvert$ (IF)	–	f = 4.5 MHz IF Input Terminals: 2, 1 IF Output Terminals: 9, 3	–	500	–	mmho
Phase Angle	θ(IF)	–		–	46	–	degrees
Feedback Capacitance	C_{fb}	–	f = 1 MHz; Terminals 2 and 9	–	<0.02	–	pF
Input Impedance Components: Parallel Input Resistance	R_i (IF)	–	Measured between Terminal Nos. 1 and 2	–	17	–	kΩ
Parallel Input Capacitance	C_i (IF)	–	f = 4.5 MHz	–	4	–	pF
Output Impedance Components: Parallel Output Resistance	R_o(IF)	–	Measured between Terminal No. 9 and gnd	–	3.25	–	kΩ
Parallel Output Capacitance	C_o(IF)	–	f = 4.5 MHz	–	75	–	pF
DETECTOR Recovered AF Voltage	V_o(af)	3	f = 4.5 MHz; V_I = 100 mV △f = ±25 kHz fm = 400 Hz	0.5	0.75	–	V(rms)
Total Harmonic Distortion	THD	3		–	0.9	2	%
Output Resistance: Terminal 7	R_o	–		–	7.5	–	kΩ
Terminal 8		–		–	300	–	Ω
ATTENUATOR			See Fig. 7				
Max. Attenuation	–	3	R_X = ∞	60	80	–	dB
Max. "Play-through" Voltage*	–	3	R_X = ∞	–	0.075	1	mV
AUDIO AMPLIFIER Voltage Gain	A(af)	4	V_I = 0.1 V(rms), f = 400 Hz	17.5	20	–	dB
Total Harmonic Distortion	THD	4	V_O = 2 V(rms), f = 400 Hz	–	1.5	–	%
Undistorted Output Voltage	–	4	THD = 5%, f = 400 Hz	2	2.5	–	V(rms)
Input Resistance	R_i(af)	–	f = 400 Hz	–	70	–	kΩ
Output Resistance	R_o(af)	–	f = 400 Hz	–	270	–	Ω

*"Playthrough" voltage is the unwanted signal, measured at Terminal 8, when the volume control is set for minimum output.

CA3065

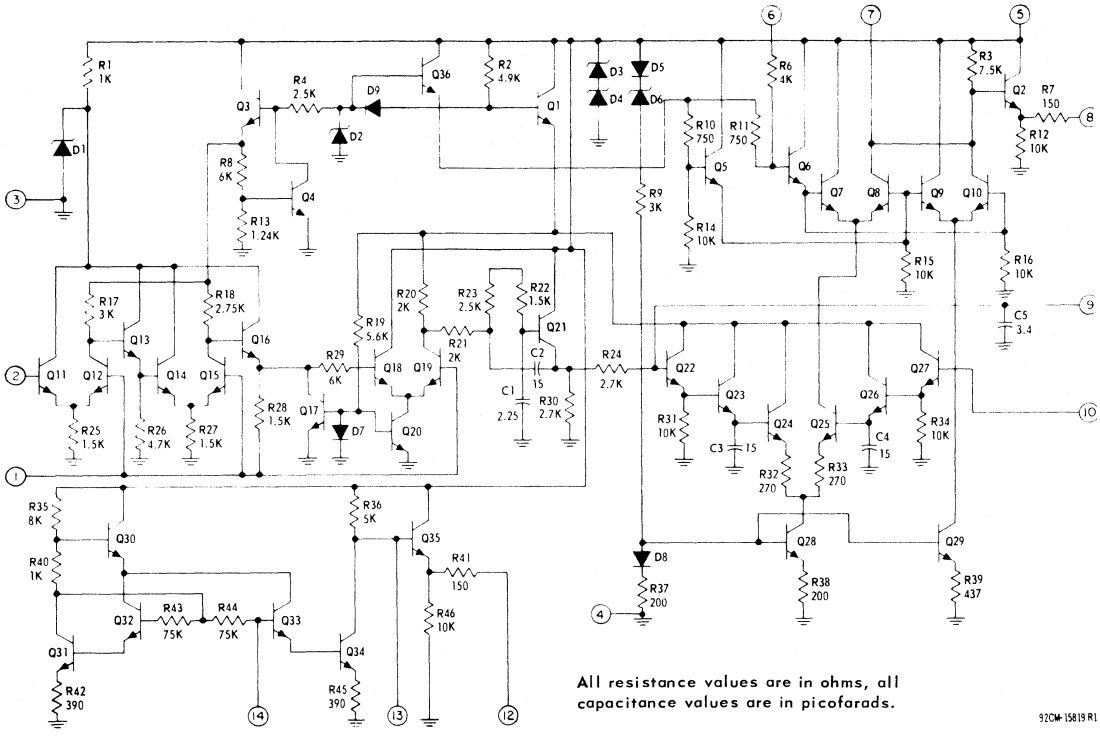


Fig. 2 - Schematic diagram of CA3065

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistanc Values provided such changes do not adversely affect the publishe performance characteristics of the device.

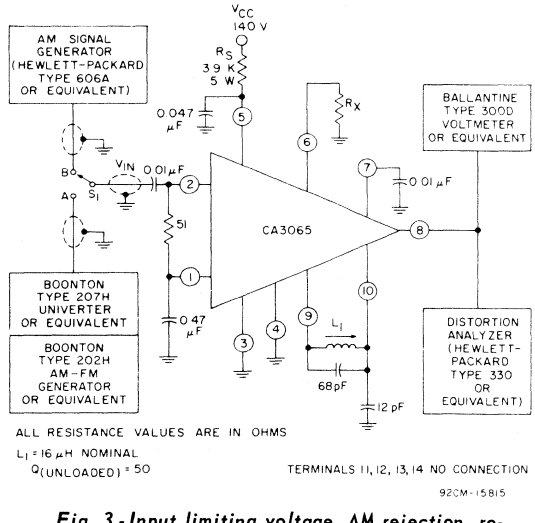


Fig. 3 - Input limiting voltage, AM rejection, recovered audio, total harmonic distortion, maximum attenuation, maximum "play-through" test circuit.

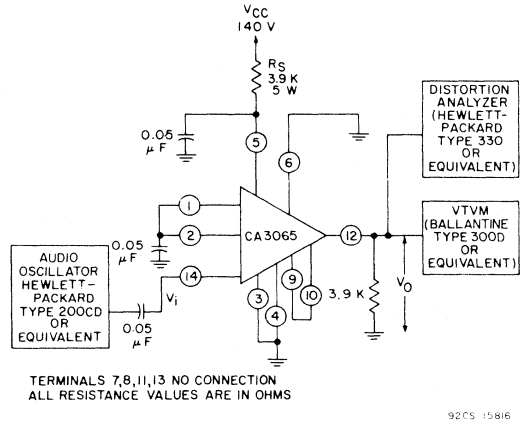
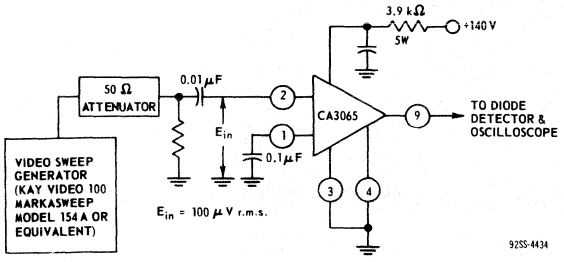
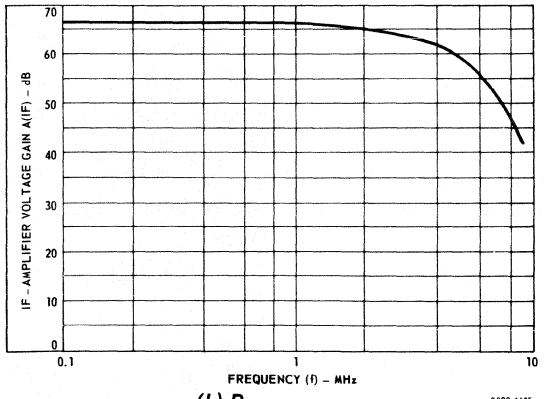


Fig. 4 - Audio voltage gain (undistorted output) test circuit.

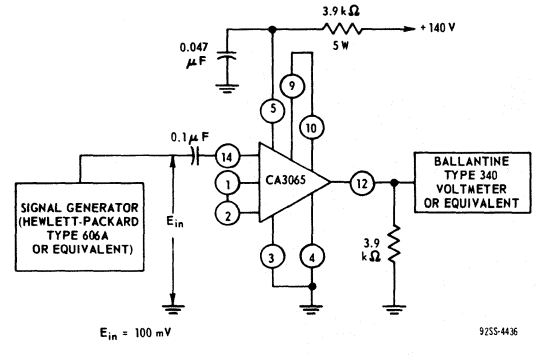


(a) Test circuit

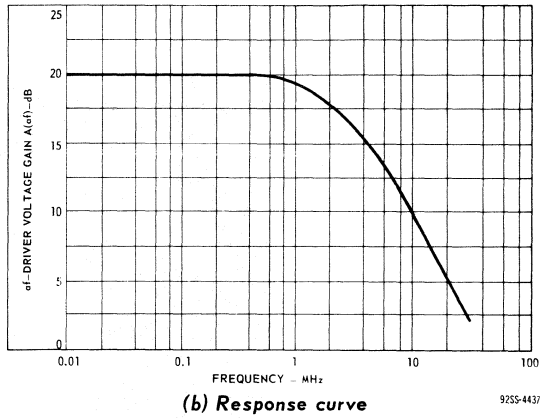


(b) Response curve

Fig. 5 - Frequency response of IF-amplifier section of CA3065



(a) Test circuit



(b) Response curve

Fig. 6 - Frequency response of af-amplifier section of CA3065

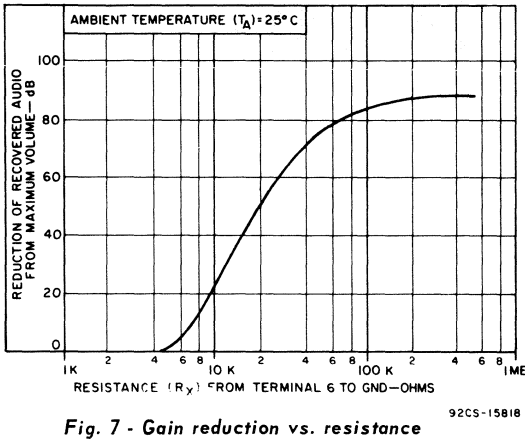


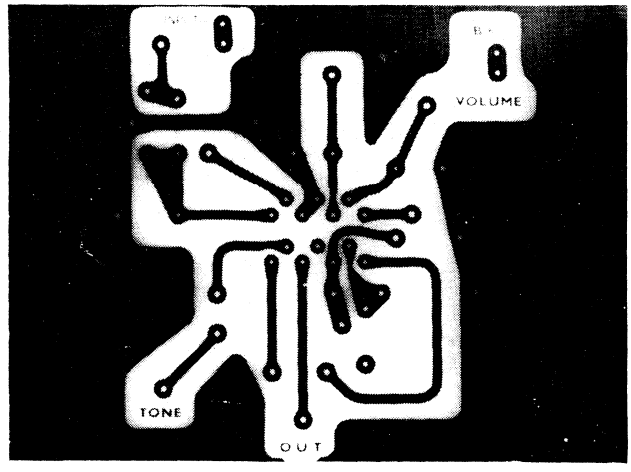
Fig. 7 - Gain reduction vs. resistance (terminal 6 to gnd)

OPERATING CONSIDERATIONS

As in all TV receivers, precaution should be taken to prevent destruction of the CA3065 in the event of cascade arcs originating in the picture tube or in the output tube. In the case of arcing in the output tube a resistor of 150k in series with terminal No. 12 and the grid of the tube is usually sufficient protection.

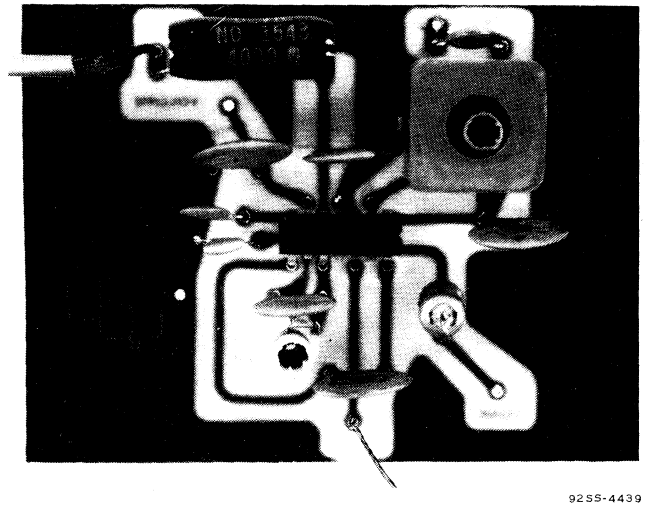
To prevent damage from picture tube arcs, a careful analysis of board layout and coupling modes (electrostatic or magnetic) may be necessary to suggest alternate layouts or appropriate locations for the placement of spark gaps to absorb the high energy discharge.

CA3065



92SS-4438

*(a) Printed circuit board – bottom view**
Full Size



92SS-4439

*(b) Parts layout – top view**
Full Size

Fig. 8 - Recommended parts layout for TV receiver sound strip using CA3065.

* A 200 mil square grid was used in the layout of passive components on the printed circuit board. The Quad-in-line formed leads conform to a standard grid spacing of 100 mil centers.

,3068

Television Video IF System

Features:

- High-gain wide-band IF amplifier: 75 dB typ. at 45 MHz
- Gain reduction with excellent stability: 50 dB typ. at 45 MHz
- Video detector with linear characteristics
- Video amplifier: 12 dB gain
- Impulse noise limiter
- Keyed AGC with noise immunity circuits
- Delayed AGC for tuner
- Buffered AFT output
- Separate sound IF intercarrier amplification
- Sound carrier detector
- 4.5 MHz sound carrier amplifier
- Isolated zener reference diode for regulated voltage supply

RCA-CA3068* is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Innovations in integrated circuit design, in addition to the many active devices and closely matched components utilized in the circuit, make the CA3068 ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad-in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

* Formerly Developmental No. TA5914

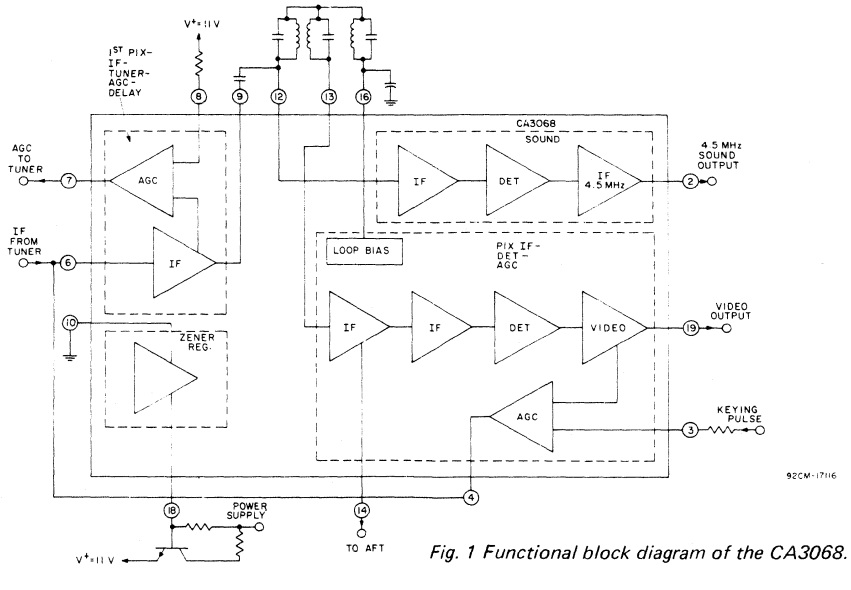


Fig. 1 Functional block diagram of the CA3068.

File Number **467**

CA3068

MAXIMUM RATINGS, *Absolute Maximum Values, at* $T_A = 25^\circ C$

DC Supply Voltage:	
Between Terminals 15 and 5*	11.3
Terminal 7 (Collector to ground)	20
Terminal 9 (Collector to ground)	20
DC Current (into Terminal 18)	2
Device Dissipation:	
Up to $T_A = 60^\circ C$	600
Above $T_A = 60^\circ C$	derate linearly 6.7 mW
Ambient Temperature Range:	
Operating	−40 to +85
Storage	− 65 to +150
Lead Temperature (During soldering):	
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265

* This rating does not apply when using the internal zener reference in conjunction with the pass transistor.

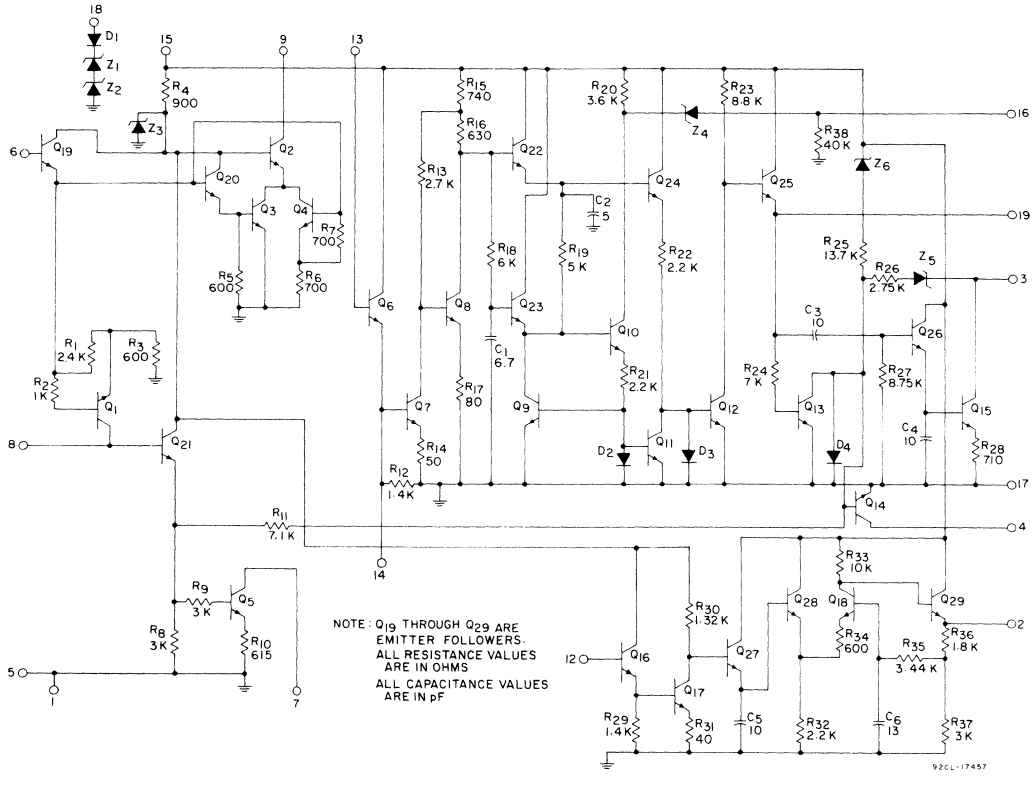


Fig. 2 - Simplified schematic diagram of the CA3068.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	CIRCUIT Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Static (DC) Characteristics							
Quiescent Circuit Current	I_{15}	–	3	15	–	45	mA
DC Voltages:							
Terminal 2 (Sound)	V_2	–	5	–	6	–	V
Terminal 3 (Keying Input)	V_3	–	3	6.4	–	10	V
Terminal 7 (1) (AGC)	V_7	–	3	16	–	21	V
Terminal 7 (2) (AGC)	V_7	–	4	–	1	–	V
Terminal 8 (AGC Delay)	V_8	–	4	–	4	–	V
Terminal 9 (Cascode Collector)	V_9	–	3	–	8.5	–	V
Terminal 16 (Bias)	V_{16}	–	3	1.1	–	2.3	V
Terminal 18 (Zener)	V_{18}	$V_5 = V_{17} = 0$ V, $I_{18} = 1$ mA	–	10.6	11.9	13.2	V
Terminal 19 (White Level)	V_{19}	–	5	6	–	10	V
Dynamic Characteristics							
Video Sensitivity	e_I	$f_O = 45.75$ MHz, Mod. (AM) = 85% at 400 Hz; Adjust e_I for 4 $V_{p\text{-}p}$ at Term. 19	6	40	100	200	μV
Sync. Tip Level Voltage	V_{19}	$f_O = 45.75$ MHz, e_I(CW) = 10 mV	6	0.4	0.8	1.6	V
Automatic Fine Tuning (AFT) Drive Level Voltage	V_{14}		6	–	15	–	mV
Delay Bias Voltage: At e_I = 10 mV	V_7	$f_O = 45.75$ MHz, e_I(CW) = 20 mV;	6	16	–	–	V
At e_I = 30 mV		Adjust R_1 for V_7 = 14 V		0.5	–	2	V
3.58 MHz Chroma Output Voltage	V_{19}	$f_O = 45.75$ MHz, e_I(step mod.) = 10 mV; $f_1 = 42.17$ MHz, e_I(step mod.) = 3.33 mV	6	0.5	0.8	–	V
4.5-MHz Sound Output Voltage	V_2	$f_O = 45.75$ MHz, e_I(step mod.) = 10 mV; $f_2 = 41.25$ MHz, e_I(step mod.) = 2.5 mV	6	50	200	–	mV
Parallel Input Impedance:							
Resistance at Term. 6	R_{I-6}	$f_O = 45.75$ MHz Impedance and Admittance measured at bias conditions as developed by circuit shown in Fig. 7	7	4	–	–	kΩ
Capacitance at Term. 6	C_{I-6}			–	2	–	pF
Resistance at Term. 12	R_{I-12}		7	–	4.5	–	kΩ
Capacitance at Term. 12	C_{I-12}			–	4	–	pF
Resistance at Term. 13	R_{I-13}		7	–	5	–	kΩ
Capacitance at Term. 13	C_{I-13}			–	4	–	pF
Parallel Output Impedance:							
Resistance at Term. 9	R_{O-9}		7	30	–	–	kΩ
Capacitance at Term. 9	C_{O-9}			–	3	–	pF
Cascode Transfer Characteristics: Magnitude of Forward Transadmittance	$\lvert y_f \rvert$		7	–	50	–	mmho
Reverse Transfer Capacitance	C_r		7	–	0.001	–	pF

CA3068

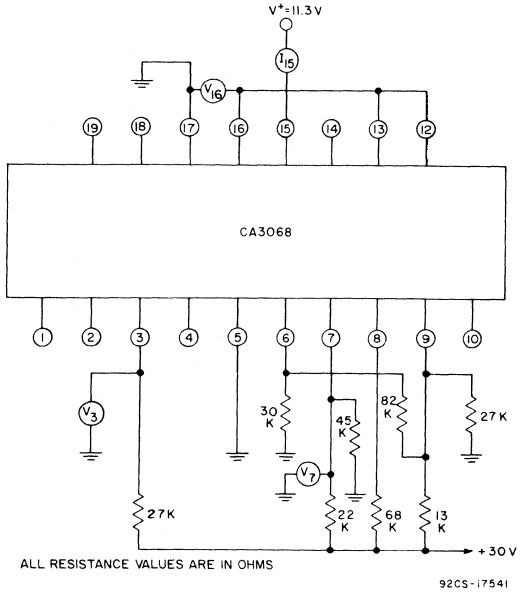


Fig. 3 – Test circuit for measurement of quiescent current (I_{15}), keying terminal voltage (V_3), bias voltage (V_{16}), AGC terminal voltage 1 (V_7), and cascode collector voltage (V_9)

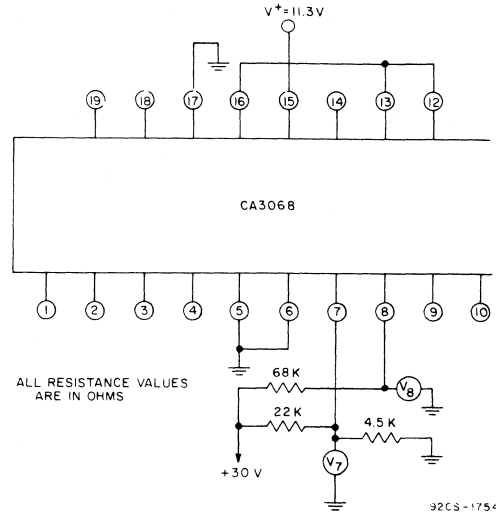


Fig. 4 – Test circuit for measurement of AGC term voltage 2 (V_7) and terminal 8 voltage (V_8).

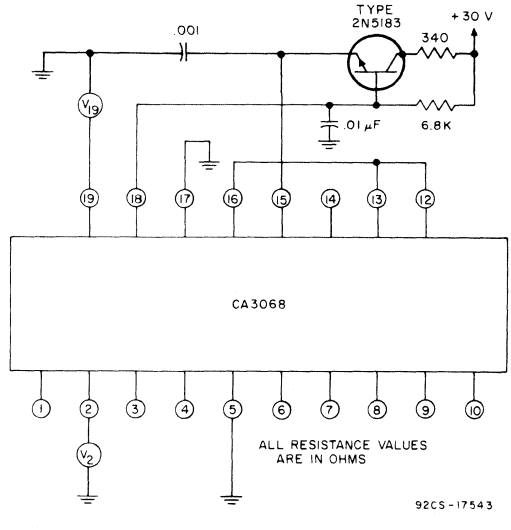
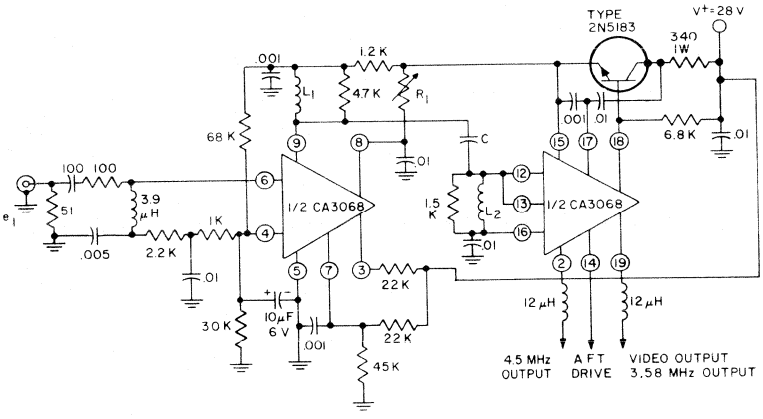


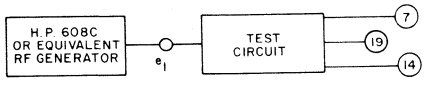
Fig. 5 – Test circuit for measurement of white level (V_{19}) and terminal 2 voltage (V_2).



R_1 = 50 KΩ POTENTIOMETER
L_1 = 2.2 μH: ADJUST No. OF TURNS FOR ALIGNMENT
L_2 = 1.5 μH: ADJUST No. OF TURNS FOR ALIGNMENT
C ≅ 1 pF : ADJUST FOR PROPER ALIGNMENT

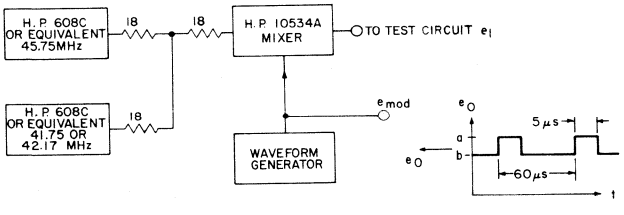
ALL RESISTANCE VALUES ARE IN OHMS

UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES:
LESS THAN 1.0 ARE IN MICROFARADS
1.0 OR GREATER ARE IN PICOFARADS



92CS-17537R1

(a) Test setup for measurement of video sensitivity, sync. tip level, delay bias, AFT drive voltage.



ALL RESISTANCE VALUES ARE IN OHMS

1 - ADJUST LEVEL "a" TO GIVE 6 dB ATTENUATION OF MIXER

2 - ADJUST LEVEL "b" SO THAT THE STEP (a-b) AT VIDEO OUTPUT TERM. IS 3 VOLTS. APPLY ONLY 45.75 MHz TO ADJUST STEP WAVEFORM.

92CS-17538

(b) Test setup for measurement of sound and chroma outputs.

Fig. 6 — Typical dynamic test circuit diagrams.

CA3068

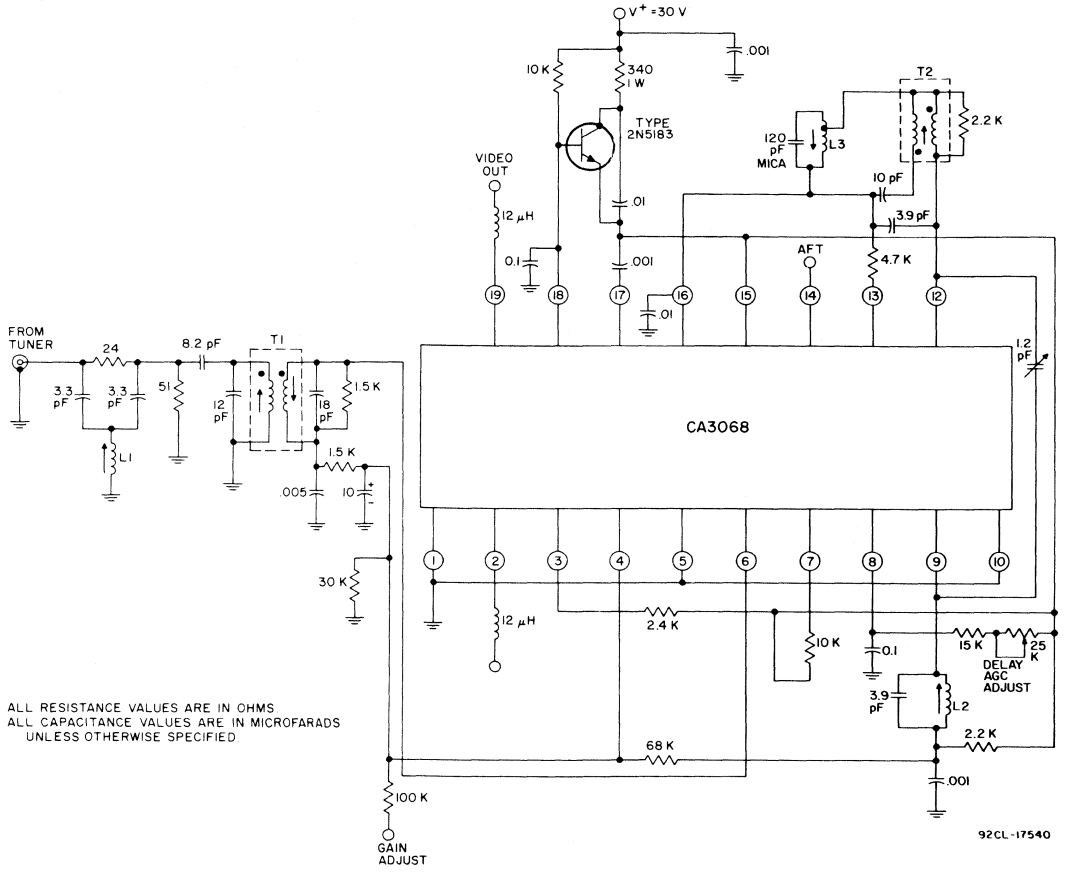


Fig. 7a – Color TV-IF amplifier test circuit.

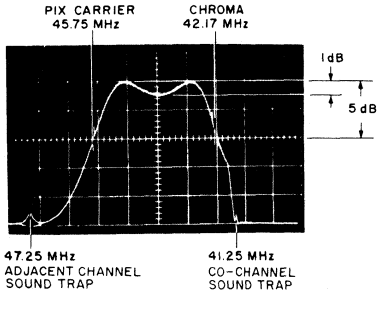


Fig. 7b – Color TV-IF amplifier with associated waveform and test circuit.

Alignment of the IF Amplifier

1. Apply a 2 to 4 mV signal from a sweep generator, Telon SV13 or equivalent to the input of the IF amplifier.
2. Apply a negative DC supply voltage, to the Gain Adju Terminal.
3. Set the gain supply voltage to provide a peak-to-pea output of 6 volts.
4. The overall response curve should conform to th waveform shown in Fig. 7b.

TYPICAL COLOR–TV VIDEO SYSTEM

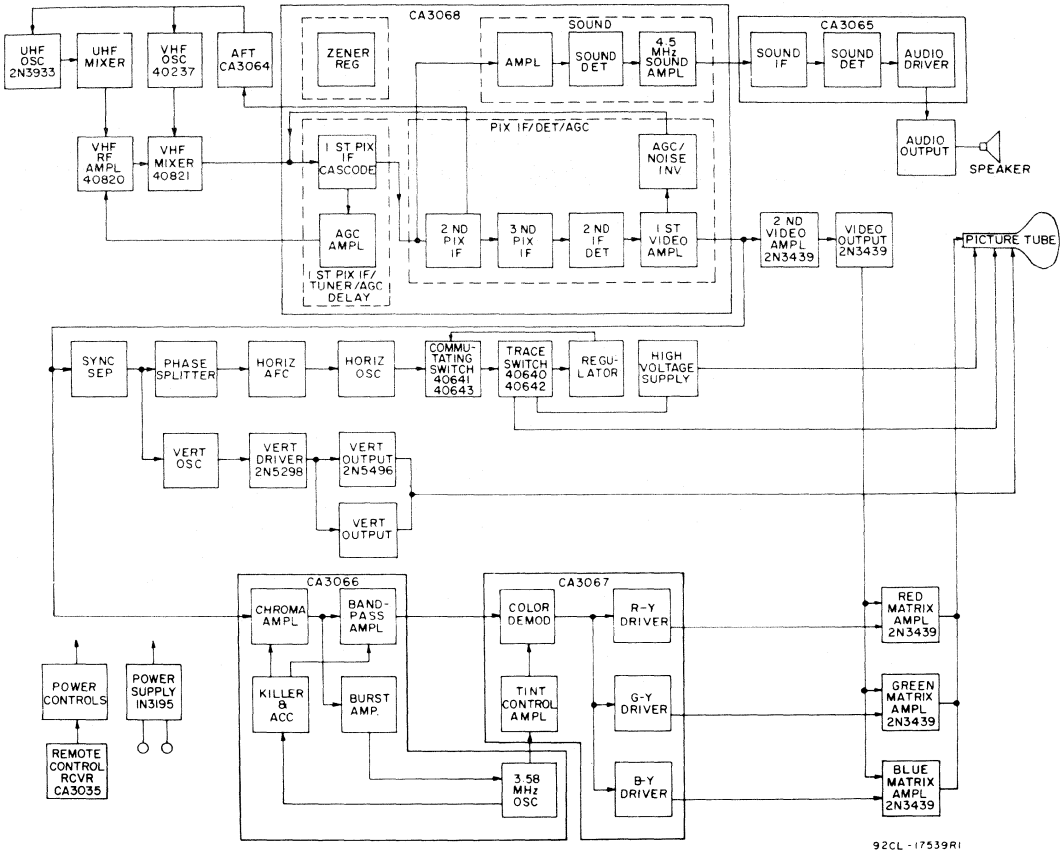


Fig. 8 – Block diagram of a typical color TV receiver utilizing the CA3068.

Application Information

A block diagram of a typical color TV application of the CA3068 is shown in Fig. 8. The input from the TV tuner is applied to the IF cascode amplifier of the IC. The cascode amplifier has a gain reduction of 50 dB typ. and a gain of 35 dB typ. The cascode output is coupled to succeeding stages via the IC lead interconnections. Associated with the cascode amplifier is an AGC delay network that provides gain control for the RF amplifier. This arrangement enables the circuit designer to introduce the desired bandpass-shaping circuitry between the cascode input stages and the remaining IF stages. These IF stages provide an additional gain of 40 dB typ. The output, taken from the emitter of the second IF stage, also provides a buffered AFT signal that is designed to drive the RCA-CA3064 TV Automatic Fine-Tuning IC.

The IF detector circuit provides an extremely linear output signal that is DC coupled to the first video amplifier. The first video amplifier has a voltage gain of 12 dB typ. The detector and video amplifier circuits provide a signal which has in addition to its linear output an extremely sharp limiting characteristic. The maximum video output level is approximately 7 volts peak-to-peak. The sharp limiting action of this circuit clips any signal (e.g. impulse noise) that exceeds this 7-volt value.

The video amplifier also provides a signal which drives a keyed AGC signal. The unique keyed AGC circuits utilize active devices that virtually eliminate noise from interfering with the action of the AGC. A separate sound section provides amplification at intercarrier frequencies, sound carrier detection, and sound carrier amplification. This sound section is designed to drive the RCA-CA3065 TV Sound System IC.

A color IF circuit with associated performance data is shown in Fig. 7. For a more detailed description of the CA3068 and related performance and IF printed circuit construction information, refer to the RCA Application Note ICAN-6303.

CA3070, CA3071, CA3072

Television Chroma System

Features:

CA3070

- Voltage Controlled Oscillator
- Keyed APC & ACC Detectors
- DC Hue Control
- Shunt Regulator

CA3071

- ACC Controlled Chroma Amplifier
- DC Chroma Gain Control
- Color Killer
- Amplifier Short-Circuit Protection

CA3072

- Synchronous Detector with Color Difference Matrix
- Emitter-Follower Output Amplifiers with Short-Circuit Protection

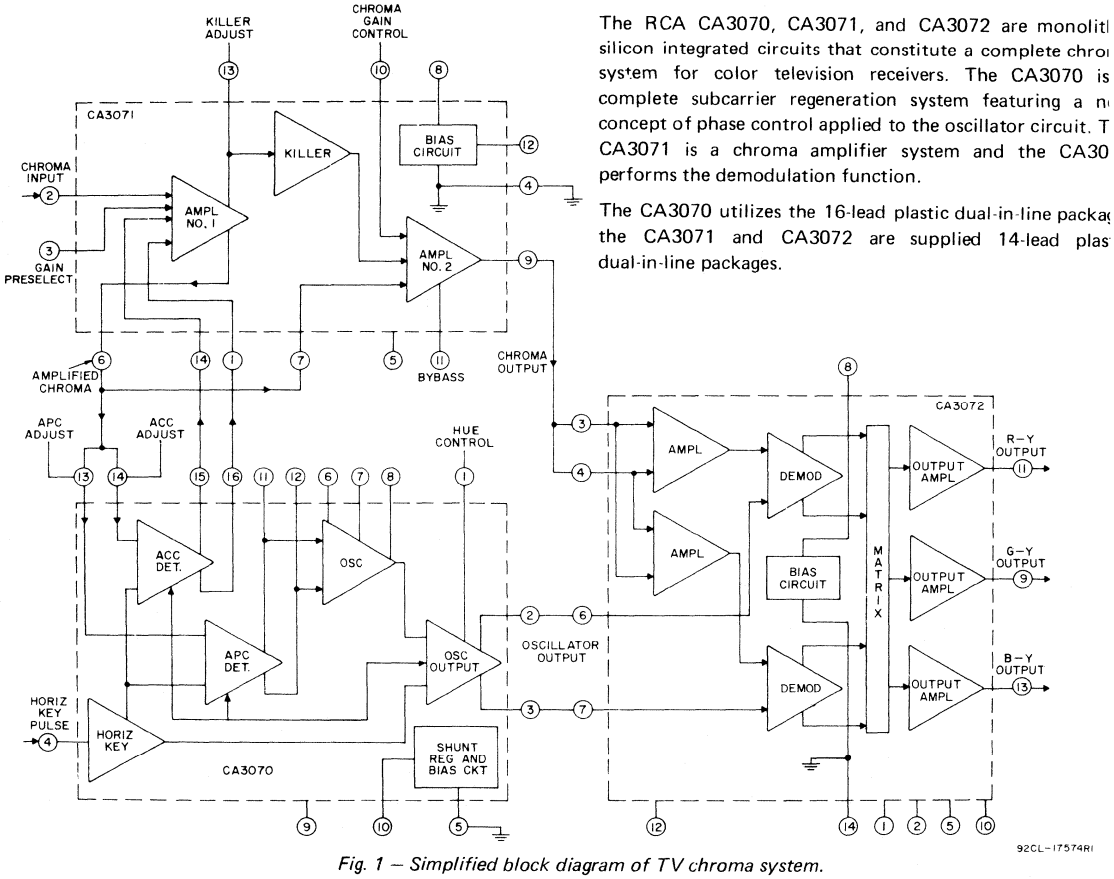


Fig. 1 – Simplified block diagram of TV chroma system.

The RCA CA3070, CA3071, and CA3072 are monolitl silicon integrated circuits that constitute a complete chro system for color television receivers. The CA3070 is complete subcarrier regeneration system featuring a n concept of phase control applied to the oscillator circuit. T CA3071 is a chroma amplifier system and the CA30 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line packa the CA3071 and CA3072 are supplied 14-lead plas dual-in-line packages.

File Number **46**

CA3070 Chroma Signal Processor

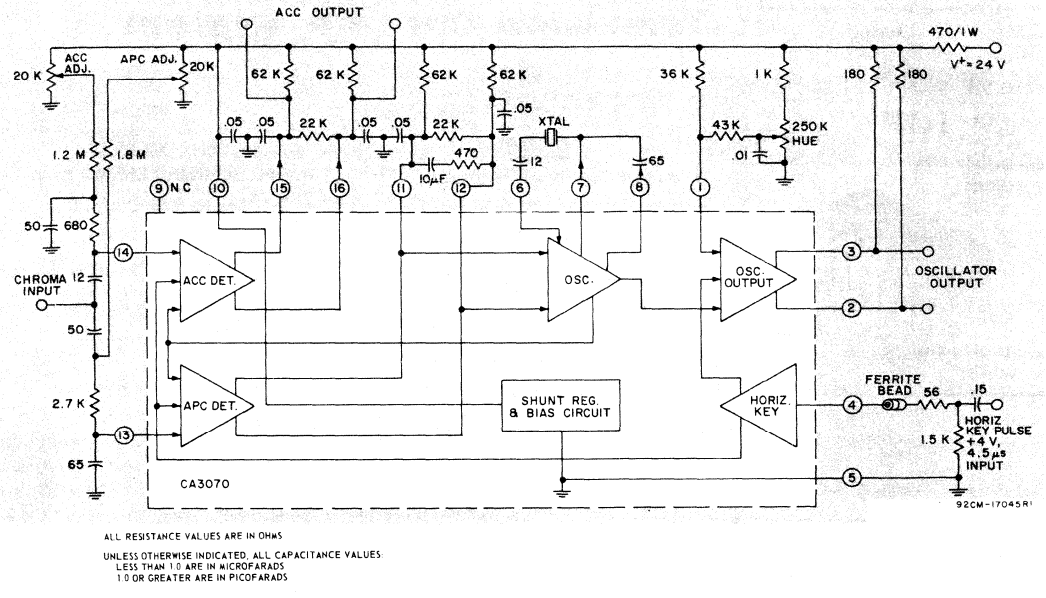


Fig. 2 – Functional diagram of RCA-CA3070.

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

CA3070, CA3071, CA3072

MAXIMUM RATINGS, *Absolute Maximum-Values at $T_A = 25°C$*

DC Supply Voltage and Current . . . . . See Charts Below
Device Dissipation:
Up to $T_A = +70°C$ . . . . . 530 mW
Above $T_A = +70°C$ . . . Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:
Operating . . . . . −40 to +85 °C
Storage . . . . . −65 to +150 °C
Lead Temperature (During Soldering):
At distance 1/32 in. (3.17 mm) from seating plane for 10 s max. . . . . +265 °C

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.
N1 Regulated voltage at terminal No. 10.
N2 Controlled by max. input current.
N3 Limited by dissipation.

Maximum Voltage and Current Ratings at $T_A = +25°C$

Terminal No.	Voltage▲ Min. Volts	Voltage▲ Max. Volts	Current Terminal No.	Current I_I mA	Current I_O mA
1	0	*	1	20	1
2	0	+16	2	–	–
3	0	+16	3	–	–
4	−5	N2	4	20	1
6	–	–	10	N3	1
7	–	–	11	–	–
8	–	–	12	–	–
10	0	N3	13	20	1
11	0	N1	14	20	1
12	0	N1			
13	0	N1			
14	0	N1			
15	0	+16			
16	0	+16			

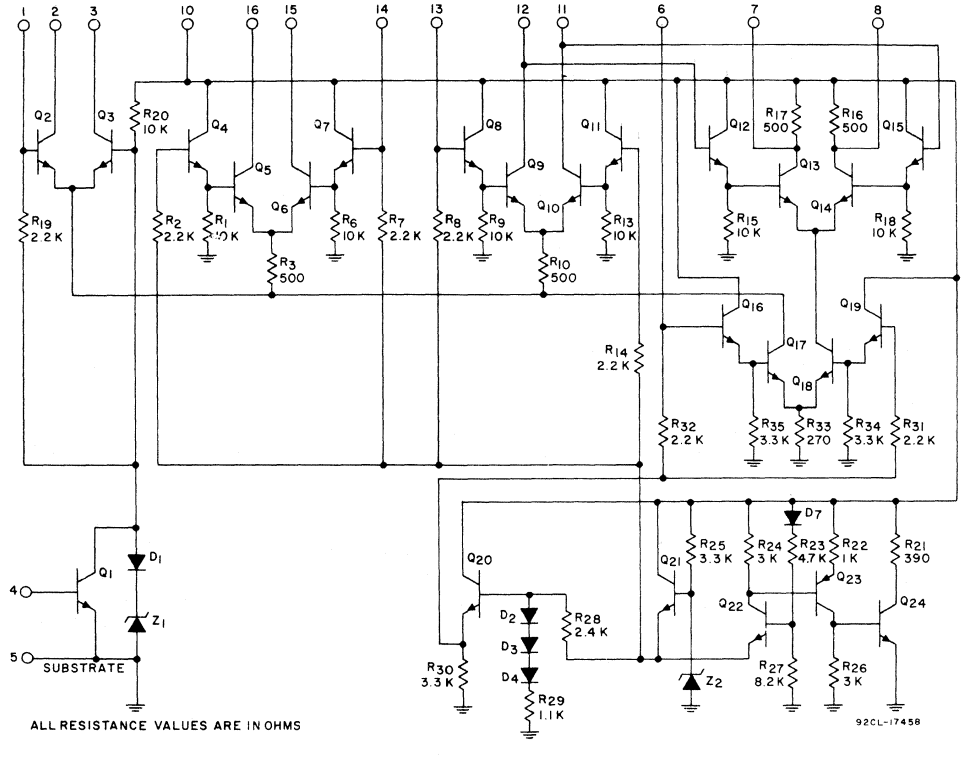


Fig. 3 – Schematic diagram CA3070.

CA3070, CA3071, CA3072

ELECTRICAL CHARACTERISTICS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3070 MIN.	LIMITS CA3070 TYP.	LIMITS CA3070 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Voltage:							
Hue Control	V_1	Switch in position 2	6.9	7.7	8.6	V	4c
Oscillator Input	V_6		–	2.8	–	V	4a
APC Input	V_{13}		–	6.5	–	V	4a
Regulator	V_{10}	V^+ = 21 V	11	12.3	13.5	V	4a
Regulator Change	V_{10}	V^+ = 27 V	–0.2	–	+0.2	V	4a
Horizontal Key Input	V_4	I_4 = –10 μA	5	—	—	V	4a
Currents:							
Oscillator Output	I_2		–	5.8	–	mA	4c
APC Output	I_{11}, I_{12}		–	1.45	—	mA	4b
ACC Output	I_{15}, I_{16}		–	1.45	–	mA	4b
Dynamic Characteristics							
Oscillator Outputs:							
Terminal No. 2	V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}	5
Terminal No. 3	V_3	S_1 in position 2	0.75	1.0	–	V_{p-p}	5
ACC Detected Output	V_{16}–V_{15}	S_1 in position 1	115	150	–	mV	5
Oscillator Pull-In Range	–		–	±400	–	Hz	5

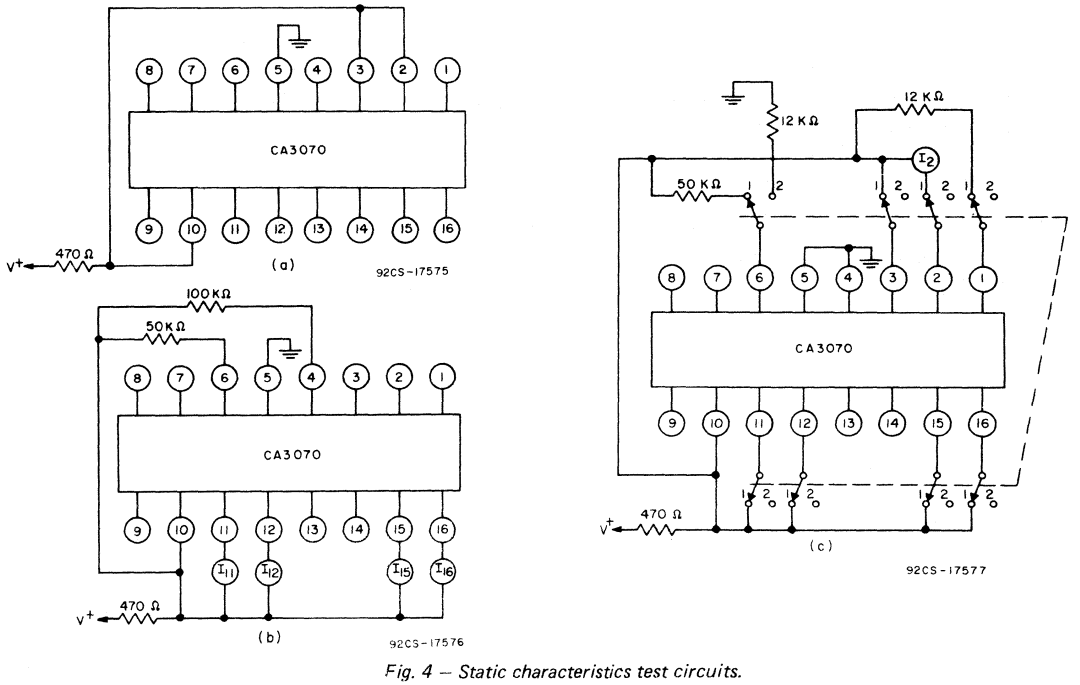


Fig. 4 – Static characteristics test circuits.

CA3070, CA3071, CA3072

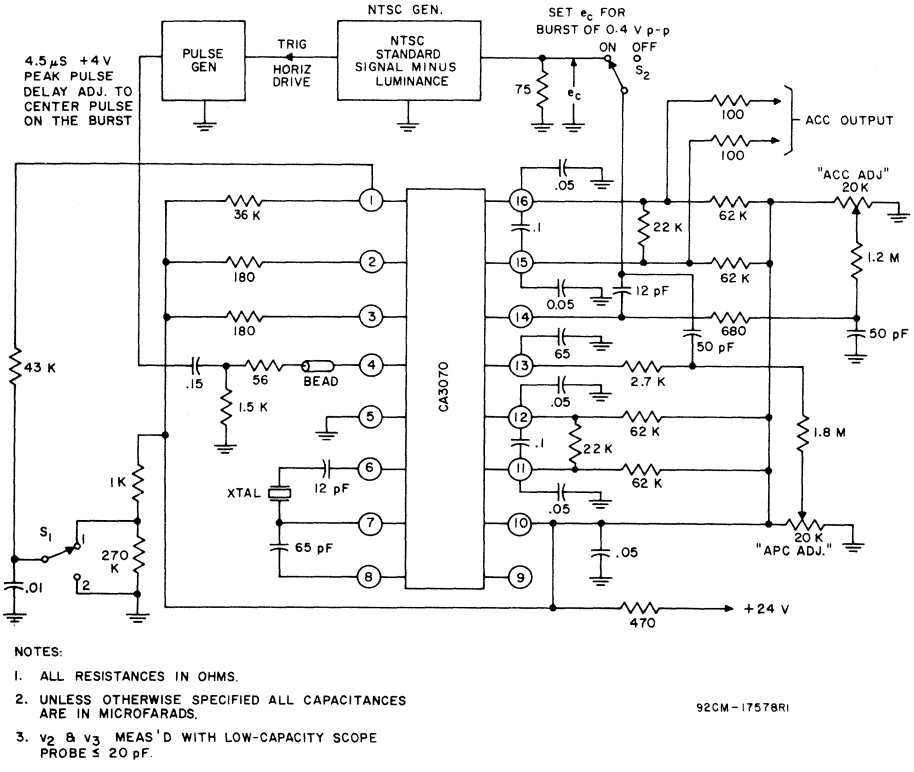


Fig. 5 – CA3070 Dynamic test circuit.

Dynamic Test Initial Adjustments

1. APC ADJUST: With S2 in "OFF" position adjust the "APC ADJ" potentiometer to set oscillator frequency at 3.579545MHz ±25 Hz. With S1 in position 1 measure frequency at terminal No. 2 output, using crystal probe shown in Fig. 6.
2. ACC ADJUST: With S2 in "OFF" position adjust "ACC ADJ" potentiometer to give an ACC output reading of 0 ±2 mV.

Procedure to Pull-in Range Measurement

1. Set S1 in position 1 and connect the crystal probe to terminal No. 2.
2. Turn S2 to "OFF" and set "APC ADJ." arm to ground.
3. Turn S2 to "ON" and gradually adjust "APC ADJ" until oscillator "locks" as witnessed by a sharp increase in ACC output voltage between terminal Nos. 15 and 16.
4. Turn S2 to "OFF" and adjust capacitor Cp of crystal probe for maximum deflection on Ballantine Meter.
5. Switch Ballantine meter to "Amplifier" position and read oscillator frequency on counter.
6. Repeat steps 2 – 5 with "APC ADJ" arm set to terminal No. 10 instead of to ground.

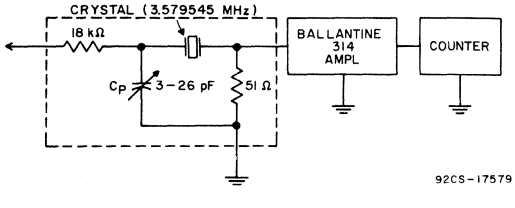


Fig. 6 – Crystal probe for frequency measurements.

A3071 Chroma Amplifier

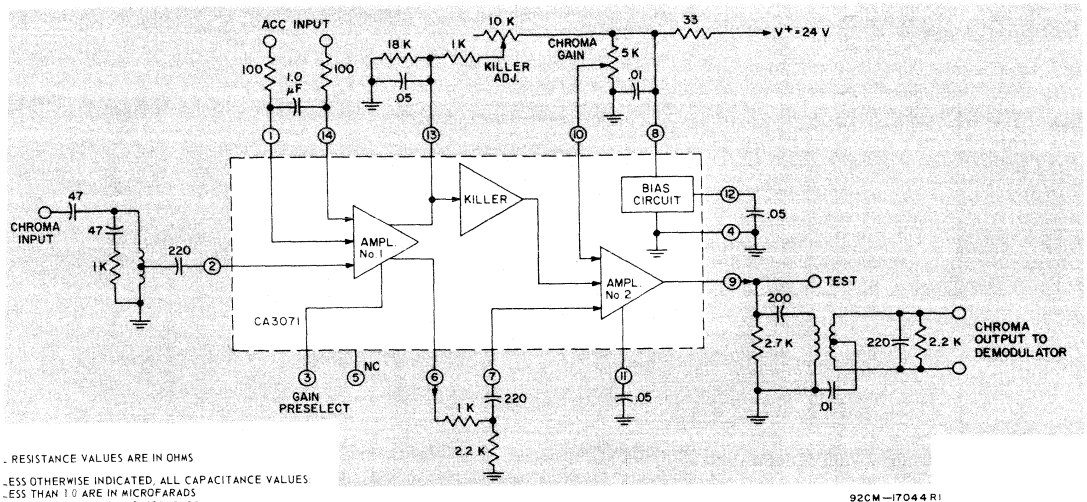


Fig. 7 – Functional diagram of RCA-CA3071.

e CA3071 is a combined two-stage chroma amplifier and ctional control circuit. The input signal is received from video amplifier and applied to terminal No. 2 of the ut amplifier stage. The first amplifier stage is part of the C system and is controlled by differential adjustment m the ACC input terminal Nos. 1 and 14. The output of 1st amplifier is directed to terminal No. 6 from where signal may be applied to the ACC detection system of CA3070 or an equivalent circuit. The output at terminal . 6 is also applied to terminal No. 7 which is the input to 2nd amplifier stage. Another output of the 1st amplifier terminal No. 13 is directed to the killer adjustment circuit. The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at* $T_A = 25^\circ C$

C Supply Voltage (Terminal 8 to Terminal 4) ..... 30 VDC

evice Dissipation:

Up to $T_A = +70^\circ C$ ..... 530 mW

Above $T_A = +70^\circ C$ .... Derate Linearly at 6.7 mW/°C

mbient Temperature Range:

Operating ..... −40 to +85 °C

Storage ..... −65 to +150 °C

ead Temperature (During Soldering):

At distance 1/32 in (3.17 mm) from seating plane for 10 s max. ..... +265 °C

Maximum Voltage and Current Ratings @ $T_A = +25^\circ C$

Current			Voltage*		
Terminal No.	I_I mA	I_O mA	Terminal No.	MIN VOLTS	MAX VOLTS
1	5	1.0	1	−5	+15
2	5	1.0	2	−5	+5
3	10	10	3	0	+2
6	1.0	20	6	0	+24
7	5	1.0	7	−5	+5
9	1.0	20	8	0	+30
12	1.0	5	9	0	+24
14	5	1.0	10	0	+24
			11	0	+24
			12	0	+20
			13	0	+20
			14	−5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

CA3070, CA3071, CA3072

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	LIMITS CA3071 TYP.	LIMITS CA3071 MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages: Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	–	17.3	–	V	8
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	–	1.75	–		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	–	20	–		
Unbalanced	V_6	S_1 Open, S_2 Closed	–	13.5	–		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	–	1.5	–		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	–	20.6	–		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g = 30 mV_{RMS} Measure v_6	14	–	–	dB	9
Amplifier No. 2 Voltage Gain	A_{V2}	V_g = 1.0 V (RMS) Measure v_7	–	14	–	dB	
Max. Chroma Output Voltage	v_9		–	2	–	V_{RMS}	13
10% Chroma Gain Control Reference Voltage	$V_8 - V_{10}$	E_g = 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	9
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g = 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_9	–	–	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g = 50 mV_{RMS}, adjust Chroma control to min. Chroma Output	–	–	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		–	12	–	MHz	11, 12
Amplifier No. 2			–	30	–		
Ampl. No. 1 Input Impedance	r_i1		–	2	–	kΩ	9
	c_i1		–	4	–	pF	
Ampl. No. 1 Output Impedance	r_o1		–	85	–	Ω	
Ampl. No. 2 Input Impedance	r_i2		–	2.1	–	kΩ	
	c_i2		–	3.5	–	pF	
Ampl. No. 2 Output Impedance	r_o2		–	85	–	Ω	

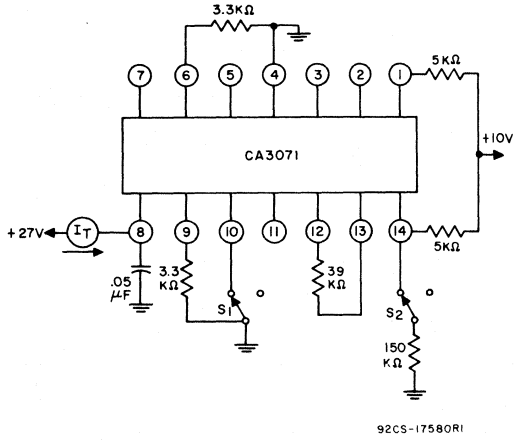


Fig. 8 – Static characteristics test circuit–CA3071.

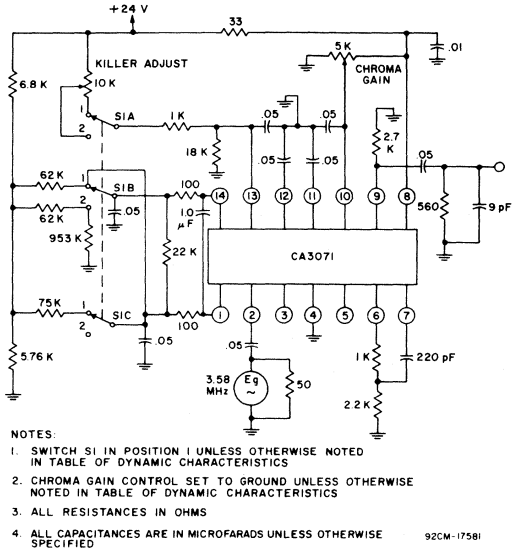


Fig. 9 – Dynamic characteristics circuit-CA3071.

CA3070, CA3071, CA3072

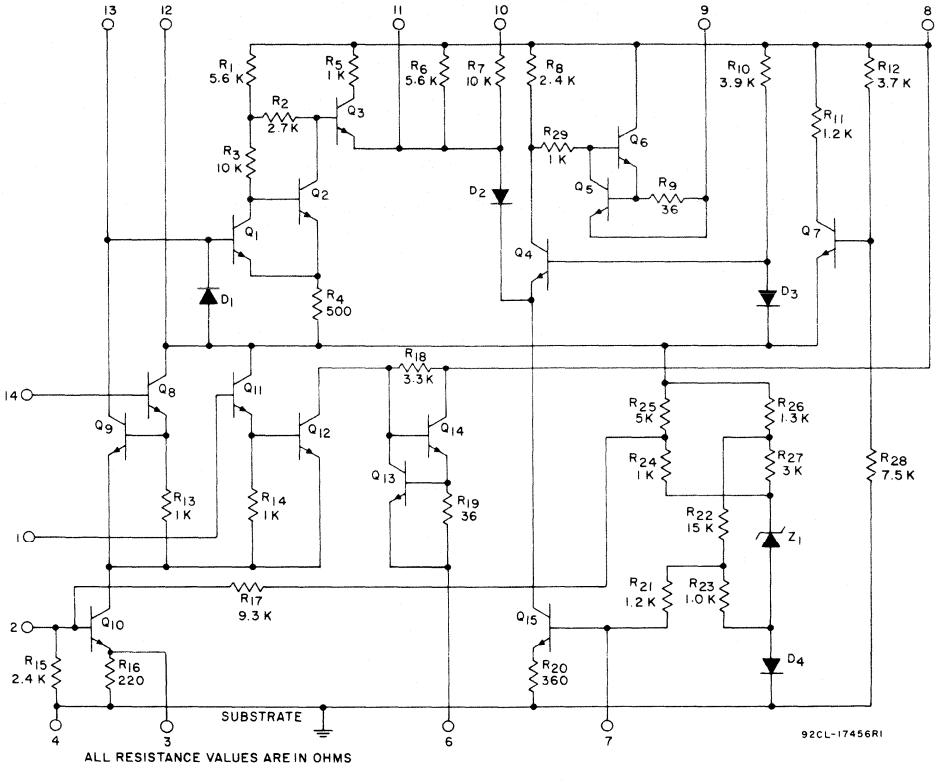


Fig.10–Schematic diagram for CA3071.

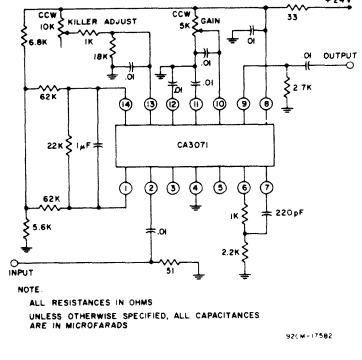


Fig. 11 – CA3071 Wideband amplifier circuit.

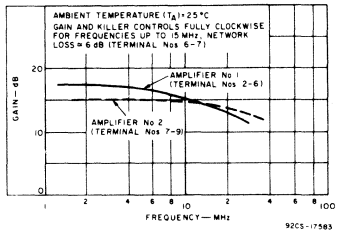


Fig. 12 – Frequency response for wideband amplifier CA3071.

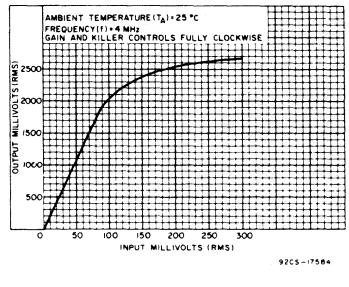


Fig. 13 – Typical CA3071 wideband amplifier linearity

CA3070, CA3071, CA3072

CA3072 Chroma Demodulator

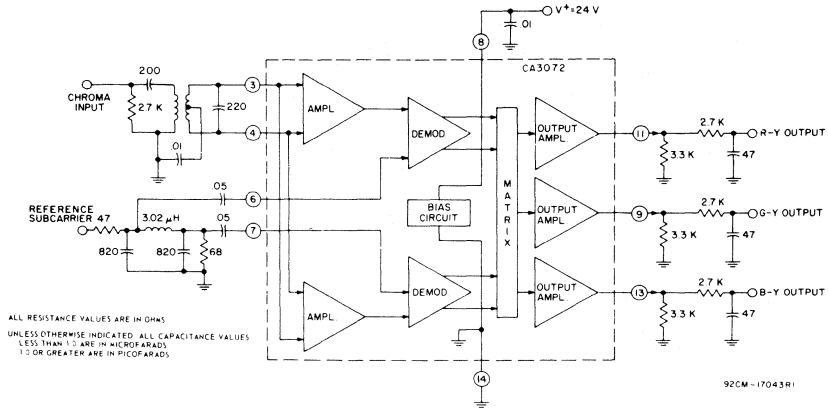


Fig. 14 – Functional diagram of RCA-CA3072.

The CA3072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the CA3072 are suitable for driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25° C*

DC Supply Voltage (Terminal 8 to Terminal 14)	27 V
Reference Input Voltage	5 V_{p-p}
Chroma Input Voltage	5 V_{p-p}
Device Dissipation:	
Up to T_A = +70°C	530 mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265°C

Maximum Voltage and Current Ratings at T_A = +25°C

	Voltage*		Current		
Terminal No.	MIN VOLTS	MAX VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	–	–
4	0	+5	4	–	–
6	0	+12	6	–	–
7	0	+12	7	–	–
8	0	+27	8	–	–
9	0	+20	9	1.0	20
11	0	+20	11	1.0	20
13	0	+20	13	1.0	20

*With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

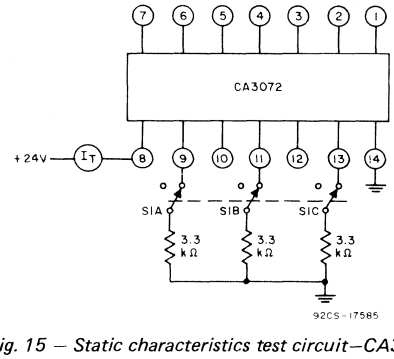


Fig. 15 – Static characteristics test circuit–CA3072.

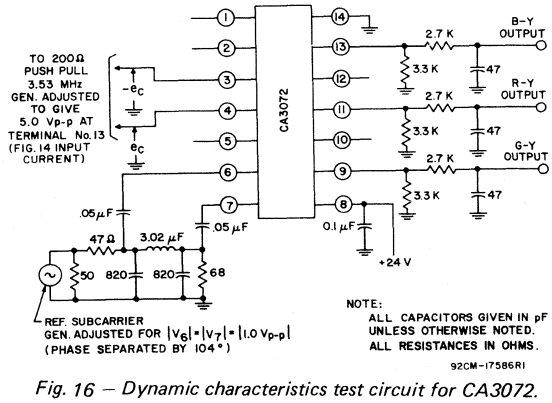


Fig. 16 – Dynamic characteristics test circuit for CA3072.

CA3070, CA3071, CA3072

ELECTRICAL CHARACTERISTICS, at T_A = 25° C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3072			UNITS	TEST CIRCUITS
			MIN.	TYP.	MAX.		FIG.
Static Characteristics							
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	26.5	mA	15
With No Output Loads		S_1 Open	–	9			
G-Y, R-Y, B-Y Outputs	V_9, V_{11}, V_{13}	S_1 Closed	13.2	14.7	15.8	V	
Chroma Inputs	V_3, V_4	S_1 Open	–	3.3	–		
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.2	–		
Dynamic Characteristics							
Demodulator Unbalance	v_9,v_{11},v_{13}	$V_3 = V_4 = 0$	–	–	0.8	V_{p-p}	16
Maximum Color Difference Output Voltage	v_{13}	$V_3 = V_4 = 0.6$ V_{p-p}	8.0	–	–	V_{p-p}	
	v_{11}		5.5	–	–		
	v_9		1.2	–	–		
Chroma Input Sensitivity	v_3	Adjust e_c for 5.0 V_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35		
Relative R-Y Output	v_{11}		3.5	–	4.2		
Relative G-Y Output	v_9		0.75	–	1.25		
V_{DC} Difference Between any two Output Terminals	$\lvert V_9 \rvert - \lvert V_{11} \rvert$ $\lvert V_9 \rvert - \lvert V_{13} \rvert$ $\lvert V_{11} \rvert - \lvert V_{13} \rvert$	$e_c = 0$	–	–	0.6	V	
Input Impedance Reference Subcarrier Inputs	r_i6, 7		–	1.7	–	kΩ	
	c_i6, 7		–	6	–	pF	
Input Impedance at Chroma Inputs	r_i3, 4		–	0.95	–	kΩ	
	c_i3, 4		–	6	–	pF	
Output Resistance	r_o9, r_o11, r_o13		–	180	–	Ω	

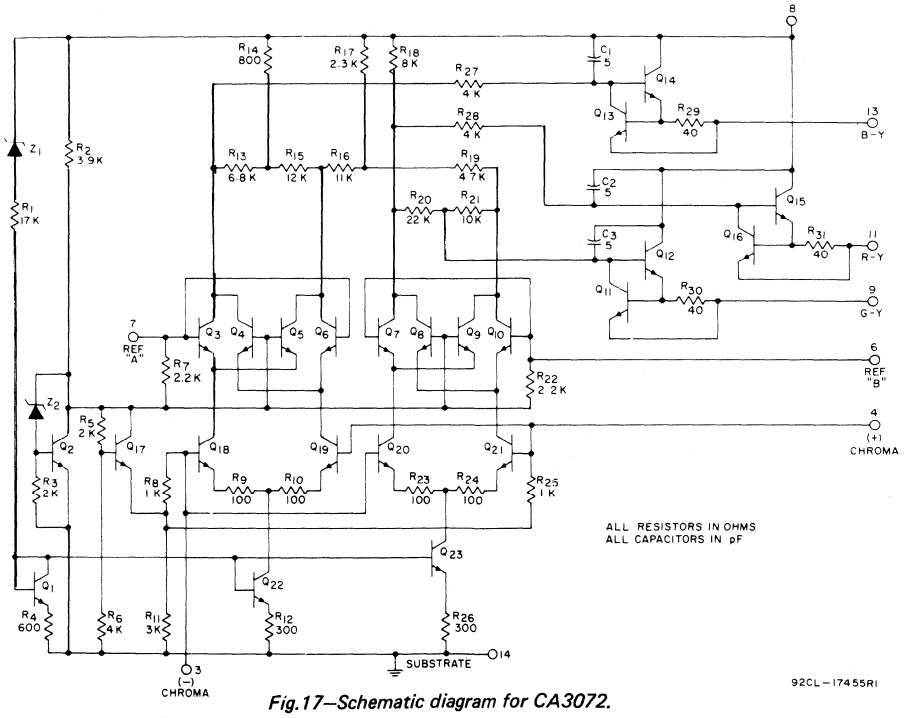


Fig.17–Schematic diagram for CA3072.

CA3070, CA3071, CA3072

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of Fig. 18 is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 3, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

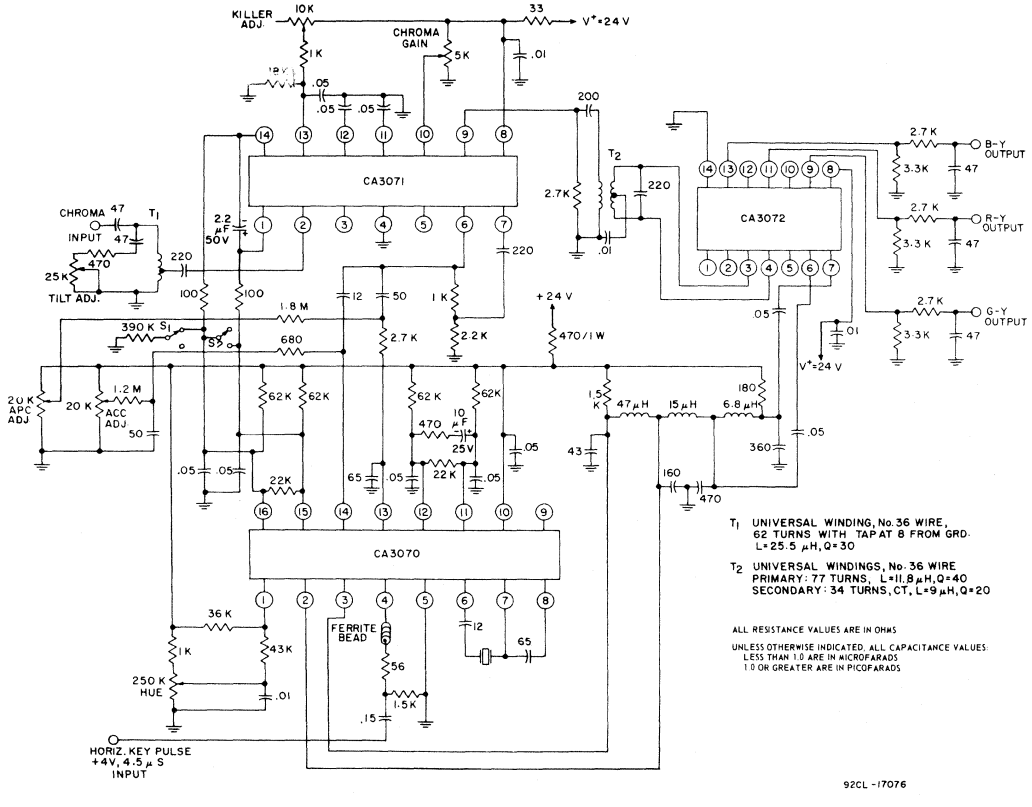


Fig. 18 – Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

ıe APC and ACC detectors are synchronous detectors ıich are keyed by the horizontal input pulse. This form of :tection eliminates the need for a burst separator as an dividual amplifier stage. When a positive pulse is present at rminal No. 4, the oscillator output is cutoff and the ;illator drive signal is diverted to the APC and ACC :tectors. Referring to Fig. 3, the APC detector (Q_9 & Q_{10}) ıd the ACC detector (Q_5 & Q_6) are emitter driven from the ;illator transistor (Q_{17}), when the oscillator output ampli- ər transistors (Q_2 & Q_3) are cutoff. The chroma signal is)plied to terminal Nos. 13 and 14. There is oscillator ırrent drive to the APC and ACC detectors during the :ying interval; burst separation is effectively accomplished / the gating action of the detectors. A further advantage of ıe keying action is the high gain made possible as a result of ıe low average current flow of the APC and ACC detectors. igh resistor values of 62 kilohms at the detector output ırminals provide proper detector bias consistent with the uty factor of the keying pulse. For a wider keying pulse, it necessary that smaller values of detector load resistors be sed.

ı the absence of the keying pulse (line period), the resistor, 20, biases the oscillator's output amplifier transistors (Q_2 & 3) on by keeping their emitters at a higher potential than ıe base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 lHz signal is now present at terminal Nos. 2 & 3. hotographs of oscilloscope traces for one line period at the ırminal Nos. 1, 2, and 3 are shown in Fig. 19 The effect of ıe keying pulse is shown in Fig. 19a, and the cutoff of the scillator output amplifier is shown in Fig. 19b and 19c.

The oscillator section of the CA3070 consists of the loop ormed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is :oupled through the series tuned crystal circuit back through erminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives he oscillator output amplifier and the APC & ACC de- ectors. Q_{17} is emitter coupled to transistor Q_{18}. The)scillator frequency and phase control is accomplished by he differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 18, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 18 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

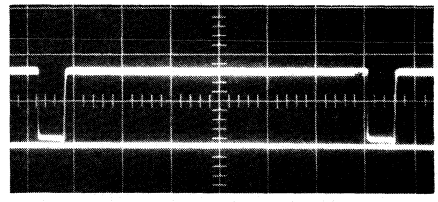


Fig. 19(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

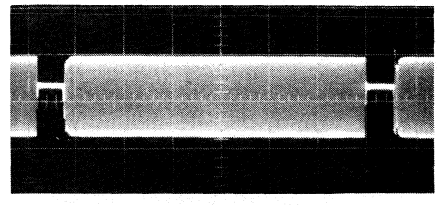


Fig. 19(b) - CA3070 terminal No. 2, 3.5 $V_{p\text{-}p}$ oscillator output; one horizontal line, (gated off during burst).

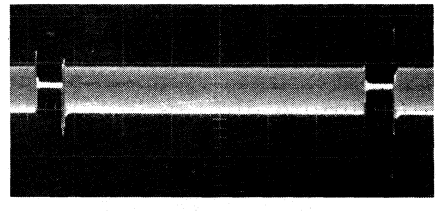


Fig. 19(c) - CA3070 terminal No. 3, 2.0 $V_{p\text{-}p}$ oscillator output; one horizontal line, (gated off during burst).

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

With the chroma signal still removed, the APC adjustment sets the frequency of the oscillator to 3.579545 MHz. Due to the gated off interval, a counter will not accurately record the frequency at the oscillator output amplifier terminals. Two simple and accurate methods are as follows: (1) a buffered crystal filter circuit, connected to the oscillator output amplifier terminals will continue to ring and fill the gated off window providing the proper interface to a counter; (2) the other method involves monitoring the demodulated output at the color difference output terminals

CA3070, CA3071, CA3072

of the CA3072. A zero beat signal, at the color difference outputs may be seen on an oscilloscope.

When these adjustments are made, similar oscilloscope traces should be seen as shown in Fig. 20.

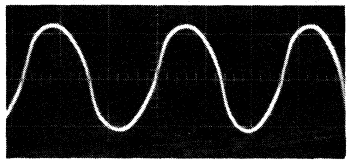


Fig. 20(a) - CA3070 terminal No. 6, oscillator waveform 1.1 V_{p-p} 3.58 MHz.

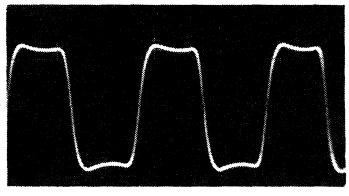


Fig. 20(b) - CA3070 terminal No. 7, oscillator waveform 1.4 V_{p-p} 3.58 MHz.

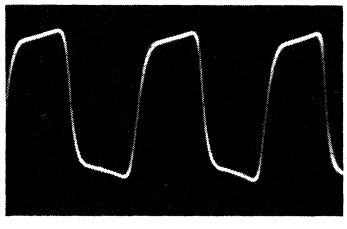


Fig. 20(c) - CA3070 terminal No. 8, oscillator waveform 1.6 V_{p-p} 3.58 MHz.

CA3071 CIRCUIT OPERATION

The CA3071 is the basic amplifier and control circuit of the chroma system. It contains the gain control functions of the ACC loop, the color killer, and the dc chroma gain control. The CA3071 is a wide band amplifier having two stages of voltage gain. Curves of frequency-response and linearity are shown in Figs. 12 & 13 for the wideband circuits shown in Fig. 11. This is the same basic amplifier as the one in the system shown in Fig. 18 except for the omission of the tuned circuits and the ACC loop connection. The amplifiers have bandwidths of greater than 10 MHz. and are usable well beyond 30 MHz. The signal swing of the wide band amplifier is in excess of 5 V_{p-p}., even with the typical load coupling as shown in Fig. 18. Fig. 21 (a, b and c) show the oscilloscope traces for an NTSC signal at the chroma input. The overall frequency-response curves are shown in Fig. 22.

CA3071 operation is as follows (Refer to Figs. 10 & 18). The input chroma signal is applied to terminal No. 2. This signal is amplified in a cascode differential circuit from Q_{10} to Q_{12}

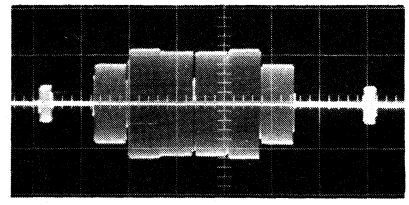


Fig. 21(a) - CA3071 chroma input 1.25 V_{p-p}; one horizonta line of NTSC input signal.

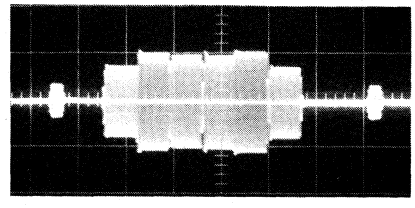


Fig. 21(b) - CA3071 terminal No. 6, amplifier No. 1 chroma output 2.3 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

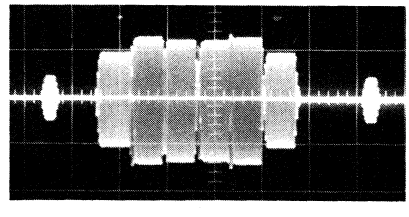


Fig. 21(c) - CA3071 terminal No. 9, amplifier No. 2 chroma output 5.5 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

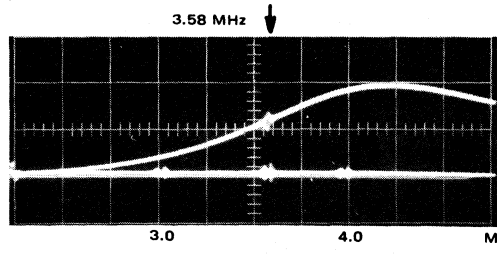


Fig. 22(a) - Frequency response sweep curve between terminal Nos. 2 & 6 for CA3071. f = 250 KHz/div.

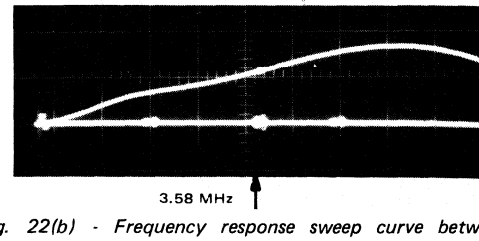


Fig. 22(b) - Frequency response sweep curve between terminal No. 2 of CA3071 and terminal No. 3 of CA3072. f = 250 KHz/div.

d the output is an emitter follower, Q_{14} (Terminal No.

The signal is divided in the Q_9 & Q_{12} differential ıplifier, depending on the applied ACC error signal ampli- ıde at terminal Nos. 1 & 14. The ACC error signal is de- ed from terminal Nos. 15 & 16 of the CA3070 and after tering, is applied to terminal Nos. 1 & 14 of the CA3071.

: low signal drive, the 390 kilohm resistor at switch S1 ormally closed) unbalances the differential amplifier for gh signal gain through Q_{12}. As the burst level at the roma input increases, the ACC drive changes differentially a positive direction at terminal No. 14 and a negative rection at terminal No. 14 and a negative direction terminal No. 1. At strong signal levels the gain is duced by diverting the balance of ac current in the fferential amplifier from Q_{12} to Q_9, which is shunted to : ground at terminal Nos. 12 and 13. The ACC loop is ɔmpleted through the chroma signal at terminal No. 6 of ıe CA3071 to terminal No. 14 (input) of the CA3070. A ɣpical ACC characteristic is shown in Fig. 23.

he chroma signal is buffer connected from terminal No. 6 › terminal No. 7 of the CA3071 and is amplified in the 2nd

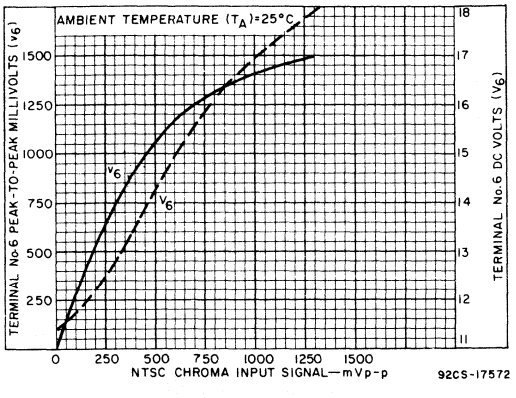


Fig. 23 - Typical ACC characteristics for chroma system of Fig. 18

ıtage of voltage gain. Both the color killer adjustment and the dc chroma gain control are applied to the 2nd stage to control the chroma output at terminal No. 9. The color killer section of the CA3071 is a Schmitt trigger & amplifier circuit consisting of transistors Q_1, Q_2 and Q_3. Under maximum chroma output conditions, the diode D_2 is reversed biased, and the signal path is through Q_{15}, Q_4 and Q_5 to terminal No. 9. When the color killer circuit is actuated, or the chroma gain control is adjusted to a higher positive voltage at terminal No. 10, the anode voltage of diode D_2 is increased to draw current from the signal path at the emitter of Q_4. This decreases the chroma gain as the potential at terminal No. 10 is increased. When the potential at terminal No. 10 is the same as terminal No. 8, the chroma output at terminal 9 is cutoff.

The color killer circuit provides an abrupt voltage swing at the anode of D_2 to cutoff the chroma output when the Schmitt trigger circuit is forward biased at terminal No. 13. In the circuit of Fig. 18, the color killer adjustment is a resistance divider circuit which establishes the threshold of burst level at which the killer operates the chroma amplifier.

CA3072 CIRCUIT OPERATION

The CA3072 is a chroma demodulator having full color difference signal demodulation capability. The chroma signal is applied to terminal Nos. 3 & 4 and the reference subcarrier signal is applied to terminals Nos. 6 & 7 of the CA3072. The output color difference signals are B-Y at terminal No. 13, R-Y at terminal No. 11, and G-Y at terminal No. 9. The typical level of differential chroma drive required at terminal Nos. 3 & 4 is 400 mV_{p-p}. The amplitude of chroma at terminal No. 6 & 7 is approximately 1.0 volt at 104° relative phase difference which results in a B-Y output amplitude of $5V_{p-p}$. The voltages of the R-Y & G-Y outputs are at 3.8 and 1.0 V_{p-p} respectively, when there is $5V_{p-p}$ output at B-Y. These comparative signals are based upon a complete phase rotation of the chroma relative to the subcarrier signal reference. The relative demodulation phase and amplitude ratios of the Fig. 18 circuit are shown in the oscilloscope trace photographs of Fig. 24. Using the hue control setting for B-Y phase at the B-Y output, the G-Y color-difference signal is approximately −104° and the R-Y color-difference signal is approximately +106°. Since the amplitude ratios are a function of the applied signal phase relationship, the NTSC color difference output signals are shown here primarily for phase reference conditions.

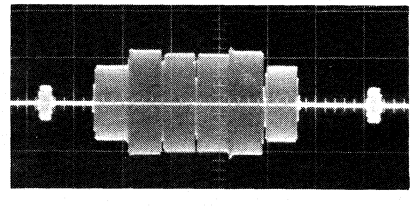


Fig. 24(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

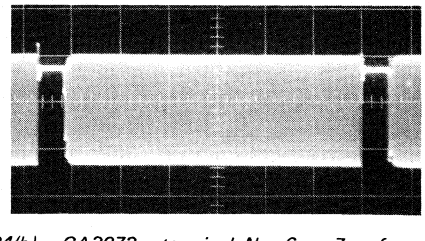


Fig. 24(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

CA3070, CA3071, CA3072

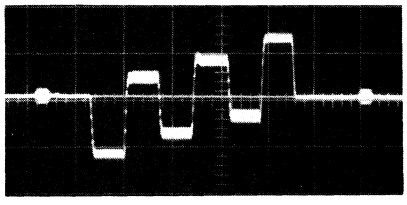


Fig. 24(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

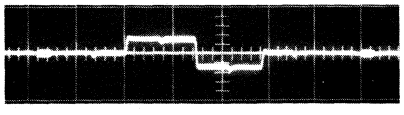


Fig. 24(d) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

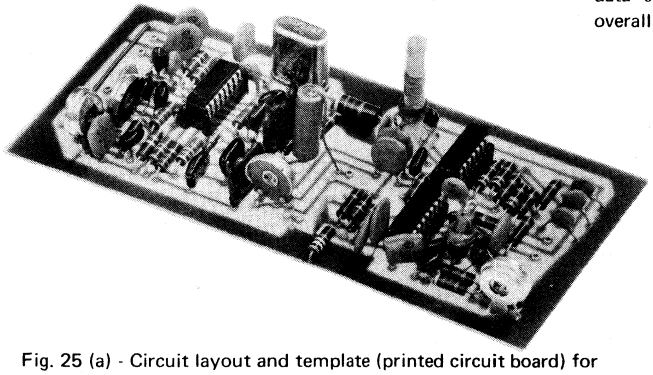


Fig. 25 (a) - Circuit layout and template (printed circuit board) for TV chroma system CA3070, CA3071, and CA3072.

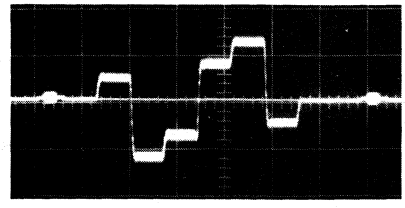


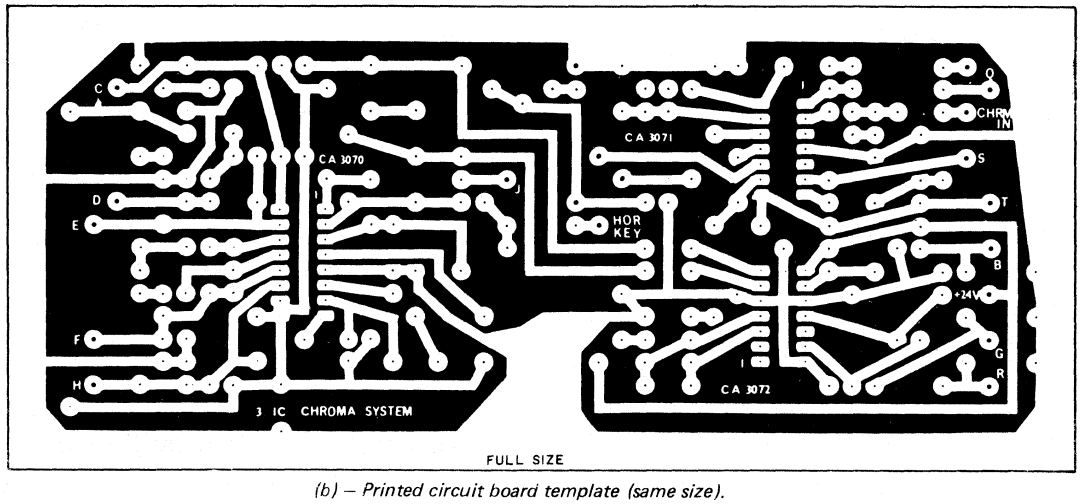
Fig. 24(e) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y outpu one horizontal line

CHROMA SYSTEM CONSTRUCTION

Fig. 25 shows the complete CA3070, CA3071 and CA307 chroma system in the Fig. 18 circuit. Table I lists the d terminal voltages for the system. The chroma gain and hu controls, as well as the switches S1 and S2 are removed. Th template circuit board layout is also shown for duplicatio purposes. It should be noted that a few component values ar modified in Fig. 18 from the dynarnic circuit values of th data sheet. These are necessary for system matching an overall filter requirements.

TABLE 1 TYPICAL CHROMA SYSTEM TERMINAL DC VOLTAGES (NO SIGNAL INPUT)

TERMINAL No.	DC VOLTS		
	CA3070	CA3071	CA3072
1	7.6	7.3	–
2	11.5	1.7	–
3	11.5	–	3.3
4	–1.7	0	3.3
5	0	–	–
6	2.8	11.4	5.9
7	11.2	1.4	5.9
8	11.2	23.0	24.0
9	–	VARIABLE	14.7
10	12.0	VARIABLE	–
11	7.8	VARIABLE	14.7
12	7.8	15.0	–
13	6.7	VARIABLE	14.7
14	6.7	7.1	0
15	7.3	–	–
16	7.1	–	–



(b) – Printed circuit board template (same size).

CA3121

V Chroma Amplifier/ emodulator

ovides Complete System for Processing Chroma
nen Used with RCA-CA3070 or CA3170

EATURES:

Excellent linearity in dc chroma gain-control circuit
Improved filtering resulting in reduced 7.2 MHz output from the color demodulators
Current limiting for short-circuit protection
Good tolerance to B+ supply variations
Good temperature coefficient stability

ne RCA-CA3121E is a monolithic silicon integrated circuit nroma amplifier/demodulator with ACC and killer control r color-TV receivers. It is designed to function compatibly ith the CA3070 or CA3170 in a two-package chroma stem. Figs. 5 and 6 show a functional block diagram and ie outboard circuitry of a typical two-package chroma system incorporating the CA3121E and CA3170, respectively.

The CA3121E is supplied in a 16-lead dual-in-line plastic package.

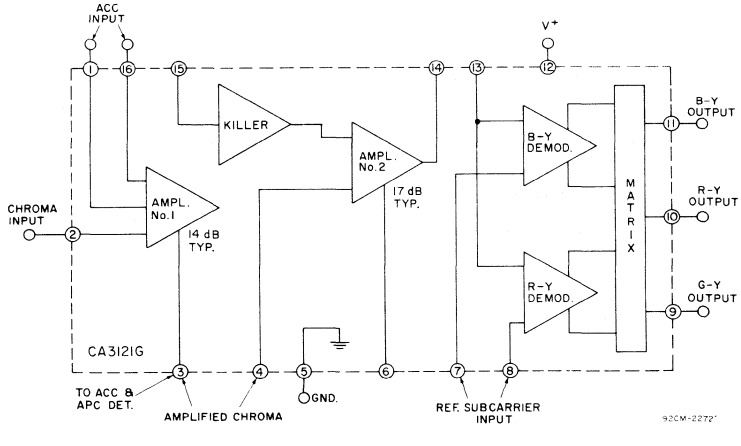


Fig. 1 — Functional block diagram of the CA3121E.

File Number **688**

CA3121

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

Supply Voltage	30 V
Device Dissipation:	
Up to $T_A = 55^oC$	1 W
Above $T_A = 55^oC$	derate linearly 10.5 mW/^oC
Operating Temperature Range	−40 to +85^oC
Storage Temperature Range	−65 to +150^oC
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265^oC

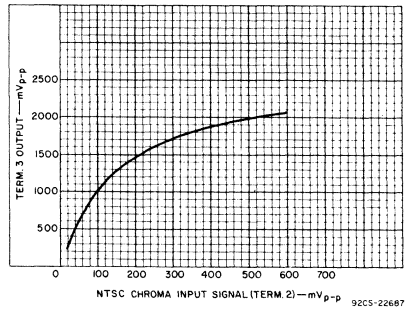


Fig. 2 —Typical ACC plot for the CA3121E when used with the CA3070.

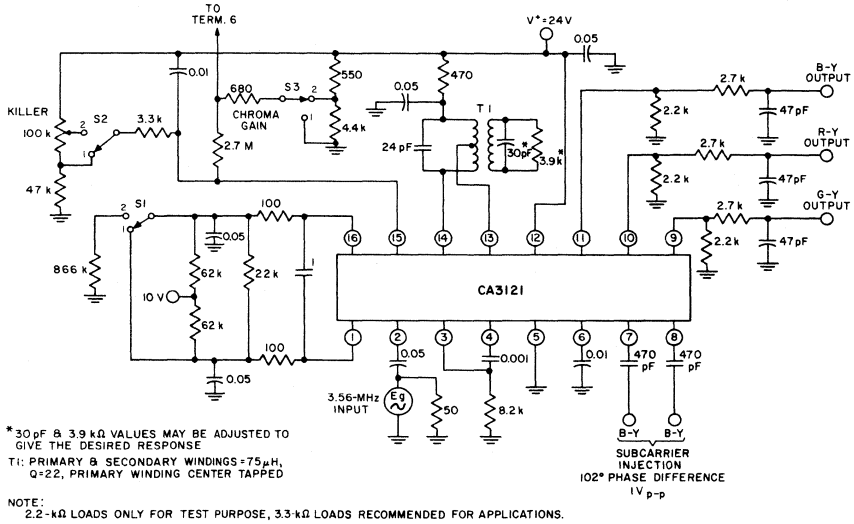


Fig. 3 — Typical characteristics test circuit for the CA3121E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C and Reference to Test Circuit (Fig. 3)

CHARACTERISTIC, TERMINAL MEASURED, AND SYMBOL	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current I_T	–	–	40	50	mA
Input Sensitivity V_2	Vary Eg; set V_4 for 55 mV RMS	6	10	15	mV RMS
Second-Stage Sensitivity V_4	Vary Eg; set V_{11} for 2 V RMS	25	55	100	mV RMS
Output Voltage (Killer off) V_{11}	Switch Position: S1=2, S2=2, S3=2 Adjust killer potentiometer until output drops	–	–	70	mV RMS
Demodulator Characteristics:					
Output Voltages V_9, V_{10}, V_{11}	–	13	14.3	15.6	V
DC Output Balance (Between any 2 outputs)	–	–0.6	–	+0.6	V
Unbalance V_9, V_{10}, V_{11}	Eg=0; Swith Position: S1=1, S2=1, S3=1	–	–	0.8	Vp-p
Relative Outputs— R-Y V_{10}	Vary Eg; set V_{11} for 2 V RMS	1.4	1.52	1.68	V RMS
G-Y V9		0.3	0.4	0.5	V RMS
Relative Phase— R-Y V_{10}	Vary Eg; set V_{11} for 2 V RMS; read phase of V_{10} and V_9	–101	–106	–111	degrees
G-Y V_9	with V_{11} as reference	112	104	96	degrees
Max. Output Voltage V_{11}	Eg = 750 mV	2.8	–	–	V RMS

CIRCUIT OPERATION

The CA3121E consists of three basic circuit sections: (1) amplifier No.1, (2) amplifier No.2, and (3) demodulator. Amplifier No.1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No.1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070, CA3170 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No.2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No.1 acts upon amplifier No.2 to greatly reduce its gain.

The output from amplifier No.2 (Terminal 14) is applied, through a filtering network, to the demodulator input (Terminal 13). The demodulator also receives the R-Y and B-Y demodulation subcarrier signals (Terminals 7 and 8) from the oscillator output of the Chroma Signal Processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3121E reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, and B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

CA3121

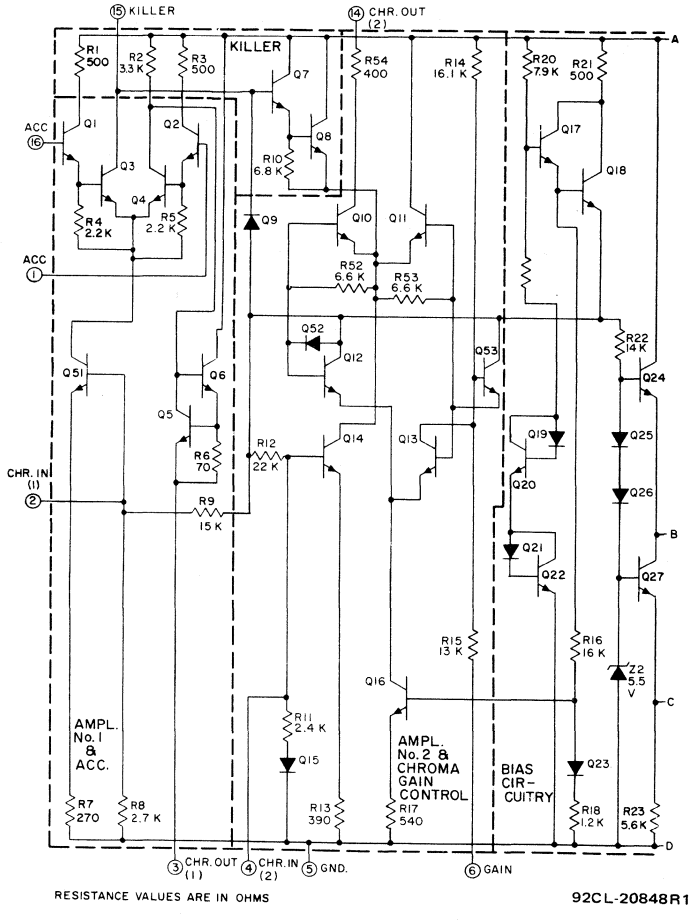


Fig. 4 - Schematic diagram of the CA3121E (cont'd on next page).

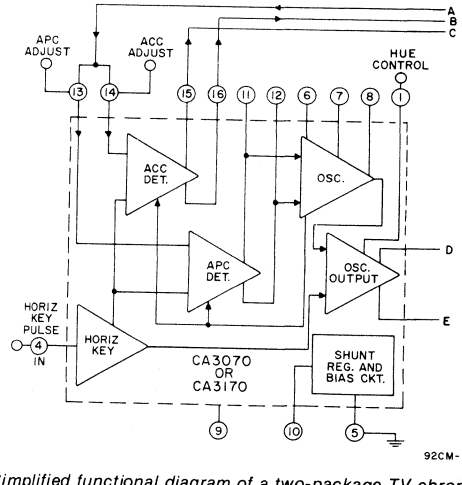


Fig. 5 — Simplified functional diagram of a two-package TV chroma system utilizing the CA3121E and CA3070 or CA3170 (cont'd on next page).

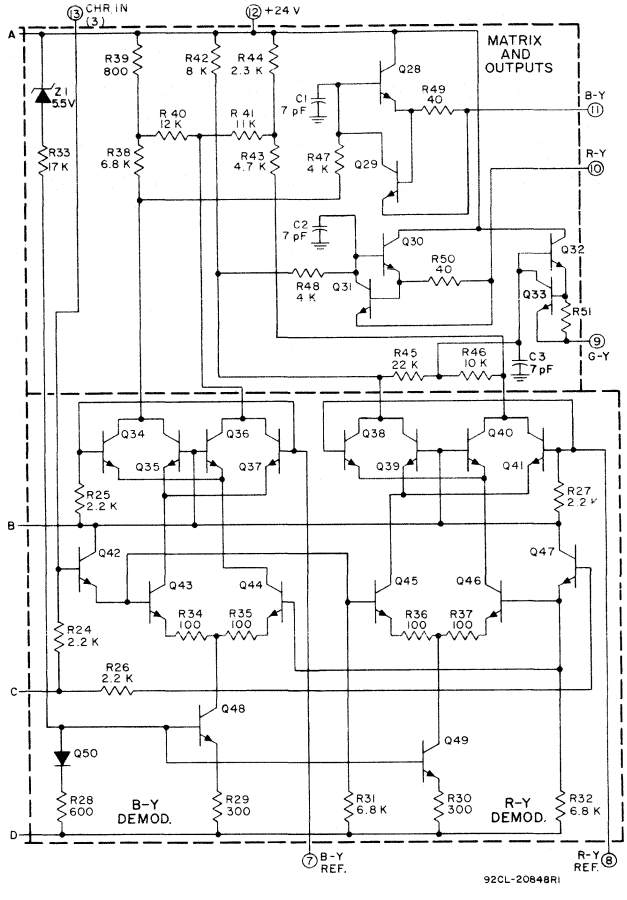


Fig. 4 - Schematic diagram of the CA3121E (cont'd from previous page).

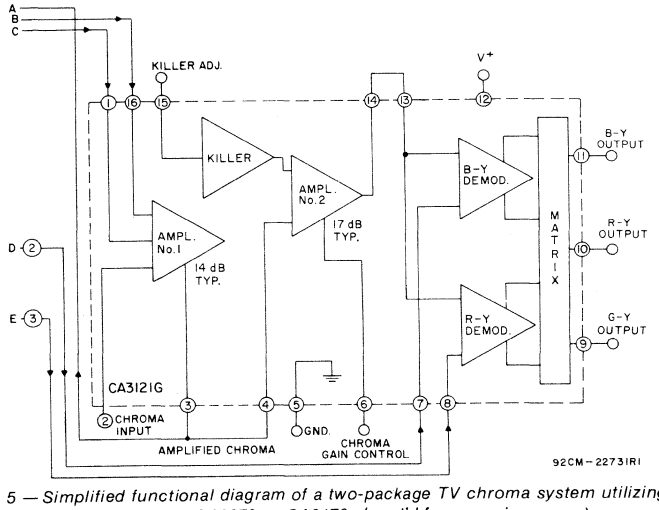


Fig. 5 — Simplified functional diagram of a two-package TV chroma system utilizing the CA3121E and CA3070 or CA3170 (cont'd from previous page).

CA3121

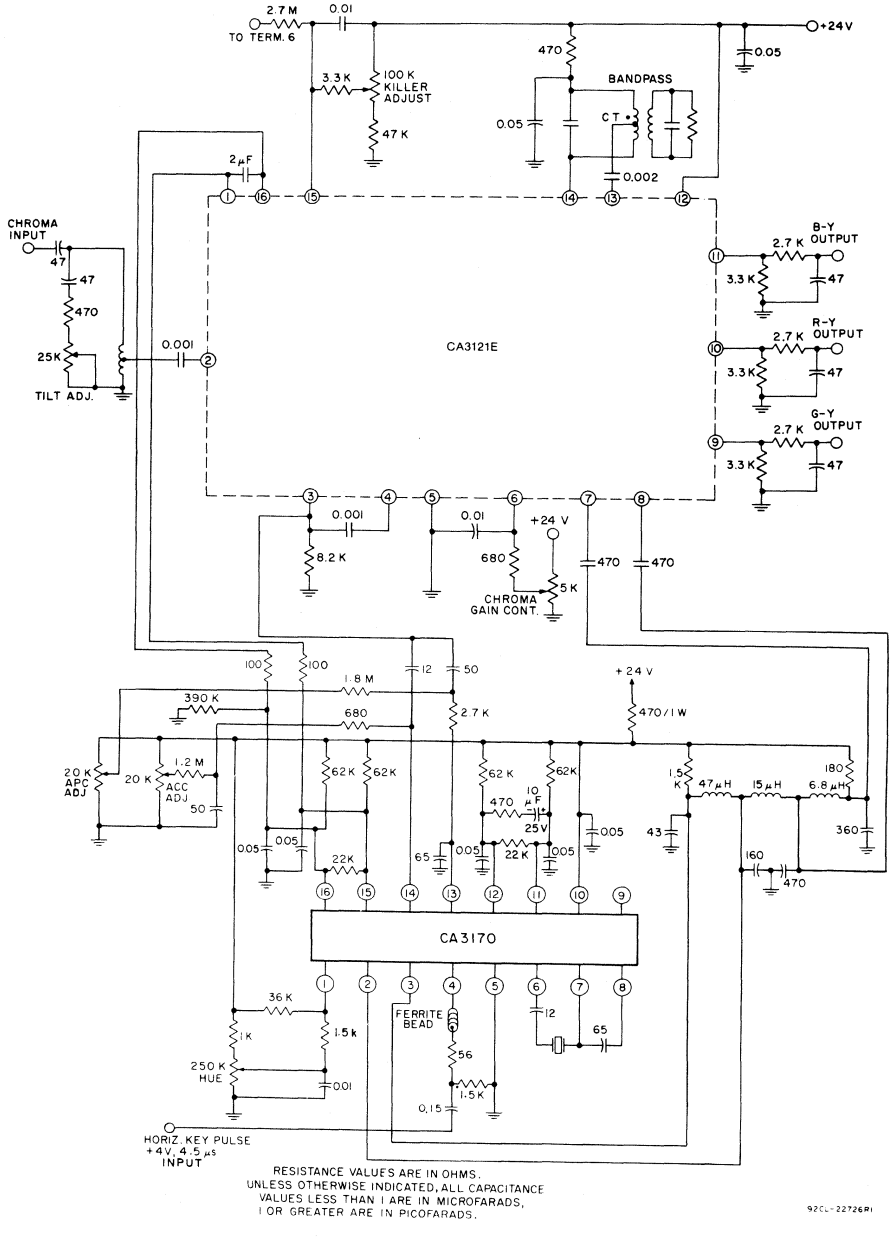


Fig. 6 — Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3170.

CA3125

'elevision Chroma Demodulator

'eatures:

- **Luminance input**
- **Blanking control input**
- **Three separate demodulators with independent phase control**
- **Low output offset voltage** ..... **0.4 V**

CA-CA3125E is a monolithic silicon integrated-circuit roma demodulator having three separate demodulators ith independent phase control. It is designed to function mpatibly with the CA1398E IC Chroma Processor as well other commercially available Chroma Processors in R-G-B stems of color-TV receivers. Fig. 2 shows a functional ock diagram of a 2-package TV Chroma System incorporating e CA3125E and CA1398E. The CA3125E is supplied in a l-lead dual-in-line plastic package.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

SUPPLY VOLTAGE	25 V
SUPPLY CURRENT	20 mA
AMBIENT-TEMPERATURE RANGE:	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 s max.	265°C

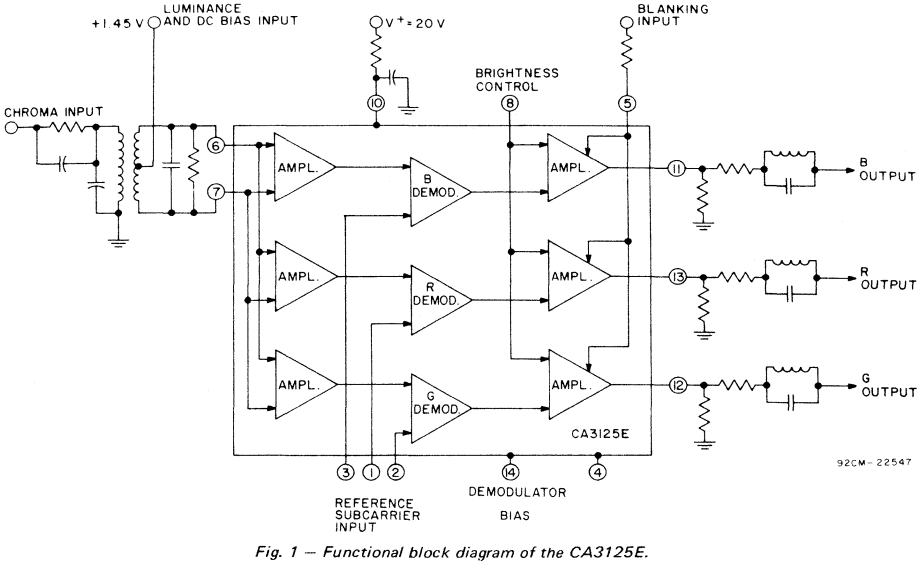


Fig. 1 — Functional block diagram of the CA3125E.

File Number **685**

CA3125

TYPICAL STATIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ VOLTS

SUPPLY CURRENT ..... 9.6 mA

BRIGHTNESS CONTROL VOLTAGE:
Measured with 8 volts at Terminals 11, 12, and 13 ..... 1.4 V

MAX. OUTPUT DIFFERENCE VOLTAGE:
Measured between any two of Terminals 11, 12, and 13 ..... ±0.4 V

MAXIMUM DC DETECTOR UNBALANCE VOLTAGE:
DC voltage shift on Terminals 11, 12, and 13 when Terminals 1, 2, and 3 are alternately biased 0.5 volt positive, then negative with reference to Terminal 14 ..... +150 mV

TYPICAL DYNAMIC CHARACTERISTICS AT $T_A = 25°C$, $V^+ = +20$ volts

BLUE CHROMA GAIN:
Peak-to-peak voltage at Terminal 11 with 1.0 volt peak-to-peak applied differentially between Terminals 6 and 7, and with a subcarrier injection voltage of 1 volt peak-to-peak 7.36 V

RED GAIN RATIO:
$\frac{\text{Peak-to-peak voltage at Terminal 13}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$ 1

GREEN GAIN RATIO:
$\frac{\text{Peak-to-peak voltage at Terminal 12}}{\text{Peak-to-peak voltage at Terminal 11}} \times 100$ .....

LUMINANCE GAIN:
Peak-to-peak voltage measured at Terminals 11, 12, and 13, with a peak-to-peak voltage of 0.1 volt applied to Terminals 6 and 7 (common mode), and with no subcarrier injection ..... 0.7 V

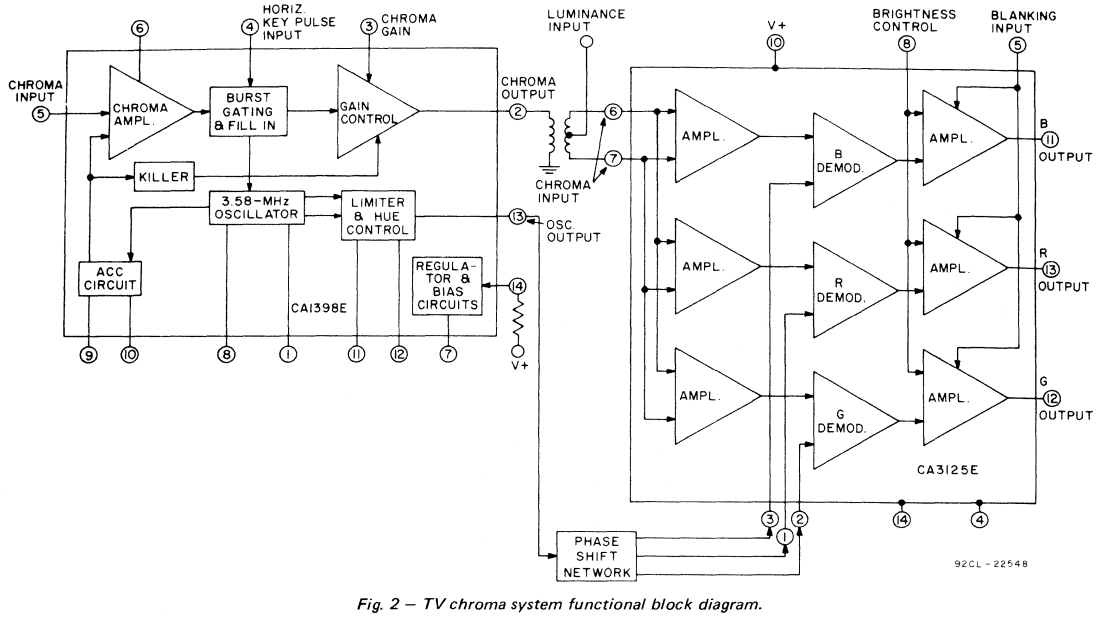


Fig. 2 – TV chroma system functional block diagram.

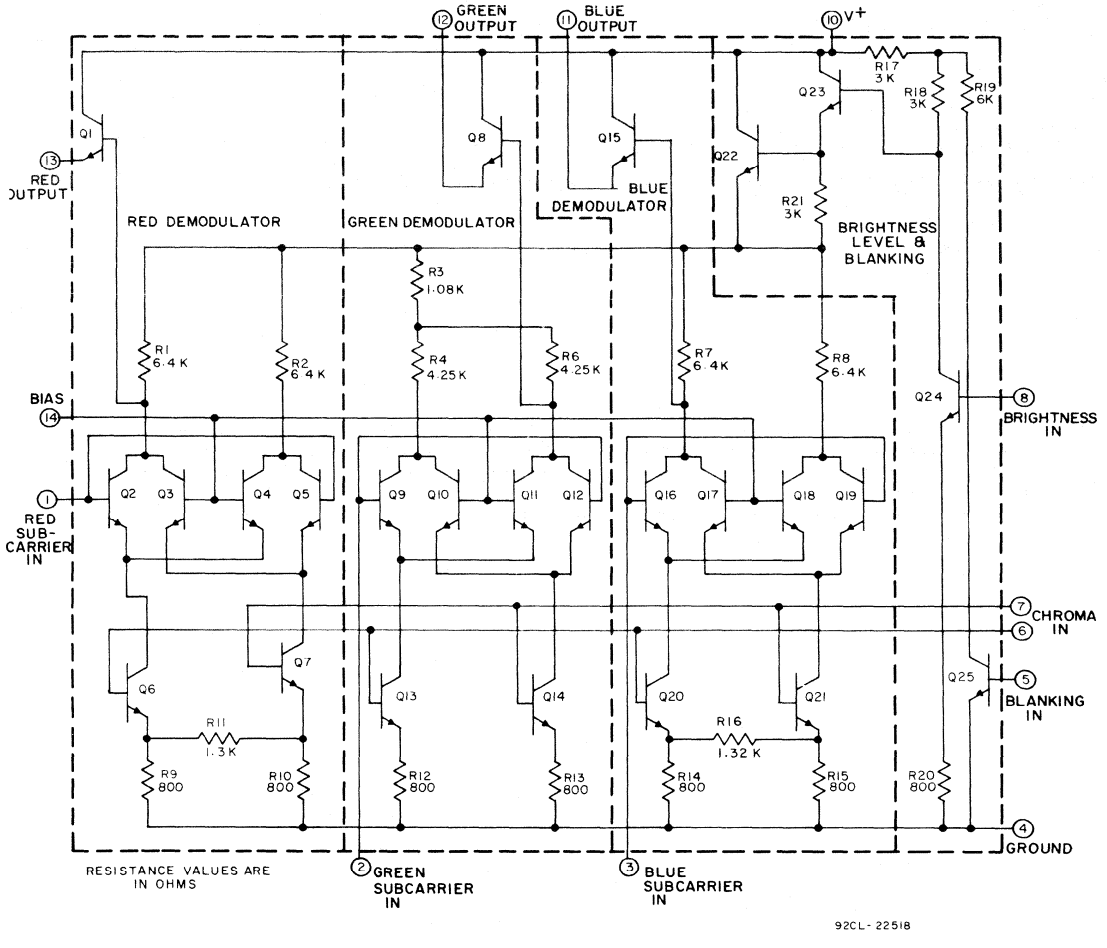


Fig. 3 – Schematic diagram of the CA3125E.

CA3134

TV Sound IF and Audio Output Subsystems

Features:

- *Output power 3 W (typ.) at $V^+ = 24$ V, $R_L = 16\ \Omega$*
- *Power amplifier with current limiting and thermal shutdown*
- *Wide power-supply range: 12 V to 33 V*
- *Low quiescent current: 30 mA typ.*
- *5-kHz deviation sensitivity: 1 W output typ.*
- *3-dB limiting sensitivity: 200 μV typ.*
- *Excellent AM rejection: 50 dB typ.*

The RCA-CA3134 combines the sound IF and audio output subsystems on a single monolithic integrated circuit to provide a television sound system for color or black-and-white applications. Each device includes a multistage IF amplifier-limiter, an FM detector, and an audio power amplifier that is designed to drive an 8-, 16-, or 32-ohm speaker.

The CA3134EM and CA3134QM are supplied in the 16-lead plastic "power slab" package with a tin-plated copper strap heat sink attached. The CA3134EM is supplied with dual-in-line leads and the CA3134QM is supplied with dual-quad-formed leads.

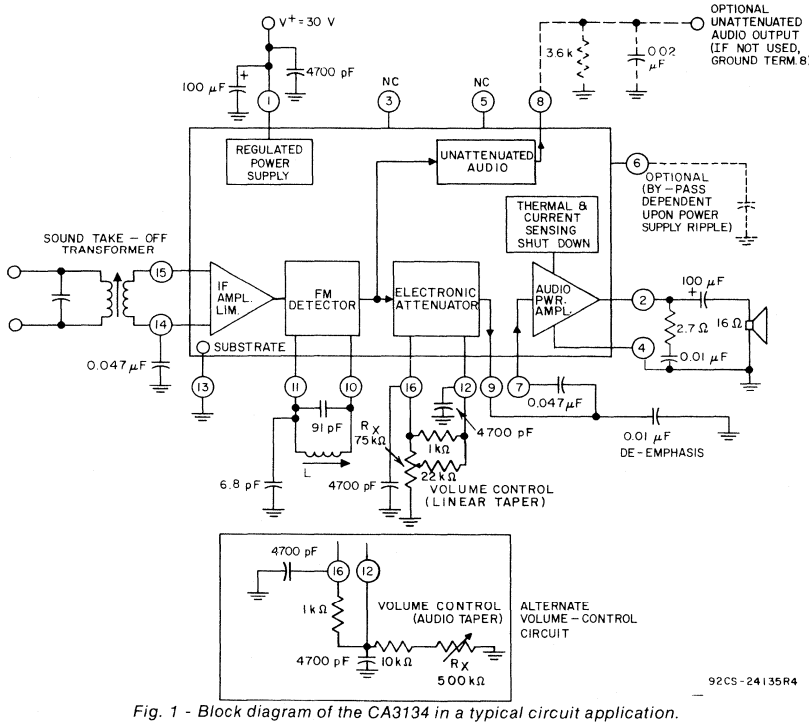


Fig. 1 - Block diagram of the CA3134 in a typical circuit application.

File Number **1097**

CA3134

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between Term. 1, V+ and Terms. 4, audio-output ground and 13, substrate ..... 33 V
INPUT SIGNAL VOLTAGE (Between Terms. 14 and 15) ..... ±3 V
DEVICE DISSIPATION:
With Copper-Strap Heat Sink -
Soldered to PC Board
Up to T_A = 25°C ..... 5 W
Above T_A = 25°C ..... derate linearly 40 mW/°C
Unsoldered
Up to T_A = 25°C ..... 2.9 W
Above T_A = 25°C ..... derate linearly 24 mW/°C
THERMAL RESISTANCE
Junction to Slab ..... 5°C/W
AMBIENT TEMPERATURE RANGE:
Operating ..... -40 to +85°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (During Soldering):
At a distance 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

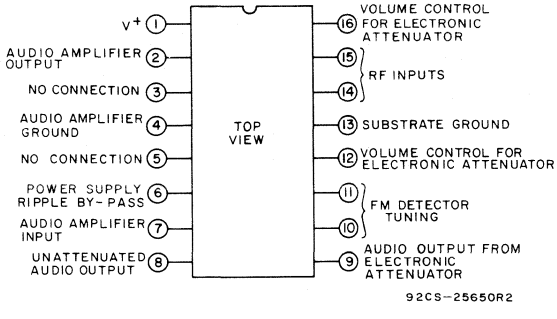


Fig. 2 - Terminal diagram of the CA3134EM and CA3134QM.

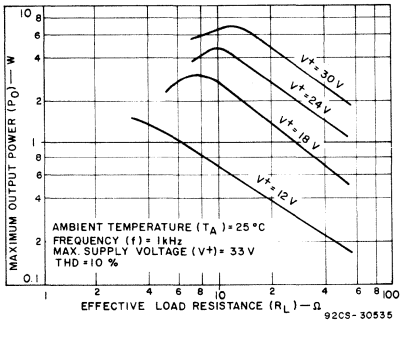


Fig. 3 - Maximum outpower as a function of effective load resistance.

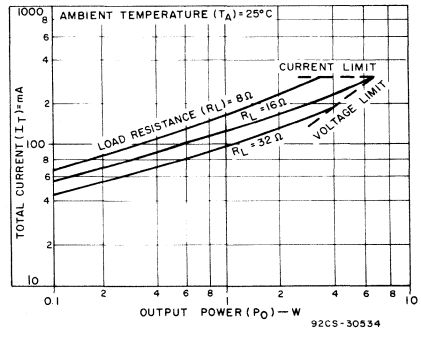


Fig. 4 - Total supply current as a function of output power.

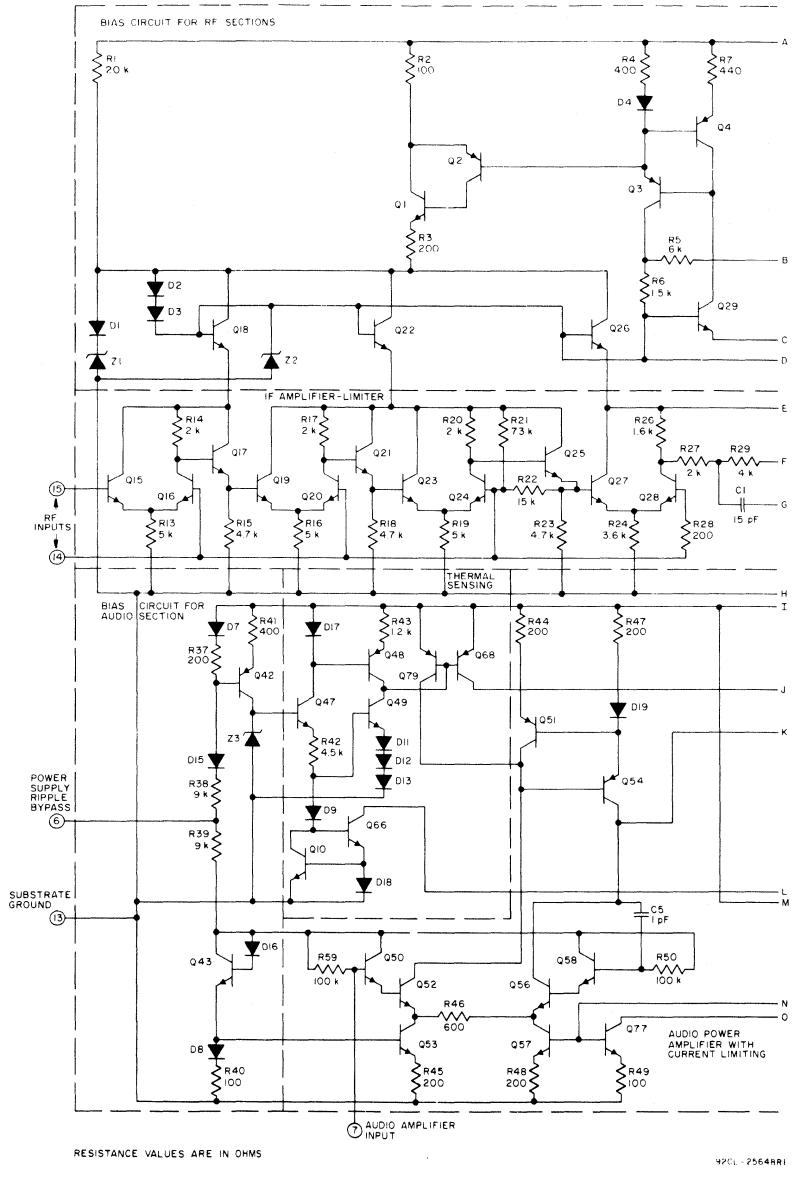


Fig. 5 - Schematic diagram of the CA3134 (cont'd on next page).

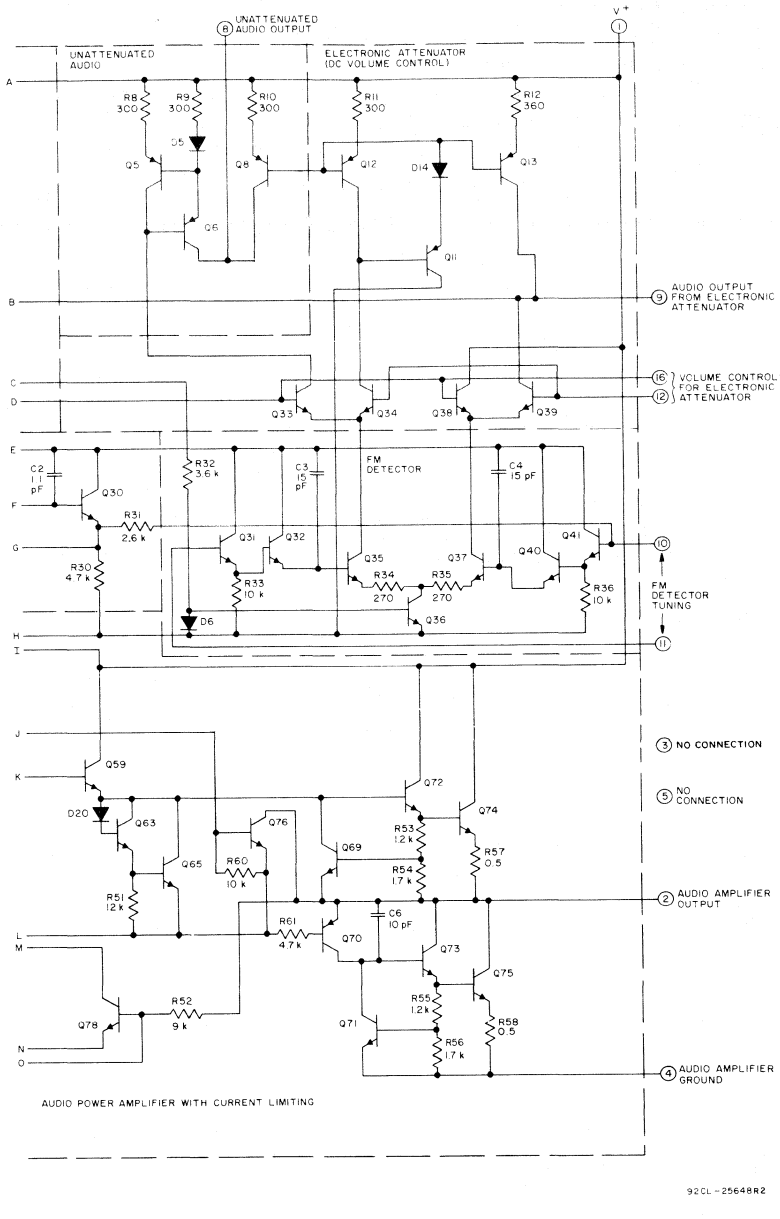


Fig. 5 - Schematic diagram of the CA3134 (cont'd from previous page).

CA3134

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A=25° C, V^+=+30 V (applied to Term. 1), DC Volume Control, R_X=75 KΩ, R_L=16 Ω, unless otherwise indicated. Refer to Fig. 1.

CHARACTERISTIC	SPECIAL TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
Current into Term. 1, I_1	P_O = 0	15	30	45	mA
Dynamic Characteristics					
IF AMPLIFIER: Input Limiting Voltage, V_{15} (lim) (at -3 dB point)	f_o = 45 MHz, f_m = 400 Hz, Δf = ±25 kHz	—	200	400	μV
AM Rejection, AMR	f_o = 4.5 MHz, f_m = 400 Hz, Modulation Index = 0.3, V_{15} = 20 mV	40	50	—	dB
Input Resistance, R_I	V_{15} = 35 mV	—	25	—	KΩ
Input Capacitance, C_I	V_{15} = 35 mV	—	3	—	pF
DETECTOR: Recovered af Voltage (Term. 9), V_o(af)	f_o = 4.5 MHz, f_m = 400 Hz,	—	700	—	mV
Total Harmonic Distortion, (THD)	Δf = ±25 kHz, V_{15} = 100 mV	—	0.8	3	%
Output Resistance, R_o	At Term. 9	—	7.5	—	KΩ
ATTENUATOR: Maximum Attenuation	R_x = 0	—	10	15	mV
UNATTENUATED AUDIO: Recovered af Voltage (Term 8), V_o(af)	f_o = 4.5 MHz, f_m = 400 Hz,	—	600	—	mV
Total Harmonic Distortion (THD)	Δf = ±25 kHz, V_{15} = 100 mV	—	0.8	—	%
AUDIO POWER AMPLIFIER: Voltage Gain, A(af)	f = 1 kHz	—	35	—	dB
System Total Harmonic Distortion THD (System)	P_o = 1W (I_T = 140 mA typ.)	—	1.5	—	%
	P_o = 2W (I_T = 180 mA typ.)	—	1.6	3	%
Power Output, P_o	THD (System) = 10% (I_T = 210 mA typ.)	—	5	—	W
Input Resistance, R_I(af)	f = 1 kHz	—	100	—	KΩ

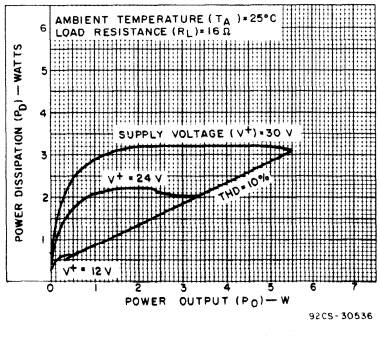


Fig. 6 - Power dissipation as a function of output power.

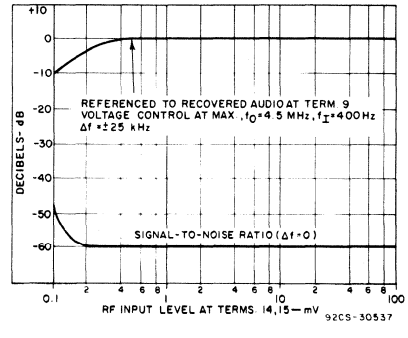


Fig. 7 - Recovered audio, and signal-to-noise ratio as a function of rf input level.

CA3142

TV Sync Processor

For Color and Monochrome Receivers

Features:

- *Internal impulse noise processing*
- *Sync separator - low impedance, dual polarity*
- *Strobed AGC system*
- *IF AGC output*
- *Delayed outputs for forward or reverse AGC tuners*
- *Automatic noise threshold and AGC detector level control*
- *High-impedance video input*
- *Low-impedance video output*
- *Choice of external time constants for sync separator*
- *Negative power supply not required*
- *RF AGC delay externally controlled*

The RCA-CA3142 is a monolithic silicon integrated circuit TV signal processor for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit design of the CA3142 features impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques.

The CA3142 is supplied in a 16-lead dual-in-line plastic package (E suffix).

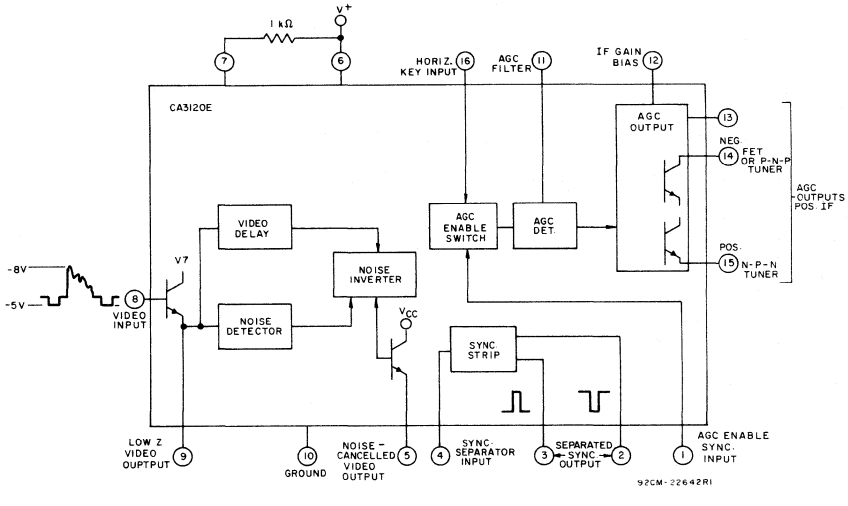


Fig. 1 - Simplified block diagram of the CA3142.

File Number **907**

CA3142

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 6, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	CA3142 LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	3.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	100	μA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	μA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	36	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	μA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	μA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	μA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA

CA3142

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A=25°C*

DC SUPPLY VOLTAGE ..... 30 V

DEVICE DISSIPATION:

Up to T_A = 55°C ..... 750 mW

Above T_A = 55°C ..... Derate linearly at 7.9 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... -40 to +85°C

Storage ..... -65 to +150°C

LEAD TEMPERATURE (During Soldering):

At a distance not less than 1/32 in. (0.79 mm) from case for 10 s max. ..... +265°C

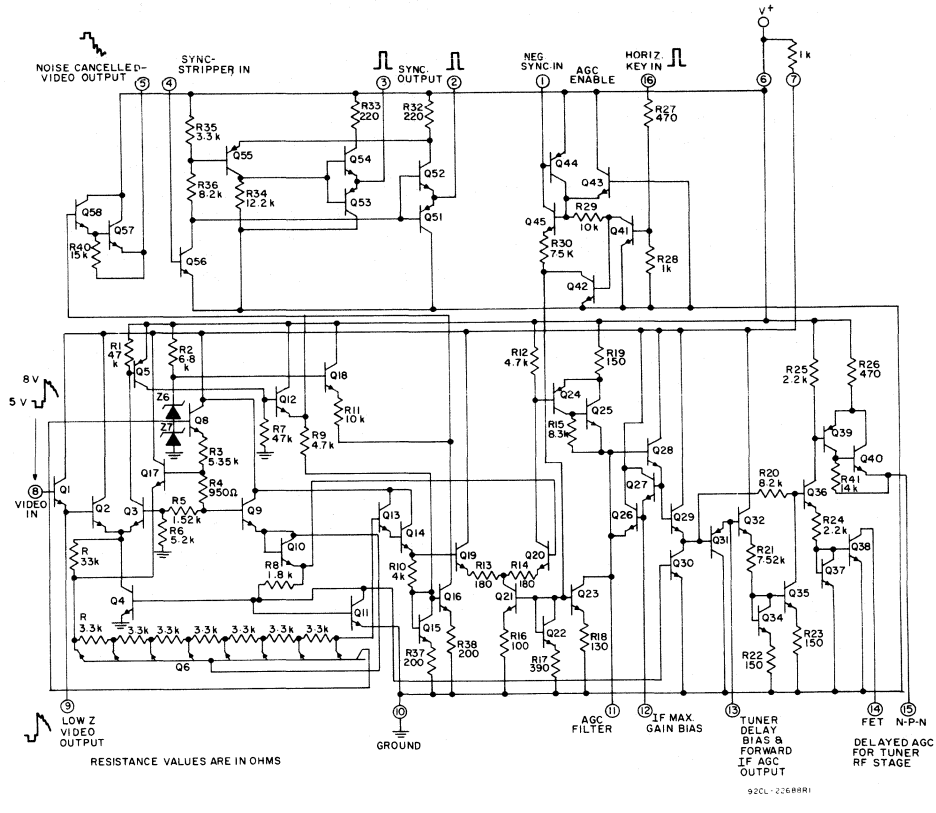


Fig. 2 - Schematic diagram of the CA3142.

CA3142

Circuit Description*

An AGC sample-and hold system generates control voltages proportional to the video level. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. The control voltages (AGC outputs) are supplied to the tuner's RF stage and the IF amplifier to maintain the video level at a constant value.

The composite positive and negative output sync signals are developed across a low impedance source (totem-pole circuit) at an amplitude of approximately 20 volts peak-to-peak.

Video Chain and Impulse Noise Inverter — The input video signal applied at Terminal 8 is white "positive" with a required amplitude in the range of 2 to 4 volts. The DC level of the sync peaks, AGC threshold voltage (V_{TH}) is approximately 5 volts. The level is maintained at 5 volts by the AGC loop in the circuit, comprised of the CA3142 and the TV receiver RF and IF amplifiers. A low source impedance video signal is available from the emitter of Q1 (Terminal 9 in Fig. 2). The external resistor (R_{X1} in Fig. 9) reduces the dissipation of Q1. The emitter-follower output of Q1 is directly coupled to a differential comparator stage (Q2, Q3). Unless a negative-going pulse is present, Q2 functions as an emitter follower and also cuts off transistors Q3, Q5, and Q12.

The output of Q2 is applied through a signal delay network, consisting of transistor Q60 and associated resistors, to the Darlington followers (Q13 and Q14). The delayed video signal at Q14 is fed via its emitter to an AGC comparator Q19 and to the junction of a noise-cancelling amplifier stage (Q16). The noise-cancelled video signal is inverted and amplified by Q16 and then connected to a Darlington emitter-follower output stage (Q57, Q58).

If impulse noise is present on the video signal, Q3 conducts and turns on transistors Q5 and Q12. Q5 inverts and "stretches" the noise pulse width. The output of Q5 is applied to an emitter follower stage (Q12). The signal from Q12, in turn, is applied to the summing junction to the noise-cancelling amplifier Q16. The noise pulse, which has now been amplified, inverted and stretched, is added to the delayed video signal from the emitter of Q14.

Because the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been widened ("stretched") approximately 500 nanoseconds, the output of the combined signal no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise.

The noise-cancelled video signal, amplified and buffered, is available at Terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the noise-cancelled output signal is approximately twice the amplitude of the input video signal at Terminal 8.

Sync Separator (See Fig. 3) — The sync separator stage (Q56) clamps the detected sync tips to a fixed reference voltage (≅0.7 V) across its base-emitter junction, and amplifies a portion of the sync signal to provide dual polarity sync-signal outputs at Terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance complementary emitter-follower stages; a base current of 100 microamperes into Terminal 4 is sufficient to generate full-amplitude sync signals.

The choice of coupling the noise-cancelled video-signal from the emitter-follower (Terminal 5) to the sync separator (Terminal 4) is a user option. Fig. 4 shows three typical coupling networks.

Fig. 5 illustrates the operation of the AGC circuits. An input ramp signal, simulating the potential to which the AGC filter capacitor may be charged, is applied to Terminal 11. The forward IF AGC output voltage appears at Terminal 13. Under low-signal level conditions (represented by A to B in Fig. 5) the output level is approximately 1.4 volts less than the voltage applied to Terminal 12.

The circuit designer should select the voltage at Terminal 12 to provide the maximum IF gain required for the system. At intermediate signal level conditions (represented by B to C in Fig. 5), the IF AGC signal follows the AGC filter potential. The tuner(s) will operate at maximum gain for good signal-to-noise ratios at these equivalent input signal levels. Point C is a turnover point determined by the open-circuit potential of the tuner-delay bias potentiometer. At this potential, further change in the IF AGC output is inhibited (for good dynamic range) and the tuner AGC potentials are activated (represented by C to D).

The output at Terminal 14 with suitable level shifting is used for tuners requiring reverse AGC, such as MOSFET or electron-tube types. The output at Terminal 15 is used for tuners requiring forward AGC, such as tuners utilizing n-p-n bipolar transistors.

*For additional information refer to the IEEE "Transactions on Broadcast and TV Receivers," August 1970, pp 185-195, Vol. BTR No. 3. Also refer to ICAN-6302.

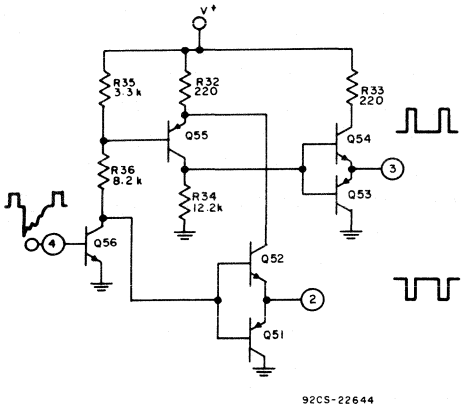


Fig. 3 - Sync separator stage.

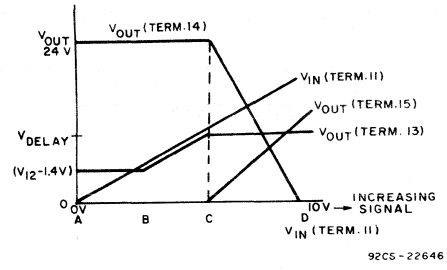


Fig. 5 - Typical operation of the AGC circuits using the CA3142.

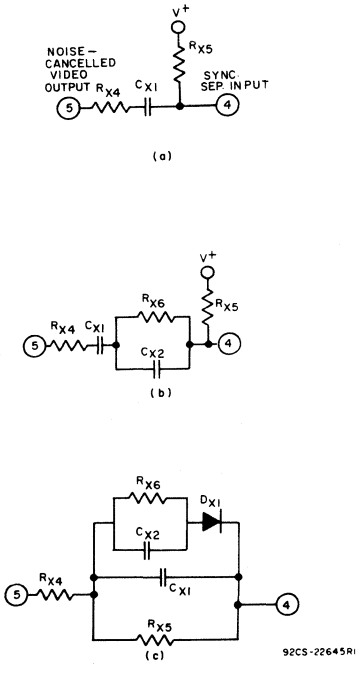


Fig. 4 - Typical coupling networks (Term. 5 to Term. 4).

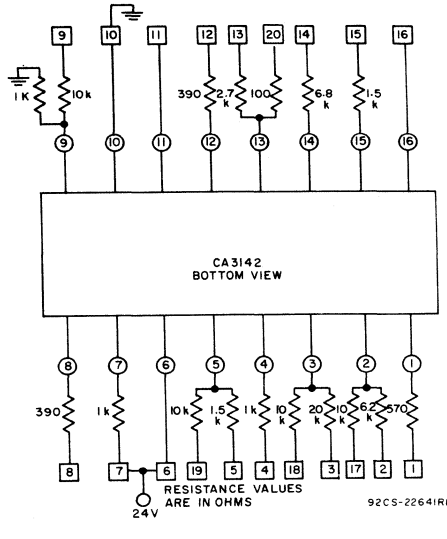
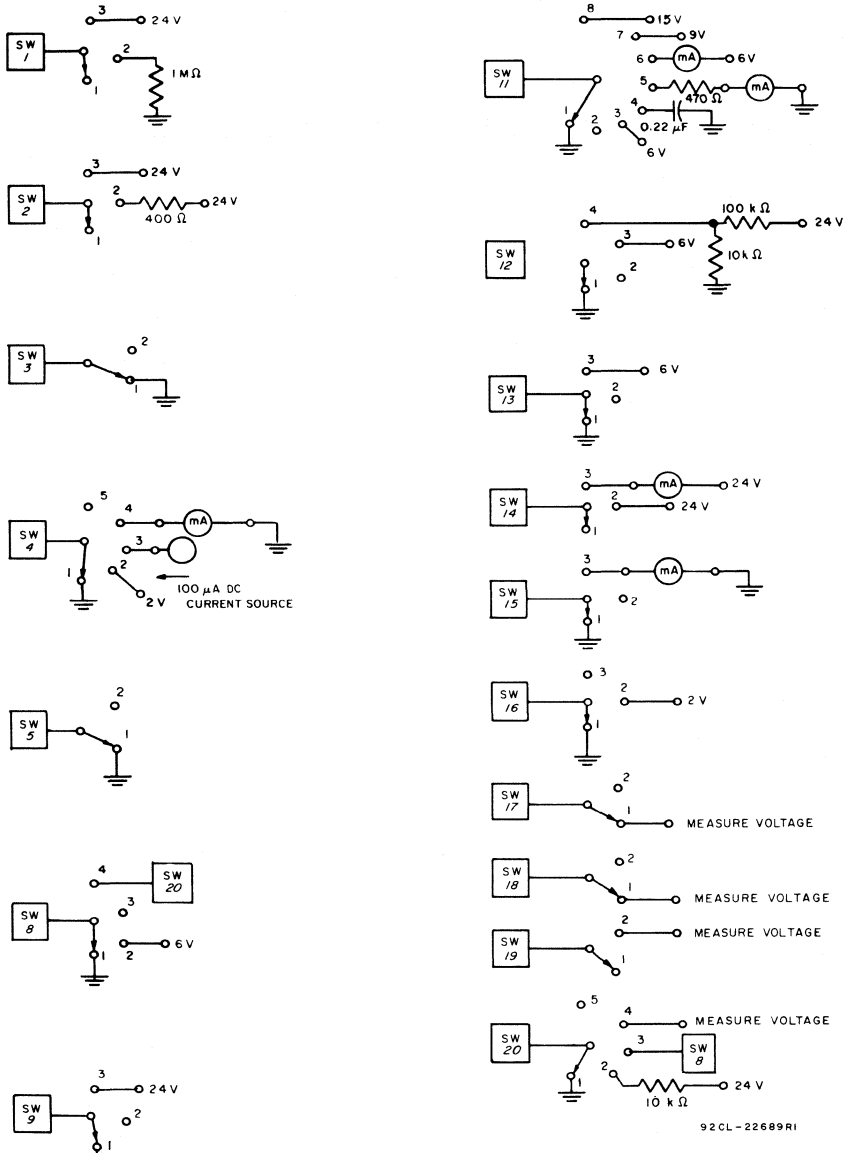


Fig. 6 - Test circuit for measuring electrical characteristics of the CA3142. Refer to Figs. 7 and 8 for switch selector positions.

CA3142



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 6 and 8.

CAUTION: Remove power before selecting or adjusting switches

Fig. 7 - Test condition selector switch arrangement for measuring the electrical characteristics of the CA3142.

CHARACTERISTIC	TEST CONDITIONS — SWITCH NUMBERS / SWITCH POSITION																	TERMINAL MEASURED
	1	*2*	*3*	*4*	*5*	*8*	*9*	*11*	*12*	*13*	*14*	*15*	*16*	*17*	*18*	*19*	*20*	
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	*2 6 7 9 14*
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	*8*
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	*19*
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

NOTE: Switch numbers in italics correspond to numbers in square boxes in Figs. 6 and 7.

Fig. 8 – Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs. 6 and 7 for test circuit and test-condition selector-switch arrangements.

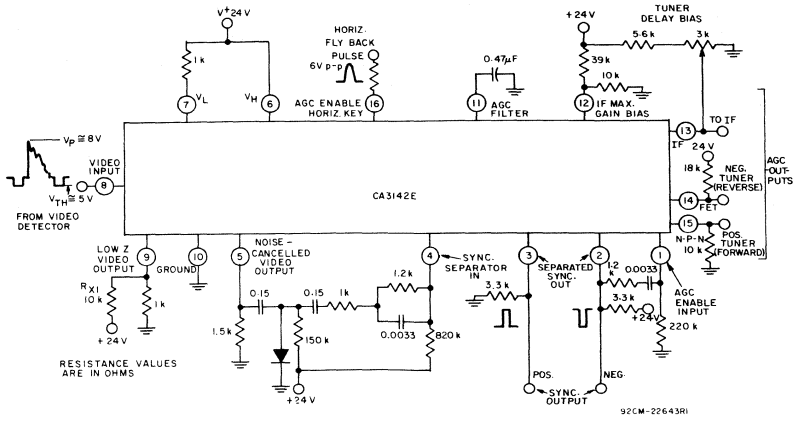


Fig. 9 - Typical application using the CA3142.

CA3151

Single Chip TV Chroma Processor/Demodulator

FEATURES:

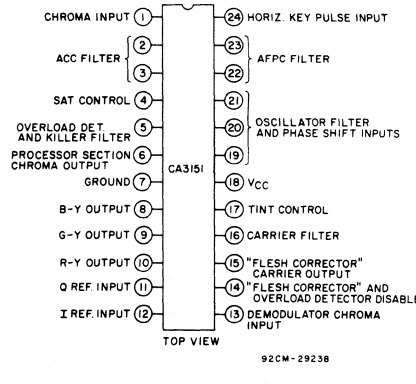
- *All chroma processing and demodulating circuitry on a single chip in a 24-lead plastic package*
- *Phase-locked subcarrier regeneration utilizing sample-and-hold techniques*
- *Supplementary ACC with overload detector to prevent over saturation of the picture tube*
- *Linear dc controls for chroma gain and tint*
- *Dynamic "flesh correction"—corrects purple and green flesh colors without affecting primary colors*
- *Balanced chroma demodulators with low output impedance for direct coupling*
- *Internal rf filtering*
- *Requires few external components*
- *Low system dissipation—nominal 0.5 W*

The RCA-CA3151E is a monolithic silicon integrated circuit that performs the complete chroma processor and demodulating functions for color TV. This simple chip contains all the features of the CA3126 chroma processor and the CA3137 chroma demodulator.

The CA3151E is supplied in the 24-lead dual-in-line plas package.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
Between Terminals 18 and 7 ..... 13.2 V
DEVICE DISSIPATION:
Up to T_A = 55°C ..... 825 mW
Above T_A = 55°C ..... Derate linearly at 8.7 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... -40 to +85°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C



TERMINAL DIAGRAM

File Number **1160**

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 11.6$ V

CHARACTERISTIC	TEST CONDITIONS							TYPICAL VALUE	UNITS
	S_1	S_2	S_3	Chroma In	Burst In	V_4	V_{17}		
STATIC (See Fig. 1)									
Supply Current, I_T								42	mA
R-Y, G-Y, B-Y, Outputs, V_8, V_9, V_{10}								5.3	Vdc
Oscillator Reference Inputs, V_{11}, V_{12}								3.7	Vdc
Chroma Demodulator Input, V_{13}								2.9	Vdc
Chroma Processor Input, V_1								2.2	Vdc
DYNAMIC (See Fig. 2)									
Minimum Oscillator Pull-In Range*, V_{12}	2	1	1	273 mV_{p-p}		1.5 V	7 V	±300	Hz
Oscillator Level, V_{12}	2	1	1					0.6	V_{p-p}
100 Percent ACC, V_{13}	1	1	1					1	V_{p-p}
Minimum Gain Control, V_{13}	1	1	1			11.6 V		20	mV_{p-p}
50 Percent Gain Control, V_{13}	1	1	1			6 V		50	% of 100% ACC Value
200 Percent ACC, V_{13}	1	1	1	546 mV_{p-p}		1.5 V		100	% of 100% ACC Value
20 Percent ACC, V_{13}	1	1	1	54.6 V_{p-p}				100	% of 100% ACC Value
Maximum Kill Output, V_{13}	1	1	1	54.6 mV_{p-p}	4 mV_{p-p}			20	mV_{p-p}
Minimum Unkill Output, V_{13}	1	1	1		30 mV_{p-p}			400	mV_{p-p}
Overload Detector (OLD), V_{13}	1	1	2	546 mV_{p-p}	273 mV_{p-p}			1	V_{p-p}
R-Y Sensitivity, V_{10} E_g = 282 mV_{p-p}, 3.53 MHz	1	2	1	0				0.8	V_{p-p}
R-Y Ratio B-Y/R-Y, V_8**	1	2	1					120	%
G-Y Ratio G-Y/R-Y, V_9**	1	2	1					33	%
Max. R-Y Output, V_{10} E_g = 2 V_{p-p}, 3.53 MHz	1	2	1					3	V_{p-p}
Minimum Tint Control Range, ϕ13	1	1	1	273 mV_{p-p}		1.5 V	0 V to 11.6 V	80	Degrees

* Tune C_2 to 3,579,845 Hz with S_1 in position 2. Put S_1 in position 1, and check for pull in. Repeat for frequency tuned to 3,579,245 Hz. For other tests, frequency tuned to 3,579,545 ± 10 Hz. ** All input levels up to 2 V_{p-p}.

CA3151

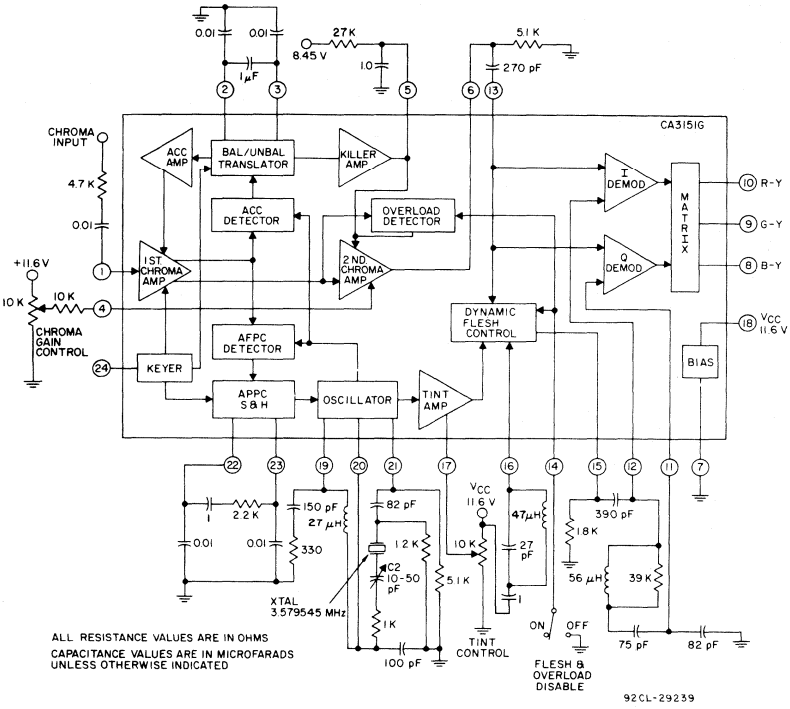


Fig. 1 — Functional diagram, static test circuit, and typical application circuit.

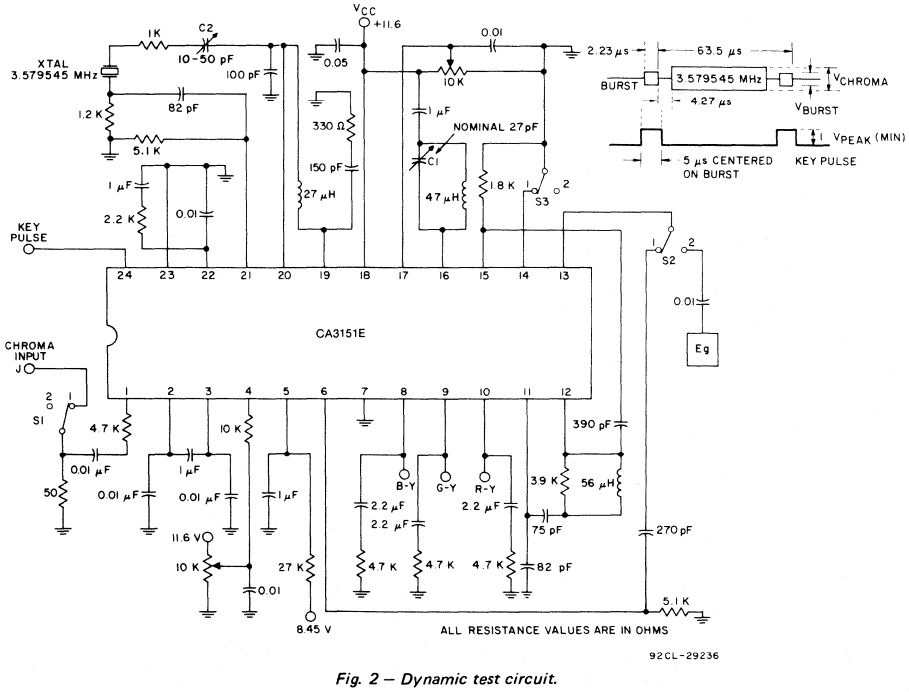


Fig. 2 — Dynamic test circuit.

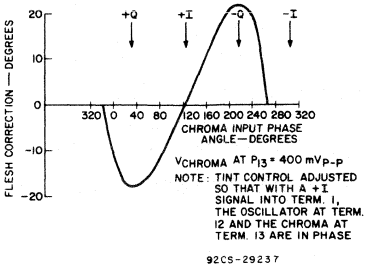


Fig. 3 — "Flesh" correction of oscillator phase angle as a function of chroma input phase angle.

CA3156

Video/Chroma Processor

Features:

- *Automatic black-level control*
- *Automatic controls for contrast and peaking*
- *Automatic color-level control*
- *Horizontal and vertical blanking*
- *Automatic beam-current limiting*
- *Positive or negative vertical blanking pulses*
- *Internal noise protection for automatic functions*

The RCA-CA3156E is a monolithic silicon integrated circuit that performs the luminance processing functions in color TV receivers. This circuit amplifies chroma signals, provides horizontal and vertical blanking, and automatically controls contrast, brightness, peaking, and black and chroma levels.

The CA3156E is well-suited for color TV receiver applic tions which use the CA3159E horizontal processor, t CA3216Q chroma processor, and the CA3172E col demodulator.

The CA3156E is supplied in a 16-lead dual-in-line plast package.

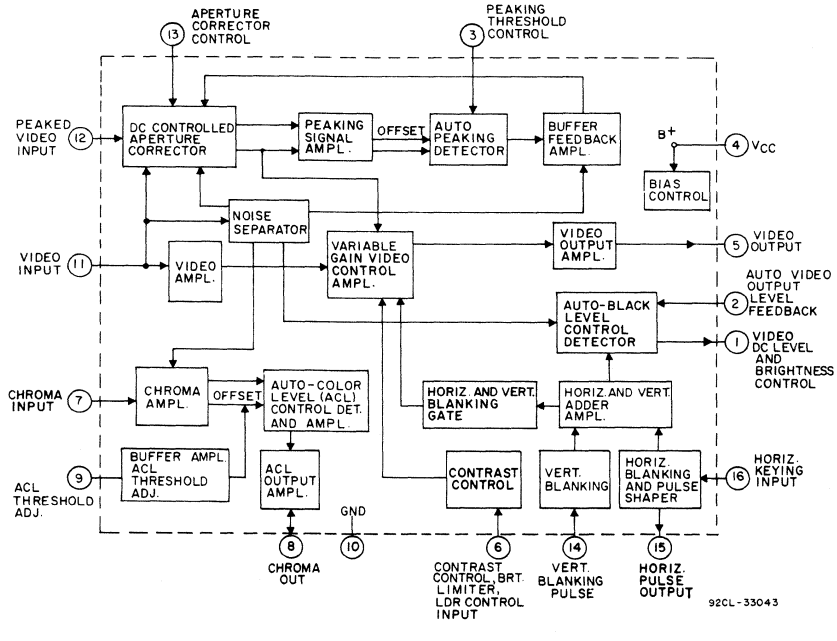


Fig. 1 - Block diagram of CA3156E.

File Number **1265**

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $V^+ = 24$ V and Referenced to Test Circuit (See Fig. 3)

CHARACTERISTIC	TEST CONDITION	LIMITS			UNITS
		Min.	Typ.	Max.	
Static Characteristics					
Total Supply Current		13	16.0	19	mA
Reference Bias Level Pin 7			5.25		V
Reference Level Pin 2 $S_2 = 2$ (with 1 mA into Pin 1) $S_3 = 2$			12.2		V
Dynamic Characteristics					
Max. Video Gain—Read e_o	$e_{in} = 1$ V_{p-p} f = 100 kHz S5 to Pos. 1		13.5		dB
Min. Video Gain—Read e_o	$e_{in} = 1$ V_{p-p} f = 100 kHz S5 to Pos. 2		−4.4		dB
Relative Freq. Response—Read e_o	$e_{in} = 1$ V_{p-p} f = 3.58 MHz S5 to Pos. 1		−0.2		dB
Contrast Gain Reduction—Read e_o	$e_{in} = 1$ V_{p-p} f = 100 kHz S5 Pos. 1 to Pos. 2		−17.9		dB
Auto-Peaking Level–Read P_3 to P_{13}	$e_{in} = 1$ V_{p-p} S5 to Pos. 1		165		mV
Auto-Peaking Level–Read P_3 to P_{13}	$e_{in} = 0.5$ V_{p-p} S5 to Pos. 1		115		mV
Auto-Peaking Level–Read P_3 to P_{13}	$e_{in} = 0$ V_{p-p} S5 to Pos. 1		0		mV
Max. Chroma Out Level—Read P_8 $E_5 = 5$ V dc	$e_c = 1$ V_{p-p} f = 3.58 MHz S4 off		5		V
Min. Chroma Out Level—Read P_8 $E_5 = 5$ V dc	$e_c = 1$ V_{p-p} f = 3.58 MHz S4 on		10		V

CA3156

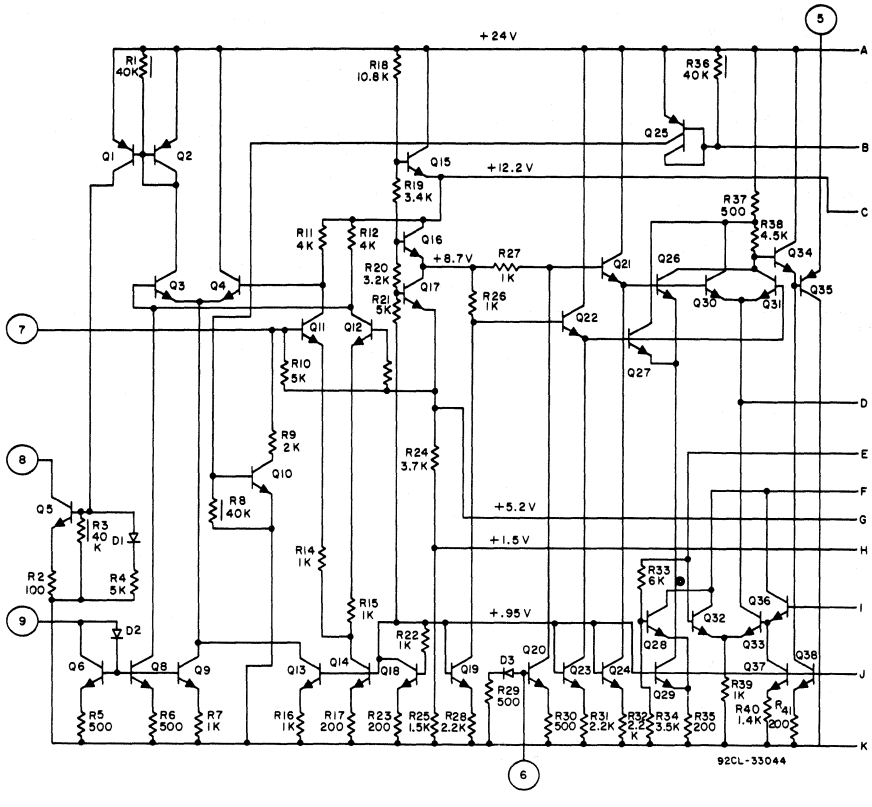


Fig. 2 - Schematic diagram of CA3156E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE . . . . . 30 V
DC SUPPLY CURRENT . . . . . 21 mA
DEVICE DISSIPATION:
  Up to $T_A = 25\,°C$ . . . . . 750 mW
  Above $T_A = 25\,°C$ . . . . . Derate linearly at 11.1 mW/ °C
AMBIENT TEMPERATURE RANGE:
  Operating . . . . . 0 to 60 °C
  Storage . . . . . −55 to 150 °C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
    from case for 10 seconds max. . . . . + 265 °C

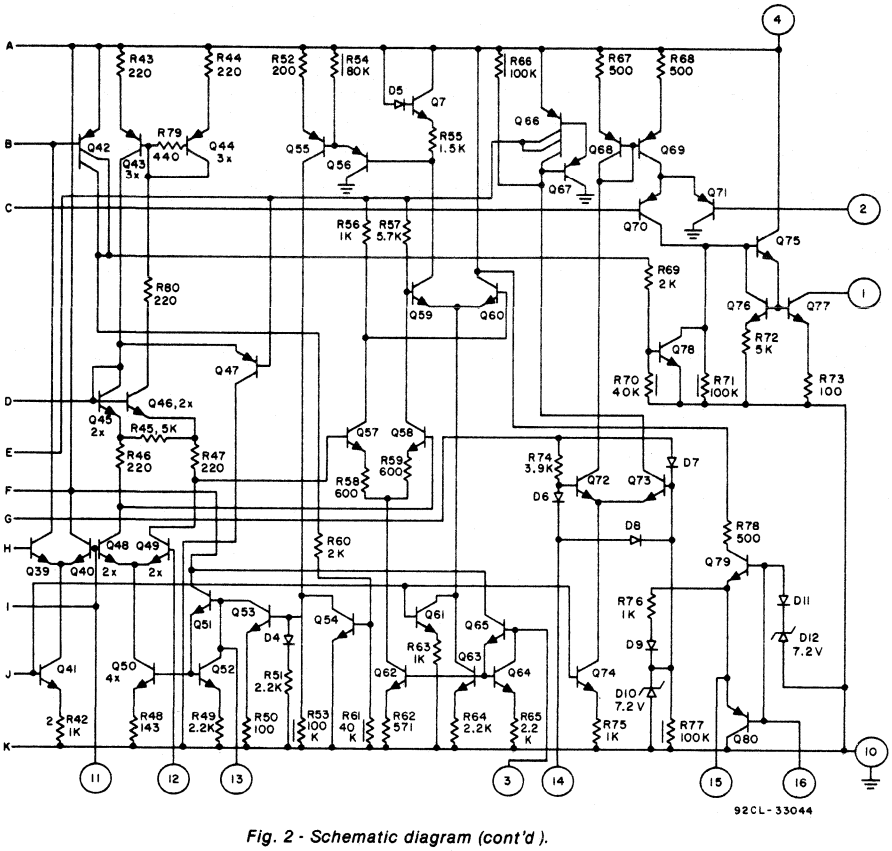
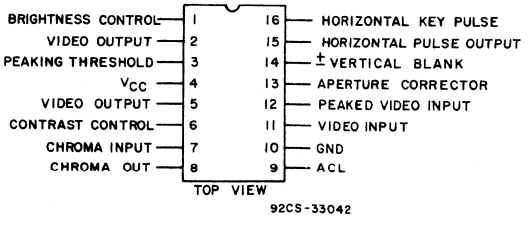


Fig. 2 - Schematic diagram (cont'd).



Terminal Assignment

CA3156

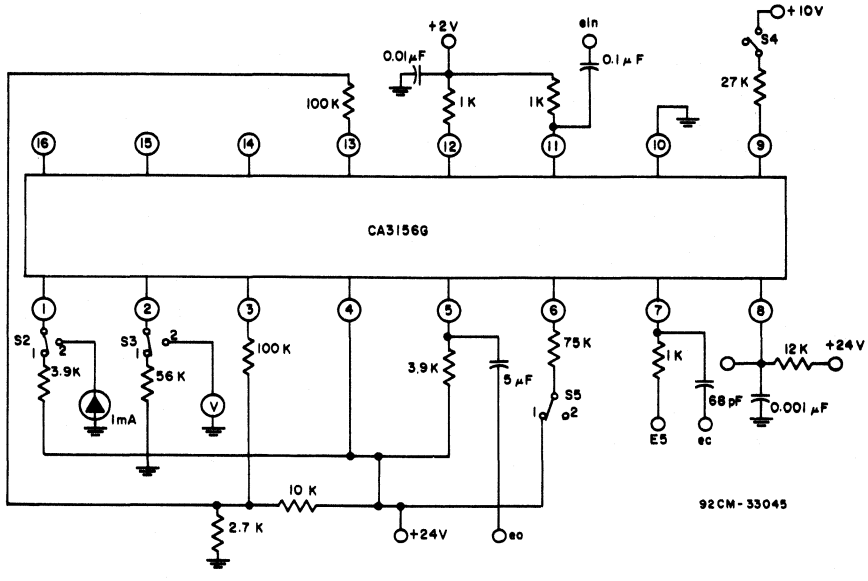


Fig. 3 - CA3156E test circuit.

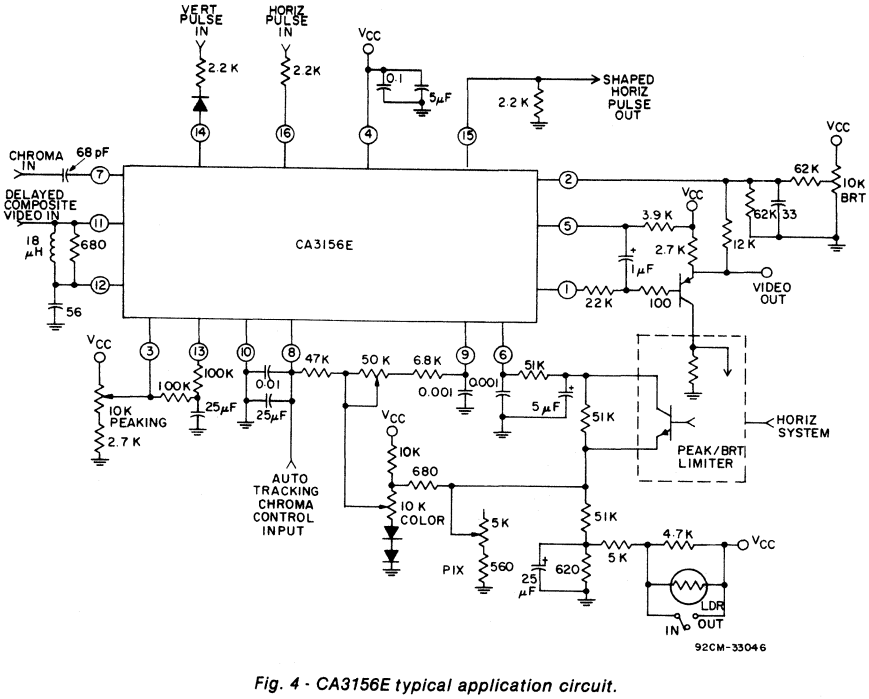


Fig. 4 - CA3156E typical application circuit.

CA3170

TV Chroma System

FEATURES:

- *Voltage-controlled oscillator*
- *Keyed APC and ACC detectors*
- *DC hue control*
- *Shunt regulator*

The RCA-CA3170E is a monolithic silicon integrated circuit that performs the functions of subcarrier regeneration, ACC and APC detection, and tint control in color television receivers. It is designed to function compatibly with the CA3121E TV Chroma Amplifier/Demodulator in a 2-package chroma system.

The CA3170E is a TV Chroma System of advanced design that incorporates all the features of the CA3070E but with the added advantage of the modified Hue Control Characteristic. With the CA3170E, the designer can provide a front panel hue control that functions linearly over its entire range, a particularly desirable consumer feature.

The CA3170E is supplied in the 16-lead dual-in-line plastic package.

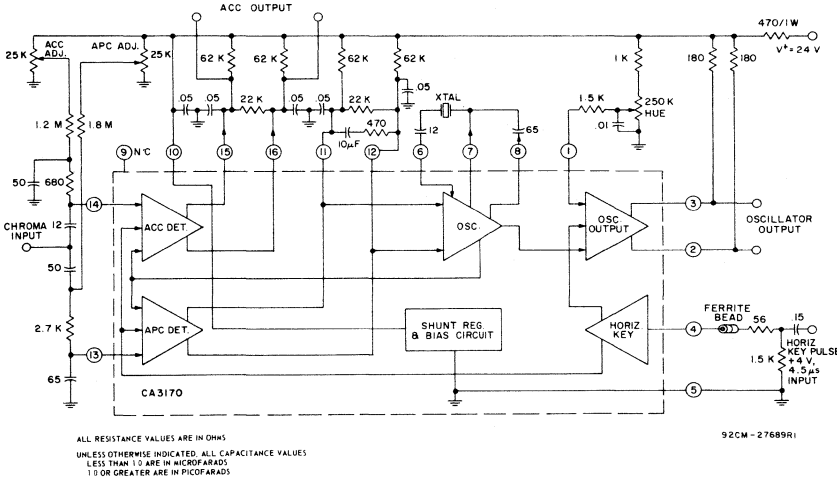


Fig. 1 — Functional block diagram of CA3170E.

File Number **1129**

CA3170

ELECTRICAL CHARACTERISTCS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SPECIAL TEST CONDITIONS	LIMITS CA3170 MIN.	LIMITS CA3170 TYP.	LIMITS CA3170 MAX.	UNITS
Static Characteristics					
Voltage: Hue Control, V_1	See Fig.7				V
Oscillator Input, V_6	S_1 CLOSED, S_3 OFF; S_2, S_4, S_5 OPEN, See Fig. 8	–	2.6	–	V
APC Input, V_{13}	S_1 CLOSED, S_3 OFF; S_2, S_4, S_5 OPEN, See Fig. 8	–	5.4	–	V
Regulator, V_{10}	V^+ = 21 V; S_1 CLOSED, S_3 OFF; S_2, S_4, S_5 OPEN, See Fig. 8	11	12.3	13.5	V
Regulator Change, V_{10}	V^+ = 27 V; S_1 CLOSED, S_3 OFF; S_2, S_4, S_5 OPEN, See Fig. 8	-0.2	–	+0.2	V
Horizontal Key Input, V_4	I_4 = -10 μA; S_1 CLOSED, S_3 OFF; S_2, S_4, S_5 OPEN, See Fig. 8	5	–	–	V
Currents: Oscillator Output, I_2	S_1, S_2, S_4, S_5 CLOSED, S_3 in position 2, See Fig. 8	–	5.8	–	mA
APC Output, I_{11}, I_{12}	S_1, S_5 OPEN, S_2, S_4 CLOSED, S_3 in position 1, See Fig. 8	–	1.45	–	mA
ACC Output, I_{15}, I_{16}	S_1, S_5 OPEN, S_2, S_4 CLOSED, S_3 in position 1, See Fig. 8	–	1.45	–	mA
Dynamic Characteristics (See Figure 6)					
Oscillator Outputs: Terminal No. 2, V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}
Terminal No. 3, V_3	S_1 in position 2	0.75	1.0	–	V_{p-p}
ACC Detected Output V_{16} - V_{15}	S_1 in position 1	115	150	–	mV
Oscillator Pull-In Range	S_1 in position 1	–	±400	–	Hz

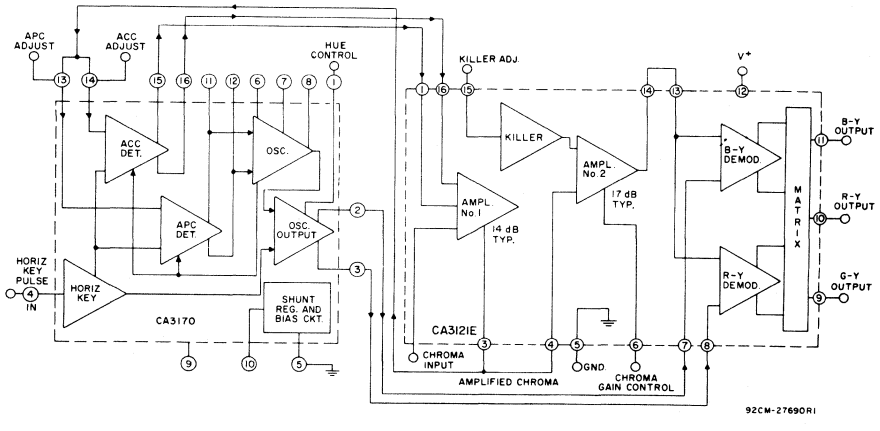


Fig. 2 Simplified functional diagram of a two-package TV chroma system utilizing the CA3170E and CA3121E.

CIRCUIT DESCRIPTION

The CA3170E is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3121E is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval. The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 16 of the CA3121E. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator. To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3170E includes a shunt regulator to establish a 12-volt dc supply.

MAXIMUM RATINGS, *Absolute-Maximum:*

DEVICE DISSIPATION:*
- Up to $T_A = 55^\circ C$ . . . . . 750 mW
- Above $T_A = 55^\circ C$ . . . . . derate linearly 7.9 mW/°C

AMBIENT–TEMPERATURE RANGE:
- Operating . . . . . −40 to +85°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During soldering):
- At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max. . . . . +265°C

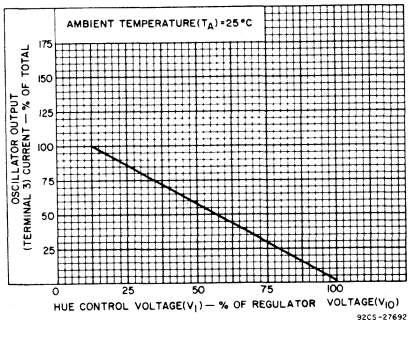


Fig. 3 — Typical hue control characteristic.

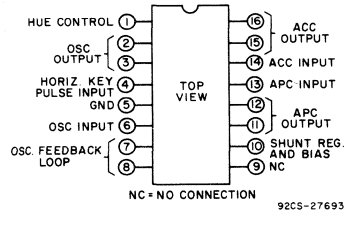


Fig. 4 — Terminal diagram of the CA3170E.

CA3170

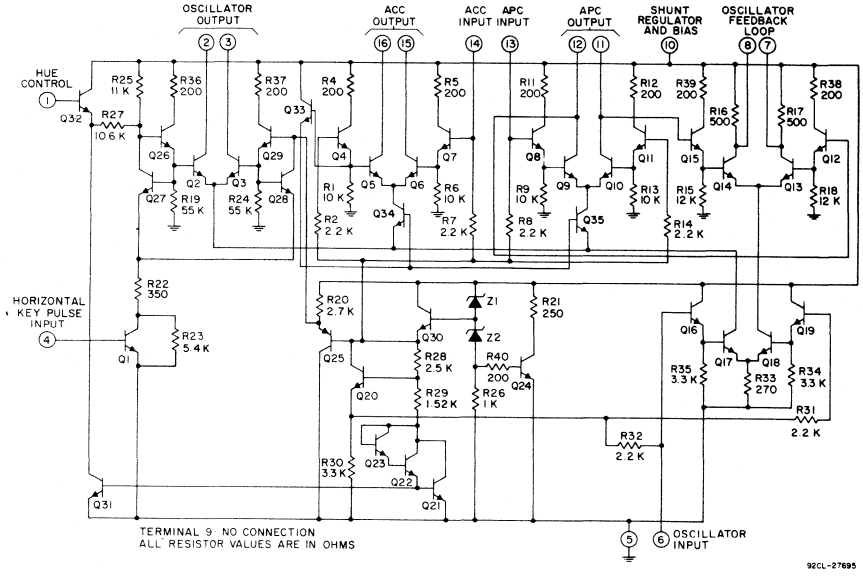


Fig. 5 — Schematic diagram of the CA3170E.

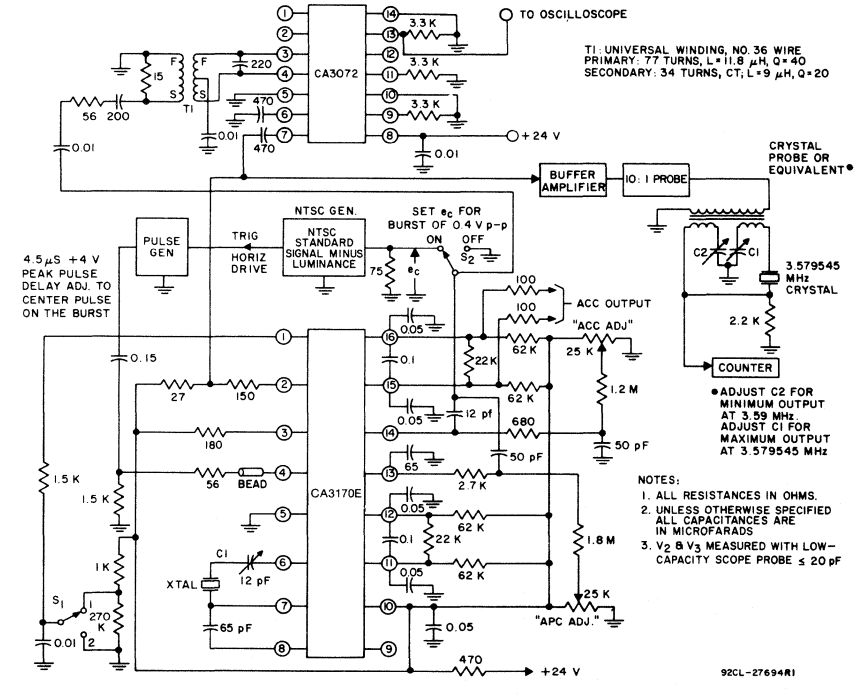


Fig. 6 — Dynamic characteristics test circuit.

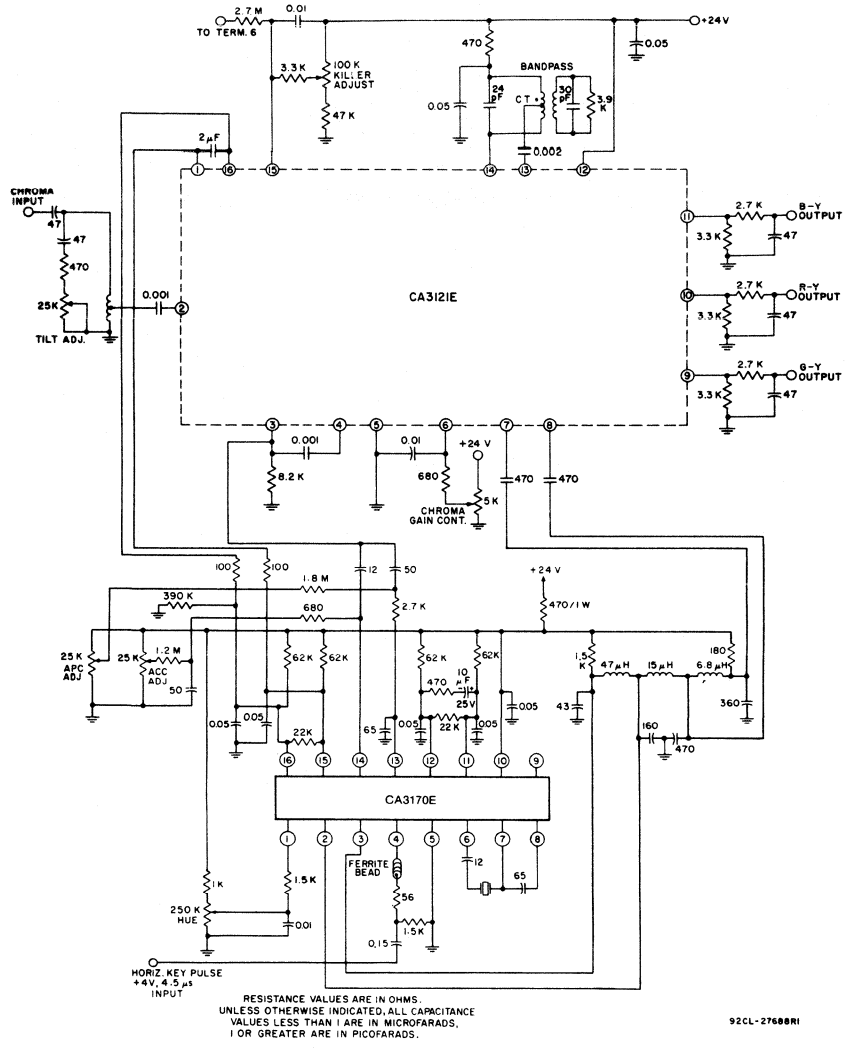


Fig. 7 —Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3170E.

DYNAMIC TEST PROCEDURE

1. With S2 in "OFF" position, short terminals 11 and 12. Then with S1 in 1 position, adjust CX for a frequency of 3.579545 MHz ± 5 Hz. Measure the frequency using the frequency counter or by zero beat indication on the oscilloscope.
2. Remove short from terminals 11 and 12, and adjust "APC" control for zero beat on the oscilloscope. With S2 in "ON" position, pattern on oscilloscope must lock.
3. With S2 in "OFF" position adjust "ACC" control to give output reading of 0 ± 2 mV between terminals 15 and 16. Then with S2 in "ON" position, read "ACC" output.
4. Example of pull-in testing to ± 200 Hz: With S2 in "OFF" position, adjust CX for frequency of 3.579545 + 200 Hz. Then with S1 in position 1 and S2 in "ON" position, pattern on oscilloscope must lock.
5. Repeat Step 4 with CX adjusted to - 200 Hz.

CA3170

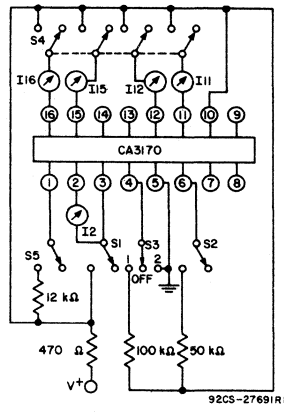


Fig. 8 – Static characteristics test circuit

CA3172

TV Chroma Demodulator

SYSTEM FEATURES:

- *Synchronous detector with color-difference matrix*
- *Emitter-follower output amplifier with short-circuit protection*
- *Typical R-Y output ratio of 0.95 and 89°, G-Y output ratio of 0.33 and 244°, and B-Y output ratio of 1.0 and 0°*

The RCA-CA3172E is a monolithic silicon integrated circuit intended for use as a chroma demodulator in TV applications. It is operated from a 24-volt supply.

The device has synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color-difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4, while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color-difference signals, after matrix, have a fixed relationship of amplitude and phase.

The outputs of the CA3172E are suitable for driving high-level color-difference or R, G, and B output amplifiers. The emitter-follower stages used to drive the high-level color amplifiers have short-circuit protection.

The CA3172E is supplied in a 14-lead dual-in-line plastic package.

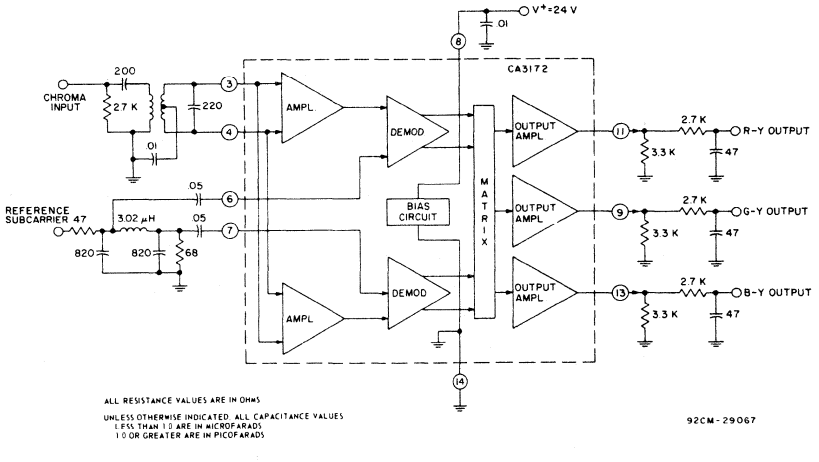


Fig. 1 — Functional diagram of RCA-CA3172E.

File Number **1130**

CA3172

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25°C*

DC SUPPLY VOLTAGE (Terminal 8 to Terminal 14)	27	V
REFERENCE INPUT VOLTAGE	5	V_{p-p}
CHROMA INPUT VOLTAGE	5	V_{p-p}
DEVICE DISSIPATION:		
Up to T_A = +70°C	530 mW	
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C	
AMBIENT TEMPERATURE RANGE:		
Operating	−40 to +85°C	
Storage	−65 to +150°C	
LEAD TEMPERATURE (During Soldering):		
At distance 1/32 in. (3.17 mm) from seating plane for 10 s max.	+265°C	

Maximum Voltage and Current Ratings at T_A = +25°C

Voltage*			Current		
Terminal No.	MIN VOLTS	MAX VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	–	–
4	0	+5	4	–	–
6	0	+12	6	–	–
7	0	+12	7	–	–
8	0	+27	8	–	–
9	0	+20	9	1.0	20
11	0	+20	11	1.0	20
13	0	+20	13	1.0	20

* With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8

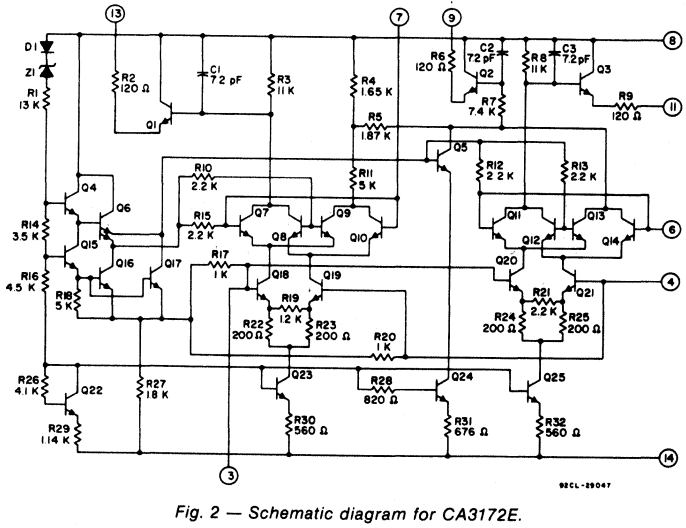


Fig. 2 — Schematic diagram for CA3172E.

CA3172

ELECTRICAL CHARACTERISTICS, *at T_A = 25°C and V^+ = +24 V unless otherwise specified*

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3172			UNITS
			MIN.	TYP.	MAX.	
Static Characteristics[a]						
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	28.5	mA
With No Output Loads		S_1 Open	–	9	–	
G-Y, R-Y, B-Y Outputs	V_9 V_{11}, V_{13}	S_1 Closed	13	14.5	15.5	V
Chroma Inputs	V_3, V_4	S_1 Open	–	3.6	–	
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.4	–	
Dynamic Characteristics[b]						
Demodulator Unbalance	V_9, V_{11}, V_{13}	$V_3 = V_4 = 0$	–	–	0.6	V_{p-p}
Maximum Color Difference Output Voltage	V_{13}	$V_3 = V_4 = 0.35\ V_{p-p}$	5	–	–	V_{p-p}
Chroma Input Sensitivity	V_3	Adjust e_c for 5.0 V_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35	
R-Y Output Ratio	V_{11}		–	0.95	–	
G-Y Output Ratio	V_9		–	0.32	–	
V_{DC} Difference Between any two Output Terminals	$\lvert V_9\rvert - \lvert V_{11}\rvert$ $\lvert V_9\rvert - \lvert V_{13}\rvert$ $\lvert V_{11}\rvert - \lvert V_{13}\rvert$	$e_c = 0$	–	–	0.6	V
Input Impedance Reference Subcarrier	R_i 6, 7 C_i 6, 7		– –	1.7 6	– –	kΩ pF
Input Impedance at Chroma Inputs	R_i 3, 4 C_i 3, 4		– –	0.95 6	– –	kΩ pF
Output Resistance	R_o 9, R_o 11, R_o 13		–	180	–	Ω

[a] Test circuit Fig. 3

[b] Test circuit Fig. 4

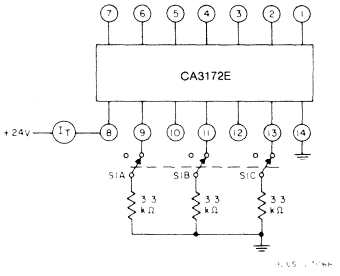


Fig. 3 – Static characteristics test circuit.

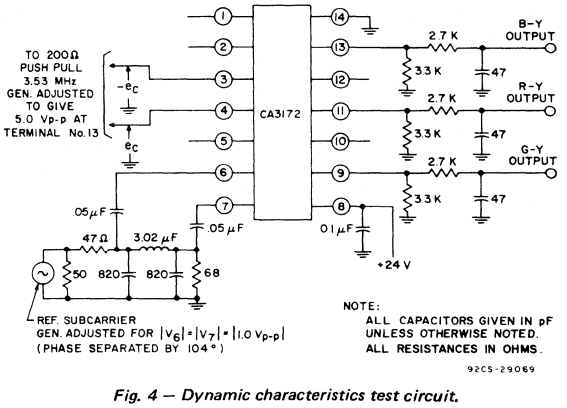


Fig. 4 – Dynamic characteristics test circuit.

CA3202

TV Horizontal/Vertical Countdown Digital Sync System

Features:

- *Automatic forced asynchronous mode to remove jitter*
- *Improved low voltage start-up operation*
- *Lower zero-state horizontal-drive pulse output*
- *Improved symmetry for horizontal-drive output*
- *Improved automatic standard operation*
- *Noise detector*
- *Handles standard NTSC and non-standard signals*
- *Automatic mode recognition*
- *Clock input*
- *Vertical ramp (sawtooth) generator*
- *Vertical amplifier*
- *Vertical blanking generator*
- *Horizontal drive pulse output*
- *Ratio-voltage regulator*
- *Inherent interlace for NTSC signals*
- *Vertical-hold control eliminated*
- *Supply-voltage range=10.8 to 13.2 V*
- *Rapid pull-in*
- *Co-channel sync lockout for NTSC signals*
- *I^2L logic*

The RCA CA3202E is an improved version of RCA CA3157. In some video playback units, there are incorrect frequency relationships between horizontal and field frequencies. Automatic forced asynchronous mode eliminates jitter when equalizer pulses are correct, but these incorrect frequency relationships exist.

Automatic standard mode occurs upon detection of nine or more equalizing pulses during a six-line-width vertical driving period after seven fields of coincidence between integrated vertical (IV) sync and internal counter output. Standard mode is retained for seven fields of missing or mutilated vertical sync pulses.

If two or more noise pulses are detected at terminal 12 during a 384-line active scan time, a noise detector reverts the system to standard mode at the next field of coincidence (without the seven fields of coincidence delay). Thus, the unit stays in standard mode during tuner channel changes.

As in the CA3157, an automatic mode-recognition system places the unit in standard mode for NTSC signals or into non-synchronous mode for non-standard sync signals.

Fig. 1 shows that the chip includes a sawtooth generator, vertical amplifier, ratio-voltage regulator, and a countdown and phasing circuit that eliminates an external vertical hold control.

An external oscillator (CA3154) supplies an input to terminal 9 that is 32 times the horizontal rate. An internal divide-by-16 counter converts this input ($32f_H$) to $2f_H$ for use elsewhere. This $2f_H$ signal is further divided to f_H, which is available at terminal 11 to drive the horizontal deflection circuits. A divide-by-525 counter further divides the $2f_H$ signal to generate the vertical ramp generator timing pulses and the vertical blanking pulse.

A phasing circuit (part of the mode recognition and vertical regeneration circuits) insures that the 525 counter is reset in coincidence with the vertical sync. It does this by comparing the internally generated vertical pulse with an external integrated vertical sync signal applied to terminal 12. The automatic mode recognition circuit forces the CA3202E into the standard mode for NTSC signals or into the non-synchronous mode for non-standard sync signals such as video games. An input control signal (or no connection) at terminal 8 places the CA3202E into non-synchronous operation.

A phasing and timing logic circuit checks to see if the line counter is in sync with the IV signal at terminal 12. Seven consecutive fields of in-phase coincidence with the IV signal are needed to achieve standard mode unless two or more noise pulses are de-detected at input terminal 12 during the active scan time. In this case, normal mode will be acquired in one field.

In the standard divide-by-525 mode, the integrated vertical pulse is used only to provide coincidence with the 545 count (counter preset=20, 545−20=525) in the phase detector circuit. The vertical ramp is timed by the output of the 525 counter. In standard mode, the CA3202E will maintain the divide-by-525 count for six fields of lost or mutilated sync. If the seventh field does not have the correct coincidence, the unit will switch to non-standard mode. In this mode, the vertical sync is derived from the integrated vertical pulse on a field-to-field basis. A noise immunity of 384 lines is provided. In the absence of sync pulses, the count will be 684 instead of 525 so that rapid vertical capture may be achieved when sync is restored. Non-standard mode still may be selected by removing ground from terminal 8.

The vertical retrace signal is converted to a ramp signal if a capacitor is connected between terminal 3 and ground. The ramp's slope corresponds to vertical size and is controlled by changing the input current to terminal 2. The ramp is connected to the inverting input of a difference amplifier. The output of this amplifier, connected to terminal 6, is used to drive the vertical output stage. The non-inverting input of the difference amplifier is at terminal 5. A voltage derived from yoke current may be applied to this terminal for linearity improvement.

The pulse width of the vertical blanking signal at terminal 7 is 608 clocks wide in the synchronous mode, and is adjustable in width by changing the monostable rc network at terminal 10 for the non-synchronous mode.

The proportional voltage regulator output at terminal 4 is about 43% of the supply voltage at terminal 12. The maximum external load current is 20-mA peak.

The CA3202E is supplied in the 14-lead dual-in-line plastic package.

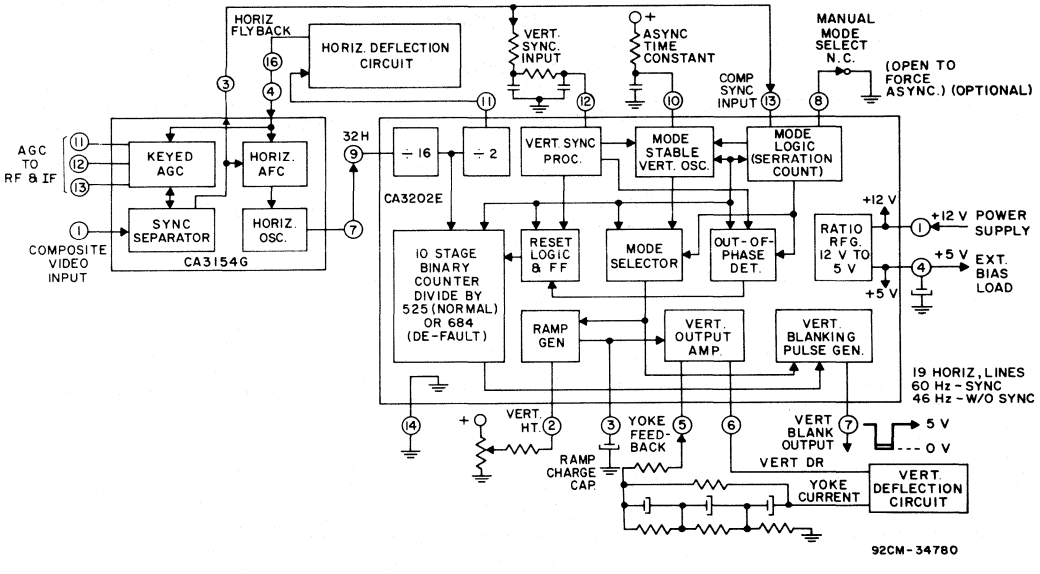


Fig. 1 - CA3202E horizontal/vertical countdown integrated circuit.

CA3202

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 15 V

DEVICE DISSIPATION:

Up to T_A=70°C ..... 530 mW

Above T_A=70°C ..... derate linearly at 6.7 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to 70°C

Storage ..... −55 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A=25°C, all switches open unless otherwise specified.
See Fig. 2, Test Points 2 and 14=Gnd.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Amplifier Gain, V6	S2,S5,S6 Closed, Note 1, Test pt. 1=12 V, 16=1 V_{RMS} at 1 kHz	0.178	3.16	V_{RMS}
Horizontal Frequency Divider Ratio, $f_g \div f_{11}$	S3,S7,S8 Closed, Note 7, Test pt. 1=14.4 V	32	32	RATIO
Horizontal Pulse Width, Term. 11	S3,S7,S8 Closed, Notes 9,10, Test pt. 1=8.4 V	28	34	μs
	S3,S7,S8 Closed, Notes 9,10,11, Test pt. 1=14.4 V	28	34	μs
Asynchronous Non-Coincident Frequency Divide Ratio, $f_g \div f_3$	S3,S7,S8 Closed, Notes 9,12,13,14,15, Test pt. 1=14.4 V, 8=0.2 V, 12 =1.5 V	10944	10944	RATIO
Ramp Charge Pulse Width, Term. 3	S3,S7,S8 Closed, Notes 13,15, Test pt. 1=14.4 V, 8=0.2 V, 12=1.5 V	585	985	μs
Asynchronous Coincident Noise Immunity, Hold-Off Freq. Divider Ratio, $f_8 \div f_3$	Notes 9,12,13,15,16,17, Test pt. 1=14.4 V, 8=0.2 V	7872	7872	RATIO
Synchronous Divider Ratio, $f_g \div f_3$	S3,S7,S8 Closed, Notes 9,13,15,18,19, Test pt. 1=14.4 V, 8=0.2 V, 12=1.5 V	8400	8400	RATIO
Ramp Charge Pulse Width, Term. 3	S3,S7,S8 Closed, Notes 9,10,13,15,18,20, Test pt. 1=14.4 V, 8=0.2 V, 12=1.5 V	190	194	CLOCKS
Vertical Blanking Pulse Width, Term. 7	S3,S7,S8 Closed, Notes 9,10,13,15,18,21 Test pt. 1=14.4 V, 8=0.2, 12=1.5 V	606	610	CLOCKS

ELECTRICAL CHARACTERISTICS at T_A=25° C, all switches open unless otherwise specified. See Fig. 2, Test Points 2 and 14=Gnd.

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		Min.	Max.	
Mode Recognition Field Count, Freq. Divider Ratio, $f_g \div f_3$	S3,S7,S8 Closed, Notes 9,13,14,15,18,22, Test pt. 1=12.0 V, 8=0.2 V, 12=1.5 V			
Synchronous to Non-Synchronous	Initial Fields 9 Serrations	8400	8400	
	First Field, 8 Ser.	8400	8400	
	Second Field, 8 Ser.	8400	8400	
	Third Field, 8 Ser.	8400	8400	
	Fourth Field, 8 Ser.	8400	8400	RATIO
	Fifth Field, 8 Ser.	8400	8400	
	Sixth Field, 8 Ser.	8400	8400	
	Seventh Field, 8 Ser.	10944	10944	
Mode-Recognition Field Count, Freq. Divider Ratio, $f_g \div f_3$	S3,S7,S8 Closed, Notes 9,13,15,18,23, Test pt. 1=12.0 V, 8=0.2 V			
Non-Synchronous to Synchronous	First Field	8384	8384	
	Second Field	8384	8384	
	Third Field	8384	8384	
	Fourth Field	8384	8384	
	Fifth Field	8384	8384	RATIO
	Sixth Field	8384	8384	
	Seventh Field	8384	8384	
	Eighth Field	8400	8400	
	Ninth Field	8400	8400	
Fast Standard-Mode Resynchronization	S3,S7,S8 Closed, Notes 9,13,15, Test pt. 1=12.0 V, 8=0.2 V			

NOTES:

1. Stop clock when terminal 7 is high.
2. Stop clock when terminal 9 is low.
3. Stop clock when terminal 9 is high.
4. Stop clock when terminal 7 is low.
5. Stop clock when terminal 11 is high.
6. Stop clock when terminal 11 is low.
7. Clock frequency=600 kHz; clock amplitude: low ≤ 0.45 V, high ≥ 0.95 V (5 V max.).
8. Frequency at terminal 9 (clock) divided by frequency at terminal 11 (hor. out).
9. Clock frequency=500 kHz, clock amplitude same as in Note 7.
10. Pulse width measured at 2 V point on output waveform.
11. Total capacity=50 pF when measuring pulse width.
12. Sync serrations=8 (see Fig. 4).
13. Sync amplitude: low state ≤ 1.2 V; high state ≥ 4 V (6 V max. with positive sync tips).
14. Frequency at terminal 9 (clock) divided by frequency at terminal 3 (ramp control).
15. Initialize or repeat initialization procedure before doing this test (see Fig. 2).
16. Apply a pulse 1 clock wide, 7808 clocks after first positive transition at terminal 3 (see Fig. 5).
17. Default count determined by 684 x 16(H)=10944.
18. Sync serrations=9.
19. Hold-off count determined by 492 x 16(H)=7872.
20. Number of clocks occurring within ramp gate period (see Fig. 6).
21. Number of clocks occurring during the blanking gate period (see Fig. 7).
22. This series of tests checks the mode recognition circuit. The first test after initialization applies 9 serrations at the sync input terminal. The IC should go to the synchronous count ratio of 8400. During the next seven fields only 8 serrations are applied. The CA3202E should maintain the synchronous count ratio of 8400 for the first six fields. At the seventh field the CA3202E should go to default count of 10944. The test concludes with a 9-serration input. The CA3202E should revert to a synchronous count of 8400 (see Fig. 8).
23. This test checks the operation of the out-of-sync detector by applying out-of-phase sync pulses to terminal 12. The CA3202E will count eight fields before resetting to the sync pulse (see Fig. 9).
24. Initialize by 8384 sync for eight fields before test.
25. This test verifies the operation of the fast resync performance by simulating a noise pulse (5 to 50 clocks wide) applied to the I.V. terminal 4000 to 6000 clocks (8 ms to 12 ms) after I.V. sync. Initialize to non-sync mode before performing this test. The IC should resync in the next field and be maintained for the standard confidence count of seven fields.

CA3202

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=12 V, Switches open unless otherwise specified. See Fig. 2. Test Points 2, 8, 12 and 14 grounded unless otherwise specified.

CHARACTERISTIC	TEST CONDITIONS	CONNECT TEST POINTS AS SHOWN BELOW — TEST POINT NOS.								LIMITS		UNITS
		1	3	4	5	6	10	11	13	Min.	Max.	
Ratio Regulator Voltage, V_4:												
Load	S2 Closed, Note 1	12V		−20 mA	2V					4.9	5.5	V
No Load		14.4V			2V					5.8	6.8	
Vertical Blanking Output, V_7:												
Unblanked	S2 Closed,	12V		−20 mA	G					2.5	5	V
Blanked	Notes 1, 4	12V			G					0.09	0.5	
Horizontal Output Voltage, V_{11}:												
High	Test pt. 15=8V, S2 Closed,	14.4			G					7	8.1	V
Low	Notes 5, 6	12V			G			20 mA		0	0.12	
Vertical Output Voltage, V_6:												
Off	S4 Closed, Note 1	12V			G	1 mA				0.6	1.4	V
On	S3 Closed, Note 1	12V	G			−20 mA				3.4	5.1	
Difference Voltage, V_3–V_5	S2 Closed, Note 1	12V			4V	−20 mA				-0.15	0.15	V
Supply Current, I_1	S2 Closed, Note 1	14.4V			2V					10	35	mA
Clock Current, I_9: Low	Test pt. 9=GND S2 Closed, Note 2	14.4V			2V					−180	−70	μA
Voltage, V_9	S2 Closed, Note 3	14.4V			2V					—	0.75	V
Composite Sync Input Current, I_{13}:												
Sync High	S2 Closed, Note 3	12V			2V				4V	100	700	μA
Sync Low		14.4V			2V				0V	−25	25	
Forced Asynchronous Current, I_8	S2 Closed, Note 3, Test pt. 8=4.5V	12V			2V					1	3.2	mA
Ramp Current, I_3	S3 Closed, Note 1, Test pt. 2=50 μA	12V	4.5V							45	57	μA
Δ Ramp Current, ΔI_3	S3 Closed, Note 1, Test pt. 2–50 μA	12V	1.5V							−3	3	μA
Async Time Constant Current, I_{10}:												
Charge	S2 Closed, Note 4	12V			2V		3V			10	40	μA
Discharge		12V			2V		4.5V			1	5	mA
Vert. Sync. Input Current, I_{12}:												
Normal	S2 Closed, Note 4, Test pt. 12=2.3V	12V			2V					−0.1	5	μA
Overdrive	S2 Closed, Note 4, Test pt. 12=3V	12V			2V					0.1	3	mA

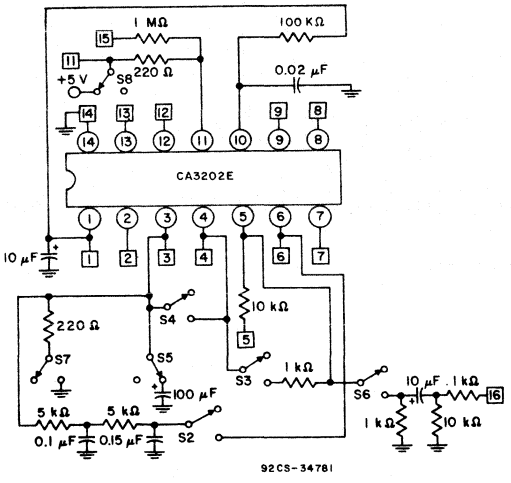


Fig. 2 - Electrical characteristics test circuit.

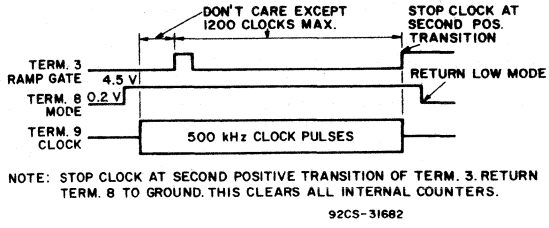


Fig. 3 - Initialization timing diagram (applies to all tests referenced to Note 15).

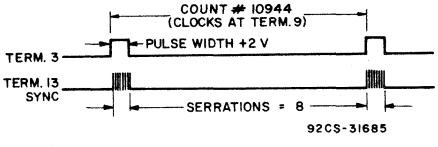


Fig. 4 - Asynchronous non-coincident divide ratio (applies to all tests referenced to Note 12).

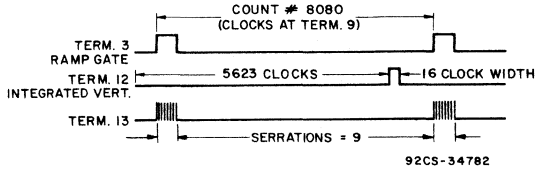


Fig. 5 - Synchronous non-coincidence noise recovery (fast resync).

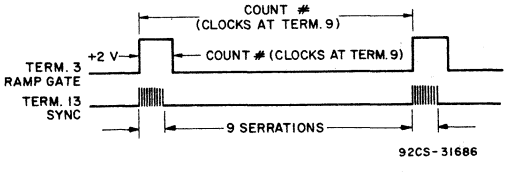


Fig. 6 - Synchronous non-coincident divider ratio and ramp gate pulse width (applies to test referenced to Note 20).

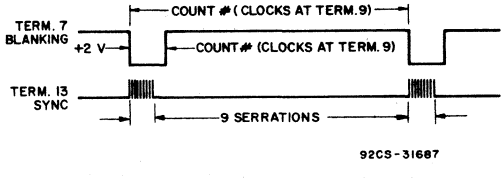


Fig. 7 - Blanking synchronous divider ratio and blanking pulse width (applies to test referenced to Note 21).

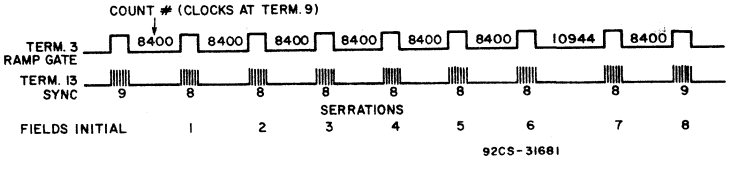


Fig. 8 - Mode recognition field count test (applies to test referenced to Note 22).

CA3202

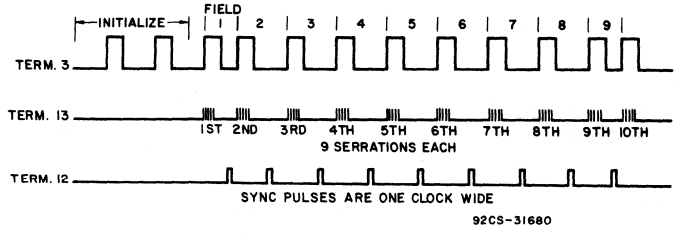


Fig. 9 – Out-of-sync detector test for confidence of coincidence field count at terminal 3 (applies to test referenced to Note 23).

Advance Information/
Preliminary Data

CA3237

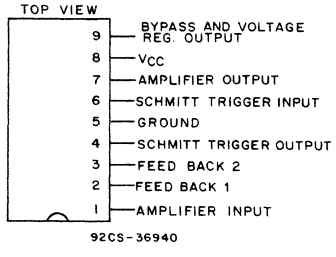
IR Remote-Control Amplifier

Features:

- *Integrated circuit package - 9-pin SIP*
- *Excellent overload characteristics*
- *High-gain amplifiers*
- *Schmitt trigger switching*
- *12 volt power supply*
- *Low power dissipation*
- *Internal regulation*
- *Nominal 100 μV sensitivity*
- *Nominal 50K input impedance*

The RCA type CA3237E• Linear Integrated Circuit is intended for infrared remote control receiver applications for TV receivers. The sensor for the remote control receiver consists of a photo-diode that senses the 40 kHz pulse code modulated control signal from the infrared carrier. The other functional parts of the system include an amplifier-limiter, a narrow band filter, a detector, a Schmitt trigger, and a decoder. The RCA CA3237E provides the amplifier limiter and the Schmitt trigger. The amplifier limiter consists of two stages. Both stages have externally accessible feedback points for external gain programming. Internal voltage regulation is provided. The RCA CA3237E is supplied in the nine lead single-in-line package. The RCA CA3237E is pin-for-pin compatible with the AN5020.

•Formerly RCA developmental type TA11167



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values (TA = 25° C unless otherwise specified):*

DC SUPPLY-VOLTAGE, (VCC)	14.4 V
DC SUPPLY CURRENT (ICC)	25 mA
POWER DISSIPATION PER PACKAGE:	
Up to TA = 85° C	360 mW
TEMPERATURE RANGE:	
OPERATING	-40 to +85° C
STORAGE	-55 to +150° C
MAXIMUM JUNCTION TEMPERATURE	+150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At a distance not less than 1/16 inch (1.59 mm) from case for 10 s max.	+260° C

Note: Recommended supply voltage range (VCC) is 9.6 to 14.4 volts.

File Number **1480**

CA3237

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V_{CC} = 12 Volts (unless specified otherwise). See Figure 3 for Test Circuit.

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Static (DC) Characteristics	Switch 1 open, Switch 2 in position 3 (input open)				
Supply Current	V_{CC} = 14.4 V	—	6	10	mA
Balance Voltage, Pin 3		—	2.5	—	V
Bias Voltage, Pin 2		—	2.8	—	V
Regulator Voltage, Pin 9		—	6.3	—	V
Op-Amp Bias Voltage, Pin 7		—	—	1.7	V
Dynamic Characteristics	Switch 1 open unless specified otherwise				
Amplifier High Level, (Pin 7 out)	V_1 in = 5V p-p, freq. = 40 kHz, Switch 2 in position 1	2.5	—	—	Vp-p
Amplifier Gain (V_1 in)	Pin 7 out = 800 mV p-p, freq. = 40 kHz, Switch 2 in position 1	—	—	500	μV p-p
Schmitt Trigger Output Voltage High (Pin 4 out)	Pin 6 = 1.5 V DC, Switch 2 in position 3 (input open)	4.0	—	5.0	V_{DC}
Schmitt Trigger Output Voltage Low, (Pin 4 out)	Pin 6 = 0.3 VDC, Switch 2 in position 3 (input open)	0	—	0.8	V_{DC}
Schmitt Trigger High Trip Voltage (Pin 6 in)	Pin 4 out = 4.0 VDC, Switch 2 in position 3 (input open)	—	—	1.3	V_{DC}
Schmitt Trigger Low Trip Voltage (Pin 6 in)	Pin 4 out = 0.8 VDC, Switch 2 in position 3 (input open)	0.5	—	—	V_{DC}
Functional Test (Pin 4 out)	V_{CC} = 9.6, 12.0 or 14.4V, V_1 in = 5V p-p, freq. = 40 kHz, Switch 1 closed, Switch 2 in position 1	2.0	—	—	V_{DC}
Output noise (at T.P.A)	Switch 2 in position 2 (input grounded)	—	—	10	mV RMS

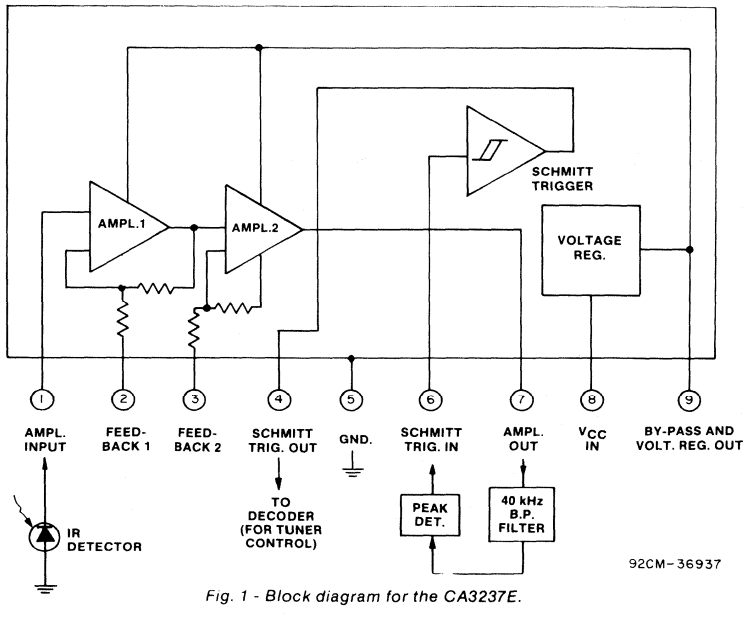


Fig. 1 - Block diagram for the CA3237E.

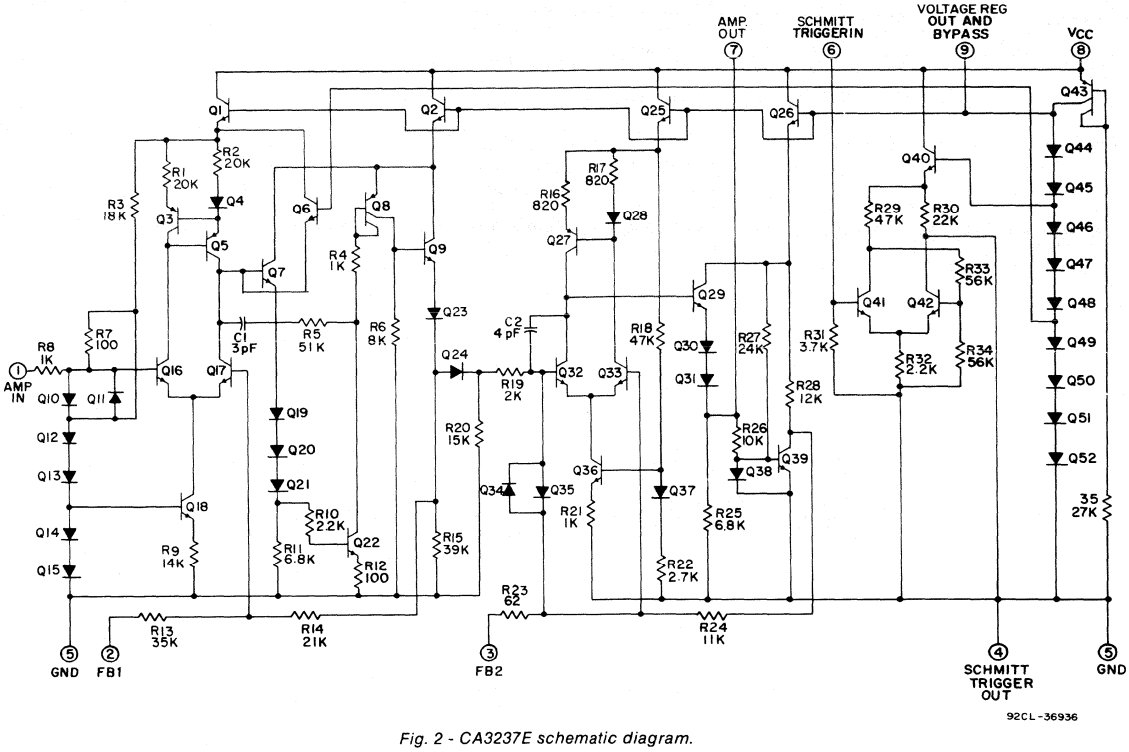


Fig. 2 - CA3237E schematic diagram.

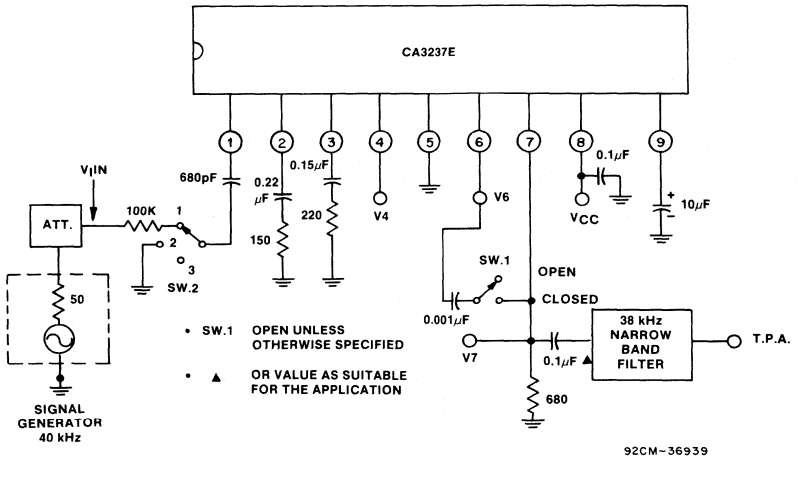


Fig. 3 - CA3237E test circuit.

CA7607, CA7611

Video IF Amplifier System for Color and Black and White TV Receivers

Especially Suitable for SAW Filter Applications

Features:

- *High-gain wideband IF output*
- *Excellent S/N ratio*
- *Excellent DG/DP characteristics*
- *Black and white noise inverters*
- *Peak AGC*
- *Fast uniform AGC action*
- *Wide-gain reduction range*
- *Synchronous AFT detector*
- *High gain AFT*
- *Synchronous video detector*
- *Negative video output*
- *VTR switch*

RCA CA7607 and CA7611• perform video IF amplification, video detection and amplification, AFT detection and amplification and AGC control of video IF and tuner stages. The CA7607 is suitable for FET applications; the CA7611 is used for NPN tuner stages and has a higher value of RF AGC control current.

•The CA7607 was formerly RCA Dev. No. TA10770; the CA7611 was formerly RCA Dev. No. TA11025.

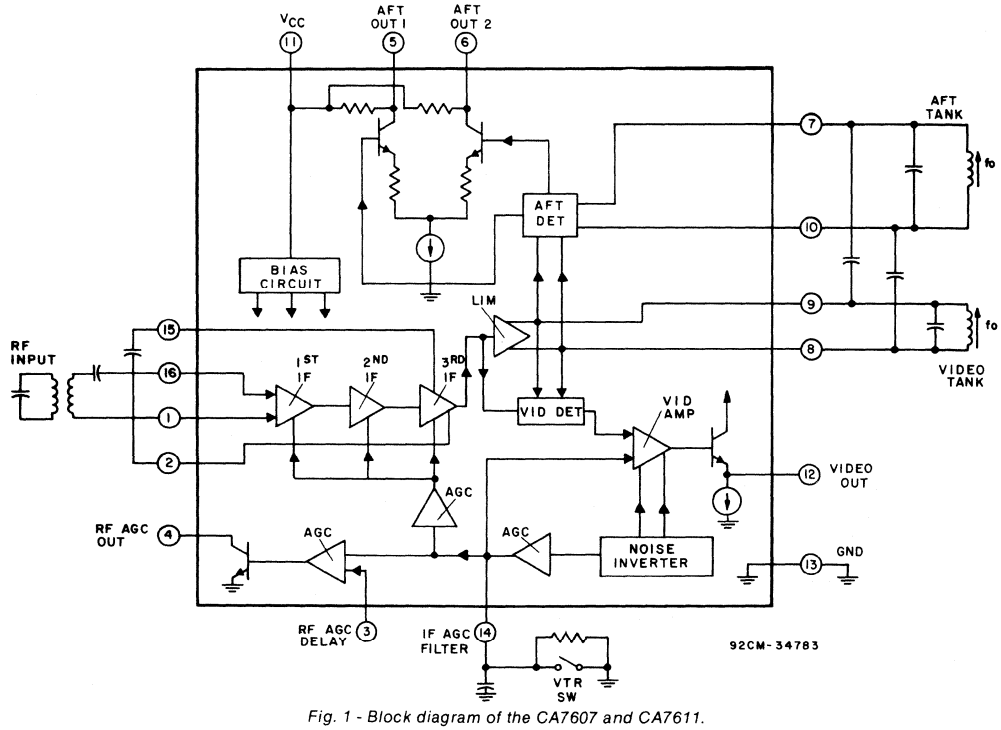


Fig. 1 - Block diagram of the CA7607 and CA7611.

File Number **1350**

CA7607, CA7611

A three-stage, wideband IF amplifier employs an advanced gain reduction circuit for a wide range of AGC gain control with excellent stability at all gain conditions.

A synchronous video demodulator having a low distortion reference amplifier provides a negative-polarity video output signal containing negligible intermodulation products.

Noise inverters prevent ultra white and black spots in the picture.

A separate synchronous demodulator is used for AFT detection giving an accurate and sensitive AFT (12 kHz/V typ.).

A VTR switch permits removing internal video when using a VTR.

The CA7607 and CA7611 are supplied in 16-lead dual-in-line plastic packages (E suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Between Terminals 11-13 ..... 15 V
- Between Terminals 4-13 ..... 15 V

VIDEO OUTPUT CURRENT, I12 ..... 6 mA

DEVICE DISSIPATION:
- Up to T_A = 70°C ..... 890 mW
- Above T_A = 70°C ..... Derate linearly 11.2 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -40 to +70°C
- Storage ..... -65 to +150°C

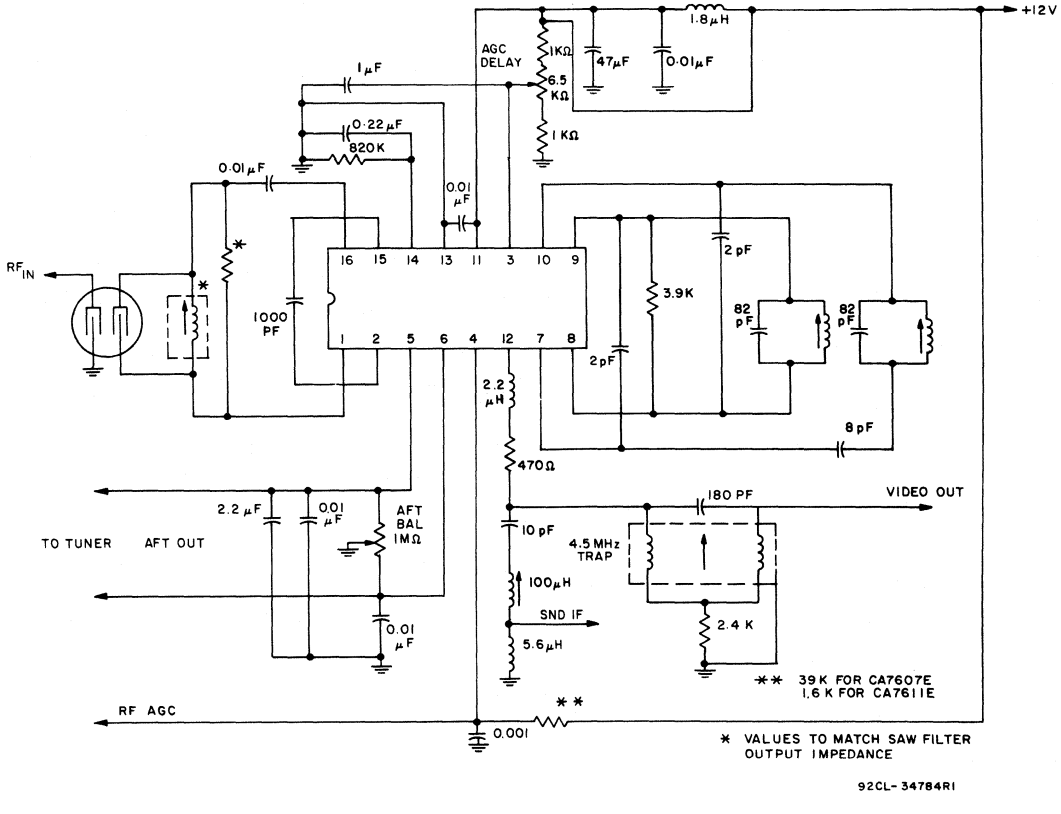


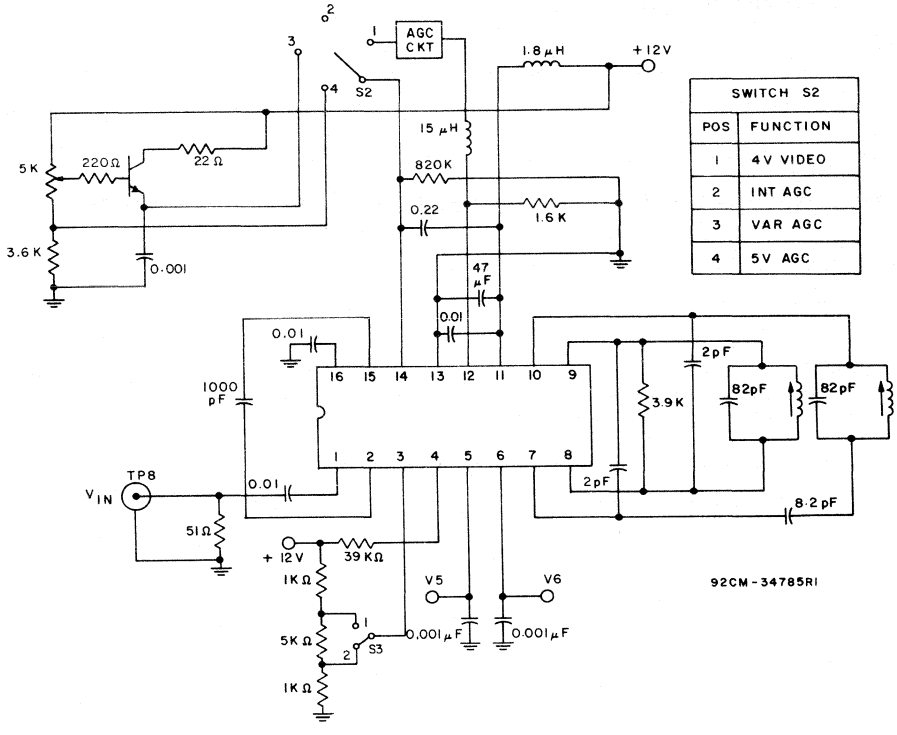
Fig. 2 - Typical application circuit for the CA7607 and CA7611.

CA7607, CA7611

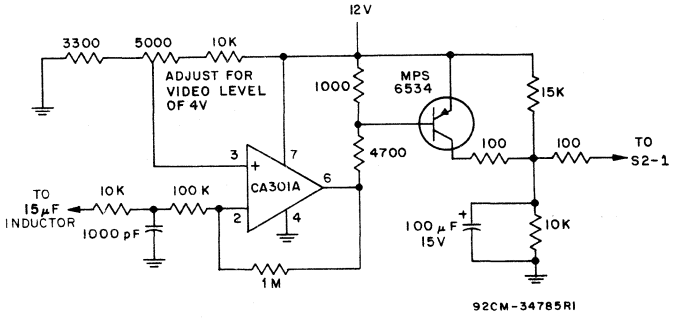
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V+ = 12 V, V_{IN} at TP8 (Fig. 3)

CHARACTERISTIC	TEST CONDITIONS	S2	S3	LIMITS			UNITS
				Min.	Typ.	Max.	
Recommended Supply Voltage				10.8	12	13.2	V dc
Supply Current, I11	V_{IN} = 0	4	1	42	51	63	mA
Video DC Output Voltage, V12	V_{IN} = 0	4	1	5.2	5.5	5.8	V dc
AFT DC Output Voltage, V5	V_{IN} = 0	4	1	5.3	7.3	8.3	V dc
AFT DC Output Voltage, V6	V_{IN} = 0	4	1	5.3	7.3	8.3	V dc
AFT Output Offset Voltage, V5-V6	V_{IN} = 0	4	1	-1.5	0	1.5	V dc
RF AGC Residual Output Voltage, $V4_{sat}$	CA7607	4	1	0	0.2	0.5	V dc
	CA7611	4	2				
RF AGC Voltage Drop, V11-V4	CA7607	2	2	-0.1	0	0.1	V dc
	CA7611	4	1				
Maximum Video Sensitivity, V12	V_{IN} = 25 μV rms CW	2	2	-0.25	0.25	1	V dc
Minimum Video Sensitivity, V12	V_{IN} = 110 μV rms CW	2	2	1	2	3.8	V dc
Synch Tip Level Voltage, V12	V_{IN} = 15 mV rms	2	2	2.3	2.5	2.7	V dc
Black Noise Threshold Level Voltage, V12	V_{IN} = 50 mV rms at 45.75 MHz @ 30% AM Mod 1 kHz	3	2	1.4	1.6	1.8	V dc
Black Noise Clamp Level, V12		3	2	2.9	3.3	3.7	V dc
Video Freq. Response at 3.58 MHz, V12		1	2	-2	0	+1	dB
Video Freq. Response at 4.5 MHz, V12		1	2	-3	-2	+2	dB
920-kHz Beat, V12	V_{IN1} = 33 mV rms CW V_{IN2} = 11 mV rms CW V_{IN3} = 11 mV rms CW	1	2	31	38	—	dB
Video Amplifier Bandwidth, V12 +BW		1	2	4.5	5.5	10	MHz
Suppression of Carrier, V12	V_{IN} = 25 mV at 45.75 MHz @ 80% AM Mod 1 kHz	3	2	40	50	—	dB
Suppression of 2nd Harmonic, V12		3	2	35	50	—	dB
Differential Phase, V12		2	2	—	3.5	6	degree
Differential Gain, V12		2	2	—	7	10	%
Picture-to-Noise Ratio, PIN 12	V_{IN} = 25 mV at 45.75 MHz CW	1	2	53	58	—	dB
Picture-to-Noise Ratio, PIN 12	V_{IN} = 7.5 mV at 45.75 MHz CW	1	2	50	54	—	dB
AFT Sensitivity $\frac{\Delta f}{V5\text{-}V6}$	V_{IN} = 15 mV rms CW	2	2	6	12	16	kHz/V
AFT Output at 44.75 MHz, V5	V_{IN} = 15 mV rms CW	2	2	11.4	11.9	12.1	V dc
AFT Output at 44.75 MHz, V6	V_{IN} = 15 mV rms CW	2	2	1.6	2.1	2.8	V dc
AFT Output at 46.75 MHz, V5	V_{IN} = 15 mV rms CW	2	2	1.6	2.1	2.8	V dc
AFT Output at 46.75 MHz, V6	V_{IN} = 15 mV rms CW	2	2	11.4	11.9	12.1	V dc
RF Delay 1, V4	V_{IN} = 15 mV rms at 45.75 MHz CW CA7607	2	1	0	1	10.4	V dc
	CA7611	2	2				
RF Delay 2, V4	V_{IN} = 100 mV rms at 45.75 MHz CW CA7607	2	2	10.6	12	12.1	V dc
	CA7611	2	1				
RF AGC Leakage Current, I4L				—	—	1	μA
Maximum Available Current, $I4_{max}$	CA7607			0.3	—	—	mA
	CA7611			7	—	—	
RF Delay Low, V4	CA7607	2	1	0.2	5	15	mV
	CA7611	2	2				
RF Delay High, V4	CA7607	2	2	100	200	1000	mV
	CA7611	2	1				
Input Impedance, PIN 1-16		4		— —	3 3	— —	kΩ pF

CA7607, CA7611



SWITCH S2	
POS	FUNCTION
1	4V VIDEO
2	INT AGC
3	VAR AGC
4	5V AGC



Detail of AGC circuit.

Fig. 3 - Test circuit for the CA7607 and CA7611.

LM1822N

Product Preview

Video IF Amplifier/PLL Detector System

Features:

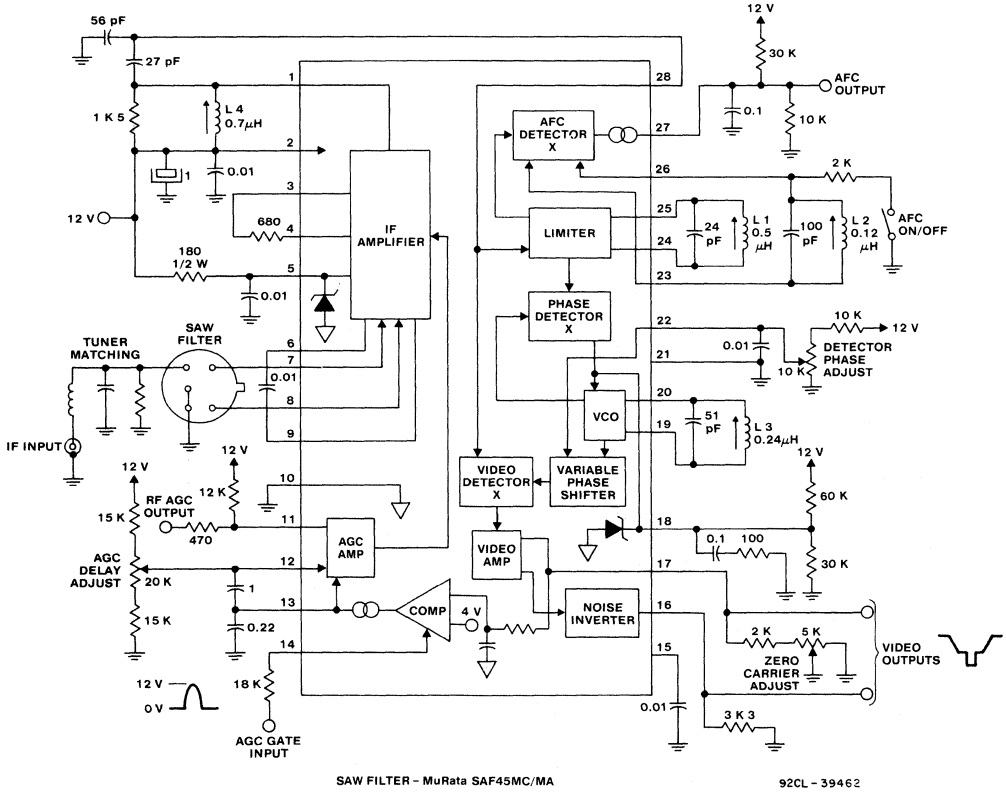
- *Common-base IF inputs for SAW filters*
- *Synchronous video detector using PLL*
- *Adjustable zero-carrier output level*
- *White spot noise inverter for luma amplifiers*
- *AFT detector with adjustable output bias*
- *Excellent detector small-signal linearity*
- *Excellent stability*
- *System operation to 70 MHz*

The RCA LM1822N is a complete video IF signal processing system. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous detector with noise inversion, an AFC detector, and gated AGC.

This integrated circuit is suitable for TV receivers and TV cable converter applications requiring high-quality video recovery.

The LM1822N is supplied in a 24-lead dual-in-line plastic package.

*Formerly RCA Developmental Type No. TA11928B.



SAW FILTER – MuRata SAF45MC/MA

L 1 – 9 1/2 T
L 2 – 4 1/2 T
L 3 – 6 1/2 T
L 4 – 11 1/2 T
} #22 WIRE ON 3/16" FORM WITH HF CORE, SHIELDED

ALL CAPS IN μF UNLESS NOTED

92CL-39462

Block diagram and typical application of the LM1822N.

Preview data only

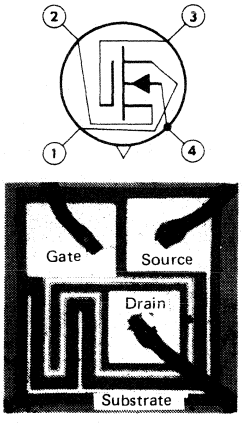
Small-Signal MOSFETs

Small-Signal MOSFETs — Technical Data

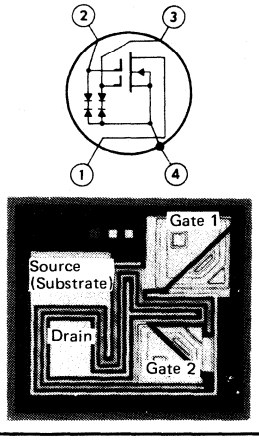
Type No.	Description	Page No.
Single Gate		
3N128	High-Gain, low-noise RF amplifier, IF amplifier, oscillator, and DC amplifier	1038
3N142	High-Gain, Low-noise RF amplifier, oscillator and DC amplifier	1043
3N143	Mixer and oscillator	1038
3N152	High-Gain, Low-noise premium-performance RF amplifier, mixer, and oscillator	1048
3N153	DC amplifier	1053
3N154	Low-leakage premium-performance RF amplifier	1056
40467A	200-MHz General purpose RF amplifier and oscillator	1037
40468	100-MHz RF amplifier	1037
40559A	100-MHz oscillator or mixer	1037
Dual-Gate Protected		
3N187	RF amplifier, mixer, and IF amplifier	1060
3N200	High-gain Rf amplifier, mixer, and IF amplifier	1068
3N204	Low-noise RF amplifier	1074
3N205	Low-noise mixer	1074
3N206	Low-noise IF amplifier	1074
40673	200-MHz RF amplifier, mixer, and IF amplifier	1037
40819	RF Amplifier, Mixer and IF Amplifier	1037
40820	RF Amplifier	1037
40821	RF Mixer	1037
40822	RF Amplifier	1037
40823	RF Mixer	1037
40841	General Purpose	1037

RCA Small-Signal MOSFETs (MOS Insulated-Gate Field-Effect Transistors)

Single-Gate Types



Dual-Gate Protected Types



RCA Single-gate and dual-gate MOSFETs offer these features and benefits to the designer:

- Extremely high input resistance — imposes virtually no loading on AGC voltage source
- Very low feedback capacitance
- High forward transconductance
- Wide dynamic range — handle positive and negative input-signal excursions without diode-current loading
- Wide AGC range
- Virtually no AGC power required
- Very low gate leakage current — relatively insensitive to temperature variations
- Negative temperature coefficient of drain current — makes "thermal runaway" virtually impossible
- Zero offset voltage — especially desirable for chopper applications
- Bulk (substrate) terminal available on all single-gate types
- Substantially better cross-modulation characteristics and lower spurious response than junction-type FET's and bipolar transistors
- Operating-temperature range, all types: −65 to +175°C

RCA Dual-gate MOSFETs offer these additional features

- Extremely low feedback capacitance
- Reduced oscillator feedthrough
- Higher frequency capabilities
- Exceptionally high forward transconductance
- Higher vhf power gain
- No neutralization required
- Increased gain reduction with AGC
- Cross-modulation characteristics actually improve as device approaches cutoff
- Unique advantages for mixer, product-detector, remote gain control, color-demodulator, balanced-modulator, chopper, clipper, and gated-amplifier applications
- Can function as a triode equivalent device when the two gates are connected to a single terminal

Quick-Selection Guide

Application	Industrial Types								Consumer Types								
	Single-Gate						Dual-Gate Protected		Single-Gate			Dual-Gate Protected					
	3N128	3N142	3N143	3N152	3N153	3N154	3N187	3N200	40819	40467A	40468A	40559A	3N204	3N205	3N206	40673	40820	40821	40822	40823	40841
RF Amplifier, Mixer	■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Chopper					■																■
General-Purpose Amplifier		■																			■
Oscillator	■	■	■	■		■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■
Low-Noise				■			■	■					■	■							
Low-Leakage					■																
High-Gain				■			■	■					■	■	■						
Gain-Controlled							■	■	■				■	■	■	■	■	■	■	■	■
Premium-Performance				■			■	■													

3N128, 3N143

Silicon MOS Transistor

For Amplifier Mixer & Oscillator Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

Features:

- *Large dynamic range*
- *Greatly reduces spurious responses in receiver front ends*
- *Permits use of vacuum-tube biasing techniques*
- *Excellent thermal stability*
- *Superior crossmodulation capability*

Applications:

- *VHF amplifiers, mixers, converters and if-amplifiers in communication receivers*
- *High impedance timing circuits*
- *Detectors, oscillators, frequency multipliers, phase splitters, pulse stretchers and current limiters*
- *Electrometer amplifiers*
- *Voltage-controlled attenuators*
- *High impedance differential amplifiers*

RCA-3N128 and 3N143• are N-channel depletion-type silicon field-effect transistors utilizing the MOS construction. The 3N128 is intended primarily for VHF amplifier service in military and industrial applications. It also is extremely well suited for use in dc and low-frequency amplifier applications requiring a transistor having high power gain, very high input impedance, and low gate leakage.

The 3N143 is designed for use as a VHF mixer and oscillator. Because of their improved transfer characteristic and increased dynamic range the 3N128 and 3N143 provide substantially better cross-modulation performance in linear amplifier applications than conventional (bipolar) transistors and are free from diodecurrent loading common to junction type FET's. Thes transistors are hermetically sealed in JEDEC TO-72 met packages and utilize full-gate construction.

Application data for RCA-3N128, including biasing re quirements, basic circuit configurations, selection of optimu operating point, and methods for automatic gain control ar given in RCA Application Note AN-3193, "Application Cor siderations for the RCA-3N128 VHF MOS Field-Effe Transistor".

• Formerly Developmental Nos. TA2840 and TA7275, respectivel

Maximum Ratings, *Absolute-Maximum Values:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} ..... +20 max.

GATE-TO-SOURCE VOLTAGE, V_{GS}:

Continuous dc ..... +1, −8 max.

Peak ac ..... ±15 max.

DRAIN CURRENT, I_D (PULSED) ..... 50 m

Peak duration ≤ 20 ms, duty factor ≤ 0.15

TRANSISTOR DISSIPATION, P_T:

At ambient temperatures up to 25 °C ..... 400 m

above 25 °C ..... derate at 2.67 mW/

AMBIENT TEMPERATURE RANGE:

Storage and Operating ..... −65 to +175

LEAD TEMPERATURE (During Soldering):

At distances not closer than 1/32 inch to seating surface for 10 seconds maximum ..... 265 max.

3N128, 3N143

ELECTRICAL CHARACTERISTICS: (At T_A = 25°C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS						UNITS
			3N128			3N143			
			MIN	TYP	MAX	MIN	TYP	MAX	
Forward Transconductance	g_{fs}	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	- 5,000	10,000 7,500	- 12,000	- 5,000	- 7,500	 12,000	μmho μmho
Magnitude of Forward Transadmittance	$\|y_{fs}\|$	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	5,000	7,500	-	-	-		μmho
Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V T_A = 25°C V_{DS} = 0, V_{GS} = -8 V T_A = 125°C	- -	0.1 -	50 5	- -	0.1 -	1000 100	pA nA
Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	-	5.5	7	pF
Small-Signal Short-Circuit Reverse Transfer Capacitance*	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	0.12	0.20	-	0.12	0.20	pF
Small-Signal, Short-Circuit Output Capacitance	C_{oss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	1.4	-	-	1.4	-	pF
Gate Leakage Resistance	R_{GS}	V_{DS} = 0, V_{GS} = -8 V	-	10^{14}	-	-	10^{14}	-	Ω
Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	-	200	-	Ω
Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-2	-3.5	-8	-2	-3.5	-8	V
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V V_{GS} = -8 V	-	-	50	-	-	50	μA
Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	5	15	25	10	20	50	mA
Input Conductance	g_{is}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	--	-	-	-	-	10	μmho
Output Conductance	g_{os}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	-	-	-	-	-	1,000	μmho
Power Gain Maximum Available Gain Maximum Usable Gain (Neutralized) see Fig.1	G_{PS}	V_{DS} = 15V, I_D = 5 mA, f = 200 MHz	 15 13.5	 20 16	 - -	 - -	 - -	 - -	 dB dB
Power Gain (Conversion (See Fig.3)	$G_{PS(c)}$	V_{DS} = 15 V, I_D = 1 mA, f_{in} = 200 MHz f_{out} = 30 MHz	-	-	-	10	13.5	-	dB
Noise Figure (see Figs. 1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	3.5	5	-	-	-	

* Three-Terminal Measurement: Source Returned to Guard Terminal.

** Pulse Test: Pulse Duration 20 ms max. Duty Factor ≤ 0.15.

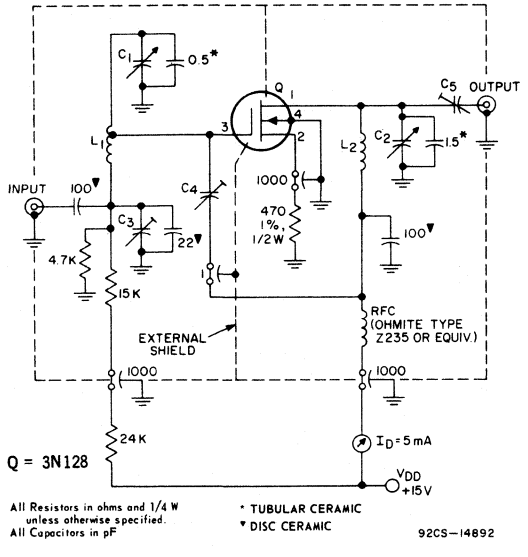


Fig.1 - Test Circuit used to Measure 200 MHz Maximum Usable Power Gain and Noise Figure

C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

3N128, 3N143

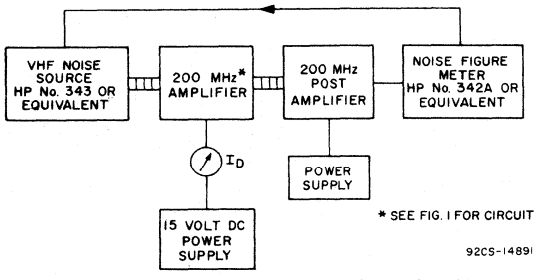
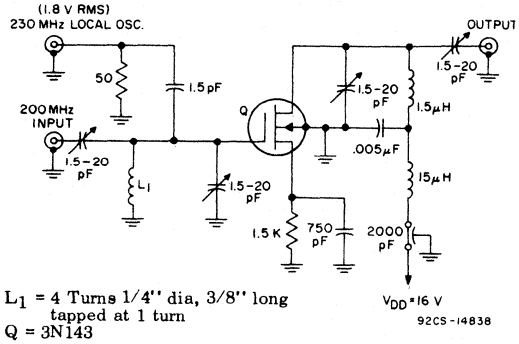


Fig.2 – Noise Figure Measurement Setup for 3N128



L_1 = 4 Turns 1/4" dia, 3/8" long tapped at 1 turn
Q = 3N143

Fig.3 - Conversion Power Gain Test Circuit.

TYPICAL CHARACTERISTICS

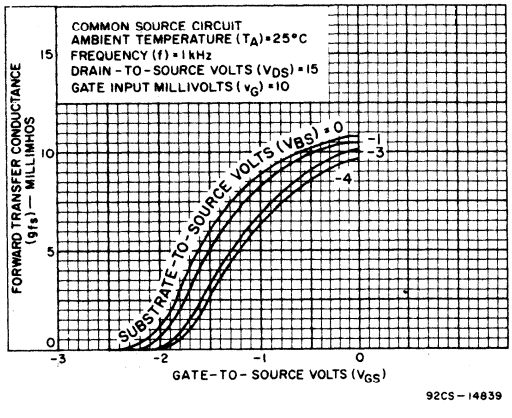


Fig.4 - Forward Transconductance vs Gate-Bias Voltage.

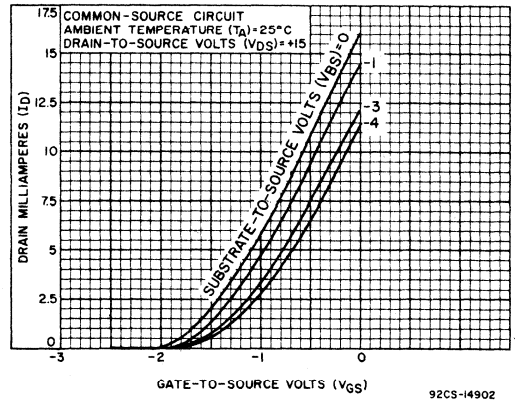


Fig.5 - Drain Current vs Gate-to-Source Voltage.

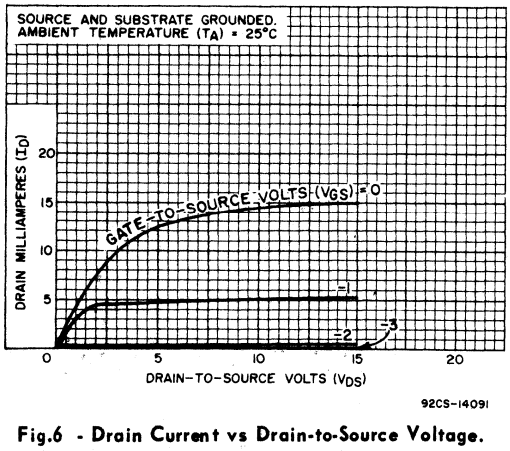


Fig.6 - Drain Current vs Drain-to-Source Voltage.

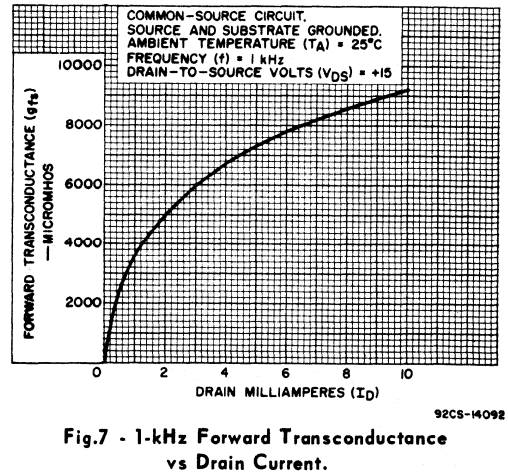


Fig.7 - 1-kHz Forward Transconductance vs Drain Current.

TYPICAL 200-MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs DRAIN CURRENT

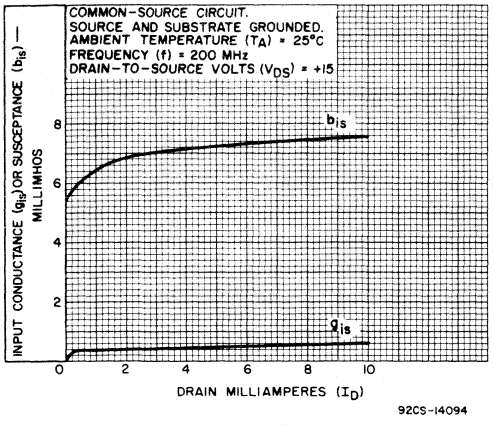


Fig.8 - Input Admittance (Y_{is}) Components.

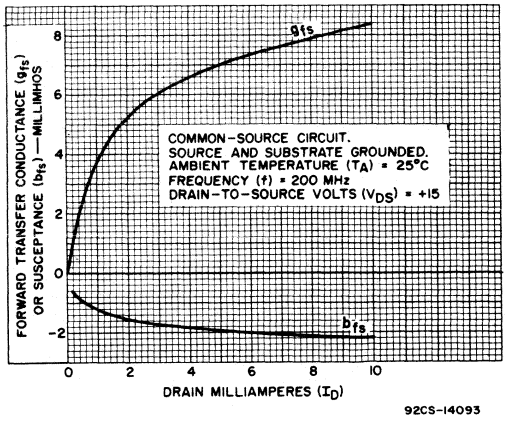


Fig.9 - Forward Transadmittance (Y_{fs}) Components.

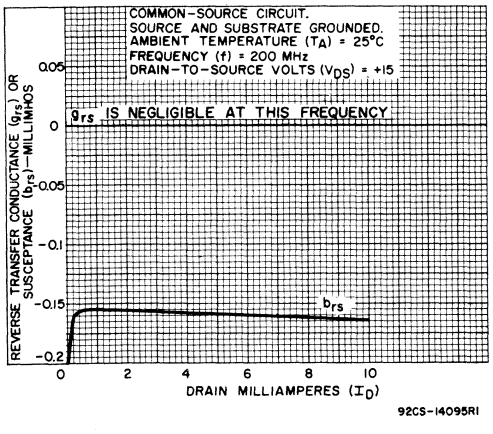


Fig.10 - Reverse Transadmittance (Y_{rs}) Components.

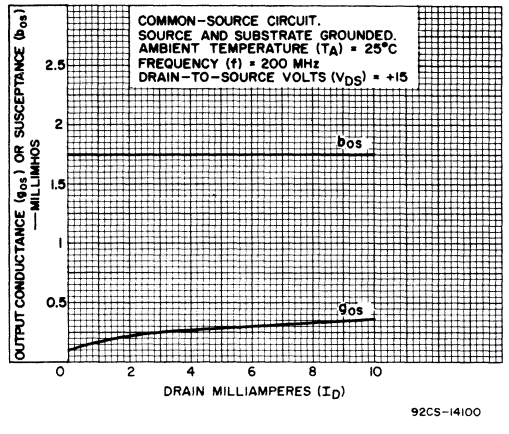
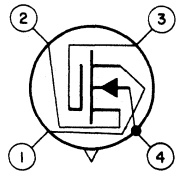


Fig.11 - Output Admittance (Y_{os}) Components.

3N128, 3N143

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

OPERATING CONSIDERATIONS

The flexible leads of the 3N128 and 3N143 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

These devices should not be connected into or d connected from circuits with the power on becau high transient voltages may cause permanent da age to the devices.

3N142

ilicon Insulated-Gate ield-Effect Transistor

)r Industrial and Military Applications to 175 MHz

atures:

Large dynamic range
Enhanced signal-handling capacity for low cross modulation
Dual-polarity gate permits positive and negative swing without degradation of input impedance
Reduced spurious responses in FM receivers
Permits use of vacuum-tube biasing techniques
Excellent thermal stability for critical oscillator designs

Applications:

- *RF amplifier, mixer, and oscillator in:*
  CB and mobile communication receivers
  Aircraft and marine receivers
  CATV and MATV equipment
- *Industrial control circuits*
- *Variable attenuators*
- *Current limiters*
- *Instrumentation equipment*
- *High-impedance timing circuits*

CA-3N142• is a silicon, insulated-gate field-effect transistor the N-channel depletion type utilizing the MOS* construc- n. It features

high input resistance — 1000 megohms

low feedback capacitance — 0.2pF max.

low noise figure — 4dB typ.

high useful power gain —
neutralized — 17dB typ. } at 100MHz
unneutralized — 14dB typ. }

hermetically sealed TO-104 metal package

RCA-3N142 is intended primarily for use as the rf amplifier in FM receivers covering the 88 to 108MHz band, but can be used for general amplifier applications at frequencies up to 175 MHz.

The wide dynamic range of the 3N142 reduces cross-modulation effects in AM receivers and minimizes the generation of spurious responses in FM receivers.

• Formerly Dev. No. TA7306.

* Metal-Oxide-Semiconductor.

laximum Ratings, *Absolute-Maximum Values:*

RAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max. V
ATE-TO-SOURCE VOLTAGE, V_{GS}:	
Continuous	0 to −8 max. V
Instantaneous	±15 max. V
RAIN-TO-GATE VOLTAGE, V_{DG}	+20 max. V
RAIN CURRENT, I_D**	50 max. mA
RANSISTOR DISSIPATION, P_T:	
At ambient temperatures up to 85 °C	100 max. mW
At ambient temperatures above 85 °C	derate at 6.67mW/°C
MBIENT TEMPERATURE RANGE:	
Storage	−65 to +100 °C
Operating	−65 to +100 °C
EAD TEMPERATURE (During Soldering):	
At distances ≥1/32" from seating surface for 10 seconds max.	265 max. °C

* Pulse Value. Pulse duration, 20 ms max., Duty factor ≤ 0.1

3N142

ELECTRICAL CHARACTERISTICS, at T_A = 25° C Unless Otherwise Specified. Bulk (Substrate) Connected to Source

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS			UNIT
		FREQUENCY f	DC DRAIN-TO-SOURCE VOLTAGE V_{DS}	DC GATE-TO-SOURCE VOLTAGE V_{GS}	DC DRAIN CURRENT I_D	TYPE 3N142			
		MHz	V	V	mA	Min.	Typ.	Max.	
Drain-to-Source Cutoff Current	$I_{D}(off)$		20	−8		—	—	100	μA
Zero-Bias Drain Current*	I_{DSS}		15	0		5	20	50	mA
Gate Reverse Current	I_{GSS}	T_A = 25°C	0	−8		—	—	1	nA
		T_A = 100°C	0	−8		—	—	100	nA
Gate-to-Source Cutoff Voltage	$V_{GS}(off)$		20		0.05	−2	−5	−8	V
Small-Signal, Short-Circuit Reverse-Transfer Capacitance (Drain-to-Gate)	C_{rss}	1	15		5	—	0.12	0.2	pF
Input Resistance	r_{is}	100	15		5	2	4.5	—	KΩ
Input Capacitance	C_{iss}	1	15		5	—	5.5	10	pF
Output Resistance	r_{os}	100	15		5	2.25	4.2	—	KΩ
Output Capacitance	C_{oss}	100	15		5	—	1.4	—	pF
Forward Transconductance	g_{fs}	100	15		5	4	7.5	—	mmho
Maximum Available Power Gain	MAG	100	15		5	—	24	—	dB
Maximum Usable Power Gain (Unneutralized)	MUG	100	15		5	—	14	—	dB
Maximum Usable Power Gain (Neutralized)	MUG	100	15		5	15	17	—	dB
Noise Figure	NF	100	15		5	—	4	5	dB

* Pulse test: Pulse Duration 20 ms max. Duty Factor ≤0.15.

OPERATING CONSIDERATIONS

The flexible leads of the 3N142 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into, or dis connected from, circuits with the power on becaus high transient voltages may cause permanent dam age to the device.

TYPICAL CHARACTERISTICS

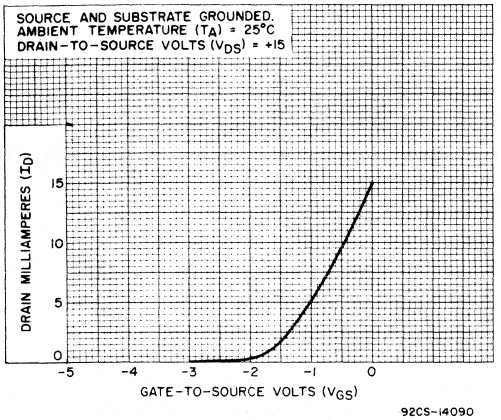


Fig. 1 – Typical Characteristic of Drain Current (I_D) vs Gate-to-Source Voltage (V_{GS})

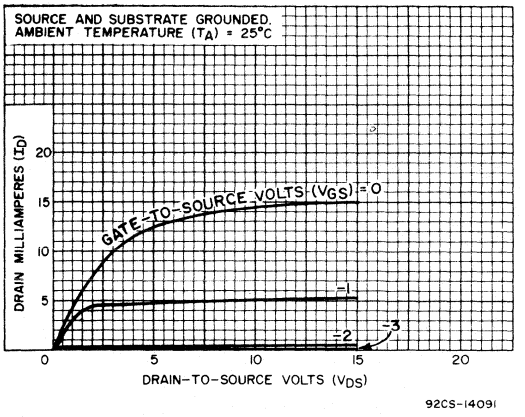


Fig. 2 – Drain Current (I_D) vs Drain-to-Source Voltage (V_{DS})

TYPICAL y PARAMETER CHARACTERISTICS

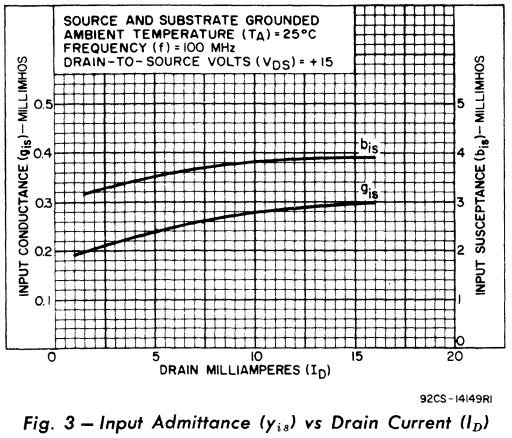


Fig. 3 – Input Admittance (y_{is}) vs Drain Current (I_D)

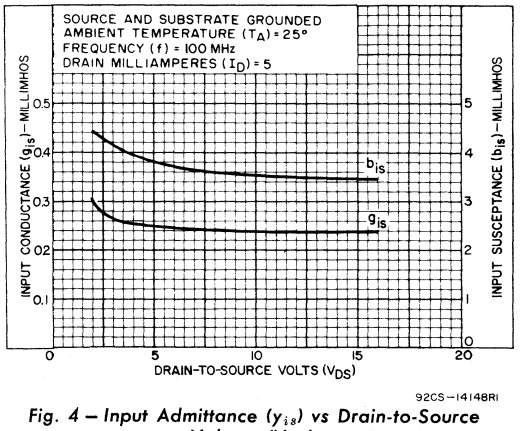


Fig. 4 – Input Admittance (y_{is}) vs Drain-to-Source Voltage (V_{DS})

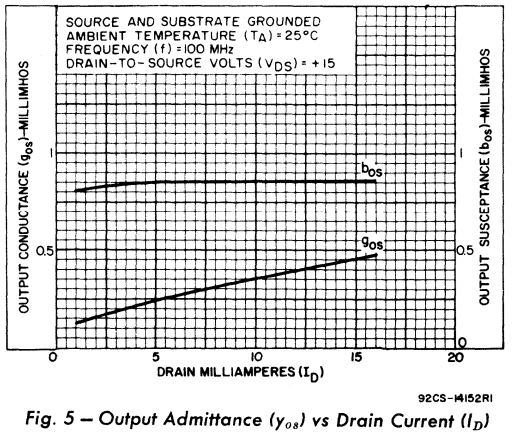


Fig. 5 – Output Admittance (y_{os}) vs Drain Current (I_D)

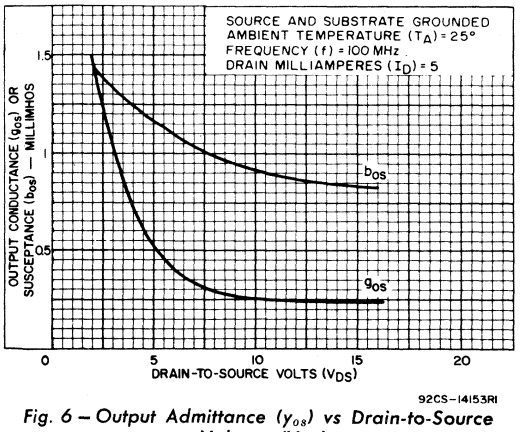


Fig. 6 – Output Admittance (y_{os}) vs Drain-to-Source Voltage (V_{DS})

3N142

TYPICAL y PARAMETER CHARACTERISTICS

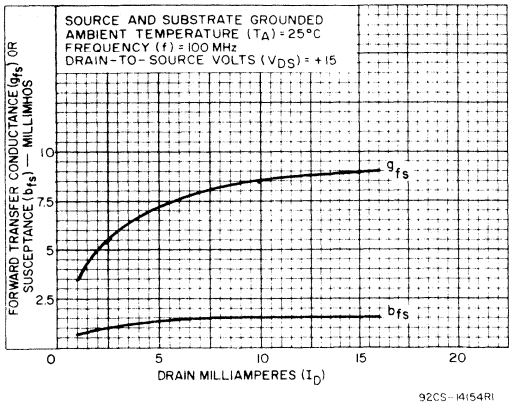


Fig. 7 – Forward Transadmittance (y_{fs}) vs Drain Current (I_D)

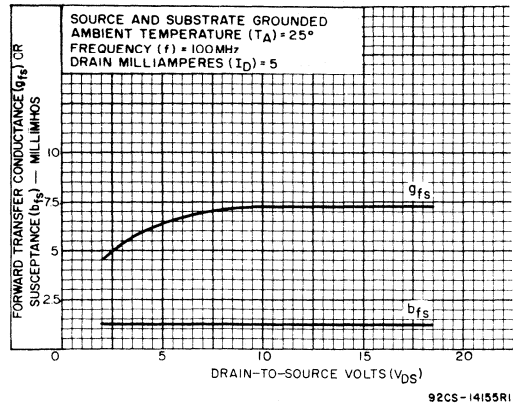


Fig. 8 – Forward Transadmittance (y_{fs}) vs Drain-to-Source Voltage (V_{DS})

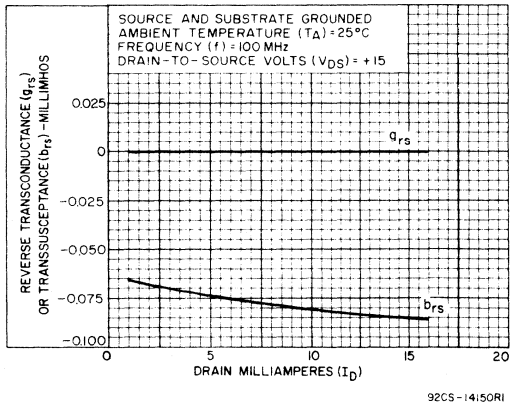


Fig. 9 – Reverse Transadmittance (y_{rs}) vs Drain Current (I_D)

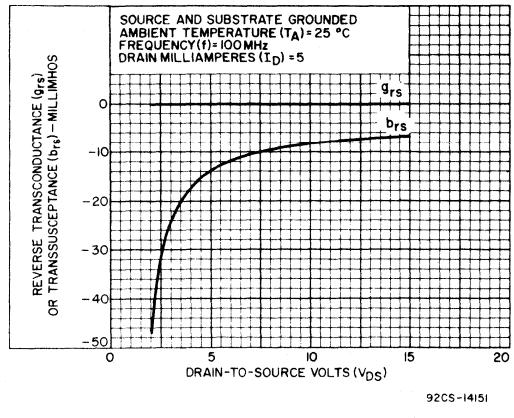


Fig. 10 – Reverse Transadmittance (y_{rs}) vs Drain-to-Source Voltage (V_{DS})

TYPICAL COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs FREQUENCY

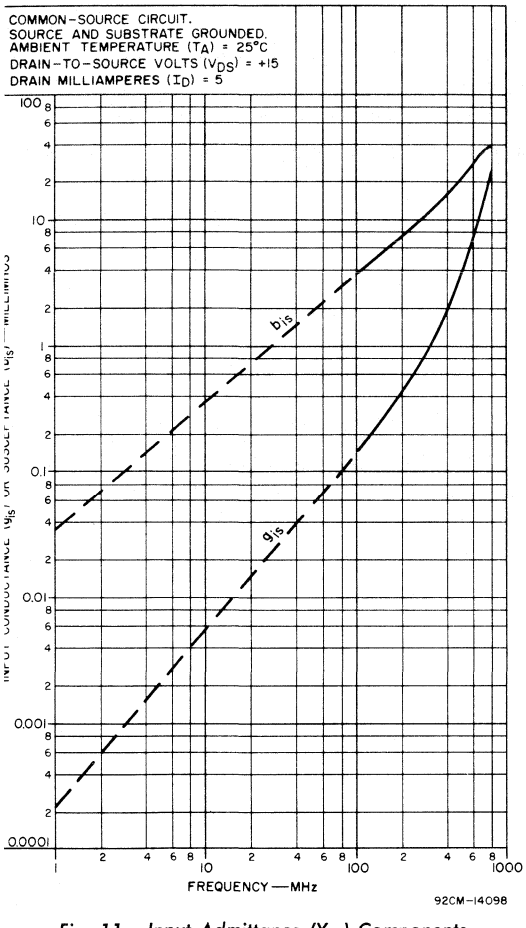


Fig. 11 – Input Admittance (Y_{is}) Components

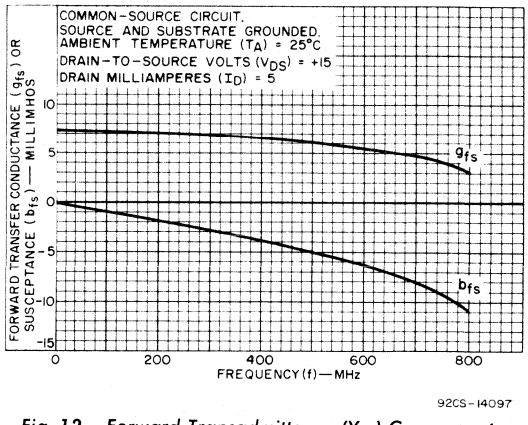


Fig. 12 – Forward Transadmittance (Y_{fs}) Components

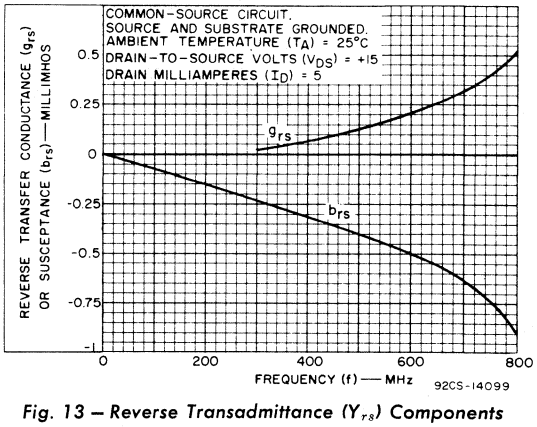
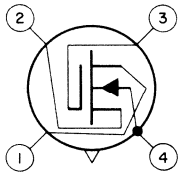


Fig. 13 – Reverse Transadmittance (Y_{rs}) Components

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - SOURCE
LEAD 3 - INSULATED GATE
LEAD 4 - BULK (SUBSTRATE) AND CASE

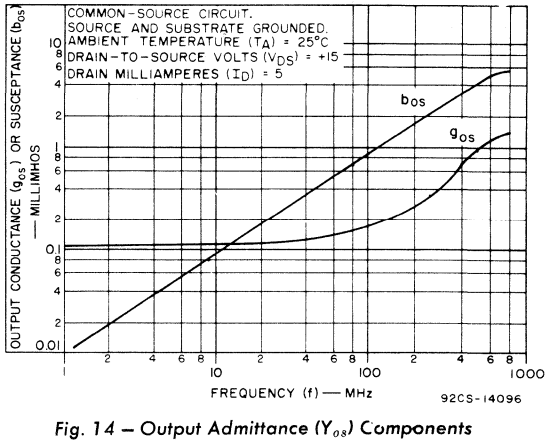


Fig. 14 – Output Admittance (Y_{os}) Components

3N152

Silicon MOS Transistor

For Low-Noise RF Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

Features:

- *Large dynamic range*
- *Greatly reduced spurious responses*
- *Permits use of vacuum-tube biasing techniques*
- *Excellent thermal stability*
- *Superior cross-modulation performance and greater dynamic range than bipolar transistors*

RCA 3N152• is an N-channel depletion-type silicon field-effect transistor utilizing the MOS construction. It is intended primarily for VHF amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N152 with the substrate in the reversed bias mode can provide substantially better cross-modulation performance in linear amplifier applications than conventional bipolar transistors. The insulated gate with its extremely low reverse (leakage) current eliminates the problem of diode-current loading of the input circuit under strong input conditions, which is common to junction-type FET's. These features in addition to low feedback capacitance permit the design of circuits providing superior high-frequency operation and high gain without neutralization. The 3N152 utilizes full-gate construction and is hermetically sealed in a JEDEC TO-72 metal package.

• Formerly Developmental No. TA7353.

Maximum Ratings, *Absolute-Maximum Values:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} ..... +20 max. V

GATE-TO-SOURCE VOLTAGE, V_{GS}:

Continuous (dc) ..... +1, −8 max. V

Peak ac ..... ±15 max. V

DRAIN CURRENT, I_D▲ ..... 50 max. mA

TRANSISTOR DISSIPATION:

At ambient temperatures up to 25 °C ..... 400 max. mW

above 25 °C ..... derate at 2.67 mW/°C

AMBIENT TEMPERATURE RANGE:

Storage ..... −65 to +175 °C

Operating ..... −65 to +175 °C

LEAD TEMPERATURE (During Soldering):

At distances not closer than 1/32 inch to seating surface for 10 seconds maximum ..... 265 max. °C

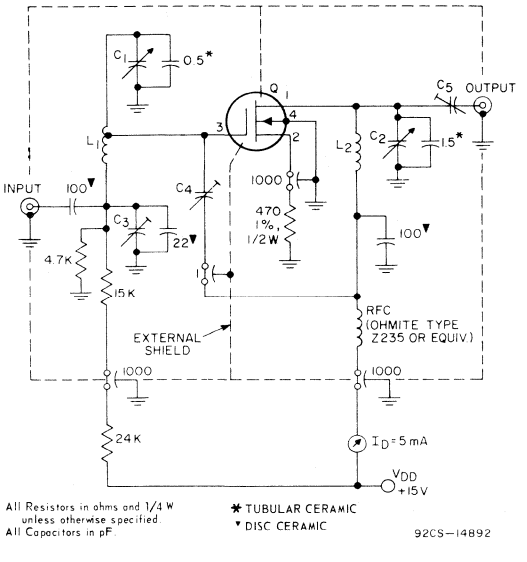
▲ Pulsed:
Pulse duration ≤ 20 ms
Duty factor ≤ 0.15

ELECTRICAL CHARACTERISTICS: (At T_A = 25°C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N152 Min.	Typ.	Max.	UNITS
Forward Transconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
Magnitude of Forward Transadmittance	$\|y_{fs}\|$	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	5000	–	–	μmho
Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25°C V_{DS} = 0, V_{GS} = -8 V, T_A = 85°C	– –	0.0001 –	1 10	nA nA
Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	–	5.5	7	pF
Small-Signal Short-Circuit Reverse Transfer Capacitance*	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	–	0.12	0.2	pF
Small-Signal Short-Circuit Output Capacitance	C_{oss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	–	1.4	–	pF
Drain-to-Source Channel Resistance	$r_{DS(on)}$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	–	200	–	Ω
Gate-to-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 50 μA	-2	-3.5	-8	V
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{DS} = 20 V, V_{GS} = -8 V	–	–	50	μA
Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	10	20	50	mA
Input Conductance	g_{is}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	–	450	–	μmho
Output Conductance	g_{os}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	–	300	–	μmho
Power Gain Maximum Available Gain Maximum Usable Gain (Neutralized) see Fig.1	G_{PS}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	16 14.5	20 16	– –	dB dB
Noise Figure (see Figs.1 & 2)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	–	2.5	3.5	dB

* Three-Terminal Measurement: Source Returned to Guard Terminal. ** Pulse Test: Pulse Duration ≤ 20 ms Duty Factor ≤ 0.15.



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - Test Circuit used to Measure 200-MHz Maximum Usable Power Gain and Noise Figure.

3N152

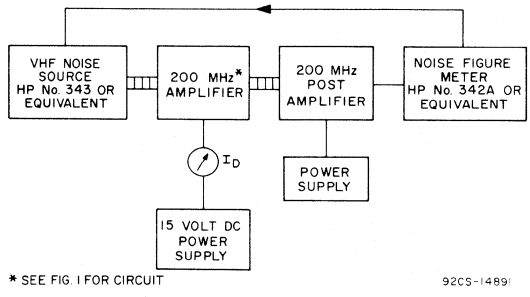


Fig.2 - Noise Figure Measurement Setup.

TYPICAL CHARACTERISTICS

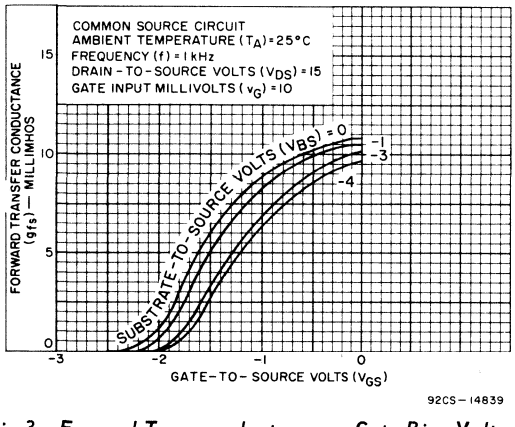


Fig.3 - Forward Transconductance vs Gate-Bias Voltage.

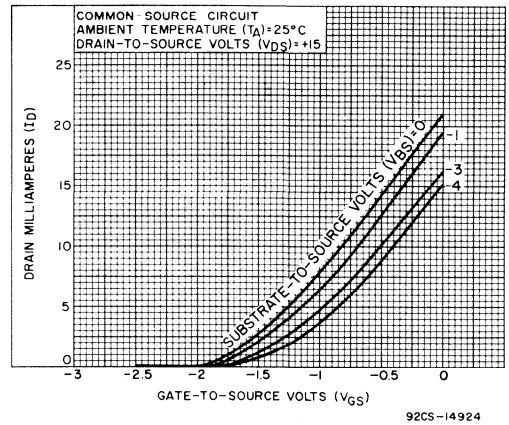


Fig.4 - Drain Current vs Gate-to-Source Voltage.

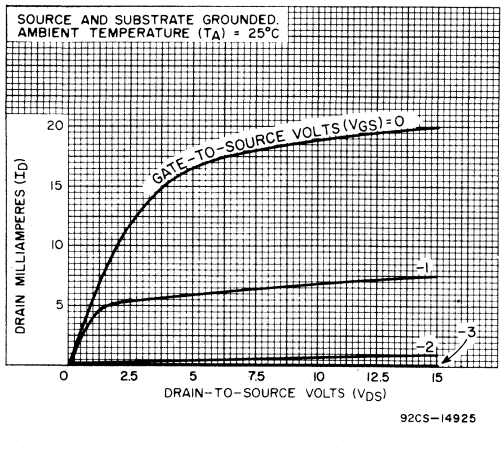


Fig.5 - Drain Current vs Drain-to-Source Voltage.

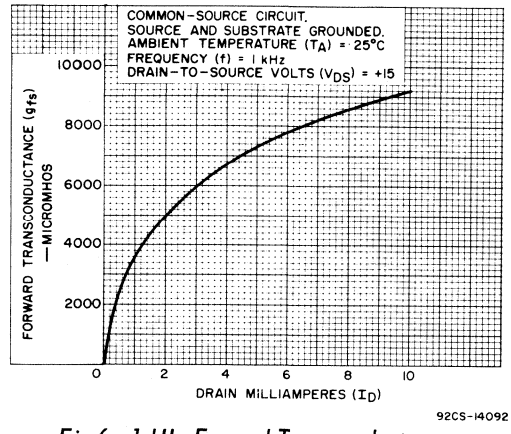


Fig.6 - 1-kHz Forward Transconductance vs Drain Current.

TYPICAL 200-MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs DRAIN CURRENT

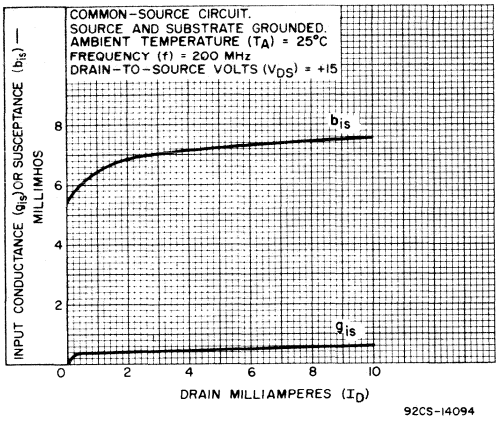


Fig.7 - Input Admittance (Y_{is}) Components.

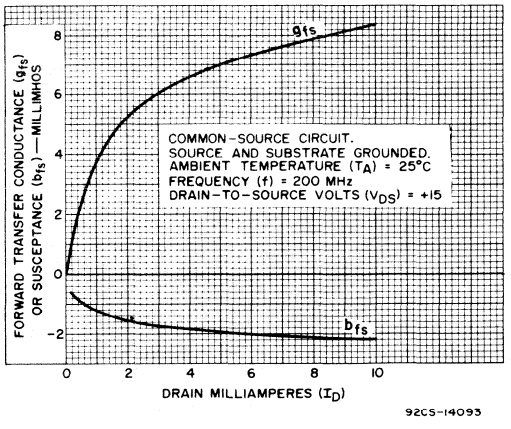


Fig.8 - Forward Transadmittance (Y_{fs}) Components.

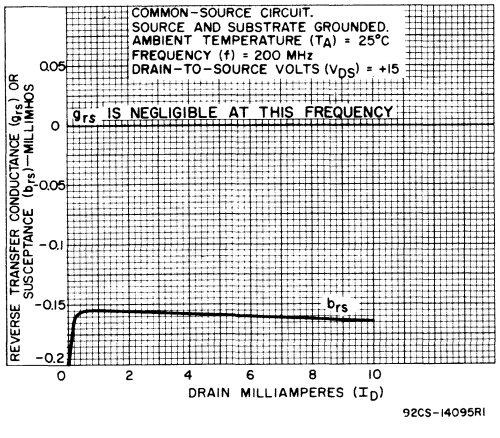


Fig.9 - Reverse Transadmittance (Y_{rs}) Components.

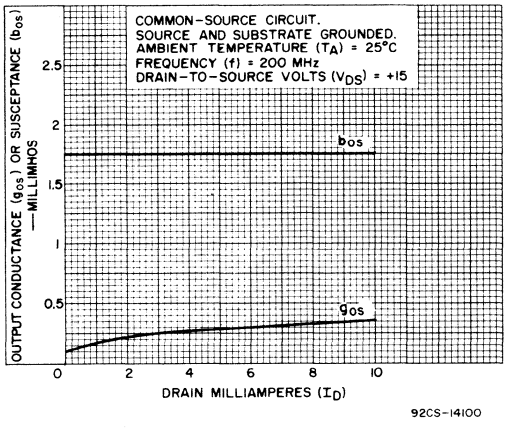
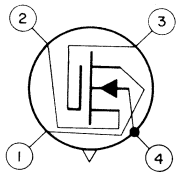


Fig.10 - Output Admittance (Y_{os}) Components.

3N152

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

OPERATING CONSIDERATIONS

The flexible leads of the 3N152 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

This device should not be connected into or dis connected from circuits with the power on because hig transient voltages may cause permanent damage t the devices.

3N153

;ilicon Insulated-Gate 'ield-Effect Transistor

or Chopper and Multiplex Service in Communications, avigation, and Instrumentation Equipment and in dustrial Control Circuits

eatures:

Excellent thermal stability
Virtually zero inherent offset voltage
Low leakage current: 50 pA max.
Low "on" resistance—$r_{DS(on)}$ = 200Ω typ.
High "off" resistance—$R_{DS(off)}$ = 10^{10}Ω typ.
Low feedback capacitance—C_{rss} = 0.34 pF typ.
Low input capacitance—C_{iss} = 6 pF typ.

Applications:

- *Choppers*
- *Multiplexers*
- *Servo Amplifiers*
- *Computer Operational Amplifiers*
- *Sampling Circuits*
- *Electrometer Amplifiers*

CA 3N153• is a silicon, insulated-gate field-effect transistor the N-channel depletion type, utilizing the MOS* construc- on. It is intended primarily for critical chopper and multiplex pplications up to 60 MHz.

he insulated gate provides a very high value of input esistance (10^{10} ohms typ.) which is relatively insensitive to mperature and is independent of gate-bias conditions positive, negative, or zero bias). The 3N153 also features ex- emely low feedback capacitance (0.34pF typ.) and virtually ero inherent offset voltage.

his transistor features a Terminal Arrangement in which the ate and source connections are interchanged to provide max- num isolation between the output (drain) and the input (gate) terminals. Although this new basing configuration does not appreciably change the measured device feedback capacitance, it permits the use of external inter-terminal shields to reduce the feedback due to external capacitances, particularly on printed circuit boards. This feature makes it possible to minimize feedthrough capacitance.

The 3N153 is hermetically sealed in the JEDEC TO-72 package and features a gate metallization that covers the entire source-to-drain channel.

• Formerly Dev. No. TA7352.

* Metal-Oxide-Semiconductor.

laximum Ratings, *Absolute-Maximum Values:*

(Substrate connected to source unless otherwise specified)

RAIN-TO-SOURCE VOLTAGE, V_{DS}	+20 max. V
RAIN-TO-SUBSTRATE VOLTAGE, V_{DB}	+20, −0.3 max. V
OURCE-TO-SUBSTRATE VOLTAGE, V_{SB}	+20, −0.3 max. V
C GATE-TO-SOURCE VOLTAGE, V_{GS}	+6, −8 max. V
EAK GATE-TO-SOURCE VOLTAGE, V_{GS}	±14 max. V
RAIN CURRENT, I_D (Pulse duration 20 ms, duty factor ≤ 0.10)	50 max. mA
RANSISTOR DISSIPATION, P_T:	
At ambient temperatures	
from −65 to +25 °C	400 max. mW
above 25 °C	derate linearly at 2.67 mW/°C
MBIENT TEMPERATURE RANGE:	
Storage	−65 to +175 °C
Operating	−65 to +175 °C
EAD TEMPERATURE	
(During soldering):	
At distance ≥ 1/32" to seating surface for 10 seconds max.	265 max. °C

3N153

ELECTRICAL CHARACTERISTICS, at T_A = 25° C, Unless Otherwise Specified. Substrate Connected to Source.

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS Type 3N153			UNITS
			Min.	Typ.	Max.	
Gate-Leakage Current	I_{GSS}	V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 25°C V_{GS} = +6,-8V; V_{DS} = 0V; T_A = 125°C	- -	0.1 -	50 1	pA nA
Static Drain-to-Source "ON" Resistance	$r_{DS(on)}$	V_{GS} = 0V, V_{DS} = 0V	-	200	300	Ω
Drain-to-Source "OFF" Resistance	$R_{DS(off)}$	V_{GS} = -8V, V_{DS} = +1V	10^9	10^{10}	-	Ω
Drain-to-Source Cutoff Current	$I_{D(off)}$	V_{GS} = -8V, V_{DS} = +1V, T_A = 25°C V_{GS} = -8V, V_{DS} = +1V, T_A = 125°C	- -	0.1 0.1	1 1	nA μA
Small-Signal, Short-Circuit, Reverse Transfer Capacitance	C_{rss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz V_{DS} = 15V, I_D = 5 mA, f = 1 MHz	- -	0.34 0.12	0.5 0.2	pF pF
Small-Signal, Short-Circuit, Input Capacitance	C_{iss}	V_{GS} = -8V, V_{DS} = 0V, f = 1 MHz	-	6	8	pF
Small-Signal, Drain-to-Source Capacitance	C_{ds}	V_{DS} = 0V, V_{GS} = -8V, f = 1 MHz	-	-	3	pF
Zero-Gate-Bias Forward Transconductance	g_{fs}	V_{GS} = 0V, V_{DS} = +15V	-	10,000	-	μmho
Offset Voltage	V_0	V_{GS} = +6,-8V; V_{DS} = 0V	-	0*	-	V

* In measurements of Offset Voltage, thermocouple effects and contact potentials in the measurement setup may cause erroneous readings 1 microvolt or more. These errors may be minimized by the use of solder having a low thermal e.m.f., such as Leeds & Northrup No.107-1.0. or equivalent.

OPERATING CONSIDERATIONS

The flexible leads of the 3N153 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the device against high electric fields.

This device should not be connected into or dis connected from circuits with the power on becaus high transient voltages may cause permanent damag to the device.

TYPICAL CHARACTERISTICS

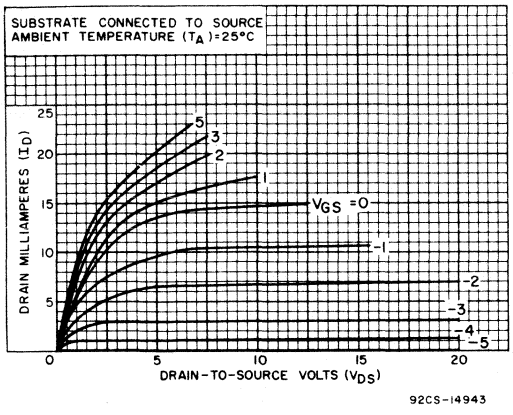


Fig.1 - Drain current vs. drain-to-source voltage.

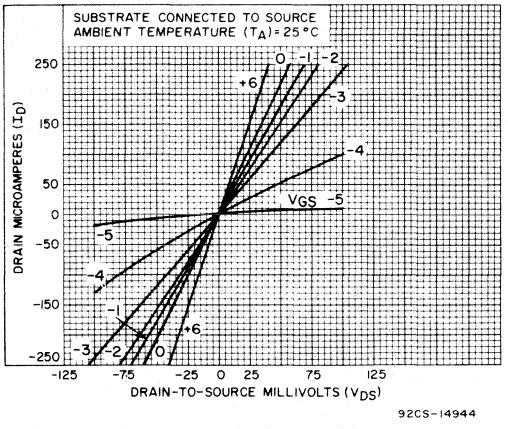


Fig.2 - Low-level drain current vs. drain-to-source voltage.

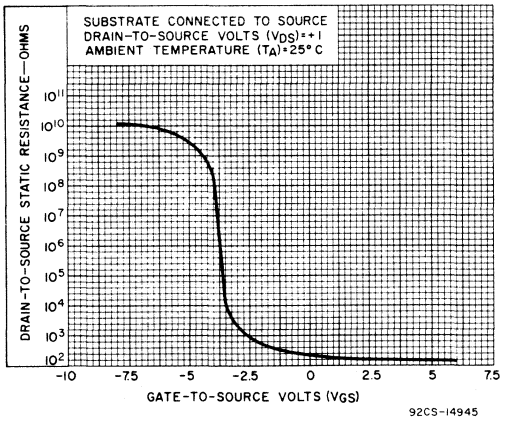
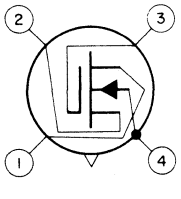


Fig.3 - Drain-to-source static resistance vs. gate-to-source voltage.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

3N154

Silicon MOS Transistor

For Critical Amplifier Applications in Military & Industrial VHF Communications Equipment Operating up to 250 MHz

Features:

- *Large dynamic range*
- *Greatly reduced spurious responses*
- *Permits use of vacuum-tube biasing techniques*
- *Excellent thermal stability*
- *Superior cross-modulation performance and greater dynamic range than bipolar transistors*

RCA 3N154• is an n-channel depletion-type silicon field-effect transistor utilizing the MOS construction. It is intended primarily for vhf amplifier applications up to 250 MHz in military and industrial equipment.

Because of its improved transfer characteristic and exceptionally wide dynamic range, the 3N154 can provide substantially better crossmodulation performance in linear amplifier applications than conventional bipolar transistors. The extremely low gate leakage current eliminates diode-current loading of the input circuit under strong input conditions, a p blem which is common to junction-type FET's. These featur in addition to low feedback capacitance, permit the desigr circuits providing superior high-frequency operation and h gain without neutralization. The 3N154 utilizes full-gate c struction and is hermetically sealed in a JEDEC TO-72 me package.

• Formerly Developmental No.TA7375.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°:*

DRAIN-TO-SOURCE VOLTAGE, V_{DS} ..... +2

GATE-TO-SOURCE VOLTAGE, V_{GS}:

Continuous (dc) ..... +1, −

Peak ac ..... ±1

DRAIN-TO-GATE VOLTAGE, V_{DG} 2

DRAIN CURRENT, I_D▲ 50

TRANSISTOR DISSIPATION:

At ambient temperatures { up to 25 °C ..... 400 r; above 25 °C ..... derate at 2.67 mW

AMBIENT TEMPERATURE RANGE:

Storage ..... −65 to +17

Operating ..... −65 to +17

LEAD TEMPERATURE (During Soldering):

At distances not closer than 1/32 inch to seating surface for 10 seconds maximum 26

▲Pulsed:

Pulse duration ≤ 20 ms

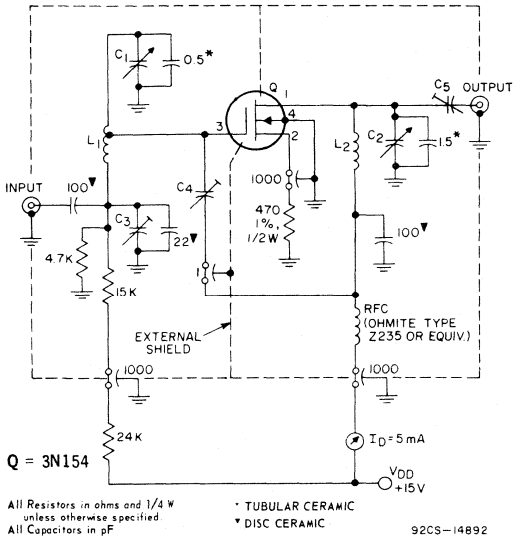
Duty factor ≤ 0.15

ELECTRICAL CHARACTERISTICS: (At T_A = 25° C)

Measured with Substrate Connected to Source Unless Otherwise Specified.

CHARACTERISTICS	SYMBOLS	CONDITIONS	LIMITS 3N154 Min.	LIMITS 3N154 Typ.	LIMITS 3N154 Max.	UNITS
Gate-to-Source Cutoff Voltage	$V_{GS}(off)$	V_{DS} = 15 V, I_D = 50 μA	-2	-3.5	-8	V
Drain-to-Source Cutoff Current	$I_D(off)$	V_{DS} = 20 V, V_{GS} = -8 V	-	-	50	μA
Zero-Bias Drain Current**	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0	10	15	25	mA
Gate Leakage Current	I_{GSS}	V_{DS} = 0, V_{GS} = -8 V, T_A = 25° C V_{DS} = 0, V_{GS} = -8 V, T_A = 125° C V_{DS} = 0, V_{GS} = +1, T_A = 25° C V_{DS} = 0, V_{GS} = +1, T_A = 125° C	- - - -	0.0001 - 0.0001 -	0.05 5 0.05 5	nA nA nA nA
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	5000	7500	-	μmho
Forward Transsconductance	g_{fs}	V_{DS} = 15 V, I_D = 5 mA, f = 1 kHz	5000	7500	12,000	μmho
Small-Signal Short-Circuit Input Capacitance	C_{iss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	5.5	7	pF
Small-Signal Short-Circuit Reverse Transfer Capacitance*	C_{rss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	0.03	0.12	0.2	pF
Small-Signal Short-Circuit Output Capacitance	C_{oss}	V_{DS} = 15 V, I_D = 5 mA, f = 0.1 to 1 MHz	-	1.4	-	pF
Gate Leakage Current Resistance	R_{GS}	V_{DS} = 0, V_{GS} = -8 V	-	10^{14}	-	Ω
Drain-to-Source Channel Resistance	$r_{DS}(on)$	V_{DS} = 0, V_{GS} = 0, f = 1 kHz	-	200	-	Ω
Input Conductance	g_{is}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	500	-	μmho
Output Conductance	g_{os}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	275	-	μmho
Power Gain	G_{PS}	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	20	-	dB
Maximum Available Gain Maximum Usable Gain (Neutralized) see Fig.1			13.5	16	-	dB
Noise Figure (see Figs.1 & 10)	NF	V_{DS} = 15 V, I_D = 5 mA, f = 200 MHz	-	3.5	5	dB

* Three-Terminal Measurement: Source Returned to Guard Terminal ** Pulse Test: Pulse Duration ≤ 20 ms Duty Factor ≤ 0.15.



C_1, C_2: 1.5-5 pF variable air capacitor: E. F. Johnson Type 160-102 or equivalent

C_3: 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent

C_4, C_5: 0.3-3 pF piston-type variable air capacitor: Roanwell Type MH-13 or equivalent

Q = 3N154

L_1: 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C_1 end of winding

L_2: Same as L_1 except winding length approx. 0.7"; no tap.

Fig.1 - Test Circuit used to Measure 200-MHz Maximum Usable Power Gain and Noise Figure.

3N154

TYPICAL CHARACTERISTICS

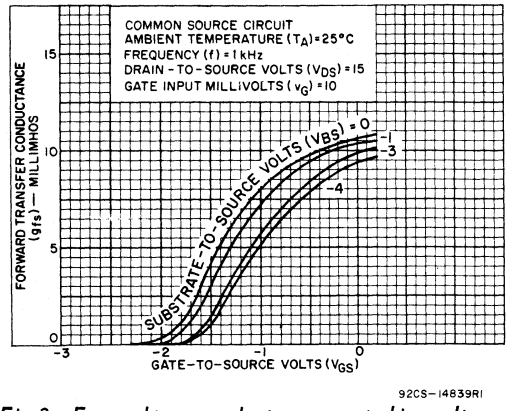


Fig.2 - Forward transconductance vs gate-bias voltage.

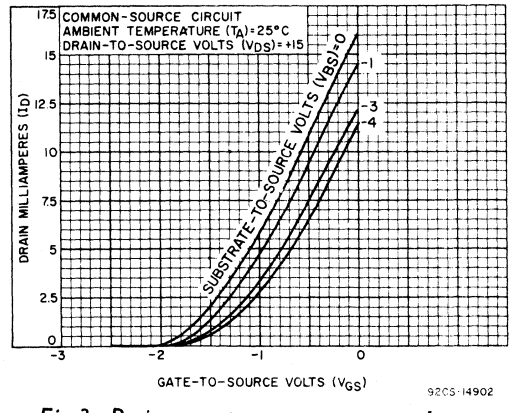


Fig.3 - Drain current vs gate-to-source voltage.

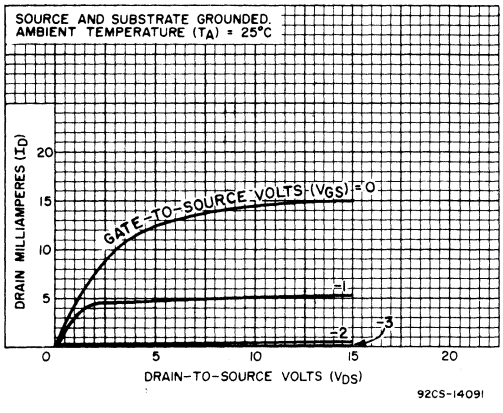


Fig.4 - Drain current vs drain-to-source voltage.

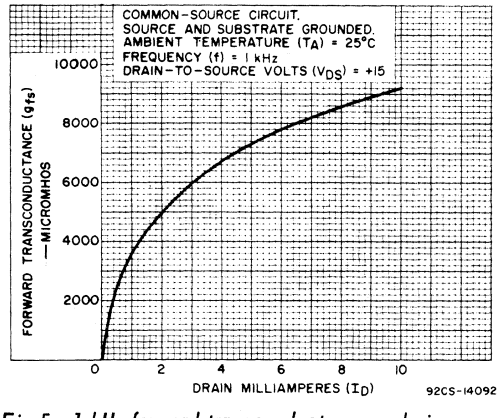


Fig.5 - 1-kHz forward transconductance vs drain current.

TYPICAL 200-MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs DRAIN CURRENT

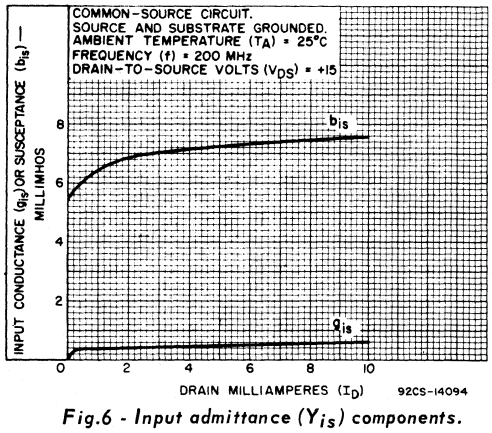


Fig.6 - Input admittance (Y_{is}) components.

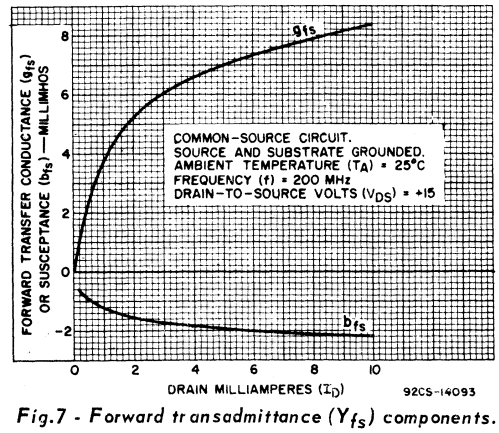


Fig.7 - Forward transadmittance (Y_{fs}) components.

TYPICAL 200-MHz COMMON-SOURCE ADMITTANCE (Y) COMPONENTS vs DRAIN CURRENT

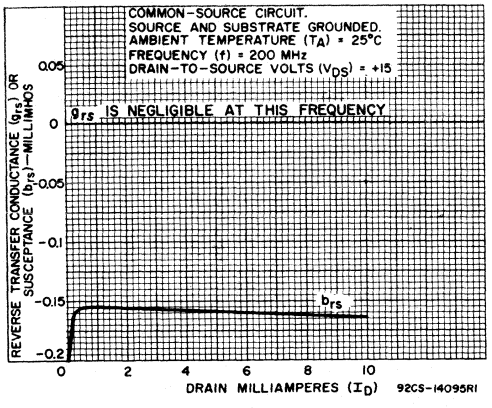


Fig.8 - Reverse transadmittance (Y_{rs}) components.

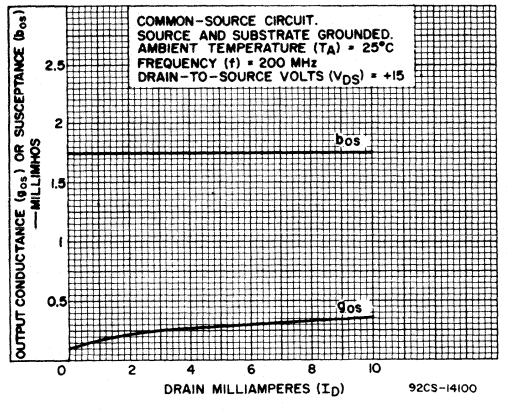


Fig.9 - Output admittance (Y_{os}) components.

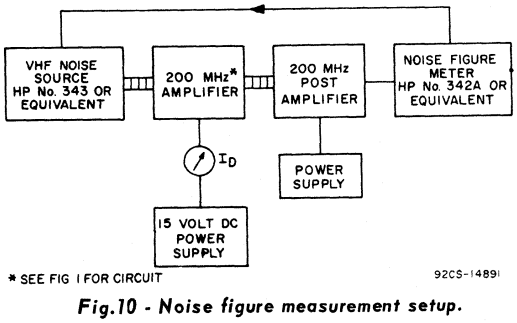
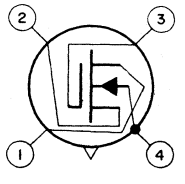


Fig.10 - Noise figure measurement setup.

TERMINAL DIAGRAM



1 - Drain
2 - Source
3 - Insulated Gate
4 - Bulk (Substrate) and Case

OPERATING CONSIDERATIONS

The flexible leads of the 3N154 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons should be grounded, and appropriate precautions should be taken to protect the devices against high electric fields.

This device should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the device.

3N187

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 300 MHz

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 12,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 18 dB(typ.) at 200 MHz
- Low VHF noise figure — 3.5 dB(typ.) at 200 MHz

RCA-3N187● is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N187 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N187 make it useful for a wide variety of rf-amplifier applications at frequencies up to 300 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N187 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N187 is hermetically sealed in the metal JEDEC TO-72 package.

● Formerly developmental type TA7669
▲ Metal-Oxide-Semiconductor

Applications

- RF amplifier, mixer, and IF amplifier in military, and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET's
- Wide dynamic range permits large-signal handling before overload
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Maximum Ratings,

Absolute-Maximum Values, at T_A = 25°C

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No. 1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No. 2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
* LEAD TEMPERATURE (During Soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

3N187

ELECTRICAL CHARACTERISTICS, at T_A = 25° C unless otherwise specified

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G2S} = +4 V		-0.5	-2	-4	V
Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA V_{G1S} = 0		-0.5	-2	-4	V
Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V V_{G2S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V V_{G2S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V V_{G1S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V V_{G1S} = V_{DS} = 0	T_A = 25° C T_A = 100° C	– –	– –	50 5	nA μA
Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V V_{G2S} = +4 V V_{G1S} = 0		5	15	30	mA
Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 kHz		7000	12,000	18,000	μmho
Small-Signal, Short-Circuit Input Capacitance†	C_{iss}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 1 MHz		4.0	6.0	8.5	pF
Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
Small-Signal, Short-Circuit Output Capacitanc	C_{oss}			–	2.0	–	pF
Power Gain (see Fig. 1)	G_{PS}	V_{DS} = +15 V, I_D = 10 mA V_{G2S} = +4 V, f = 200 MHz		16	18	22	dB
Maximum Available Power Gain	MAG			–	20	–	dB
Maximum Usable Power Gain (unneutralized)	MUG			–	20▲	–	dB
Noise Figure (see Fig. 1)	NF			–	3.5	4.5	dB
Magnitude of Forward Transadmittance	$\|Y_{fs}\|$			–	12,000	–	μmho
Phase Angle of Forward Transadmittance	θ			–	-35	–	Degrees
Magnitude of Reverse Transadmittance	$\|Y_{rs}\|$			–	25	–	μmho
Angle of Reverse Transadmittance	θ_{rs}			–	-25	–	Degrees
Input Resistance	r_{iss}			–	1.0	–	kΩ
Output Resistance	r_{oss}			–	2.8	–	kΩ
Gate-to-Source Forward Breakdown Voltage: Gate No. 1 Gate No. 2	$V_{(BR)G1SSF}$ $V_{(BR)G2SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA		6.5	10	–	V
Gate-to-Source Reverse Breakdown Voltage: Gate No. 1 Gate No. 2	$V_{(BR)G1SSR}$ $V_{(BR)G2SSR}$	I_{G1SSR} = I_{G2SSR} = -100 μA		-6.5	-10	–	V

▲ Limited only by practical design considerations.

† Capacitance between Gate No. 1 and all other terminals

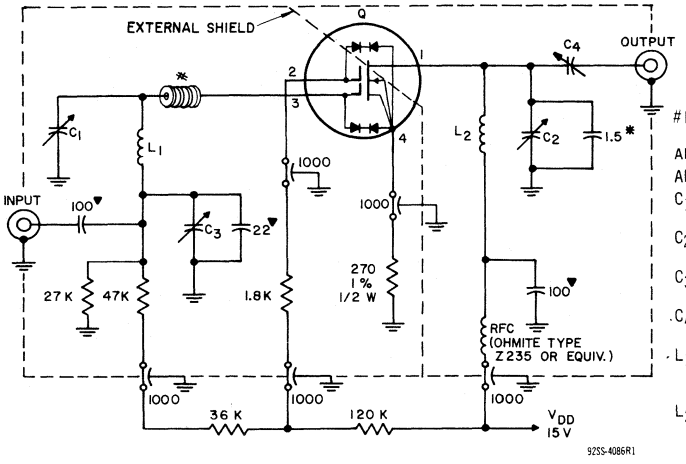
♦ Three-terminal measurement with Gate No. 2 and Source returned to ground terminal.

* In accordance with JEDEC Registration Data Format JS-9 RDF-19A

OPERATING CONSIDERATIONS

The flexible leads of the 3N187 are usually soldered to th circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

3N187



Ferrite bead (4); Pyroferric Co. "Carbonyl J" 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness. Q = 3N187 ▼ Disc ceramic. * Tubular ceramic.

All resistors in ohms

All capacitors in pF

C_1: 1.8–8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.

C_2: 1.5–5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.

C_3: 1–10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent.

C_4: 0.8–4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.

L_1: 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon. Internal diameter of winding = 0.25 in, winding length approx. 0.08 in.

L_2: 4½ turns silver-plated 0.02-in thick, 0.085-0.095-in. wide, 5/16-in. ID. Coil ≈.90 in. long.

Fig. 1 - 200 MHz Power gain and noise figure test circuit

Typical Characteristics

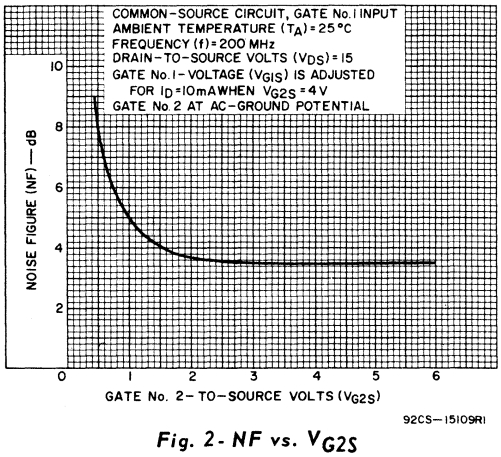


Fig. 2 - NF vs. V_{G2S}

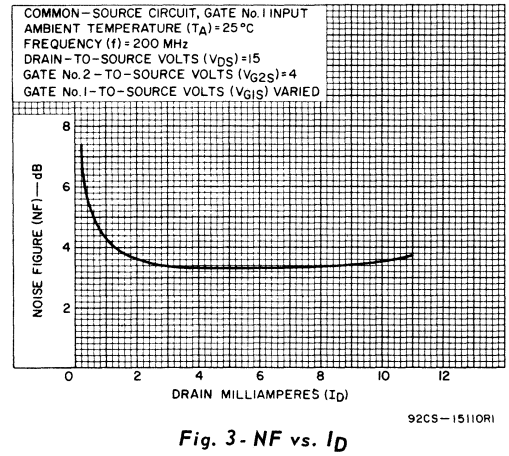


Fig. 3 - NF vs. I_D

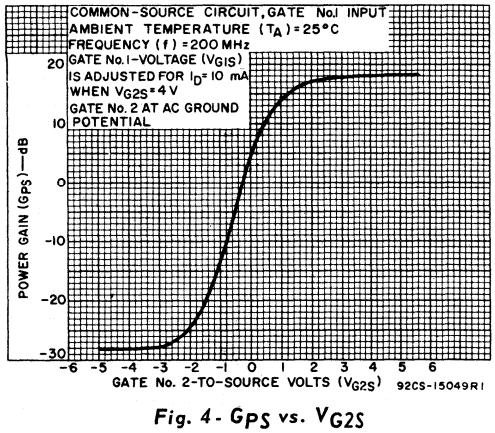


Fig. 4 - G_{PS} vs. V_{G2S}

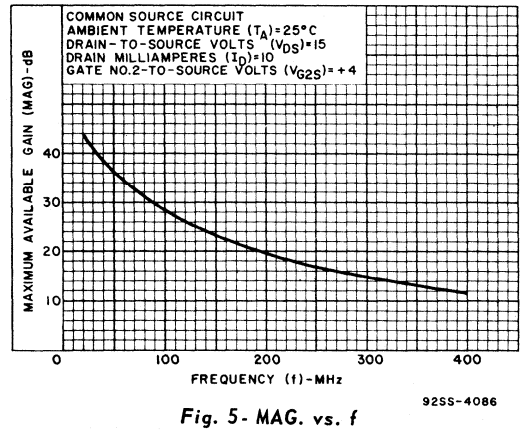


Fig. 5 - MAG. vs. f

Typical Characteristics

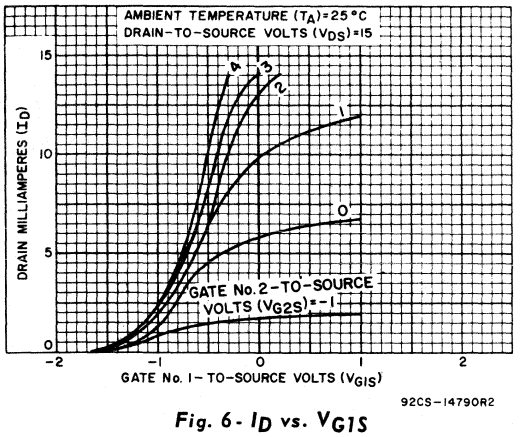


Fig. 6 - I_D vs. V_{G1S}

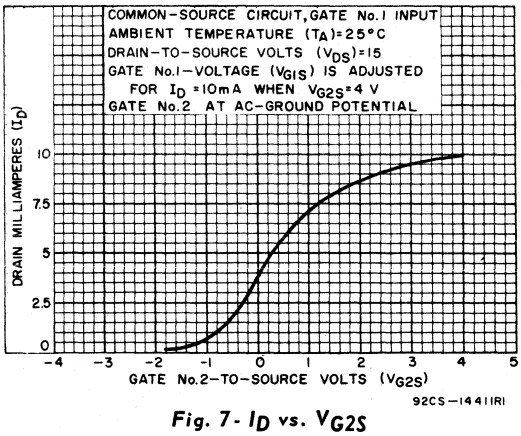


Fig. 7 - I_D vs. V_{G2S}

Typical y Parameters vs. V_{DS}

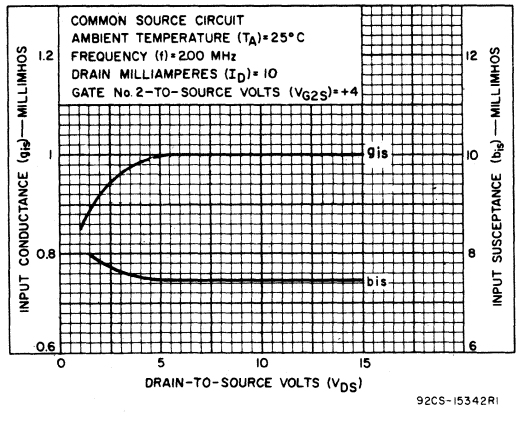


Fig. 8 - y_{is} vs. V_{DS}

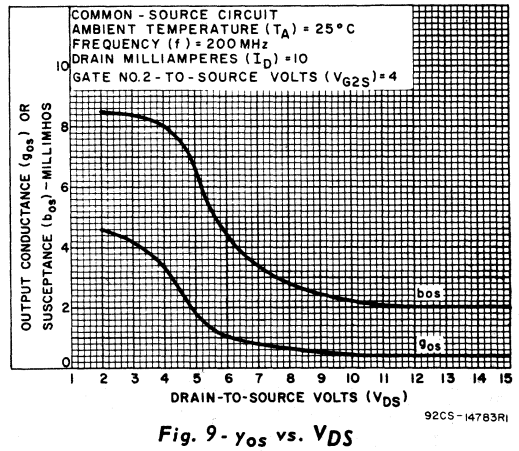


Fig. 9 - y_{os} vs. V_{DS}

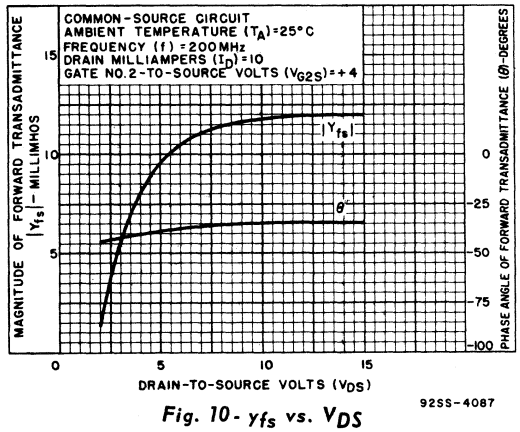


Fig. 10 - y_{fs} vs. V_{DS}

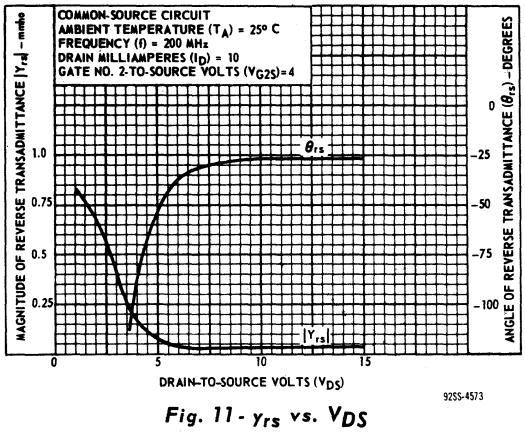


Fig. 11 - y_{rs} vs. V_{DS}

3N187

Typical y Parameters vs. I_D

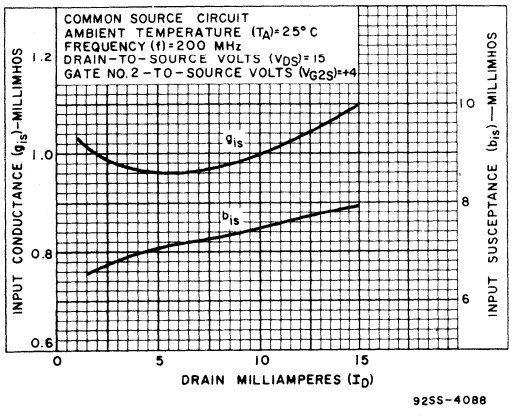


Fig. 12 - y_{is} vs. I_D

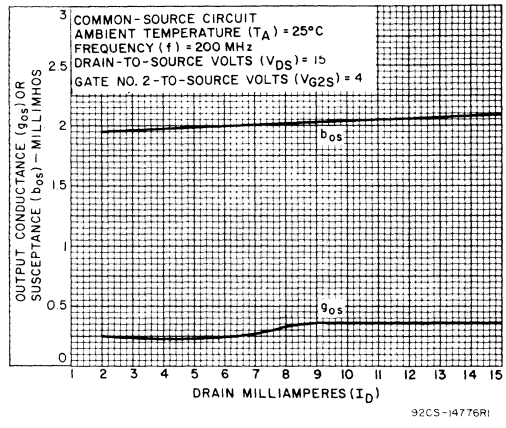


Fig. 13 - y_{os} vs. I_D

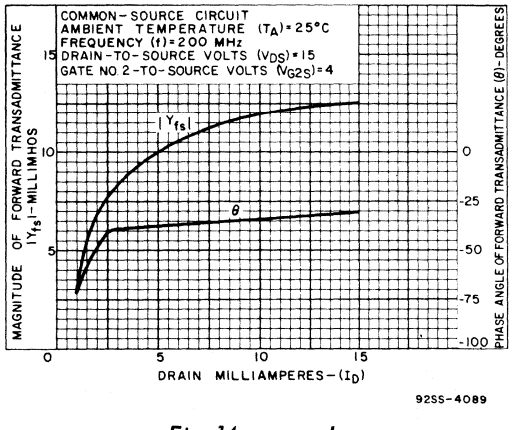


Fig. 14 - y_{fs} vs. I_D

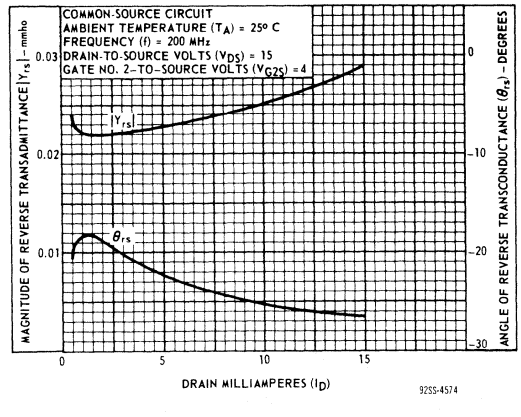


Fig. 15 - y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}

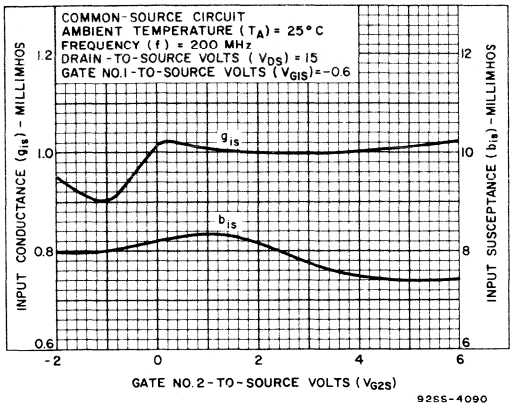


Fig. 16 - y_{is} vs. V_{G2S}

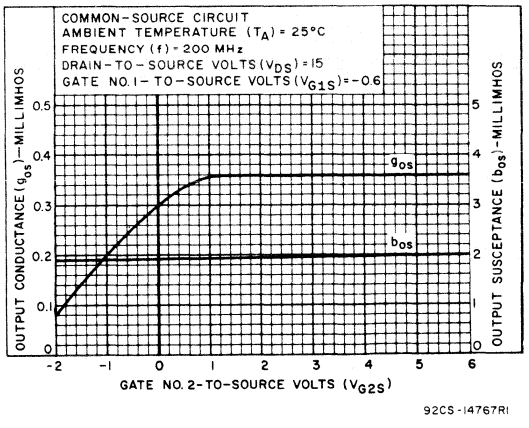


Fig. 17 - y_{os} vs. V_{G2S}

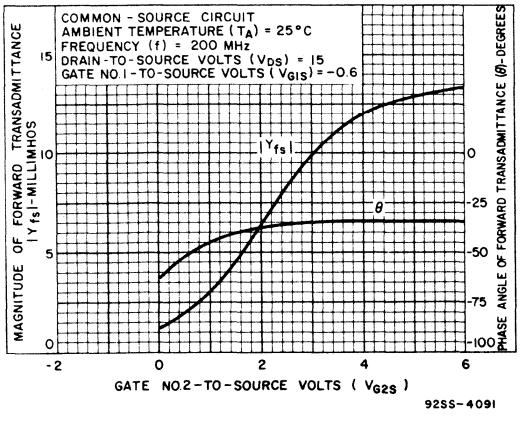


Fig. 18 - y_{fs} vs. V_{G2S}

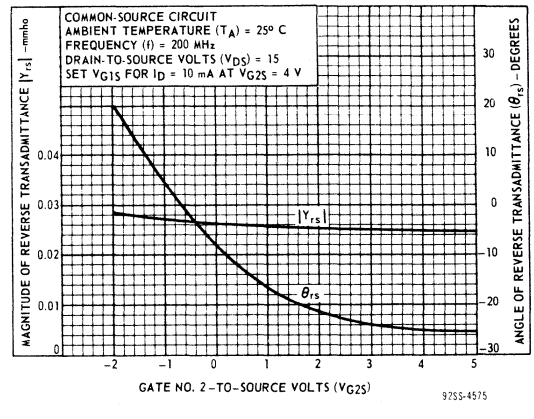


Fig. 19 - y_{rs} vs. V_{G2S}

3N187

Typical y Parameters vs. Frequency

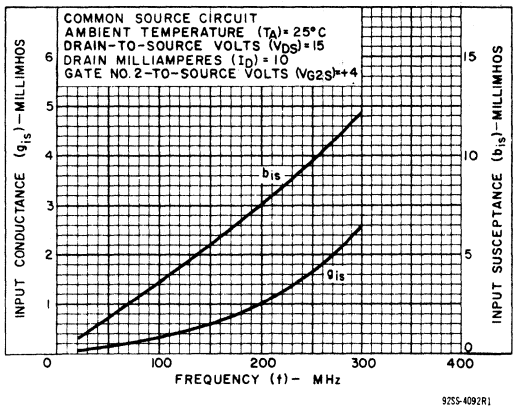


Fig. 20 - y_{is} vs. frequency

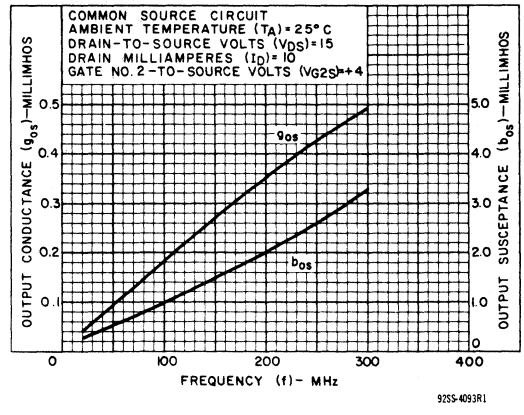


Fig. 21 - y_{os} vs. frequency

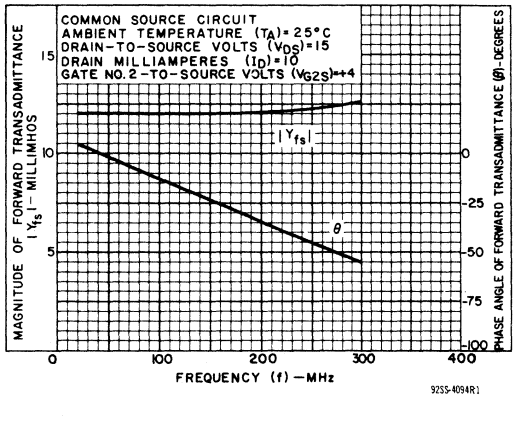


Fig. 22 - y_{fs} vs. frequency

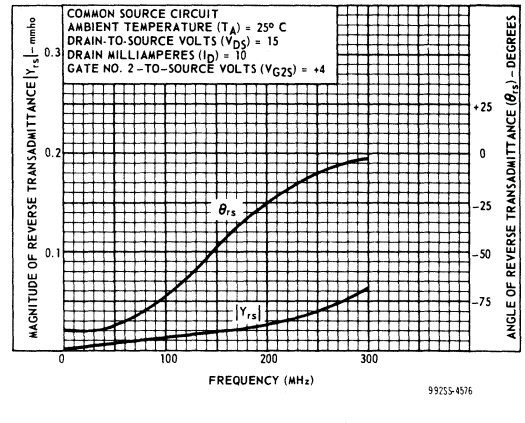


Fig. 23. - y_{rs} vs. frequency

3N187

Typical Characteristics

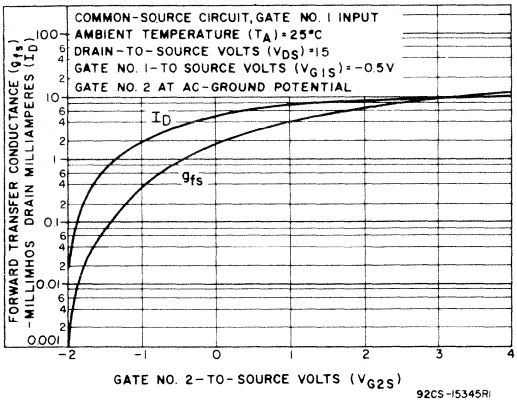


Fig. 24 - g_{fs} and I_D vs. V_{G2S}

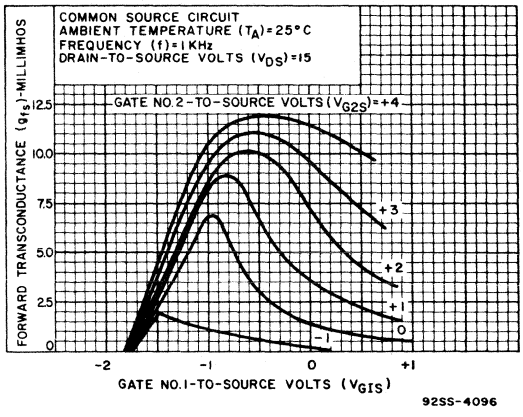


Fig. 25. - g_{fs} vs. V_{G1S}

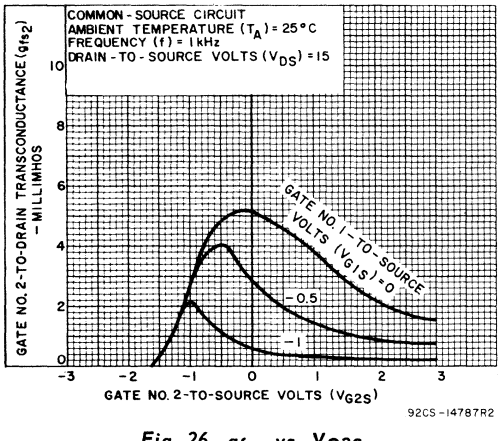
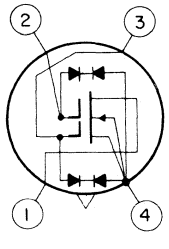


Fig. 26 - g_{fs_2} vs. V_{G2S}

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

3N200

Silicon Dual Insulated-Gate Field-Effect Transistor

With Integrated Gate-Protection Circuits

For Military and Industrial Applications up to 500 MHz

Applications

- RF amplifier, mixer, and IF amplifier in military and industrial communications equipment
- Aircraft and marine vehicular receivers
- CATV and MATV equipment
- Telemetry and multiplex equipment

RCA-3N200♦ is an n-channel silicon, depletion type, dual insulated-gate field-effect transistor.

Special back-to-back diodes are diffused directly into the MOS▲ pellet and are electrically connected between each insulated gate and the FET's source. The diodes effectively bypass any voltage transients which exceed approximately ±10 volts. This protects the gates against damage in all normal handling and usage.

A feature of the back-to-back diode configuration is that it allows the 3N200 to retain the wide input signal dynamic range inherent in the MOSFET. In addition, the low junction capacitance of these diodes adds little to the total capacitance shunting the signal gate.

The excellent overall performance characteristics of the RCA-3N200 make it useful for a wide variety of rf-amplifier applications at frequencies up to 500 MHz. The two serially-connected channels with independent control gates make possible a greater dynamic range and lower cross-modulation than is normally achieved using devices having only a single control element.

The two-gate arrangement of the 3N200 also makes possible a desirable reduction in feedback capacitance by operating in the common-source configuration and ac-grounding Gate No. 2. The reduced capacitance allows operation at maximum gain *without neutralization;* and, of special importance in rf-amplifiers, it reduces local oscillator feedthrough to the antenna.

The 3N200 is hermetically sealed in the metal JEDEC TO-72 package.

Maximum Ratings, *Absolute-Maximum Values, at* $T_A = 25^oC$

DRAIN-TO-SOURCE VOLTAGE, V_{DS}	-0.2 to +20	V
GATE No.1-TO-SOURCE VOLTAGE, V_{G1S}:		
Continuous (dc)	-6 to +3	V
Peak ac	-6 to +6	V
GATE No.2-TO-SOURCE VOLTAGE, V_{G2S}:		
Continuous (dc)	-6 to 30% of V_{DS}	V
Peak ac	-6 to +6	V
* DRAIN-TO-GATE VOLTAGE, V_{DG1} OR V_{DG2}	+20	V
* DRAIN CURRENT, I_D	50	mA
* TRANSISTOR DISSIPATION, P_T:		
At ambient temperatures up to 25°C	330	mW
At ambient temperatures above 25°C	derate linearly at 2.2 mW/°C	
* AMBIENT TEMPERATURE RANGE:		
Storage and Operating	-65 to +175	°C
LEAD TEMPERATURE (During soldering):		
At distances ≥ 1/32 inch from seating surface for 10 seconds max.	265	°C

*In accordance with JEDEC registration data format (JS-9 RDF-19A)

▲ Metal-Oxide-Semiconductor.
♦ Formerly developmental type TA7684

Performance Features

- Superior cross-modulation performance and greater dynamic range than bipolar or single-gate FET s
- Wide dynamic range permits large-signal handling before overload
- Dual-gate permits simplified agc circuitry
- Virtually no agc power required
- Greatly reduces spurious responses in FM receivers

Device Features

- Back-to-back diodes protect each gate against handling and in-circuit transients
- High forward transconductance — g_{fs} = 15,000 μmho (typ.)
- High unneutralized RF power gain — G_{ps} = 12.5 dB (typ.) at 400 MHz = 19 dB (typ.) at 200 MHz
- Low VHF noise figure — 3.9 dB (typ.) at 400 MHz 3.0 dB (typ.) at 200 MHz

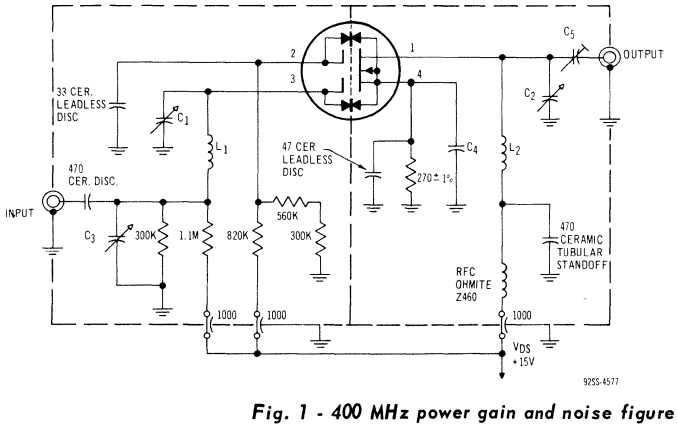
3N200

	ELECTRICAL CHARACTERISTICS at T_A = 25°C unless otherwise specified	SYMBOLS	TEST CONDITIONS		LIMITS Min.	Typ.	Max.	UNITS
*	Gate No. 1-to-Source Cutoff Voltage	$V_{G1S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G2S} = +4 V		-0.1	-1	-3	V
*	Gate No. 2-to-Source Cutoff Voltage	$V_{G2S(off)}$	V_{DS} = +15 V, I_D = 50 μA, V_{G1S} = 0		-0.1	-1	-3	V
*	Gate No. 1-Terminal Forward Current	I_{G1SSF}	V_{G1S} = +1 V, V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 1-Terminal Reverse Current	I_{G1SSR}	V_{G1S} = -6 V, V_{G2S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Forward Current	I_{G2SSF}	V_{G2S} = +6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Gate No. 2-Terminal Reverse Current	I_{G2SSR}	V_{G2S} = -6 V, V_{G1S} = V_{DS} = 0	T_A = 25°C T_A = 100°C	– –	– –	50 5	nA μA
*	Zero-Bias Drain Current	I_{DS}	V_{DS} = +15 V, V_{G1S} = 0, V_{G2S} = +4 V		0.5	5.0	12	mA
*	Forward Transconductance (Gate No. 1-to-Drain)	g_{fs}	V_{DS} = +15 V, I_D = 10 mA, V_{G2S} = +4 V	f = 1 kHz	10,000	15,000	20,000	μmho
	Small-Signal, Short-Circuit Input Capacitance†	C_{iss}		f = 1 MHz	4.0	6.0	8.5	pF
*	Small-Signal, Short-Circuit, Reverse Transfer Capacitance (Drain-to-Gate-No. 1)♦	C_{rss}			0.005	0.02	0.03	pF
	Small-Signal, Short-Circuit Output Capacitance	C_{oss}			–	2.0	–	pF
*	Power Gain (see Fig. 1)	G_{PS}		f = 400 MHz	10	12.5	–	dB
	Noise Figure (see Fig. 1)	NF			–	3.9	6.0	dB
*	Bandwidth	BW			28	–	38	MHz
*	Gate-to-Source Forward Breakdown Voltage — Gate No. 1	$V_{(BR)G1SSF}$	I_{G1SSF} = I_{G2SSF} = 100 μA	V_{G2S} = V_{DS} = 0	6.5	–	13	V
	Gate No. 2	$V_{(BR)G2SSF}$		V_{G1S} = V_{DS} = 0				
*	Gate-to-Source Reverse Breakdown Voltage — Gate No. 1	$V_{(BR)G1SSR}$	I_{G1SSR} = I_{G2SSR} = 100 μA	V_{G2S} = V_{DS} = 0	-6.5	–	-13	V
	Gate No. 2	$V_{(BR)G2SSR}$		V_{G1S} = V_{DS} = 0				

†Capacitance between Gate No. 1 and all other terminals.
♦Three-terminal measurement with Gate No. 2 and Source returned to guard terminal.
*In accordance with JEDEC registration data format (JS-9 RDF-19A)

OPERATING CONSIDERATIONS

The flexible leads of the 3N200 are usually soldered to the circuit elements. As in the case of any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.



All resistances in ohms
All capacitances in pF

C_1, C_2: 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent

C_3: 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent

C_4: Approx. 300 pF - capacitance formed between socket cover & chassis

C_5: 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent

L_1, L_2: Inductance to tune circuit

Fig. 1 - 400 MHz power gain and noise figure test circuit

3N200

Typical Characteristics

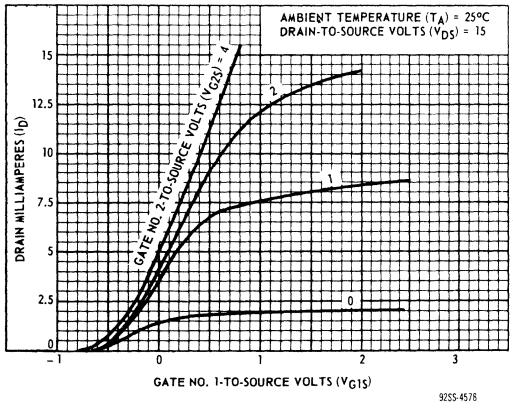


Fig. 2 - I_D vs. V_{G1S}

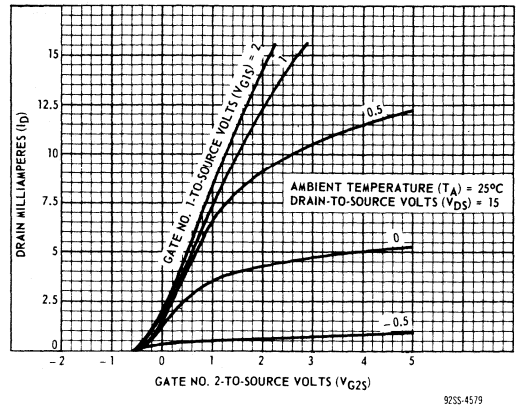


Fig. 3 - I_D vs. V_{G2S}

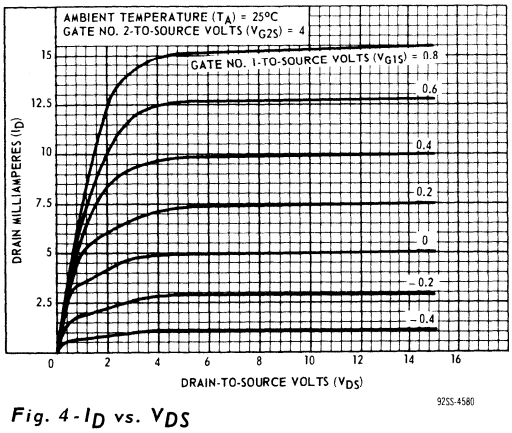


Fig. 4 - I_D vs. V_{DS}

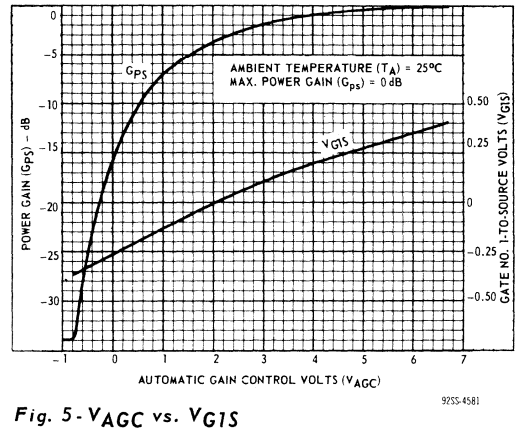


Fig. 5 - V_{AGC} vs. V_{G1S}

y and s Parameters vs. Frequency

TEST CONDITIONS: Drain-to-Source Volts (V_{DS}) = 15, Drain Milliamperes (I_D) = 10, Gate No. 2-to-Source Volts (V_{G2S}) = 4

CHARACTERISTICS	SYMBOL	FREQUENCY (MHz)					UNITS
		100	200	300	400	500	
Maximum Available Power Gain	MAG	32	24	17.5	13	10	dB
Maximum Usable Power Gain (Unneutralized)*	MUG	32	24	17.5	13	10	dB
Y Parameters							
Input Conductance	g_{is}	0.25	0.8	2.0	3.6	6.2	mmho
Input Susceptance	b_{is}	3.4	5.8	8.5	11.2	15.5	mmho
Magnitude of Forward Transadmittance	$\lvert y_{fs} \rvert$	15.3	15.3	15.4	15.5	16.3	mmho
Angle of Forward Transadmittance	$\angle y_{fs}$	−15	−25	−35	−47	−60	degrees
Output Conductance	g_{os}	0.15	0.3	0.5	0.8	1.1	mmho
Output Susceptance	b_{os}	1.5	2.7	3.6	4.25	5.0	mmho
Magnitude of Reverse Transadmittance	$\lvert y_{rs} \rvert$	0.012	0.025	0.06	0.14	0.26	mmho
Angle of Reverse Transadmittance	$\angle y_{rs}$	−60	−25	0	14	20	degrees
S Parameters							
Magnitude of Input Reflection Coeff.	$\lvert s_{is} \rvert$	0.97	0.90	0.84	0.78	0.70	
Angle of Input Reflection Coeff.	$\angle s_{is}$	−20	−32	−55	−68	−82	degrees
Magnitude of Forward Transmission Coeff.	$\lvert s_{fs} \rvert$	1.50	1.40	1.25	1.1	0.9	
Angle of Forward Transmission Coeff.	$\angle s_{fs}$	153	133	112	90	70	degrees
Mangitude of Output Reflection Coeff.	$\lvert s_{os} \rvert$	0.985	0.95	0.93	0.92	0.91	
Angle of Output Reflection Coeff.	$\angle s_{os}$	−7.5	−16	−22	−28	−34	degrees
Magnitude of Reverse Transmission Coeff.	$\lvert s_{rs} \rvert$	0.001	0.0025	0.005	0.010	0.0165	
Angle of Reverse Transmission Coeff.	$\angle s_{rs}$	100	125	141	150	142	degrees

*Limited only by practical design considerations

Typical y Parameters vs. V_{DS}

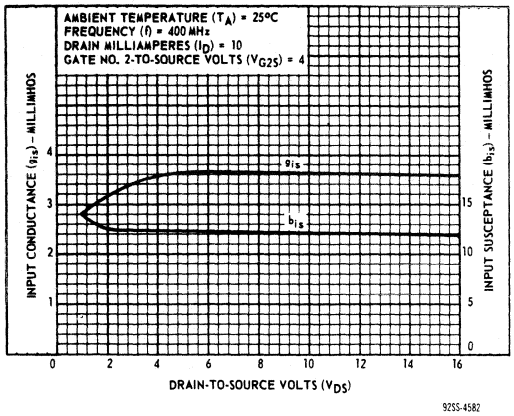


Fig. 6 - y_{is} vs. V_{DS}

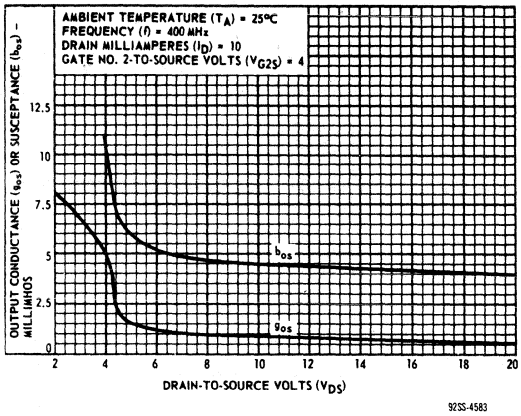


Fig. 7 - y_{os} vs. V_{DS}

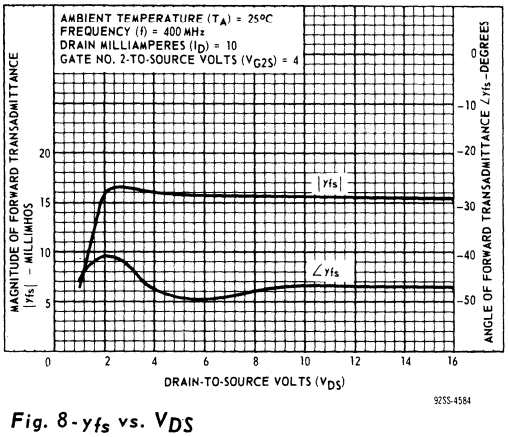


Fig. 8 - y_{fs} vs. V_{DS}

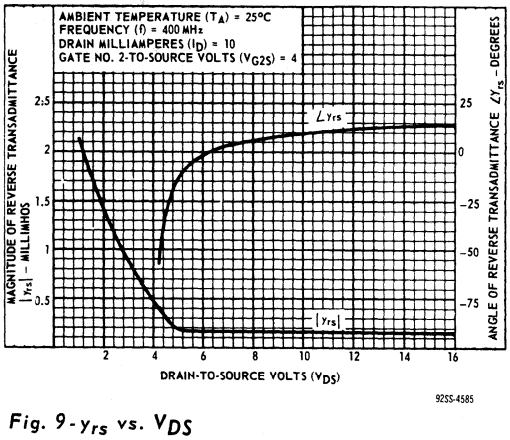


Fig. 9 - y_{rs} vs. V_{DS}

Typical y Parameters vs I_D

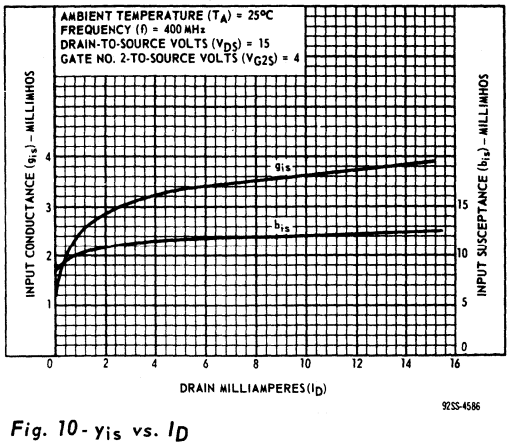


Fig. 10 - y_{is} vs. I_D

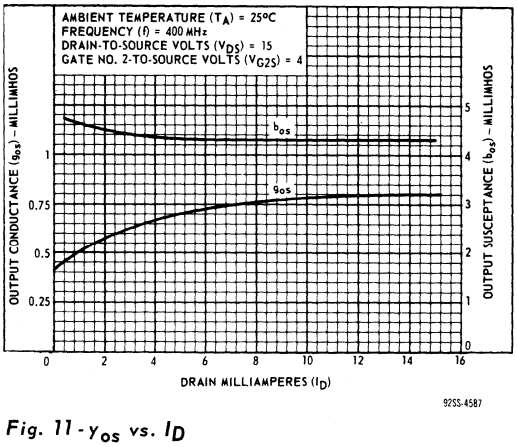


Fig. 11 - y_{os} vs. I_D

3N200

Typical y Parameters vs. I_D (cont'd)

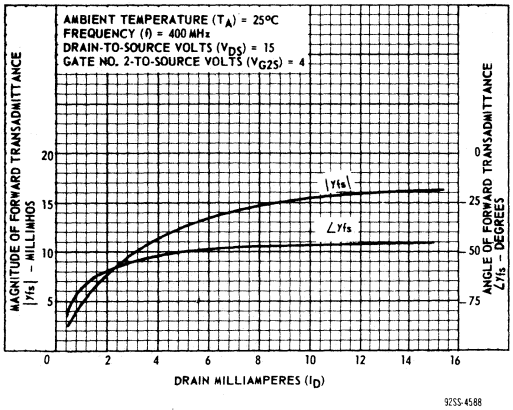


Fig. 12 - y_{fs} vs. I_D

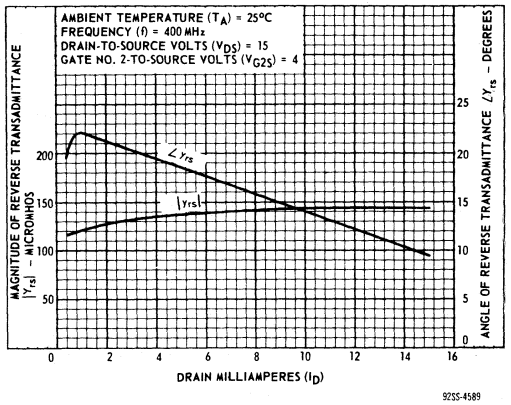


Fig. 13 - y_{rs} vs. I_D

Typical y Parameters vs. V_{G2S}

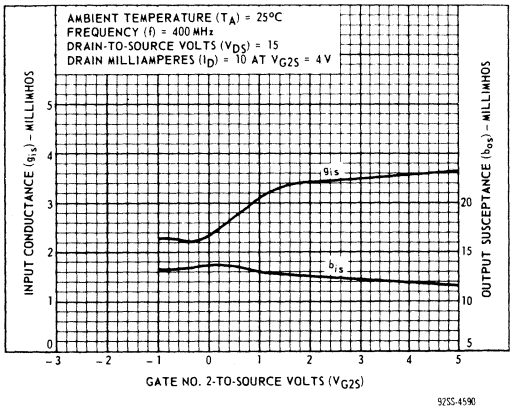


Fig. 14 - y_{is} vs. V_{G2S}

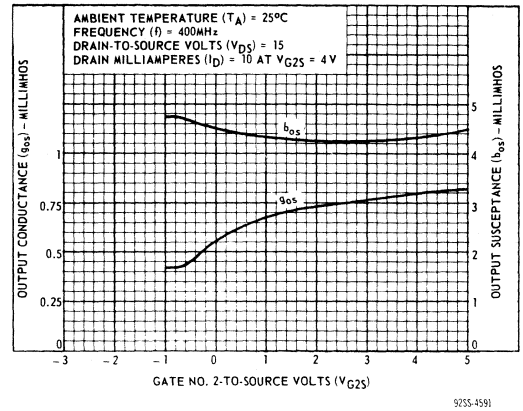


Fig. 15 - y_{os} vs. V_{G2S}

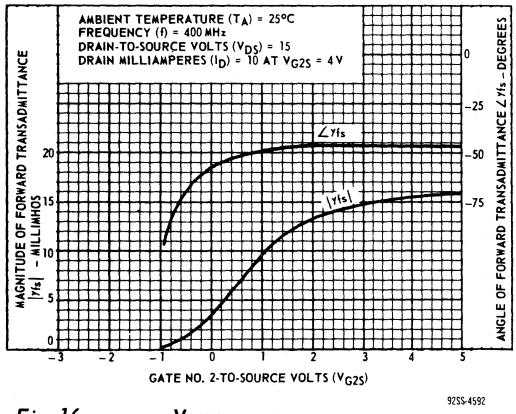


Fig. 16 - y_{fs} vs. V_{G2S}

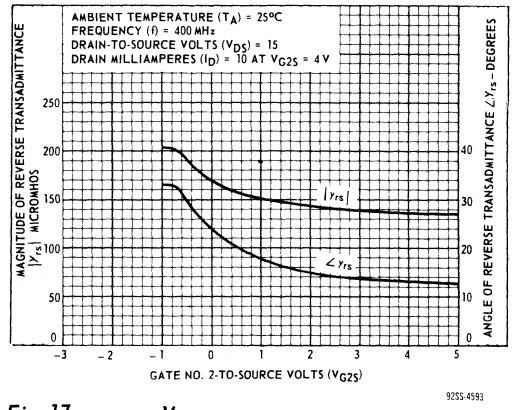


Fig. 17 - y_{rs} vs. V_{G2S}

Typical Characteristics

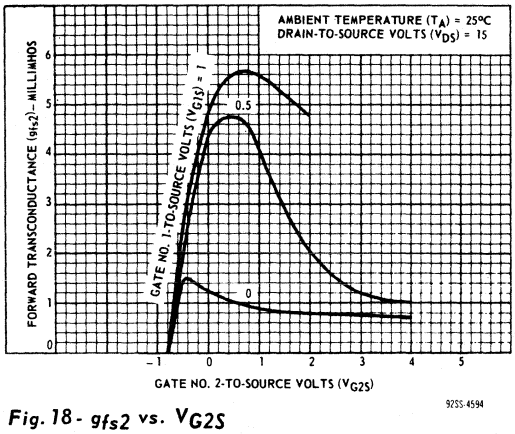


Fig. 18 - g_{fs2} vs. V_{G2S}

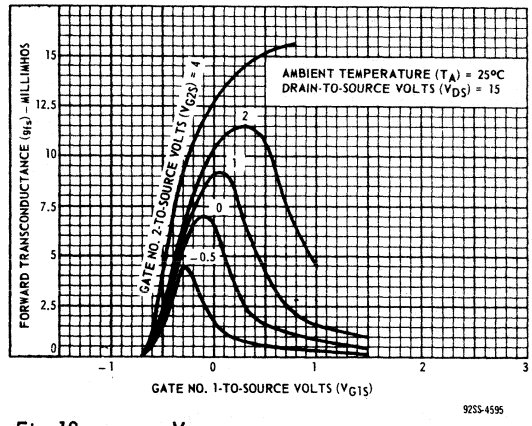


Fig. 19 - g_{fs} vs. V_{G1S}

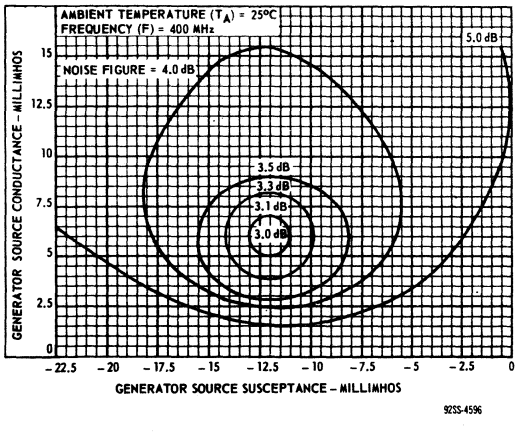
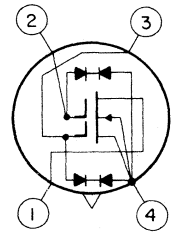


Fig. 20 - Noise figure vs. generator source admittance

TERMINAL DIAGRAM



LEAD 1 - DRAIN
LEAD 2 - GATE No. 2
LEAD 3 - GATE No. 1
LEAD 4 - SOURCE, SUBSTRATE AND CASE

3N204, 3N205, 3N206

Silicon Dual Insulated-Gate Field-Effect Transistors

With Integrated Gate-Protection Circuits for VHF TV Applications

3N204 — RF Amplifier 3N205 — Mixer
3N206 — TV IF Amplifier

Features:

- *Low C_{rss} — 0.03 pF max.*
- *High $|Y_{fs}|$ — 14 mmho typ. for 3N204 and 3N205*
- *Integrated gate-protection diodes*

The RCA-3N204, 3N205, and 3N206 are n-channel silicon, depletion type, dual-insulated gate, field-effect transistors intended for vhf TV applications. Integrated back-to-back diodes protect the gates from excessive input voltages.

The 3N204 is intended for use in vhf rf amplifiers and delivers linear, low-noise amplification. Its extremely low feedback capacitance allows high-gain stable operation without neutralization. The 3N205 is specified for low noise vhf mixer applications. The 3N206 is intended for use in tuned high-frequency amplifiers such as TV if strips.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°:*

*DRAIN-TO-GATE No. 1 VOLTAGE	30 V
* DRAIN-TO-GATE No. 2 VOLTAGE	30 V
* DRAIN-TO-SOURCE VOLTAGE	25 V
* GATE No.1-TERMINAL FORWARD CURRENT▲	10 mA
* GATE No.2-TERMINAL FORWARD CURRENT▲	10 mA
* GATE No.1-TERMINAL REVERSE CURRENT	−10 mA
* GATE No.2-TERMINAL REVERSE CURRENT	−10 mA
* CONTINUOUS DRAIN CURRENT	50 mA
* DEVICE DISSIPATION:	
Up to T_A = 25 °C	360 mW
Above T_A = 25 °C derate linearly	2.4 mW/°C
Up to T_C = 25 °C	1.2 W
Above T_C = 25 °C derate linearly	8 mW/°C
* AMBIENT TEMPERATURE RANGE:	
Operating	−65 to +175 °C
Storage	−65 to +200 °C
* LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+300 °C

▲ Forward gate-terminal current is the current into a gate terminal with a forward-gate-to-source voltage applied. This voltage is of such polarity that an increase in its magnitude causes the channel resistance to decrease.

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

3N204, 3N205, 3N206

ELECTRICAL CHARACTERISTICS, At T_A = 25°C (unless otherwise specified)

	CHARACTERISTIC	TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
*	Drain-to-Source Breakdown Voltage, $V_{(BR)DS}$	I_D = 10μA, $V_{G1S}=V_{G2S}$ = −5V		25	–	V
*	Gate No.1-to-Source Forward Breakdown Voltage, $V_{(BR)G1SSF}$[1]	I_{G1}=10mA, $V_{G2S}=V_{DS}=0$		6	30	V
*	Gate No.1-to-Source Reverse Breakdown Voltage, $V_{(BR)G1SSR}$[1]	I_{G1}= −10mA, $V_{G2S}=V_{DS}=0$		−6	−30	V
*	Gate No.2-to-Source Forward Breakdown Voltage, $V_{(BR)G2SSF}$[1]	I_{G2}=10mA, $V_{G1S}=V_{DS}=0$		6	30	V
*	Gate No.2-to-Source Reverse Breakdown Voltage, $V_{(BR)G2SSR}$[1]	I_{G2}= −10mA, $V_{G1S}=V_{DS}=0$		−6	−30	V
*	Gate No.1-Terminal Forward Current, I_{G1SSF}	V_{G1S}=5V, $V_{G2S}=V_{DS}=0$		–	10	nA
*	Gate No.1-Terminal Reverse Current, I_{G1SSR}	V_{G1S}= −5V, $V_{G2S}=V_{DS}=0$	T_A=25°C	–	−10	nA
			T_A=150°C	–	−10	μA
*	Gate No.2-Terminal Forward Current, I_{G2SSF}	V_{G2S}=5V, $V_{G1S}=V_{DS}=0$		–	10	nA
*	Gate No.2-Terminal Reverse Current, I_{G2SSR}	V_{G2S}= −5V, $V_{G1S}=V_{DS}=0$	T_A=25°C	–	−10	nA
			T_A=150°C	–	−10	μA
*	Zero-Gate No.1-Voltage Drain Current, I_{DS}[2]	V_{DS}=15V, V_{GIS}=0, V_{G2S}=4V	3N204	6	30	mA
			3N205	6	30	
			3N206	3	15	
*	Gate No.1-to-Source Cutoff Voltage, $V_{G1S(off)}$	V_{DS}=15V, V_{G2S}=4V, I_D=20μA		−0.5	−4	V
*	Gate No.2-to-Source Cutoff Voltage, $V_{G2S(off)}$	V_{DS}=15V, V_{G1S}=0, I_D=20μA		−0.2	−4	V
*	Small-Signal Common-Source Forward Transfer Admittance, $\|y_{fs}\|$[3]	V_{DS}=15V, V_{G1S}=0, V_{G2S}=4V, f=1 kHz	3N204	10	22	mmho
			3N205	10	22	
			3N206	7	17	
*	Small-Signal Common-Source Reverse Transfer Capacitance, C_{rss}	V_{DS}=15V, V_{G2S}=4V, I_D = 10 mA, f = 1 MHz		0.005	0.03	pF

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. All gate breakdown voltages are measured while the device is conducting rated gate current. This ensures that the gate-voltage-limiting network is functioning properly.
2. This characteristic must be measured using pulse techniques (t_W = 300μs, duty cycle ≤ 2%).
3. This characteristic must be measured with bias voltages applied for less than 5 seconds to avoid overheating. The signal is applied to gate No.1 with gate No.2 at ac ground.

3N204, 3N205, 3N206

OPERATING CHARACTERISTICS at T_A = 25°C

	CHARACTERISTIC	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
	3N204					
*	Common-Source Spot Noise Figure, NF	V_{DD}=18 V, V_{GG}=7 V, f = 200 MHz, See Fig.13	–	–	3.5	dB
*	Small-Signal Common-Source Insertion Power Gain, G_{ps}		20	–	28	dB
*	Bandwidth, BW		7	–	12	MHz
*	Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=18 V, ΔG_{ps}=–30dB,[1] f=200 MHz, See Fig. 13	0	--	–2	V
*	Common-Source Spot Noise Figure, NF	V_D=15 V, V_{G2S} = 4 V, f = 450 MHz, I_D = 10 mA, See Figs. 15 and 16	–	–	5	dB
*	Small-Signal Common Source Insertion Power Gain, G_{ps}		14	–	–	dB
	3N205					
*	Small-Signal Conversion Power Gain, G_{ps} (conv)	V_{DD}=18 V, f_{LO}=245 MHz,[3] f_{RF}=200 MHz, See Fig.17	17	–	28	dB
*	Bandwidth, BW		4	–	7	MHz
	3N206					
*	Common-Source Spot Noise Figure, NF	V_{DD}=24 V, V_{GG}=6 V, f=45 MHz, See Fig. 14	–	–	4	dB
*	Small-Signal Common-Source Insertion Power Gain, G_{ps}		25	–	35	dB
*	Bandwidth, BW		3	–	6	MHz
*	Gain-Control Gate-Supply Voltage, $V_{GG(GC)}$	V_{DD}=24 V, ΔG_{ps}=–30dB,[2] f=45 MHz, See Fig. 14	–1.6	–	0.6	V

*In accordance with JEDEC registration data format (JS-9 RDF-19B).

1. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 7V.
2. ΔG_{ps} is defined as the change in G_{ps} from the value at V_{GG} = 6V.
3. Amplitude at input from local oscillator is 3 V RMS.

TYPICAL CHARACTERISTICS

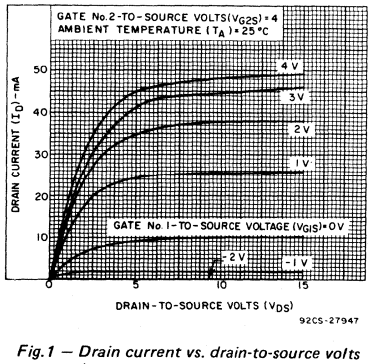


Fig.1 – Drain current vs. drain-to-source volts (pulse-tested with pulse duration = 300 μs, duty cycle ⩽2%).

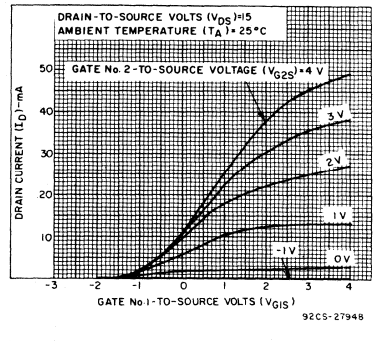


Fig.2 – Drain current vs. gate-No.1-to-source volts (pulse-tested with pulse duration = 300 μs, duty cycle ⩽ 2%).

TYPICAL Y-PARAMETER CHARACTERISTICS

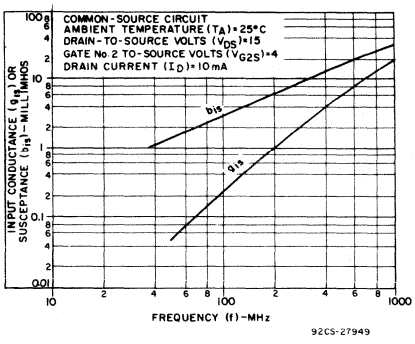


Fig.3 – Y_{is} vs. f

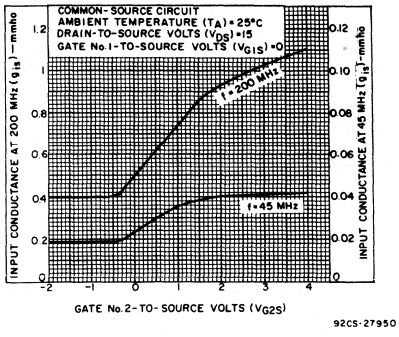


Fig.4 – Y_{is} vs. V_{G2S}

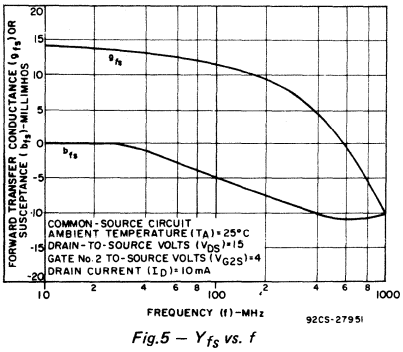


Fig.5 – Y_{fs} vs. f

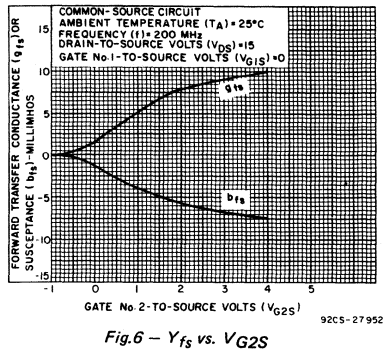


Fig.6 – Y_{fs} vs. V_{G2S}

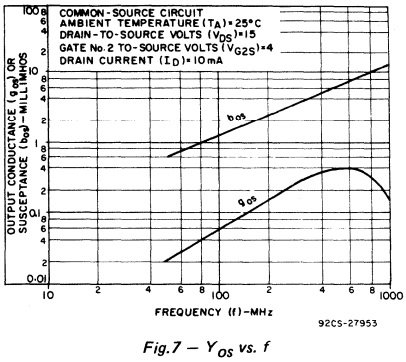


Fig.7 – Y_{os} vs. f

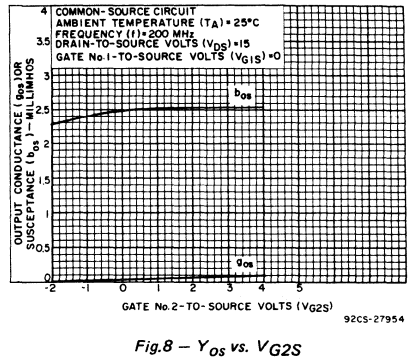


Fig.8 – Y_{os} vs. V_{G2S}

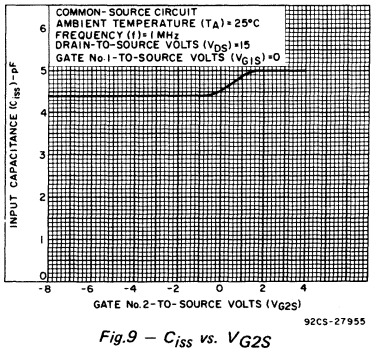


Fig.9 – C_{iss} vs. V_{G2S}

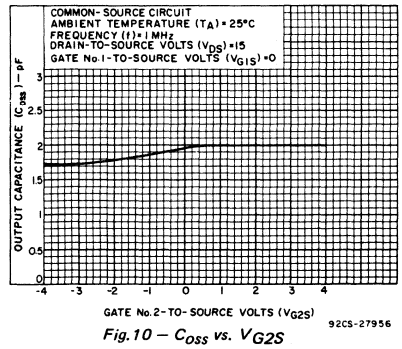


Fig.10 – C_{oss} vs. V_{G2S}

TYPICAL OPERATING CHARACTERISTICS FOR 3N204

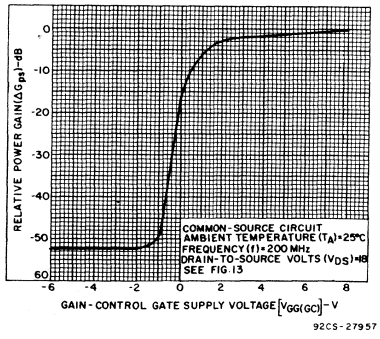


Fig.11 – ΔG_{ps} vs. $V_{GG(GC)}$

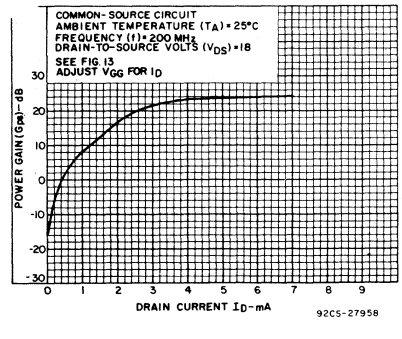


Fig.12 – G_{ps} vs. I_D

TEST CIRCUITS

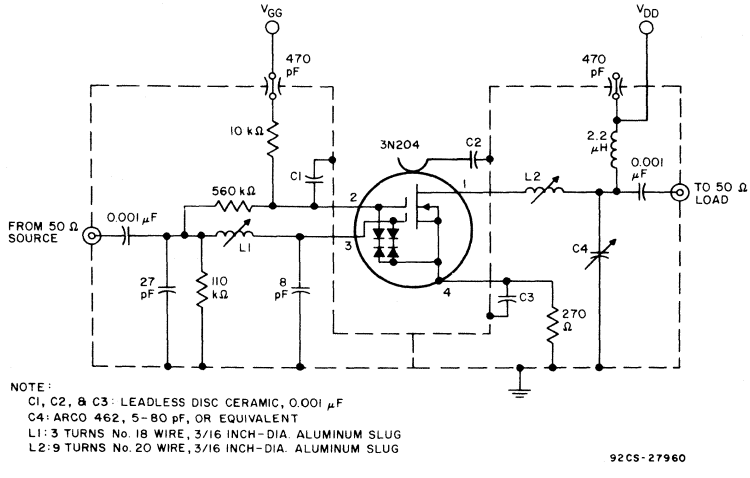
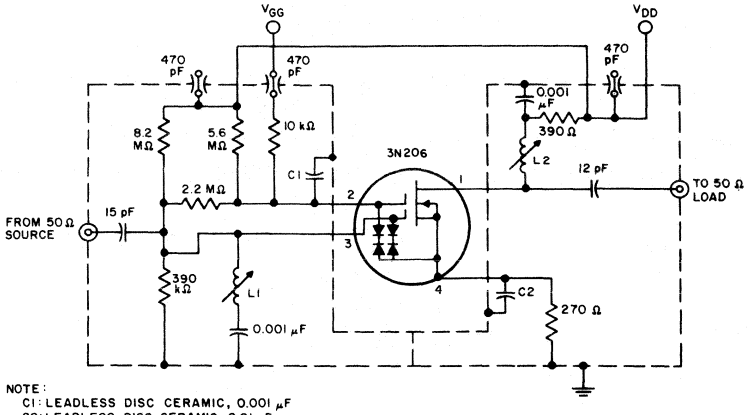


Fig.13 – 200-MHz power gain, gain-control voltage, and noise-figure test circuit for 3N204.*

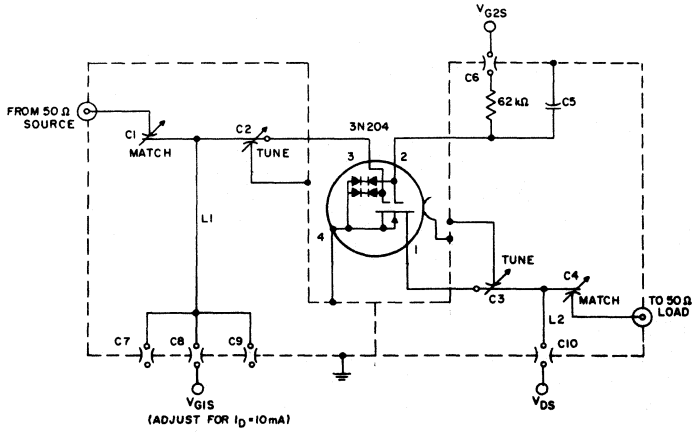
* In accordance with JEDEC registration data format (JS-9 RDF-19B).



NOTE:
C1: LEADLESS DISC CERAMIC, 0.001 μF
C2: LEADLESS DISC CERAMIC, 0.01 μF
L1: 8 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG
L2: 9 TURNS No. 28 WIRE, 5/32 INCH-DIA. FORM, TYPE "J" SLUG

92CM-27959

Fig. 14 — —45-MHz power-gain and noise-figure test circuit for 3N206.*
* In accordance with JEDEC registration data format (JS-9 RDF-19B).

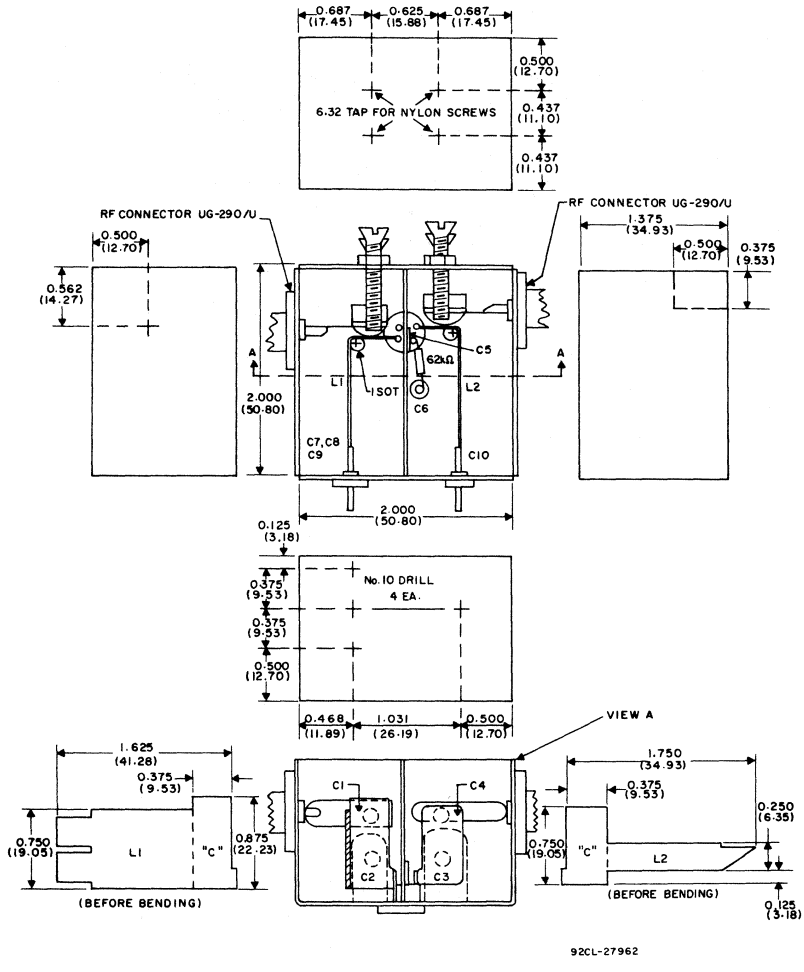


NOTE:
FOR TEST FIXTURE, SEE PICTORAL DRAWING IN FIGURE 16
C1 THRU C4: SEE FIGURE 16, NOTE D
C5: 0.001 μF LEADLESS DISC CAPACITOR
C6 THRU C10: ALLEN-BRADLEY F5AU 0.001 μF FEED-THROUGH CAPACITORS, OR EQUIVALENT
L1 & L2: SEE FIGURE 16

92CM-27961

Fig. 15 — —450-MHz power-gain and noise-figure test circuit for 3N204.*
* In accordance with JEDEC registration data format (JS-9 RDF-19B).

3N204, 3N205, 3N206



NOTES:

A. Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions, as indicated.

B. The removable top of test fixture is not shown.

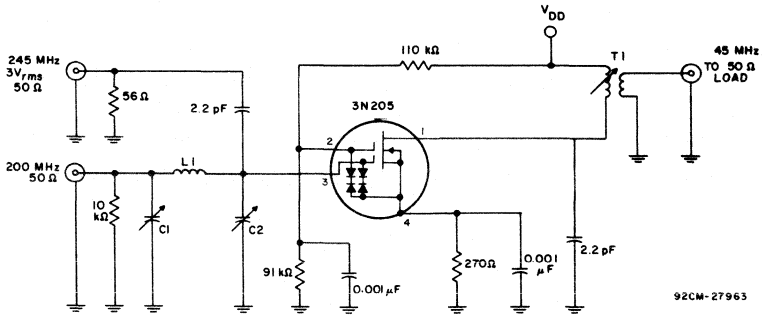
C. For clarity, the 62 kΩ resistor, the source and gate-2 socket pins, and insulating stand-off terminals (ISOT) soldered into the fold of L1 and L2 respectively for mechanical support, are not shown in view A.

D. C1 and C2 (C3 and C4) consist of shim brass and the "C" portion of L1 (L2) separated by air and the mylar tape covering the "C" portion of L1 (L2).

E. The four views surrounding the center view are as they would appear before the metal is bent up to form the sides.

Fig. 16 — —450 MHz power-gain and noise-figure test fixture.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).



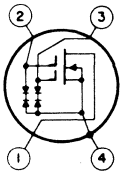
NOTE:
C1: ARCO 462, 5–80 pF, or EQUIVALENT
C2: ARCO 460, 1.5–15 pF, OR EQUIVALENT
L1: 4 TURNS No.14 WIRE, 1/4 INCH INSIDE DIA.

T1: PRI: 16 TURNS No.30 WIRE CLOSE WOUND ON 1/4 INCH DIA. FORM, TYPE "J" SLUG
SEC: 5 TURNS No.30 WIRE CENTERED OVER PRIMARY

Fig.17 – –200 MHz-to-45-MHz circuit for conversion power gain for 3N205.*

* In accordance with JEDEC registration data format (JS-9 RDF-19B).

TERMINAL DIAGRAM
Bottom View



LEAD 1 – DRAIN
LEAD 2 – GATE No.2
LEAD 3 – GATE No.1
LEAD 4 – SOURCE, SUBSTRATE AND CASE

OPERATING CONSIDERATIONS

The flexible leads of these devices are usually soldered to the circuit elements. As is the case with any high-frequency semiconductor device, the tips of soldering irons MUST be grounded.

Supplementary Information

Supplementary Information

Enhanced Product

Standard IC Circuits

Burn-in Time*	SUFFIX X 160 Hours
Temperature*	**125°C**
Bias Voltage:	
CD4000A	12 V
CD4000B	15 V
CD54/74HC/HCT/HCU	6V
Linear Special	differs by type

LSI Circuits

Burn-in Time*	160 Hours
Temperature*	**125°C**
Bias Voltage:	
CDP1800 "C" Product	7 V
All Other	6 V
CDP1800 "Non-C" Product	11 V

PRODUCT IDENTIFICATION

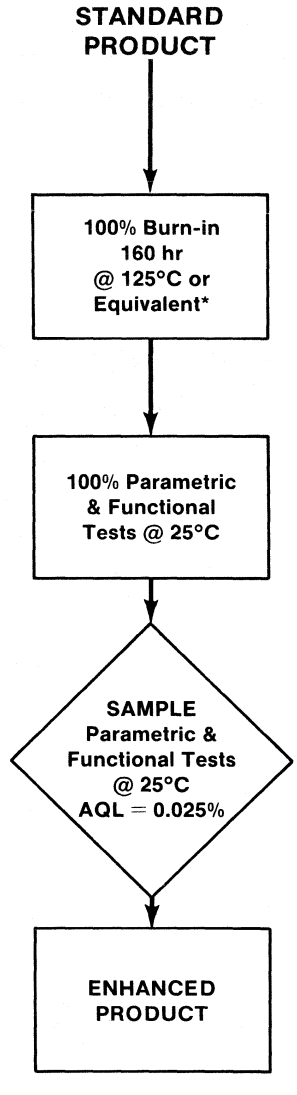
All enhanced product is identified by a suffix "x".

Example:

Standard	Enhanced
CD4001BE	CD4001BEX
CD74HCOOE	CD74HCOOEX
CA3130E	CA3130EX
CDP1854ACE	CDP1854ACEX
CDP6805G2E	CDP6805G2EX

*Or equivalent means equivalent time-temperature/voltage resulting in the same activation energy.

Product Flow



□ Production State or Process

◇ Quality Assurance Step

Enhanced Product Application

The need to achieve the enhanced reliability resulting from burn-in screening must be determined by careful analysis of system design and application.

How many IC's are incorporated into the total system? How many devices on each board?

Is the proper device being used for the application?

What are the reliability goals?

What failure rates are being experienced without screening?

Cost-effectiveness of using enhanced CMOS can be determined by mutual analysis of the economic trade-offs made possible by the following features of the program:

- Available in both plastic and frit-seal ceramic packages.
- Offered on the industry's broadest line of circuit functions.
- 0.025% AQL cumulative.
- Reduction in PC board reworking through fewer line rejects.
- Lower warranty requirements through the elimination of infant mortality failures.
- Reduced incoming inspection cost by reduction or complete elimination of test procedures.
- Reduction of system failures and related service expenses and customer complaints.

Enhanced Product Reliability Data

FAILURE RATES IN PLASTIC DUAL-IN-LINE PACKAGES

Product Category	Device Family	Temp (°C)	V_{DD} (V)	Equivalent Device Hrs.†	Failure Rate (FITs)* Standard No Burn-in	Failure Rate (FITs)* Burn-in (160 Hrs., 125°C)#
CMOS Logic	CD4000 Series	85	18	2.9×10^8	75	31
		55	18	5.6×10^9	4	1.7
QMOS	CD74 HC/HCT Series	85	6	1.5×10^9	15	6.2
		55	6	2.9×10^{10}	0.8	0.3
Memory/μP						
C^2L	CDP1800	85	7	2.4×10^7	160	67
	(RAM/ROM, I/O)	55	7	4.6×10^8	8.3	3.5
SOS	CDP1800	85	7	6.8×10^6	300	12.5
	(RAM/EPROM)	55	7	1.3×10^8	15.5	6.5
CMOS I	CDP1800	85	6	9.2×10^7	170	71
	(RAM/ROM, μCOMP/μP)	55	6	1.8×10^9	8.8	3.7
CMOS I	CDP6805	85	5	6.2×10^6	1000	417
(Poly Load)	5μSeries	55	5	1.2×10^8	52	22
CMOS II	ROMs	85	6	5.6×10^7	70	29
	(64K, 128K, 256K)	55	6	1.1×10^9	3.6	1.5
Bulk Twin	RAMs	85	6	7.7×10^7	80	33
Tub	(16K, 64K)	55	6	1.5×10^9	4	1.7
Linear‡	Various	85	8-30	8.1×10^7	150	62
		55	8-30	1.6×10^9	7.8	3.2

NOTES: *FITs are the number of failures in 10^9 device hours. The failure rate is estimated at 60% upper confidence level. To convert the above data from FITs to %/1000 hours, multiply by 10^{-4}.

†Equivalent device hours are extrapolated from accelerated test temperatures to the maximum 85°C rating and nominal use condition of 55°C, using a 1.0eV activation energy. Actual test temperatures ranged between 125°C-175°C.

#The difference in failure rate between standard and burned-in product is estimated from several sample studies.

‡The failure rates shown are based on ambient temperature. The actual junction temperature of Linear parts may vary between 25°C to 50°C above the ambient.

RCA High-Reliability CA3000 Slash-Series Linear ICs

RCA High-Reliability Slash-Series Linear ICs

RCA-CAXXXX "Slash" (/) Series types are high-reliability linear integrated circuits intended for applications in aerospace, military, and industrial equipment. These devices are electrically and mechanically identical to the standard types but are specially processed and tested to meet the electrical, mechanical, and environmental test methods and procedures established for microcircuit devices.

The standard package types and screening levels available for individual devices can be found in the table below. Screening levels /1, /3, and /3W are based on guidelines established for military product. For detailed screening information, refer to RCA DATABOOK SSD-230B, "High-Reliability Products or RCA brochure HRP-479, "High-Reliability Products." Chip versions of the standard product and quality conformance packages are offered on a custom basis only.

Electrical characteristics may be found in RCA data bulletins on specific slash (/) series types. For applications information refer to RCA databooks SSD-230B "High Reliability Products," and SSD-245, "Applications-Linear Integrated Circuits and MOSFETs."

Radiation Effects on Linear ICs

There is no dedicated process for radiation hardening of the Linear ICs. Gammacell exposure of various devices representing both the bipolar and BiMOS water technologies has resulted in information useful for design guidance when considering radiation hardness.

Devices processed under bipolar technologies tend to withstand Gamma radiation to exposure levels of 1×10^5 rads(Si) prior to experiencing significant parameter degradation, while those processed with BiMOS techniques can withstand Gamma Ray exposure levels up to 1×10^4 rads(Si) before parameter degradation takes place. RCA does not guarantee rad-hard levels for linear IC's but will conduct rad-hard testing on a custom basis.

Screening Levels for RCA High-Reliability CA3000 Slash-Series Linear ICs

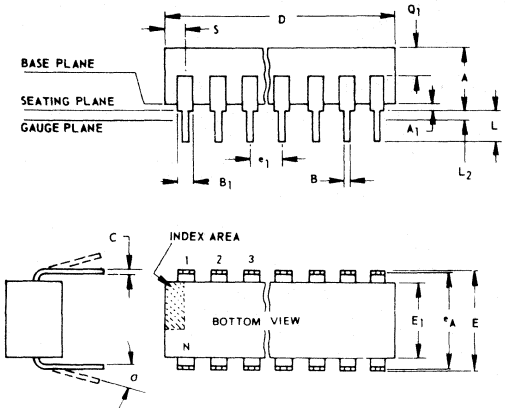
TYPE	SCREENING LEVEL (/)			PACKAGE CODE*				# OF LEADS	TYPE	SCREENING LEVEL (/)			PACKAGE CODE*				# OF LEADS
CA723	1	3	-	T	-	-	-	10	CA3081	1	3	-	-	-	-	F	16
CA741	1	3	-	T	S	-	-	8	CA3082	1	3	-	-	-	-	F	16
CA747	1	3	-	T	S	-	-	10	CA3083	-	-	3W	-	-	-	F	16
CA748	1	3	-	T	S	-	-	8	CA3085	1	3	-	T	S	-	-	8
CA1558	1	3	-	T	S	-	-	8	CA3085A	1	3	-	T	S	-	-	8
CA3000	1	3	-	T	-	-	-	10	CA3085B	1	3	-	T	S	-	-	8
CA3001	1	3	-	T	-	-	-	12	CA3089	-	-	3W	-	-	-	F	16
CA3002	1	3	-	T	-	-	-	10	CA3094	1	3	-	T	S	-	-	8
CA3006	1	3	-	T	-	-	-	12	CA3094A	1	3	-	T	S	-	-	8
CA3015	1	3	-	T	-	-	-	12	CA3100	1	3	-	T	S	-	-	8
CA3015A	1	3	-	T	-	-	-	12	CA3118A	1	3	-	T	-	-	-	12
CA3018	1	3	-	T	-	-	-	12	CA3130	1	3	-	T	S	-	-	8
CA3018A	1	3	-	T	-	-	-	12	CA3130A	1	3	-	T	S	-	-	8
CA3019	1	3	-	T	-	-	-	10	CA3140	1	3	-	T	S	-	-	8
CA3020	1	3	-	T	-	-	-	12	CA3140A	1	3	-	T	S	-	-	8
CA3020A	1	3	-	T	-	-	-	12	CA3160	1	3	-	T	S	-	-	8
CA3026	1	3	-	T	-	-	-	12	CA3160A	1	3	-	T	S	-	-	8
CA3028B	1	3	-	T	S	-	-	8	CA3193	1	3	-	T	S	-	-	8
CA3038A	1	3	-	-	-	D	-	14	CA3193A	1	3	-	T	S	-	-	8
CA3039	1	3	-	T	-	-	-	12	CA3260	1	3	-	T	S	-	-	8
CA3040	1	-	3W	T	-	-	-	12	CA3260A	1	3	-	T	S	-	-	8
CA3045	1	3	-	-	-	D	F	14	CA3290A	1	3	-	T	S	-	-	8
CA3049	1	3	-	T	-	-	-	12	CA3300	-	3	-	-	-	D	-	18
CA3058	1	3	-	-	-	D	-	14	CA3306	-	3	3W	-	-	D	-	18
CA3078	1	3	-	T	S	-	-	8	CA6741	1	3	-	T	S	-	-	8
CA3078A	1	3	-	T	S	-	-	8	**MOSFETS**								
CA3080	1	3	-	T	S	-	-	8	HR3N187	-	-	3W	T	-	-	-	4
CA3080A	1	3	-	T	S	-	-	8	HR3N200	-	-	3W	T	-	-	-	4

Note: High-reliability versions of most commercially available CAXXXX-series linear ICs not listed above can also be supplied on a custom basis.

*Package Designations: T = TO-5 Metal Can
S = TO-5 Metal Can with DIL Formed Leads
D = Weld-Seal DIL White Ceramic
F = Frit-Seal DIL Ceramic
DIL = Dual-in-Line

DIMENSIONAL OUTLINES

Dual-In-Line Welded-Seal Ceramic Packages



(D) Suffix
16-Lead Dual-In-Line
Welded-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.160	3.05	4.06	
A_1	0.020	0.065	0.51	1.65	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.840	18.93	21.33	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.000	0.76	
α	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.050	0.085	1.27	2.15	
S	0.065	0.090	1.66	2.28	

92CS-40078

NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at guage plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(D) Suffix
14-Lead Dual-In-Line
Welded-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.160	3.05	4.06	
A_1	0.020	0.065	0.51	1.65	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.000	0.76	
α	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.050	0.085	1.27	2.15	
S	0.065	0.090	1.66	2.28	

92CS-40038

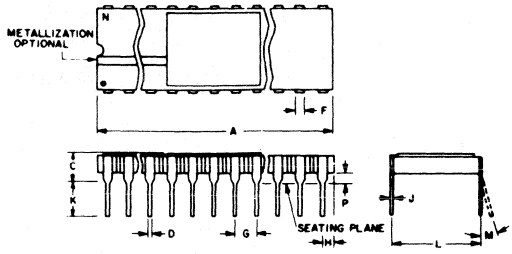
(D) Suffix
18-Lead Dual-In-Line
Welded-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.120	0.160	3.05	4.06	
A_1	0.020	0.065	0.51	1.65	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.845	0.925	21.47	23.49	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.000	0.76	
α	0°	15°	0°	15°	4
N	18		18		5
N_1	0		0		6
Q_1	0.050	0.085	1.27	2.15	
S	0.015	0.060	0.39	1.52	

92CS-40039

DIMENSIONAL OUTLINES

Dual-In-Line Side-Brazed Ceramic Packages



(D) Suffix
16-Lead Dual-In-Line
Side-Brazed Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.830	—	21.08	
C	—	0.200	—	5.08	
D	0.015	0.021	0.381	0.533	
F	0.045	0.070	1.143	1.778	1
G	0.100 BSC		2.54 BSC		1
H	0.015	0.090	0.381	2.286	
J	0.008	0.012	0.203	0.304	3
K	0.125	0.150	3.175	3.81	
L	0.290	0.310	7.366	7.874	2
M	0°	15°	0°	15°	
P	0.020	—	0.508	—	
N	16		16		

92CS-31130

(D) Suffix
18-Lead Dual-In-Line
Side-Brazed Ceramic Package

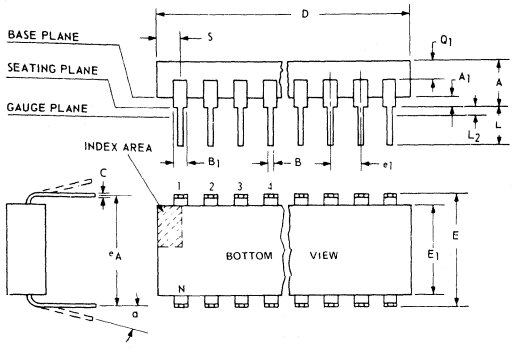
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.890	0.915	22.606	23.241	
C	—	0.200	—	5.08	
D	0.015	0.021	0.381	0.533	
F	0.054 REF		1.371 REF		1
G	0.100 BSC		2.54 BSC		1
H	0.035	0.065	0.889	1.651	
J	0.008	0.012	0.203	0.304	3
K	0.125	0.150	3.175	3.81	
L	0.290	0.310	7.366	7.874	2
M	0°	15°	0°	15°	
P	0.025	0.045	0.635	1.143	
N	18		18		

92CS-27231R1

NOTES:
1. **Leads within 0.005" (0.13 mm) radius of True Position at maximum material condition.**
2. **Dimension "L" to center of leads when formed parallel.**
3. **When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33 mm).**

DIMENSIONAL OUTLINES

Dual-In-Line Frit-Seal Ceramic Packages



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).
2. Leads within 0.005 in. (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. a applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(F) Suffix (JEDEC MO-001-AB)
14-Lead Dual-In-Line
Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.065	0.090	1.66	2.28	

92SS-4296R3

(F) Suffix (JEDEC MO-001-AC)
16-Lead Dual-In-Line
Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.015	0.060	0.39	1.52	

92CM-15967R4

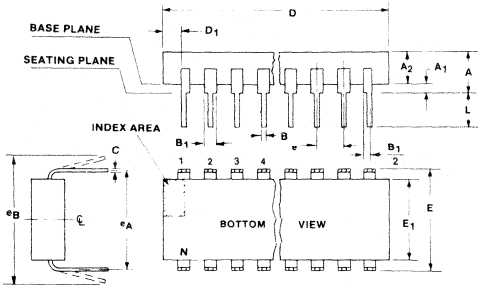
(F) Suffix
18-Lead Dual-In-Line
Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.508	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.845	0.885	21.47	22.47	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TYP		2
e_A	0.300 TP		7.62 TYP		2, 3
L	0.125	0.150	3.18	3.81	
α	0°	15°	0°	15°	4
N	18		18		5
N_1	0		0		6
S	0.015	0.060	0.39	1.52	

92CS-30630

DIMENSIONAL OUTLINES

Dual-In-Line Plastic Packages



(E) Suffix (JEDEC MS-001-AB)
8-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	8		8		11

92CS-39998

(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

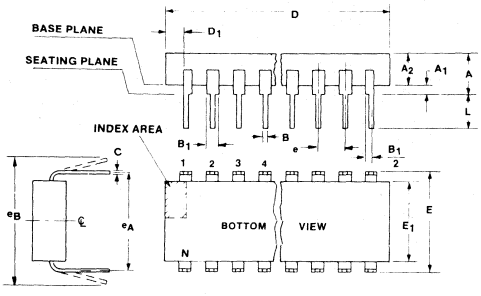
92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

DIMENSIONAL OUTLINES

Dual-In-Line Plastic Packages (Cont'd)



(E) Suffix (JEDEC MS-001-AD)
18-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	18		18		11

92CS-39996

(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

92CS-39997

(E) Suffix (JEDEC MS-010-AA)
22-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.050	1.120	26.67	28.44	4
D_1	0.005	—	0.13	—	12
E	0.390	0.425	9.91	10.79	5
E_1	0.330	0.380	8.39	9.65	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.400 BSC		10.16 BSC		9
e_B	—	0.500	—	12.70	10
L	0.115	0.160	2.93	4.06	9
N	22		22		11

92CS-39999

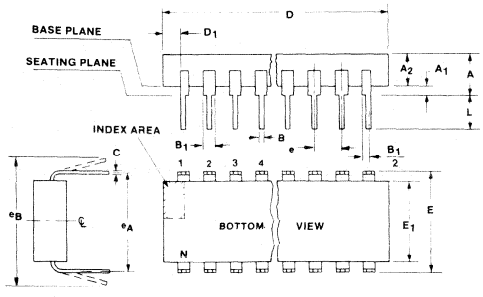
Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

DIMENSIONAL OUTLINES

Dual-In-Line Plastic Packages (Cont'd)



(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

92CS-39943

(E) Suffix (JEDEC MS-011-AA)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.150	1.290	29.3	32.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	24		24		11

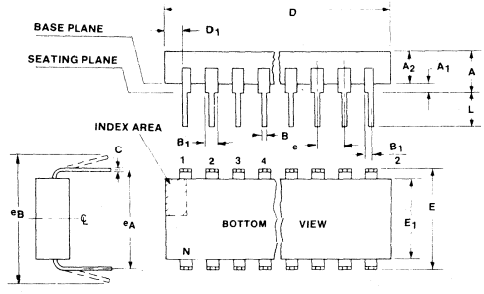
92CS-40000

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

DIMENSIONAL OUTLINES

Dual-In-Line Plastic Packages (Cont'd)



(E) Suffix (JEDEC MS-011-AB)
28-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.380	1.565	35.1	39.7	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	28		28		11

92CS-40001

(E) Suffix (JEDEC MS-011-AC)
40-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.250	—	6.35	9
A_1	0.015	—	0.39	—	9
A_2	0.125	0.195	3.18	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.980	2.095	50.3	53.2	4
D_1	0.005	—	0.13	—	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	—	0.700	—	17.78	10
L	0.115	0.200	2.93	5.08	9
N	40		40		11

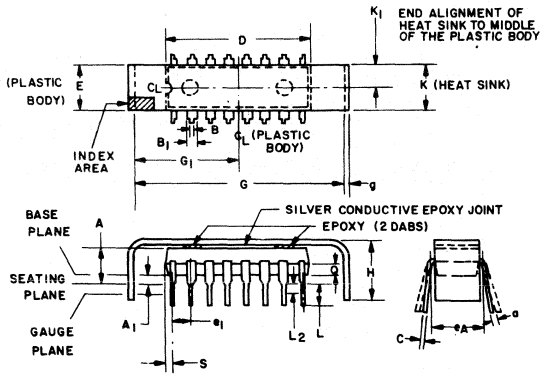
92CS-40002

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

DIMENSIONAL OUTLINES

Dual-In-Line Plastic Packages (Cont'd)



(EM) Suffix
16-Lead Modified Dual-In-Line Plastic Package with "Power Slab"

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	
E	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
G	1.125		28.58		
G_1	0.537	0.587	13.64	14.91	
g	0.030	0.036	0.76	0.91	
H	0.350		8.89		
K	0.250		6.35		7
K_1	0.093	0.157	2.36	3.99	
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.000	0.76	
α	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q	0.040	0.075	1.02	1.90	
S	0.015	0.060	0.39	1.52	

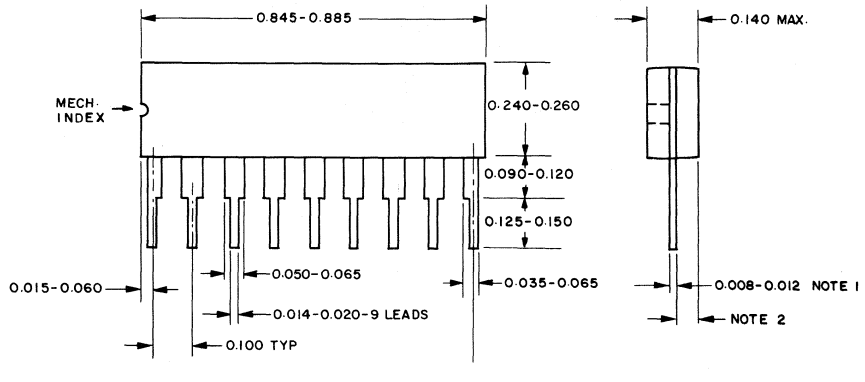
NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. **When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).**
2. **Leads within 0.005 in. (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.**
3. **e_A applies in zone L_2 when unit installed.**
4. **α applies to spread leads prior to installation.**
5. **N is the maximum quantity of lead positions.**
6. **N_1 is the quantity of allowable missing leads.**
7. **Bulging to 0.280 in. (7.11 mm) permissible at points of debossing.**

92CM-33093

Single-In-Line Plastic Package

9-Lead Single-In-Line Plastic Package (SIP)

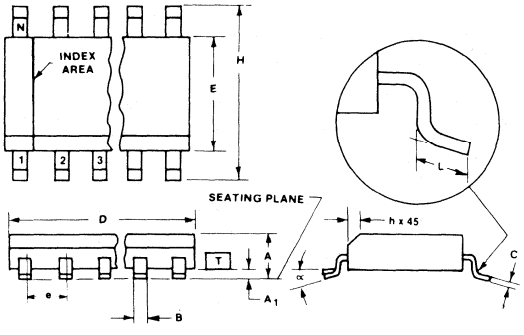


NOTES:
1. A MAXIMUM OF 0.013 ON THE LEAD THICKNESS IS TO BE MAINTAINED AFTER SOLDER COATING ON THE NARROW PORTION OF THE LEAD
2. LEAD WITHIN 0.010" RADIUS OF TRUE POSITION (TP) WITH MAXIMUM MATERIAL CONDITION.

92CS-36938

DIMENSIONAL OUTLINES

Small-Outline (SO) Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

(M) SUFFIX (JEDEC MS-012AA)
8-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39432

(M) SUFFIX (JEDEC MS-012AB)
14-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R1

(M) SUFFIX (JEDEC MS-012AC)
16-Lead Dual-In-Line
Surface-Mount Plastic Package

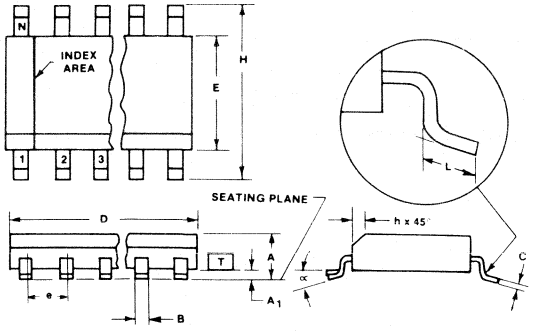
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R1

DIMENSIONAL OUTLINES

Small-Outline (SO) Packages (Cont'd)



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

(M) SUFFIX (JEDEC MS-013AA)
16-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-39433

(M) SUFFIX (JEDEC MS-013AC)
20-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-38926R1

(M) SUFFIX (JEDEC MS-013AD)
24-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-39037R1

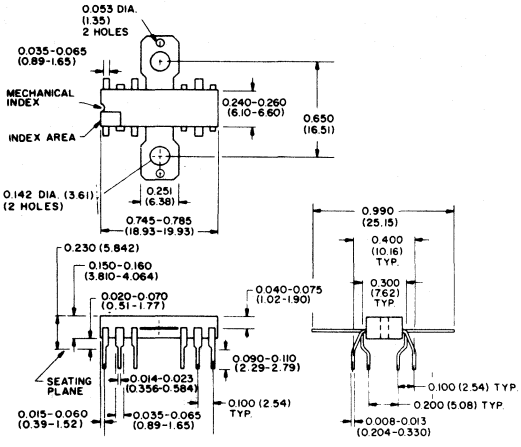
(M) SUFFIX (JEDEC MS-013AE)
28-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.70	18.10	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
∝	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-39434

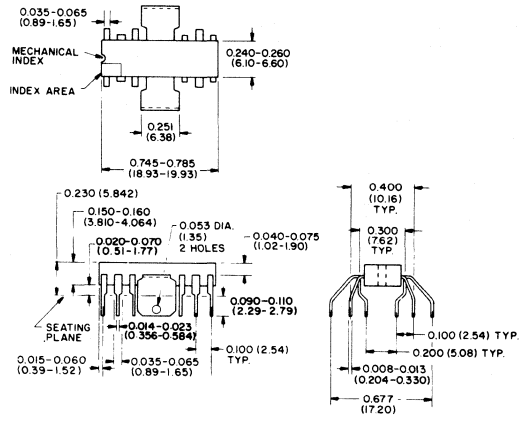
DIMENSIONAL OUTLINES

(QM) Suffix
Modified 16-Lead with Integral
Flat Wing-Tab Heat Sink

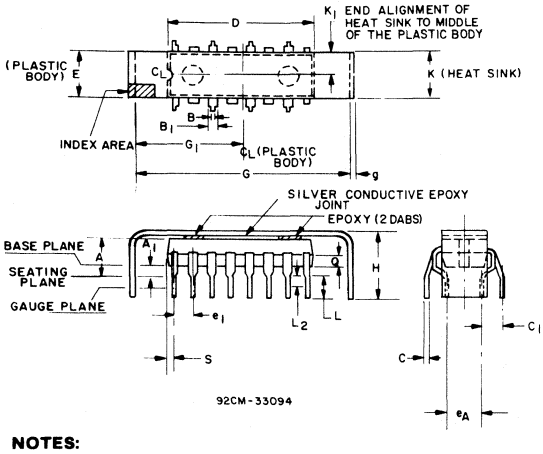


DIMENSIONS IN PARENTHESES ARE MILLIMETER EQUIVALENTS OF THE BASIC INCH DIMENSIONS

(Q) Suffix
Mofified 16-Lead with Integral
Bent Down Wing-Tab Heat Sink



(QM) Suffix
16-Lead Quad-In-Line Plastic with "Power Slab"



NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. **When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).**
2. **Leads within 0.005 in. (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.**
3. **e_A applies in zone L_2 when unit installed.**
4. **α applies to spread leads prior to installation.**
5. **N is the maximum quantity of lead positions.**
6. **N_1 is the quantity of allowable missing leads.**
7. **Bulging to 0.280 in. (7.11 mm) permissible at points of debossing.**

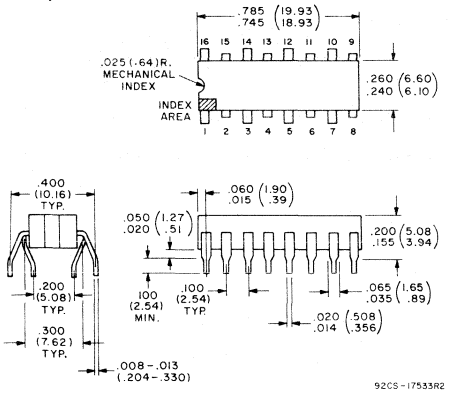
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
C_1	0.095	0.105	2.41	2.67	
D	0.745	0.785	18.93	19.93	
E	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.200 TP		7.62 TP		2, 3
G	1.125 TP		2.858 TP		
G_1	0.537	0.587	13.64	14.91	
g	0.030	0.036	0.76	0.91	
H	0.350		8.89		
K	0.250		6.35		7
K_1	0.093	0.157	2.36	3.99	
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.000	0.76	
N	16		16		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.015	0.060	0.39	1.52	

92CM-33094

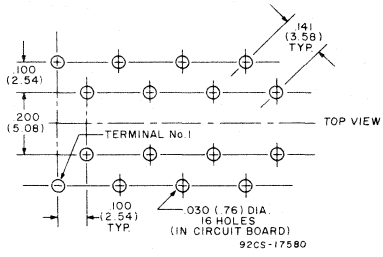
DIMENSIONAL OUTLINES

Quad-In-Line Plastic Packages

(Q) Suffix, 16-Lead



Recommended Mounting Hole Dimensions and Spacing

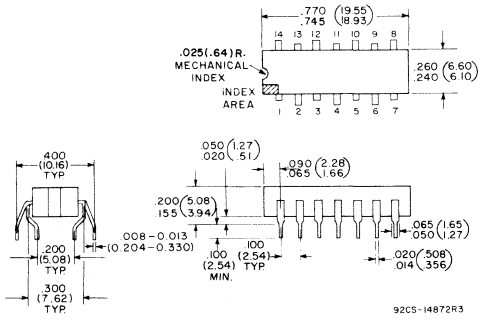


NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

QUAD-IN-LINE PLASTIC PACKAGES

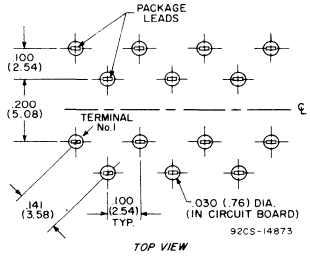
(W) Suffix, 14-Lead Staggered



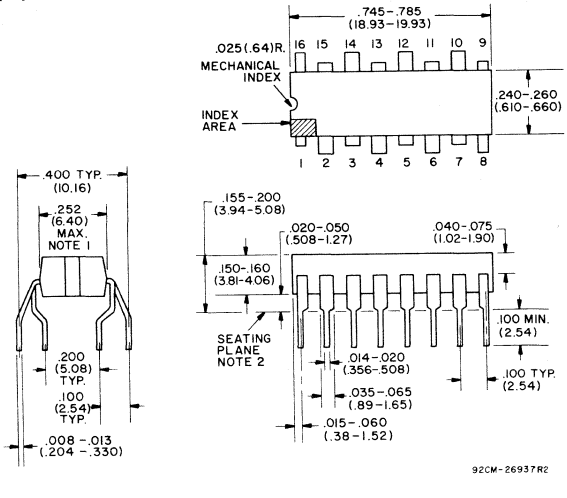
NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

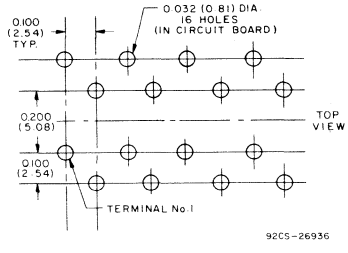
Recommended Mounting Hole Dimensions and Spacing



(W) Suffix, 16-Lead Staggered



Recommended Mounting Hole Dimensions and Spacing



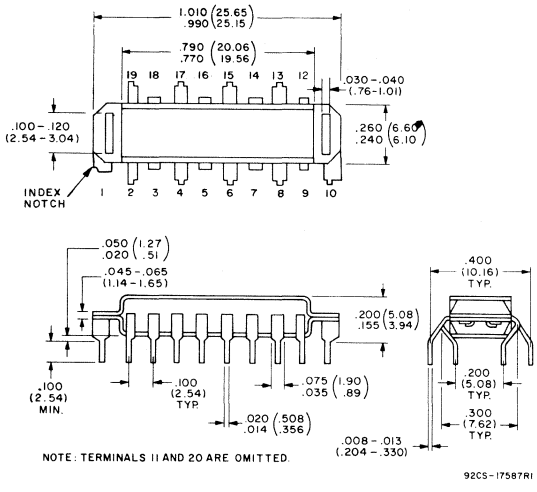
NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

DIMENSIONAL OUTLINES

Quad-In-Line Plastic Packages (Cont'd)

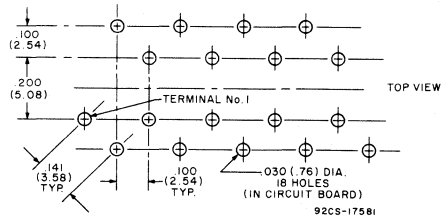
20-Lead Shielded Plastic Package



NOTE: TERMINALS 11 AND 20 ARE OMITTED.

92CS-17587RI

Recommended Mounting Hole Dimensions and Spacing



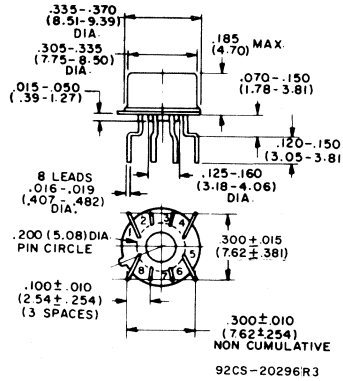
92CS-17581

NOTES:
1. Body width is measured 0.040" (1.02 mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

Dimensions in parentheses are millimeter equivalents of the basic inch dimensions.

TO-5 Style Packages

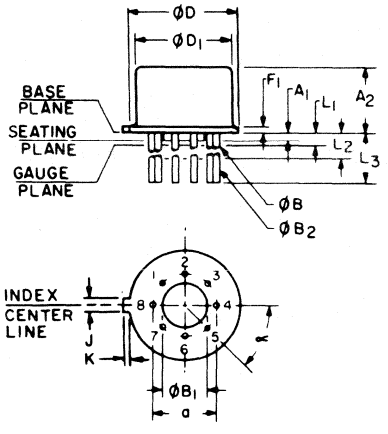
(S) Suffix
8-Lead TO-5 Style with
Dual-In-Line Formed Leads (DILCAN)



92CS-20296R3

DIMENSIONAL OUTLINES

TO-5 Style Packages (Cont'd)



NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. **Leads at gauge plane within 0.007 in. (0.178 mm) radius of True Position (TP) at maximum material condition.**
2. **ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500 in. (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm).**
3. **Measure from Max. ϕD.**
4. **N_1 is the quantity of allowable missing leads.**
5. **N is the maximum quantity of lead positions.**

(T) Suffix (JEDEC MO-006-AF)
10-Lead TO-5 Style

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	
A_2	0.165	0.185	4.19	4.70	
ϕ_B	0.016	0.019	0.407	0.482	3
ϕB_1	0	0	0	0	
ϕB_2	0.016	0.021	0.407	0.533	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	36° TP		36° TP		
N	10		10		6
N_1	1		1		5

92CS-15835

(T) Suffix (JEDEC MO-002-AL)
8-Lead TO-5 Style

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.200 TP		5.88 TP		2
A_1	0.010	0.050	0.26	1.27	
A_2	0.165	0.185	4.20	4.69	
ϕ_B	0.016	0.019	0.407	0.482	3
ϕB_1	0.125	0.160	3.18	4.06	
ϕB_2	0.016	0.021	0.407	0.482	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	45° TP		45° TP		
N	8		8		6
N_1	3		3		5

92CS-19431R3

(T) Suffix (JEDEC MO-006-AG)
12-Lead TO-5 Style

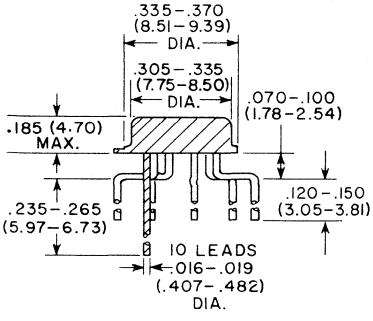
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	
A_2	0.165	0.185	4.19	4.70	
ϕ_B	0.016	0.019	0.407	0.482	3
ϕB_1	0	0	0	0	
ϕB_2	0.016	0.021	0.407	0.533	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	30° TP		30° TP		
N	12		12		6
N_1	1		1		5

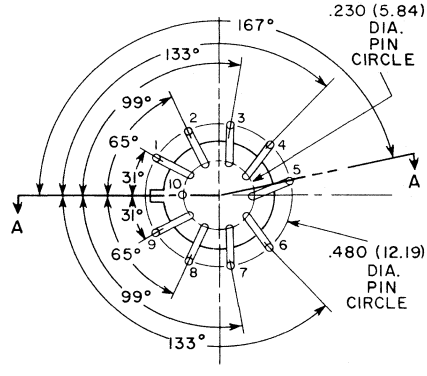
92CS-19774

DIMENSIONAL OUTLINES

TO-5 Style Packages (Cont'd)

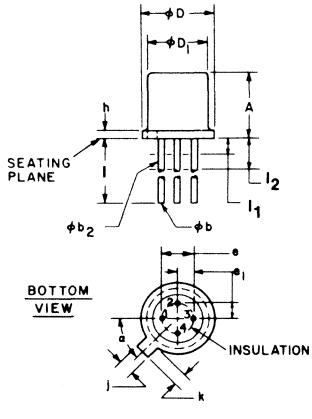
(V) Suffix
10 Formed Leads Radially
Arranged TO-5 Type
(Available in 8 and 12-Lead Versions)





92CS-14638R2

JEDEC TO-72 Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.170	0.210	4.32	5.33	
ϕb	0.016	0.021	0.406	0.533	2
ϕb_2	0.016	0.019	0.406	0.483	2
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 TP		2.54 TP		4
e_1	0.050 TP		1.27 TP		4
h	—	0.030	—	0.762	
j	0.036	0.046	0.914	1.17	
k	0.028	0.048	0.711	1.22	3
l	0.500	—	12.70	—	2
l_1	—	0.050	—	1.27	2
l_2	0.250	—	6.35	—	2
α	45° TP		45° TP		4, 6

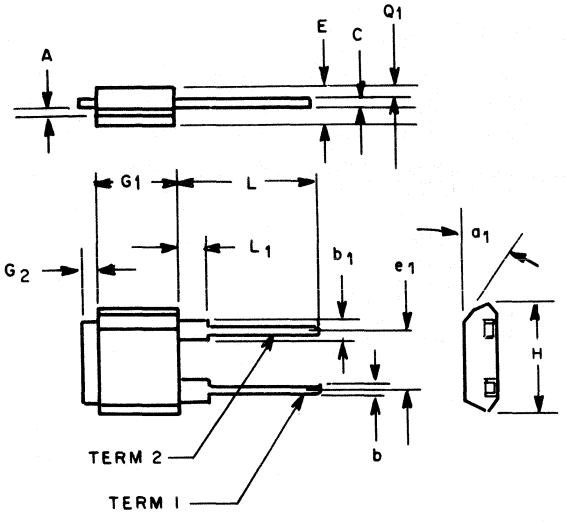
92CS-17444R1

NOTES:

1. **(Four leads). Maximum number leads omitted in this outline "none" (0). The number and position of leads actually present are indicated in the product registration. Outline designation determined by the location and minimum angular or linear spacing of any two adjacent leads.**
2. **(All leads). ϕb_2 applies between l_1 and l_2. ϕb applies between l_2 and 0.500 in. (12.7 mm) from seating plane. Diameter is uncontrolled in l_1 and beyond 0.500 in. (12.7 mm) from seating plane.**
3. **Measured from maximum diameter of the product.**
4. **Leads having maximum diameter 0.019 in. (0.483 mm) measured in gauging plane 0.054 in. (1.37 mm) + 0.001 in. (0.025 mm) - 0.000 in. (0.000 mm) below the seating plane of the product shall be within 0.007 in. (0.178 mm) of their true position relative to a maximum width tab.**
5. **The product may be measured by direct methods or by gauge.**
6. **Tab centerline.**

DIMENSIONAL OUTLINES

TO-202 Style Package



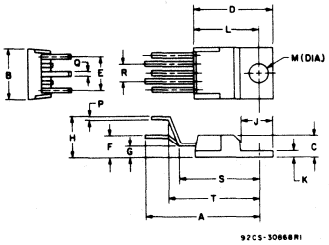
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.05	—	1.270	1
b	0.023	0.029	0.584	0.736	
b_1	0.045	0.055	1.143	1.397	1
c	0.018	0.026	0.457	0.660	
E	0.130	0.150	3.302	3.810	
e_1	0.190	0.210	4.826	5.334	
G_1	0.220	0.260	5.588	6.624	
G_2	—	0.06	—	1.524	
H	0.330	0.380	8.382	9.652	
L	0.390	0.450	9.906	11.43	
L_1	—	0.110	—	2.794	1, 2
Q_1	0.039	0.050	0.990	1.270	
a_1	—	50°	—	50°	1

92CS-39011

Notes:
1. Package contour optional within dimensions specified.
2. Lead dimensions uncontrolled in this zone.

TO-220 Style (VERSA-V1) Plastic Package

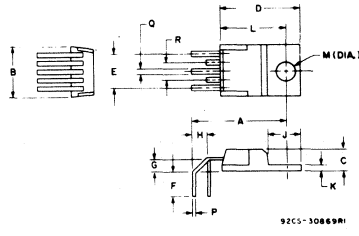
Vertical Mount



92CS-30868RI

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.876	0.896	22.25	22.75
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.168	0.188	4.268	4.775
G	0.100	0.104	2.540	2.641
H	0.320	0.340	8.128	8.638
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530
S	0.600	0.630	15.24	16.00
T	0.680	0.710	17.27	18.03

Horizontal Mount (M Suffix)

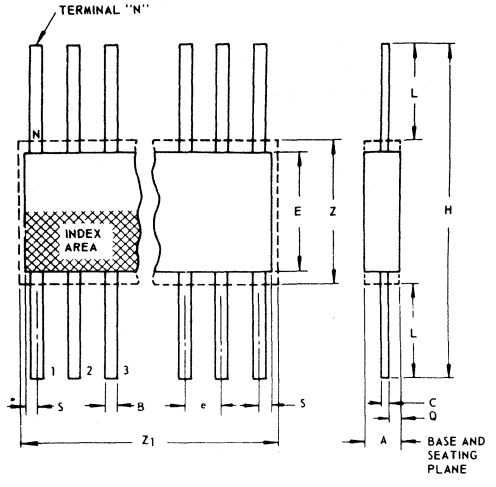


92CS-30869RI

SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.726	0.746	18.44	18.94
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.221	0.251	5.614	6.375
G	0.100	0.104	2.540	2.641
H	0.143	0.163	3.633	4.140
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530

DIMENSIONAL OUTLINES

Ceramic Flat Packs



(K) Suffix (JEDEC MO-004-AG)
16-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.008	0.100	0.21	2.54	
B	0.015	0.019	0.381	0.482	1
C	0.003	0.006	0.077	0.152	1
e	0.050 TP		1.27 TP		2
E	0.200	0.300	5.1	7.6	
H	0.600	1.000	15.3	25.4	
L	0.150	0.350	3.9	8.8	
N	16		16		3
Q	0.005	0.050	0.13	1.27	
S	0.000	0.025	0.00	0.63	
Z	0.300		7.62		4
Z_1	0.400		10.16		4

92CS-17271R3

NOTES:

1. Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
2. Leads at gauge plane within 0.005 in. (0.12 mm) radius of True Position (TP) at maximum material condition.
3. N is the maximum quantity of lead positions.
4. Z and Z_1 determine a zone within which all body and lead irregularities lie.

(K) Suffix (JEDEC MO-004-AF)
14-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.008	0.100	0.21	2.54	
B	0.015	0.019	0.381	0.482	1
C	0.003	0.006	0.077	0.152	1
e	0.050 TP		1.27 TP		2
E	0.200	0.300	5.1	7.6	
H	0.600	1.000	15.3	25.4	
L	0.150	0.350	3.9	8.8	
N	14		14		3
Q	0.005	0.050	0.13	1.27	
S	0.000	0.050	0.00	1.27	
Z	0.300		7.62		4
Z_1	0.400		10.16		4

92SS-4300R3

(K) Suffix
24-Lead

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.075	0.120	1.91	3.04	
B	0.018	0.222	0.458	0.558	1
C	0.004	0.007	0.102	0.177	1
e	0.050 TP		1.27 TP		2
E	0.600	0.700	15.24	17.78	
H	1.150	1.350	29.21	34.29	
L	0.225	0.325	5.72	8.25	
N	24		24		3
Q	0.035	0.070	0.89	1.77	
S	0.060	0.110	1.53	2.79	1
Z	0.700		17.78		4
Z_1	0.750		19.05		4

92CS-19949R2

Application Notes

1CE-402	Operating Considerations for RCA Solid State Devices
AN-3193	Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor
AN-3452	Chopper Circuits Using RCA MOS Field-Effect Transistors
AN-3535	An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer
AN-4018	Design of Gate-Protected MOS Field-Effect Transistors
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